Document Title	M102AWF2 R9 Tentativ	M102AWF2 R9 Tentative Product Specification			1/29
Document No.		Issue date	2023/02/26	Revision	00

Tentative Product Specification

To:

Product Name: M102AWF2 R9

Document Issue Date: 2023/02/26

Customer					
<u>SIGNATURE</u>					
Please return 1 copy for your confirmation					
with your signature and comments.					

InfoVision Optoelectronics				
<u>SIGNATURE</u>				
REVIEWED BY CQM				
PREPARED BY FAE				

Note: 1. Please contact InfoVision Company before designing your product based on this product.

2. The information contained herein is presented merely to indicate the characteristics and performance of our products. No responsibility is assumed by IVO for any intellectual property claims or other problems that may result from application based on the module described herein.

FQ-7-30-0-009-03D

Document Title	M102AWF2 R9 Tentative Product Specification			Page No.	2/29
Document No.		Issue date	2023/02/26	Revision	00

Revision	Date	Page	Revised Content/Summary	Remark
00	2023/02/26		First issued.	-
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Document Title	M102AWF2 R9 Tentativ	M102AWF2 R9 Tentative Product Specification			3/29
Document No.		Issue date	2023/02/26	Revision	00

CONTENTS

1.0	GENERAL DESCRIPTIONS	 	 		 4
2.0	ABSOLUTE MAXIMUM RATINGS	 	 		 6
3.0	OPTICAL CHARACTERISTICS	 	 		 7
4.0	ELECTRICAL CHARACTERISTICS	 	 		10
5.0	MECHANICAL CHARACTERISTICS	 	 		 22
6.0	RELIABILITY CONDITIONS	 	 		 25
7.0	PACKAGE SPECIFICATION	 	 	<u></u>	 26
8.0	LOT MARK	 			 27
9.0	GENERAL PRECAUTION				 28

Document Title	M102AWF2 R9 Tentativ	VF2 R9 Tentative Product Specification			4/29
Document No.		Issue date	2023/02/26	Revision	00

1.0 General Descriptions

1.1 Introduction

The M102AWF2 R9 is a Color Active Matrix Liquid Crystal Display with a back light system. The matrix uses a-Si Thin Film Transistor as a switching device. This TFT LCD has a 10.25 inch diagonally measured active display area with FHD resolution (1920horizontal by 720vertical pixels array).

1.2 Features

- Supported FHD Resolution
- LVDS Interface
- Wide View Angle
- Compatible with RoHS Standard

1.3 Product Summary

Items	<u> </u>	Specifications	Unit
Screen Diagonal		10.25	inch
Active Area (H x V)		243.65 x 91.37	mm
Number of Pixels (H x V)		1,920 x 720	-
Pixel Pitch (H x V)		0.1269 x 0.1269	mm
Pixel Arrangement		R.G.B. Vertical Stripe	-
Display Mode		Normally Black	-
White Luminance		(1000) (Typ.)	cd /m2
Contrast Ratio		(1200) (Typ.)	-
Response Time		(20) (Typ.) @ 25℃	ms
Input Voltage		(3.3) (Typ.)	V
Power Consumption		(8.73)(Max.)@ White pattern ,FV=60Hz	W
Weight		(330) (Max.)	g
Outline Dimension	W/O PCBA	(261.14) (Typ.) x (109.3) (Typ.) x (8.521) (Max.)	
(H x V x D)	With PCBA	(261.14) (Typ.) x (109.3) (Typ.) x (12.171) (Max.)	mm
Electrical Interface (Logic)		LVDS	-
Support Color		16.7 M	-
NTSC		(85) (Min.)	%
Surface Treatment		HC	-

Document Title	M102AWF2 R9 Tentative Product Specification			Page No.	5/29
Document No.		Issue date	2023/02/26	Revision	00

1.4 Functional Block Diagram

Figure 1 shows the functional block diagram of the LCD module.

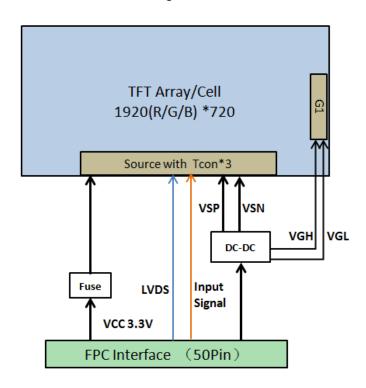


Figure 1 Block Diagram

1.5 Pixel Mapping

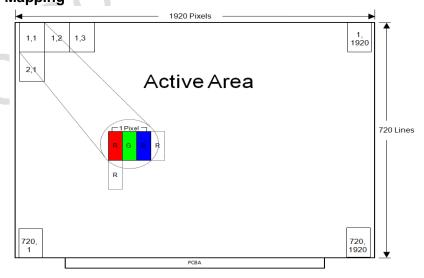


Figure 2 Pixel Mapping

Document Title	M102AWF2 R9 Tentative Product Specification			Page No.	6/29
Document No.		Issue date	2023/02/26	Revision	00

2.0 Absolute Maximum Ratings

Table 1 Electrical & Environment Absolute Rating

Item	Symbol	Min.	Max.	Unit	Note
Logic Supply Voltage	V_{DD}	(-0.3)	(4)	V	
Logic Supply Voltage	$V_{\text{DD-OTP}}$	(-0.3)	(8.8)	V	(1),(2),
Logic Input LVDS Voltage	V_{LVDS}	(0.7)	(1.7)	V	(3),(4),
Logic input signals	V_{IO}	(-0.3)	(4)	V	(5)
Operating Temperature	Tgs	(-30)	(85)	$^{\circ}$	(3)
Storage Temperature	Та	(-40)	(90)	${\mathbb C}$	

Condition: GND=0V

Note (1) All the parameters specified in the table are absolute maximum rating values that may cause faulty operation or unrecoverable damage, if exceeded. It is recommended to follow the typical value.

Note (2) All the contents of electro-optical specifications and display fineness are guaranteed under Normal Conditions. All the display fineness should be inspected under normal conditions. Normal conditions are defined as follow: Temperature: 25°C, Humidity: 55± 10%RH.

Note (3) Unpredictable results may occur when it was used in extreme conditions. T_a = Ambient Temperature, T_{gs} = Glass Surface Temperature All the display fineness should be inspected under normal conditions.

Note (4) Temperature and relative humidity range are shown in the figure below. Wet bulb temperature should be lower than $(57.8)^{\circ}$ C, and no condensation of water. Besides, protect the module from static electricity.

Note (5)Logic input signal include STBYB 、RESET、UPDN、SHLR、BIST.

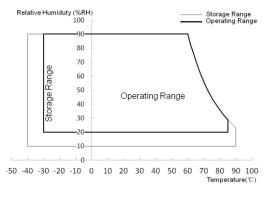


Figure 3 Absolute Ratings of Environment of the LCD Module

Document Title	M102AWF2 R9 Tentative Product Specification			Page No.	7/29
Document No.		Issue date	2023/02/26	Revision	00

3.0 Optical Characteristics

The optical characteristics are measured under stable conditions as following notes.

Table 2 Optical Characteristics

Item	Conditions		Min.	Тур.	Max.	Unit	Note	
	Horizontal	θ x+	(80)	(85)	-			
Viewing Angle	ПОПДОПІАІ	θ _{x-}	(80)	(85)	-	dograd	(4) (2) (3) (4)(9)	
(CR≥10)	Vertical	θ _{y+}	(80)	(85)	-	degree	(1),(2),(3),(4)(8)	
	vertical	θ _{y-}	(80)	(85)	-			
Contrast Ratio	Center		(900)	(1,200)	-	(C)	(1),(2),(4),(8) θx=θy=0°	
		25℃	-	(20)	(30)	ms		
Response Time	Rising + Falling	-20℃	-	-	(250)	ms	(1),(2),(5),(8) θx=θy=0°	
		-30℃	-	-	(500)	ms		
	Red x Red y Green x			(0.678)		-		
				(0.310)	Typ. +0.03	-		
				(0.263)		-		
Color Chromaticity	Green y	Green y		(0.645)		-	(1),(2),(3),(8) $\theta x = \theta y = 0^{\circ}$	
(CIE1931)	Blue x Blue y White x		-0.03	(0.153)		-		
				(0.056)		-		
				(0.307)		-		
	White y			(0.335)		-		
NTSC	-		(85)	TBD	-	%	(1),(2),(3),(8) $\theta x = \theta y = 0^{\circ}$	
White Luminance	Center		(900)	(1000)	-	cd/m ²	(1),(2),(6),(8) $\theta x = \theta y = 0^{\circ}$	
Luminance Uniformity(white)	9 Points		(80)	TBD	-	%	(1),(2),(7),(8)	
Luminance Uniformity(black)	9 Points		(50)	TBD	-	%	θx=θy=0°	

Document Title	M102AWF2 R9 Tentativ	WF2 R9 Tentative Product Specification			8/29
Document No.		Issue date	2023/02/26	Revision	00

Note (1) Measurement Setup:

The LCD module should be stabilized at given ambient temperature (25°C) for 30 minutes to avoid abrupt temperature changing during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 30 minutes in the windless room.

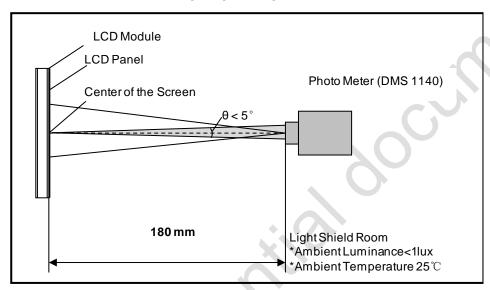


Figure 4 Measurement Setup

Note (2) The LED input parameter setting as:

 I_{LED} :(240)mA, I_{LED} =(80)mA*3

Note (3) Definition of Viewing Angle

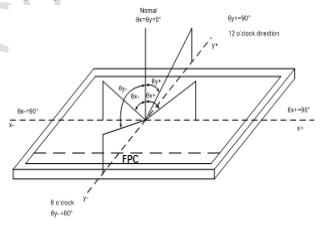


Figure 5 Definition of Viewing Angle

Note (4) Definition of Contrast Ratio (CR)

The contrast ratio can be calculated by the following expression:

Contrast Ratio (CR) = The luminance of White pattern/ The luminance of Black pattern Note (5) Definition of Response Time (T_R , T_F)

Document Title	M102AWF2 R9 Tentativ	VF2 R9 Tentative Product Specification			9/29
Document No.		Issue date	2023/02/26	Revision	00

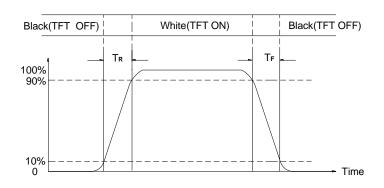


Figure 6 Definition of Response Time

Note (6) Definition of Luminance of White

Measure the luminance of White pattern (Ref.: Active Area)

Display Luminance=L1(center point)

Note (7) Definition of Luminance Uniformity (Ref.: Active Area)
Measure the luminance of White/Black pattern at 9 points.
Luminance Uniformity= Min.(L1, L2, ... L9) / Max.(L1, L2, ... L9)
H—Active Area Width, V—Active Area Height, L—Luminance

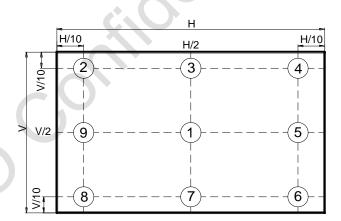


Figure 7 Measurement Locations of 9 Points

Note (8) All optical data are based on IVO given system & nominal parameter & testing machine in this document.

Document Title	M102AWF2 R9 Tentative Product Specification			Page No.	10/29
Document No.		Issue date	2023/02/26	Revision	00

4.0 Electrical Characteristics

4.1 Interface Connector

Table 3 Signal Connector Type

Item	Description
Mating Receptacle / Type	FFSKL05023G50B/STM

Table 4 Signal Connector Pin Assignment

Pin No.	Symbol	Description	Remarks
1	GND	Ground	-
2	GND	Ground	-
3	GND	Ground	-
4	VDD	Digital Power	-
5	VDD	Digital Power	-
6	VDD	Digital Power	-
7	VDD	Digital Power	-
8	GND	Ground	-
9	SPI_SDA	Serial Interface address and data input/output for SPI interface. Only for IVO use.,	
9	SPI_SDA	If not use, leave this pin floating.	-
10	SPI_SCL	Serial Interface clock input for SPI interface. Only for IVO use. If not use, leave this pin floating.	-
11	SPI_CS	Serial Interface chip enable singal for SPI interface. Only for IVO use If not use, leave this pin floating.	-
12	GND	Ground	-
13	OLV0N	Odd LVDS Data input 0-	-
14	OLV0P	Odd LVDS Data input 0+	-
15	GND	Ground	-
16	OLV1N	Odd LVDS Data input 1-	-
17	OLV1P	Odd LVDS Data input 1+	-
18	GND	Ground	-
19	OLV2N	Odd LVDS Data input 2-	-
20	OLV2P	Odd LVDS Data input 2+	-
21	GND	Ground	-

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Document Title M102AWF2 R9 Tentative Product Specification			Page No.	11/29			
Documen	t No.			Issue date	2023/02/26	Revision	00
22	OLV	CKN	Odd LVDS Clock in	put -		-	
23	OLV	CKP	Odd LVDS Clock in	 put +		-	•
24	GNE)	Ground	•		-	
25	OLV	'3N	Odd LVDS Data inp	out 3-		_	
26	OLV	'3P	Odd LVDS Data inp	out 3+		-	
27	GNE)	Ground				
28	ELV	0N	Even LVDS Data in	put 0-			•
29	ELV	0P	Even LVDS Data in	put 0+			
30	GNE)	Ground				
31	ELV	1N	Even LVDS Data in	put 1-		-	
32	ELV	1P	Even LVDS Data in	put 1+		-	•
33	GNE)	Ground			-	•
34	ELV	2N	Even LVDS Data in	put 2-		-	•
35	ELV	2P	Even LVDS Data in	put 2+	<i></i>	-	•
36	GNE)	Ground			-	
37	ELV	CKN	Even LVDS Clock in	nput -		-	
38	ELV	CKP	Even LVDS Clock in	nput +		-	
39	GNE)	Ground			-	
40	ELV	3N	Even LVDS Data in	put 3-		-	
41	ELV	3P	Even LVDS Data in	put 3+		-	
42	GNE		Ground			-	

Global Reset pin. Active low, If RESET

RESET

STBYB

on/off.

on/off.

43

44

connected to GND, the chip is in reset state. (Suggest to connecting with an RC reset circuit

This pin must meet the sequence of power

Standby mode setting pin..

STBYB=High, normal operation

for stability.Suggest RC Value: R=10K, C=1uF)

STBYB=Low, timing control, output buffer, DAC

and power circuit all off when STBYB is low.

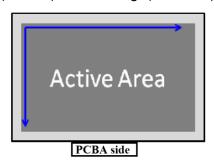
This pin must meet the sequence of power

Document Title	M102AWF2 R9 Tentative Product Specification			Page No.	12/29
Document No.		Issue date	2023/02/26	Revision	00

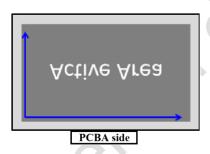
		Horizontal shift direction(Source	
		output)selection, Default Pull High(Internal pull	
45	SHLR	high resistor R=10K)	-
		SHLR=High, SOUT1→SOUT2→→SOUT1920	
		SHLR=Low, SOUT1920→SOUT2→→SOUT1	
		Vertical shift direction(Gate output)selection,	
		Default Pull High(Internal pull high resistor	
46	UPDN	R=10K)	-
		UPDN=High,Top→Bottom(Default)	
		UPDN=Low, Bottom→Top	
		Fail detection signal output。	
47	Fail_T	FAIL_T= Low, normal operation	-
		FAIL_T= High, on error condition	
48	GND	Ground	-
		LCD Panel Self Test Enable ,When it is not used,	
		Connecting to GND is recommended, Don't	
49	BIST	floating	-
		BIST=High, Bist mode	
		BIST=Low, Normal mode	
		IVO internal used only, Please don't connect by	
50	VOTP	Customer(Power input for OTP programming	-
		(8.6V)	

Document Title	M102AWF2 R9 Tentativ	VF2 R9 Tentative Product Specification			13/29
Document No.		Issue date	2023/02/26	Revision	00

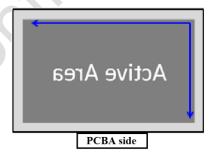
Note(1): SHLR: High(2.6~3.6V) (Default), UPDN: High(2.6~3.6V) (Default)



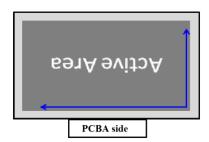
SHLR: High(2.6~3.6V) (Default), UPDN: Low(0~0.5V)



SHLR: Low(0~0.5V), UPDN: High(2.6~3.6V) (Default)



SHLR: Low(0 \sim 0.5V), UPDN: Low(0 \sim 0.5V)



Document Title	M102AWF2 R9 Tentativ	WF2 R9 Tentative Product Specification			14/29
Document No.		Issue date	2023/02/26	Revision	00

Table 5 Backlight Connector Pin Assignment

Pin No.	Symbol	Description
1	LED-PIN1	V+
2	LED-PIN2	V+
3	LED-PIN3	V+
4	LED-PIN4	/
5	LED-PIN5	NTC1
6	LED-PIN6	NTC2
7	LED-PIN7	1
8	LED-PIN8	V-
9	LED-PIN9	V-
10	LED-PIN10	V-

4.2 Signal Electrical Characteristics

4.2.1 Signal Electrical Characteristics For LVDS Receiver

The built-in LVDS receiver is compatible with (ANSI/TIA/TIA-644) standard.

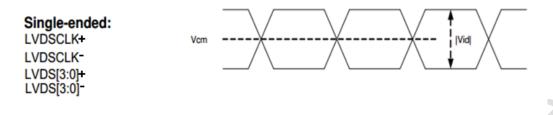
Table 6 LVDS Receiver Electrical Characteristics

Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
Differential Input High Threshold	Vth	1	1	(100)	mV	V _{CM} =+1.2V
Differential Input Low Threshold	VtI	(-100)	-	-	mV	V _{CM} =+1.2V
Magnitude Differential Input Voltage	V _{ID}	(150)	1	(600)	mV	-
Common Mode Voltage	V_{CM}	(1.0)	(1.2)	(1.7- Vid /2)	V	-

Note (1) Input signals shall be low or Hi- resistance state when VDD is off.

Note (2) All electrical characteristics for LVDS signal are defined and shall be measured at the interface connector of LCD.

Document Title	M102AWF2 R9 Tentative Product Specification			Page No.	15/29
Document No.		Issue date	2023/02/26	Revision	00



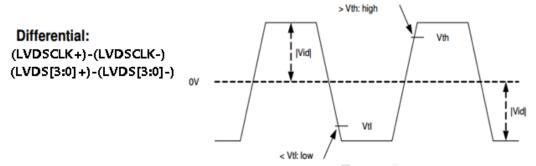


Figure 8 Voltage Definitions

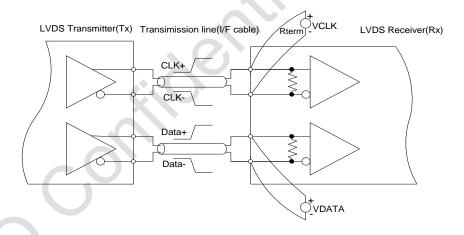


Figure 9 Measurement System

Document Title	M102AWF2 R9 Tentativ	F2 R9 Tentative Product Specification			16/29
Document No.		Issue date	2023/02/26	Revision	00

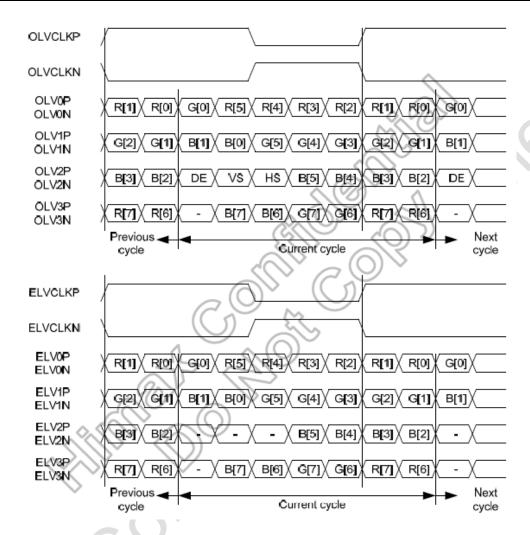
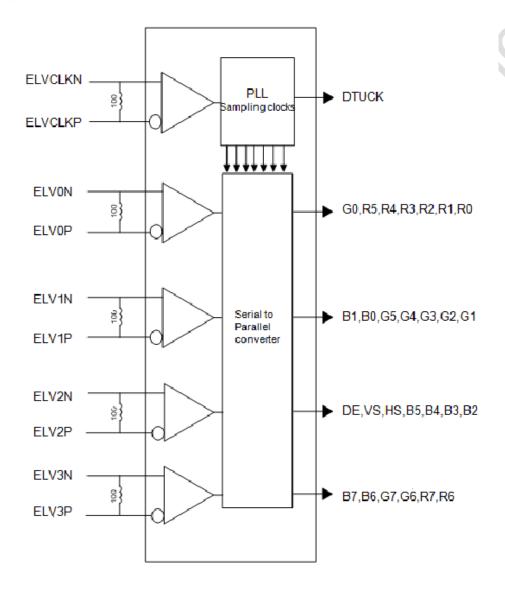


Figure 10 2 port LVDS signals, VESA format, 8-bit mode

Document Title	M102AWF2 R9 Tentativ	F2 R9 Tentative Product Specification			17/29
Document No.		Issue date	2023/02/26	Revision	00

4.2.2 LVDS Receiver Internal Circuit

Figure 11 shows the internal block diagram of the LVDS receiver. This LCD module equips termination resistors for LVDS link.



Document Title	M102AWF2 R9 Tentativ	F2 R9 Tentative Product Specification			18/29
Document No.		Issue date	2023/02/26	Revision	00

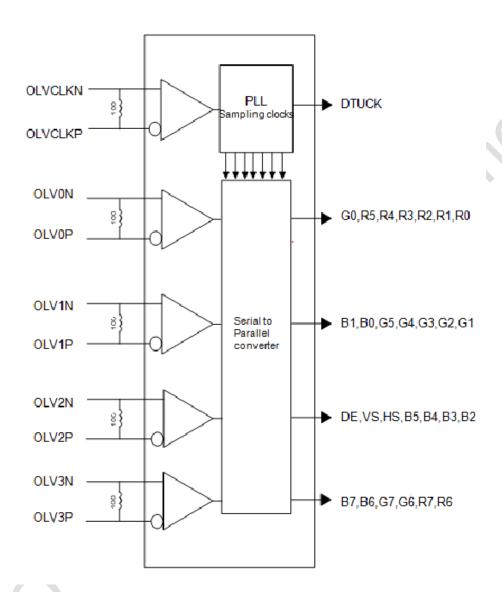


Figure 11 LVDS Receiver Internal Circuit

Document Title	M102AWF2 R9 Tentative Product Specification				19/29
Document No.		Issue date	2023/02/26	Revision	00

4.3 Interface Timings

Table 7 Interface Timings

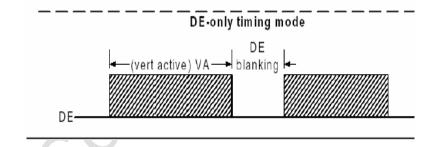
Parameter	Symbol	Min.	Тур.	Max.	Unit
LVDS Clock Frequency	F _{CLK}	(43.4)	(44.1)	(64.8)	MHz
Horizontal Total Time	T_{HP}	(990)	(1002)	(1200)	clocks
Horizontal Active Time	HA	960			clocks
HSYNC Blanking	TH _{BLANK}	(30)	(42)	(240)	clocks
Vertical Total Time	T _{VP}	(730)	(733)	(900)	lines
Vertical Active Time	VA	720			lines
VSYNC Blanking	TV_{BLANK}	(10)	(13)	(180)	lines
Frame Rate	F _V	(55)	(60)	(65)	Hz

Note1: HT * VT *Frame Frequency≤(64.8) MHz

Note2: Dual Port LVDS, Table7 shows one port LVDS.

Note3: All reliabilities are specified for timing specification based on refresh rate of 60Hz.

M102AWF2 R9 is secured only for function under lower refresh rate; 60Hz at Normal mode



Document Title	M102AWF2 R9 Tentative Product Specification			Page No.	20/29
Document No.		Issue date	2023/02/26	Revision	00

4.4 Input Power Specifications

Input power specifications are as follows.

Table 8 Input Power Specifications

Parameter		Symbol	Min.	Тур.	Max.	Unit	Note
System Power S	Supply					0	
LCD Drive Volta	LCD Drive Voltage (Logic)		(3.0)	(3.3)	(3.6)	V	(1),(2)
VDD Current	White Pattern	I _{DD}	-	-	(0.25)	А	
VDD Power Consumption	White Pattern	P _{DD}	-	-	(0.81)	W	(1),(5)
Logic Input	High level voltage	V	(0.7*VDD)	-	(VDD)	V	(1) (1)
Signal	Low level voltage	V_{Logic}	(0)	-	(0.3*VDD)	V	(1) ,(4)
Rush Current	Rush Current		-	\ - \	(1.5)	Α	(1),(6)
Allowable Logic/LCD Drive Ripple Voltage		V_{VDD-RP}	-	9)-	(200)	mV	(1),(3)
LED Power Sup	ply						
LED Input Voltag	ge	V_{LED}	(28)	-	(33)	V	(1),(2),(9)
LED Power Con	sumption	P _{LED}	O -	-	(7.92)	W	(1), (9)
LED Forward Vo	oltage	V_{F}	(2.8)	-	(3.3)	V	(1),(2),
LED Forward Cu	urrent	l _F	-	(80)	-	mA	(9)
LED Life Time@25℃		LT	(10,000)	-	-	Hours	(1),(7)
LED Life Time@	225℃	LT	(30,000)	-	-	Hours	(1),(8)
LED Life Time@	285℃	LT	(10,000)	-	-	Hours	(1),(8)

Note (1) All of the specifications are guaranteed under normal conditions. Normal conditions are defined as follow: Temperature: 25° C, Humidity: $55\pm 10\%$ RH.

Note (2) All of the absolute maximum ratings specified in the table, if exceeded, may cause faulty operation or unrecoverable damage. It is recommended to follow the typical value.

Note (3)This impedance value is needed for proper display and measured from LVDS Tx to the mating connector.

Note (4) Logic input signal include SHLR、UPDN、 BIST、RESET、STBYB.

Note (5) The specified VDD current and power consumption are measured under the VDD = (3.3) V, FV= (60) Hz condition and White pattern.

Note (6) The figures below is the measuring condition of VDD. Rush current can be measured when TRUSH is 0.5 ms.

Document Title	M102AWF2 R9 Tentative Product Specification			Page No.	21/29
Document No.		Issue date	2023/02/26	Revision	00

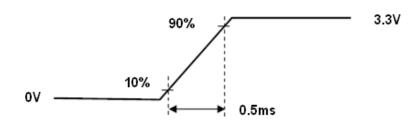
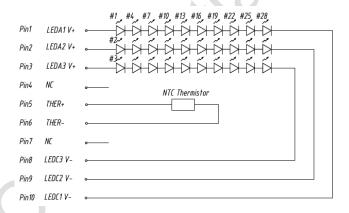


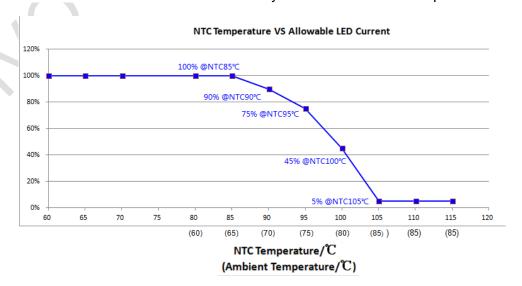
Figure 12 V_{DD} Rising Time

Note (7) The life time is determined as the sum of the lighting time till the luminance of LCD at the typical LED current reducing to 80% of the minimum value under normal operating condition. Note (8) The life time is determined as the sum of the lighting time till the luminance of LCD at the typical LED current reducing to 50% of the minimum value under normal operating condition. Note (9) Definition of VLED and PLED

 $V_{LED} = V_F \times 10$, $I_{LED} = I_F \times 3$, PLED (max.)= $V_{LED(max.)} \times I_{LED(Typ.)}$



Note (10) The allowable forward current of LED vary with environmental temperature



Document Title	M102AWF2 R9 Tentativ	VF2 R9 Tentative Product Specification			22/29
Document No.		Issue date	2023/02/26	Revision	00

4.5 Power ON/OFF Sequence

- 1.Interface signals are also shown in the chart. Signals from any system shall be Hiresistance state or low level when VDD voltage is off.
- 2. When system first start up, should keep the VDD high time longer than 200ms, otherwise may cause image sticking when VDD drop off.

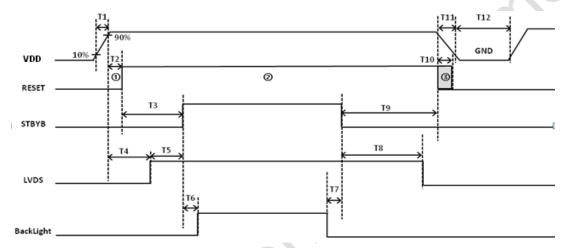


Figure 13 Power Sequence

Table 9 Power Sequencing Requirements

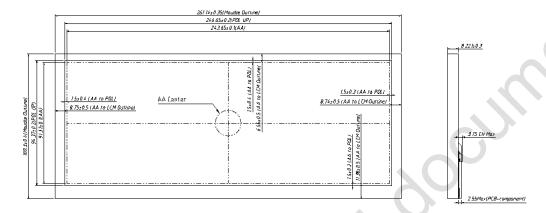
Parameter	Symbol	Min.	Тур.	Max.	Unit
VDD Rise Time	T1	(0.5)	ı	(10)	ms
VDD Good to RESET pull H	T2	(10)	ı	ı	us
RESET pull H to STBYB pull H	Т3	(90)	ı	ı	ms
VDD Good to Signal Valid	T4	(0)	ı	(50)	ms
Signal Valid to STBYB pull H	T5	(0)	(10)	-	ms
STBYB pull H to Backlight Power On	Т6	(200)	ı	-	ms
Backlight Power Off to STBYB pull L	T7	(200)	ı	-	ms
STBYB Pull L to Signal Disable	T8	(50)	(67)	(83)	ms
STBYB pull L to VDD Power off	Т9	(50)	(67)	(83)	ms
RESET off to VDD Power off	T10	(0)	-	-	ms
VDD Fall Time	T11	(0.5)	-	(30)	ms
VDD Power off	T12	(500)	-	-	ms

Note(1)RESET has 3 status in the sequence: ①Pull Low Voltage status ②Pull High Voltage Status③Hi-Z status. Please make sure RESET change to Hi-Z status while module is shutting down. Note(2)T8 and T9 suggest referring to the typ. value to ensure that T8 is equal to T9.

Document Title	M102AWF2 R9 Tentativ	M102AWF2 R9 Tentative Product Specification				
Document No.		Issue date	2023/02/26	Revision	00	

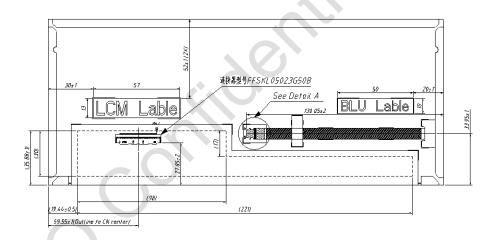
5.0 Mechanical Characteristics

5.1 Outline Drawing



Unit: mm

Figure 14 Reference Outline Drawing (Front Side)



Unit: mm

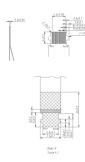


Figure 15 Reference Outline Drawing (Back Side)

Note: 1.Unnoted tolerance ±0.3mm;

Document Title	M102AWF2 R9 Tentativ	Page No.	24/29		
Document No.		Issue date	2023/02/26	Revision	00

5.2 Dimension Specifications

Table 10 Module Dimension Specifications

	tem	Min.	Тур.	Max.	Unit
Width		(260.79)	(261.14)	(261.49)	mm
Height		(108.9)	(109.3)	(109.7)	mm
Thickness	Without PCBA	(7.921)	(8.221)	(8.521)	mm
Thickness	With PCBA	-	-	(12.171)	mm
Weight	•	-	(280)	(330)	g

Note: Outline dimension measure instrument: Vernier Caliper.

Document Title	M102AWF2 R9 Tentativ	/F2 R9 Tentative Product Specification				
Document No.		Issue date	2023/02/26	Revision	00	

6.0 Reliability Conditions

Table 11 Reliability Condition

It	em	Package Test Conditions		Test Conditions					
	erature/High perating Test	Module		T _a =60℃, 90%RH, 500 hours					
	ature Operating est	Module		T_a =85°C, 500 hours	(1),(2), (3),(4)				
_	ature Operating est	Module		$T_a = -30^{\circ}C$, 500 hours	(=),(=)				
	rature Storage est	Module		T _a =90℃, 500 hours					
•	w Temperature Storage Test Module T _a = - 40°C, 500 hours				(1),(3), (4)				
Temperatur	e Shock Test	Module T _a = -40 °C (30min.)~85 °C (30mi		T _a = -40°C(30min.)~85°C(30min.),200cycles				T _a = -40°C (30min.)~85°C (30min.),200cycles	
Shook Non	hock Non-operating Test Module			50G. 6msmec, 1/2 Sine Wave					
SHOCK NOTI-	operating rest	Module	±X, ±Y, ±Z, each axis 10 times						
			half-sine	Frequency: 8Hz ~ 33Hz Stroke: 1.3mm	(1),(3),				
Vibration Non	-operating Test	Module	Sweep: 2.9G 33.3Hz ~ 400Hz X,Z		(5)				
VIDIATION NOI	r-operating rest	Module	Cycle :	15 minutes ,2 hrs for each direction of					
				X,Z; 4 hours for Y direction					
ESD Test	Contact Operating Module		±4KV,±8KV ,150pF(330Ohm)	(1),(2),					
			Air	±6KV,±15KV ,150pF(330Ohm)	(6)				

Note (1) A sample can only have one test. Outward appearance, image quality and optical data can only be checked at normal conditions according to the IVO document before reliable test. Only check the function of the module after reliability test.

- Note (2) The setting of electrical parameters should follow the typical value before reliability test.
- Note (3) During the test, it is unaccepted to have condensate water remains. Besides, protect the module from static electricity.

Note (4) The sample must be released for 24 hours under normal conditions before judging. Furthermore, all the judgment must be made under normal conditions. Normal conditions are defined as follow: Temperature: 25° C, Humidity: $55\pm 10\%$ RH. T_a = Ambient Temperature, T_{gs} = Glass Surface Temperature.

- Note (5) The module should be fixed firmly in order to avoid twisting and bending.
- Note (6) It could be regarded as pass, when the module recovers from function fault caused by ESD a few minutes later.

Document Title	M102AWF2 R9 Tentativ	M102AWF2 R9 Tentative Product Specification				
Document No.		Issue date	2023/02/26	Revision	00	

7.0 Package Specification

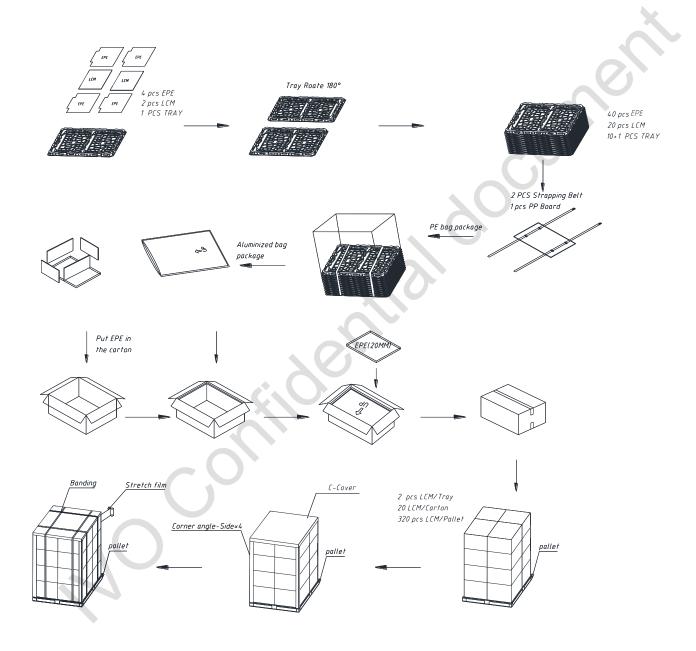
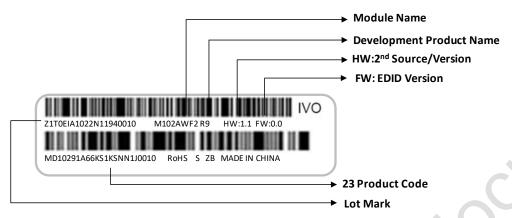


Figure 16 Packing Method

Document Title	M102AWF2 R9 Tentativ	Page No.	27/29		
Document No.		Issue date	2023/02/26	Revision	00

8.0 Lot Mark



Note: This picture is only an example.

8.1 20 Lot Mark

Code 1,2,4,5,6,7,8,9,10,11,16: IVO internal flow control code.

Code 3: Production Location.

Code 12: Production Year.

Code 13: Production Month.

Code 14,15: Production Day.

Code 17,18,19,20: Serial Number.

8.2 23 Product Barcode

Code 1,2: Manufacture District.

Code 3,4,5,6,7: IVO internal module name.

Code 8,9,10,13,16: IVO internal flow control code.

Code 11,12: Cell location Suzhou, China defined as "KS".

Code 14,15: Module location Kunshan, China defined as "KS"; Yangzhou, China defined as "YZ"; Shenzhen, China defined as "SE"; Zhuhai, China defined as "ZH"; Suzhou, China defined as "SZ".

Code 17,18,19: Year, Month, Day refer to Note(1), Note(2) and Note(3).

Note (1) Production Year

Year	2006	2007	2008	2009	2010	2011	2012	2013	 2035
Mark	6	7	8	9	Α	В	С	D	 Z

Note (2) Production Month

Month	Jan.	Feb.	Mar.	Apr.	Мау.	Jun.	Jul.	Aug.	Sep.	Oct	Nov.	Dec.
Mark	1	2	3	4	5	6	7	8	9	Α	В	С

Note (3) Production Day: 1~V. Code 20~23: Serial Number.

Document Title	M102AWF2 R9 Tentative Product Specification			Page No.	28/29
Document No.		Issue date	2023/02/26	Revision	00

9.0 General Precaution

10.1 Using Restriction

This product is not authorized for using in life supporting systems, aircraft navigation control systems, military systems and any other appliance where performance failure could be life-threatening or lead to be catastrophic.

10.2 Operation Precaution

(1) The LCD product should be operated under normal conditions.

Normal conditions are defined as below:

Temperature: 25°C Humidity: 55±10%

Display pattern: continually changing pattern (Not stationary)

- (2) Brightness and response time depend on the temperature. (It needs more time to reach normal brightness in low temperature.)
- (3) It is necessary for you to pay attention to condensation when the ambient temperature drops suddenly. Condensate water would damage the polarizer and electrical contacted parts of the module. Besides, smear or spot will remain after condensate water evaporating.
- (4) If the absolute maximum rating value was exceeded, it may damage the module.
- (5) Do not adjust the variable resistor located on the module.
- (6) Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding may be important to minimize the interference.
- (7) Image sticking may occur when the module displayed the same pattern for long time.
- (8) Do not connect or disconnect the module in the "power on" condition. Power supply should always be turned on/off by the "power on/off sequence"
- (9) Ultra-violet ray filter is necessary for outdoor operation.

10.3 Mounting Precaution

- (1) All the operators should be electrically grounded and with Ion-blown equipment turning on when mounting or handling. Dressing finger-stalls out of the gloves is important for keeping the panel clean during the incoming inspection and the process of assembly.
- (2) It is unacceptable that the material of cover case contains acetic or chloric. Besides, any other material that could generate corrosive gas or cause circuit break by electro-chemical reaction is not desirable.
- (3) The case on which a module is mounted should have sufficient strength so that external force is not transmitted to the module directly.
- (4) It is obvious that you should adopt radiation structure to satisfy the temperature specification.
- (5) So as to acquire higher luminance, the cable of the power supply should be connected directly with a minimize length.
- (6) It should be attached to the system tightly by using all holes for mounting, when the module is

Document Title	M102AWF2 R9 Tentative Product Specification			Page No.	29/29
Document No.		Issue date	2023/02/26	Revision	00

assembled. Be careful not to apply uneven force to the module, especially to the PCB on the back.

- (7) A transparent protective film needs to be attached to the surface of the module.
- (8) Do not press or scratch the polarizer exposed with anything harder than HB pencil lead. In addition, don't touch the pin exposed with bare hands directly.
- (9) Clean the polarizer gently with absorbent cotton or soft cloth when it is dirty.
- (10) Wipe off saliva or water droplet as soon as possible. Otherwise, it may cause deformation and fading of color.
- (11)Clean the panel gently with absorbent cotton or soft cloth when it is dirty. Ethanol(C_2H_5OH) is allowed to be used. Ketone (ex. Acetone), Toluene, Ethyl acid, Methyl chloride, etc are not allowed to be used for cleaning the panel, which might react with the polarizer to cause permanent damage.
- (12) Do not disassemble or modify the module. It may damage sensitive parts in the LCD module, and cause scratches or dust remains. IVO does not warrant the module, if you disassemble or modify the module.

10.4 Handling Precaution

- (1) Static electricity will generate between the film and polarizer, when the protection film is peeled off. It should be peeled off slowly and carefully by operators who are electrically grounded and with Ion-blown equipment turning on. Besides, it is recommended to peel off the film from the bonding area.
- (2) The protection film is attached to the polarizer with a small amount of glue. When the module with protection film attached is stored for a long time, a little glue may remain after peeling.
- (3) If the liquid crystal material leaks from the panel, keep it away from the eyes and mouth. In case of contact with hands, legs or clothes, it must be clean with soap thoroughly.

10.5 Storage Precaution

When storing modules as spares for long time, the following precautions must be executed.

- (1) Store them in a dark place. Do not expose to sunlight or fluorescent light. Keep the temperature between 5° C and 35° C at normal humidity.
- (2) The polarizer surface should not come in contact with any other object. It is recommended that they be stored in the container in which they were shipped.
- (3) It is recommended to use it in a short-time period, after it's unpacked. Otherwise, we would not guarantee the quality.

10.6 Others

When disposing LCD module, obey the local environmental regulations.