SPECIFICATIONS FOR OLED MODULE

MODEL NO.
BL12864JERNH$
VER.04

FOR MESSRS:

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ON DATE OF:

_____

APPROVED BY:

_____

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History of Version

Version	Contents	Date	Note
01	NEW VERSION	2012/08/15	SPEC.
02	Modify Cover page Modify Operating life time	2012/10/17	Cover page PAGE 5
03	Modify Quality Assurance	2013/01/21	Page 23
04	Modify Electrical Characteristics	2013/05/14	Page 6

C O N T E N T S

1. Numbering System

	B	L	12864	J	E	R	N	-	H	$
	0	1	2	3	4	5	6	7	8	9

0	Brand	Bolymin	
1	Module Type	C= character type G= graphic type P= TAB/TCP type R=color STN	O= COG type F= COF type L=PLED/OLED
2	Format	2002=20 characters, 2 lines 12232= 122 x 32 dots	
3	Version No.	A type	
4	LCD Color	W=OLED/White G=STN/gray Y=STN/yellow-green C=color STN	B=blue F=FSTN T=TN
5	LCD Type	R=positive/reflective P=positive/transflective	M=positive/transmissive N=negative/transmissive
6	Backlight type/color	L=LED array/ yellow-green H=LED edge/white R=LED array/red G=LED edge/yellow-green F=RGB Q=LED edge/red A=LED edge/amber N=No backlight	D=LED edge/blue E=EL/white B=EL/blue C=CCFL/white Y=LED Bottom/yellow O=LED array/orange K=LED edge/green A=LED edge/amber
7	CGRAM Font (applied only on character type)	J=English/Japanese Font E=English/European Font G=Chinese(simple) F=Chinese(traditional)	C=English/Cyrillic Font H=English/Hebrew Font A=English/Arabic Font
8	View Angle/ Operating Temperature	B=Bottom/Normal Temperature H=Bottom/Wide Temperature U=Bottom/Ultra wide Temperature	T=Top/Normal Temperature W=Top/Wide Temperature C=9H/Normal Temperature E=Top/ultra wide temperature
9	Special Code	n=positive voltage for LCD $:RoHS	

2. General Specification

(1) Mechanical Dimension

Item	Standard Value	Unit
Number of dots	128x64	dots
Module dimension (L*W*H)	41.9*65.1*1.6	mm
View area	38.45*20.21	mm
Active area	36.45*18.21	mm
Dot size	0.255(W)x0.255(H)	mm
Dot pitch	0.285(W)x0.285 (H)	mm

(2) Controller IC: SSD1325 Controller

(3) Temperature Range

Operating		-40 ~ +70℃
Storage		-40 ~ +85℃

3. Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	TOP	-40	—	+70	℃
Storage Temperature	TST	-40	—	+85	℃
Input Voltage (VDD)	VDD	-0.3	—	3.5	V
Supply Voltage (Vcc)	Vcc	8	—	16	V
Humidity	—	—	—	85	%
Operating life time	—	—	40000(1)	—	Hrs
Operating life time	—	—	50000(2)	—	Hrs
Operating life time	—	—	60000(3)	—	Hrs

Note: (A) Under Vcc = 14V, Ta = 25°C, 50% RH.

(B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.

(C) Note (1)、Note (2)、Note (3) contrast setting are under VDD = 2.7V

(1) Setting of 100 cd/m :

Contrast setting :0x68H Frame rate : 105Hz Duty setting : 1/64

(2) Setting of 80 cd/m :

Contrast setting :0x4FH Frame rate : 105Hz Duty setting : 1/64

(3) Setting of 60 cd/m :

Contrast setting :0x3AH Frame rate : 105Hz Duty setting : 1/64

4. Electrical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage For Logic	V_{DD}-V_{SS}	–	2.4	2.7	3.5	V
Supply Voltage For Panel	Vcc-Vss	–	13.5	14	14.5	V
Input High Vol	V_{IH}	–	$0.8V_{DD}$	–	V_{DD}	V
Input Low Vol	V_{IL}	–	0	–	$0.2V_{DD}$	V
Output High Vol	V_{OH}	–	$0.9V_{DD}$	–	V_{DD}	V
Output Low Vol.	V_{OL}	–	0	–	$0.1V_{DD}$	V
Supply Current (Contrast setting:0x4FH All pixels ON)	I_{DD}	–	–	18	20	mA
Supply Current	I_{CC}	–	–	700	–	uA

5. Optical Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit
View Angle	θ	160	–	–	deg
Dark Room contrast	CR	2000:1	–	–	–
Response Time	T	–	10	–	us

6. Interface Pin Function

6. **1 Pin Description**

Pin No.	Symbol	Level	Description
1	Vss	0V	Ground
2	VSL	—	This pin is the output pin for the voltage output low level for SEG signals. This pin can be kept NC or connected with a capacitor to VSS for stability.
3	Vcc	—	Positive OLED high voltage power supply
4	VCOMH	—	The COM voltage reference pin, this pin should be connected to ground through a capacitor
5	VDD	H/L	Voltage power supply for logic
6	BS1	H/L	Interface select pin
7	BS2	H/L	Interface select pin
8	CS#	H/L	Chip select pin. The driver IC will be selected When CS pin is active low.
9	RES#	H/L	Hardware reset signal
10	D/C#	H/L	This is data/command control pin, H: Data input ,L: Command input .
11	R/W#	H/L	Write strobe signal and reads data at the low level
12	E(RD)	H/L	Read strobe signal and reads data at the low level
13	DB0	H/L	Data bus line
14	DB1	H/L	Data bus line
15	DB2	H/L	Data bus line
16	DB3	H/L	Data bus line
17	DB4	H/L	Data bus line
18	DB5	H/L	Data bus line
19	DB6	H/L	Data bus line
20	DB7	H/L	Data bus line
21	IREF	—	The current reference input pin, this pin should be connected to ground through a resistor.
22	Vcc	—	Positive OLED high voltage power supply
23	NC	—	No connection
24	Vss	—	This is ground pin

6.1 MCU Interface Selection

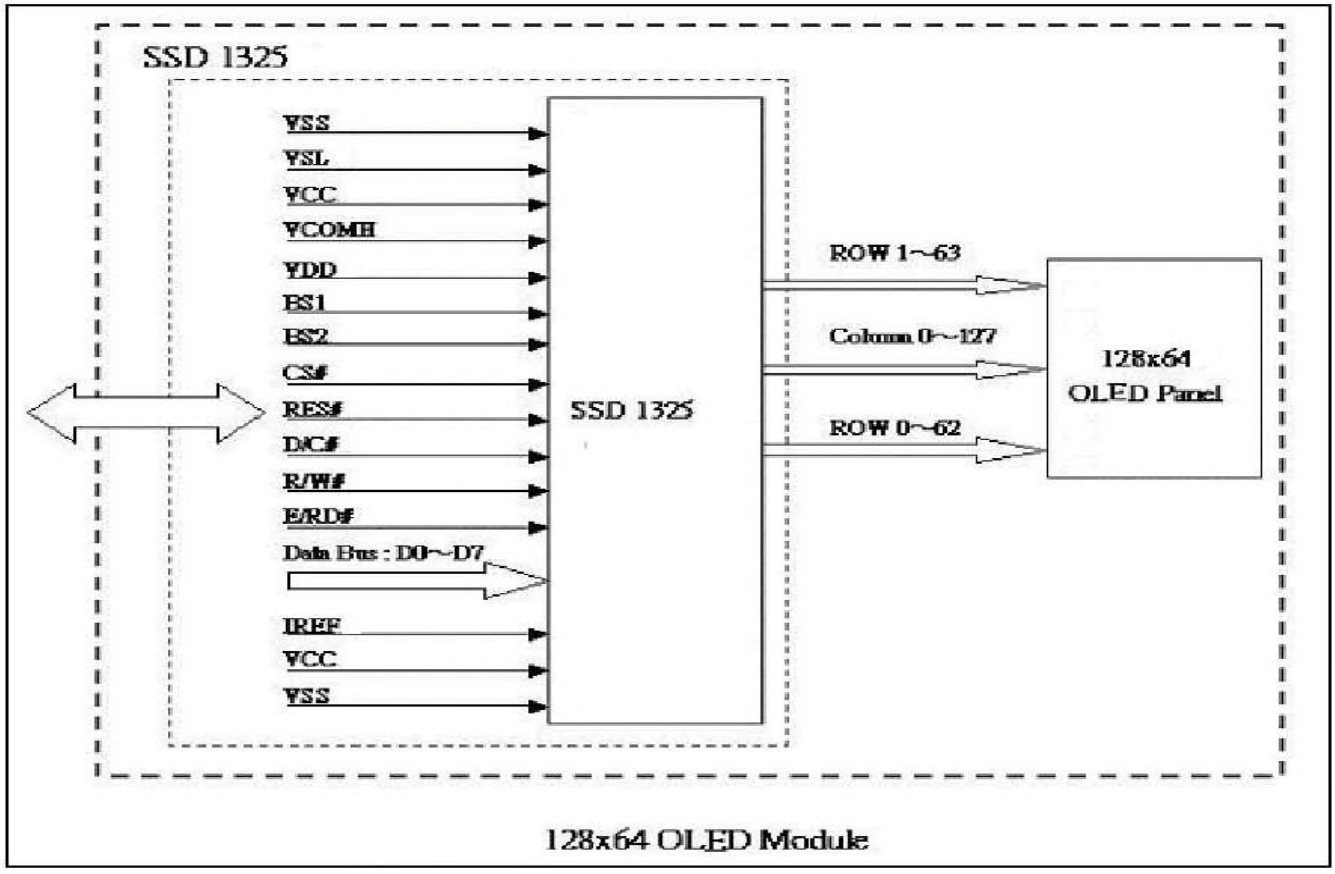
Bus Interface selection

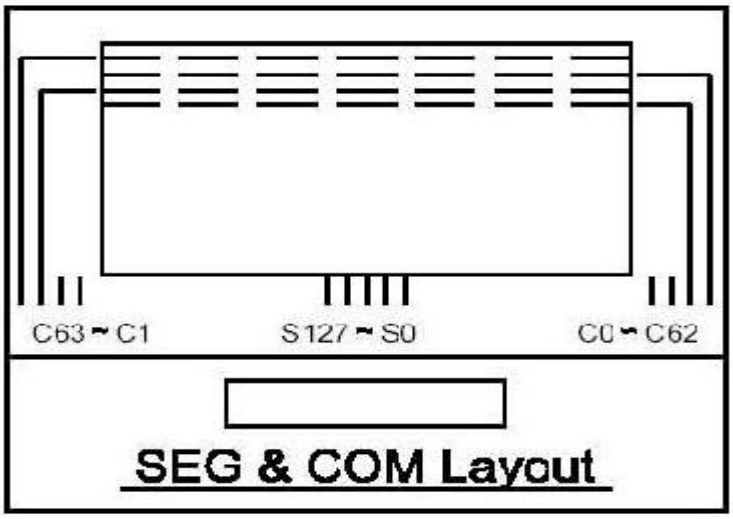
	6800-parallel interface (8 bit)	8080-parallel interface (8 bit)	Serial interface
BS1	0	1	0
BS2	1	1	0

MCU interface assignment under different bus interface mode

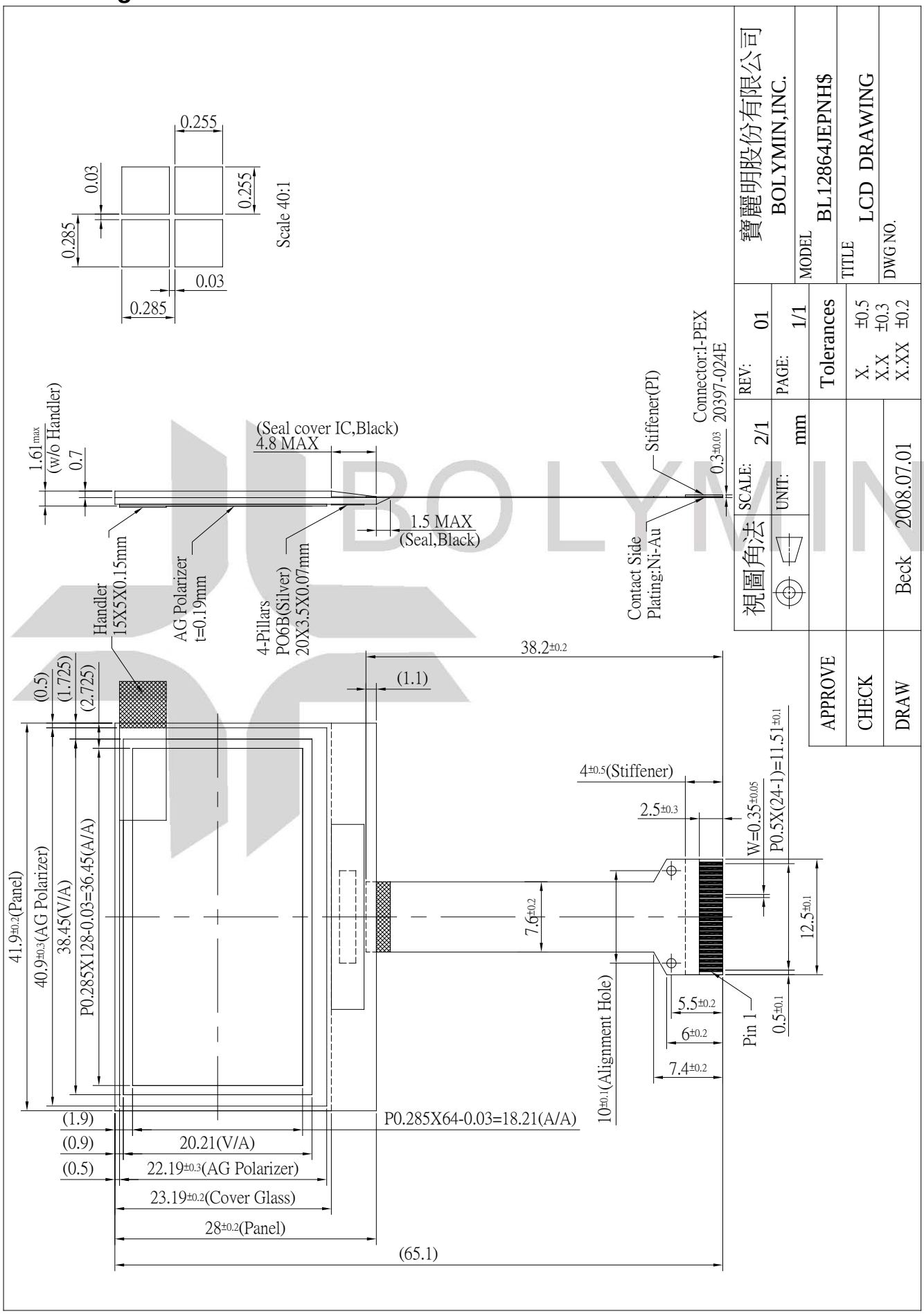
Pin Name / Bus Interface	Data/Command Interface								Control Signal				
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**E**	**R/W#**	**CS#**	**D/C#**	**RES#**
8-bit 8080	D[7:0]								RD#	WR#	CS#	D/C#	RES#
8-bit 6800	D[7:0]								E	R/W#	CS#	D/C#	RES#
SPI	Tie LOW					NC	SDIN	SCLK	Tie LOW		CS#	D/C#	RES#

7. Block Diagram





8. Drawing


寶麗明股份有限公司
BOLYMIN,INC.
MODEL
BL12864JEPNH$
TITLE
LCD DRAWING
DWG NO.
REV: 01
PAGE: 1/1
SCALE: 2/1
UNIT: mm
視圖角法
Tolerances
X. ±0.5
X.X ±0.3
X.XX ±0.2
APPROVE
CHECK
DRAW
Beck 2008.07.01
Scale 40:1
0.255
0.03
0.285
1.61max (w/o Handler)
0.7
(Seal cover IC,Black)
4.8 MAX
1.5 MAX
(Seal,Black)
Stiffener(PI)
Connector:I-PEX 20397-024E
0.3±0.03
Handler 15X5X0.15mm
AG Polarizer t=0.19mm
4-Pillars PO6B(Silver) 20X3.5X0.07mm
Contact Side Plating:Ni-Au
38.2±0.2
(1.1)
(0.5)
(1.725)
(2.725)
41.9±0.2(Panel)
40.9±0.3(AG Polarizer)
38.45(V/A)
P0.285X128-0.03=36.45(A/A)
4±0.5(Stiffener)
2.5±0.3
W=0.35±0.05
P0.5X(24-1)=11.51±0.1
7.6±0.2
12.5±0.1
10±0.1(Alignment Hole)
5.5±0.2
6±0.2
7.4±0.2
Pin 1
0.5±0.1
(1.9)
P0.285X64-0.03=18.21(A/A)
(0.9)
20.21(V/A)
(0.5)
22.19±0.3(AG Polarizer)
23.19±0.2(Cover Glass)
28±0.2(Panel)
(65.1)

9. SSD1325controller data

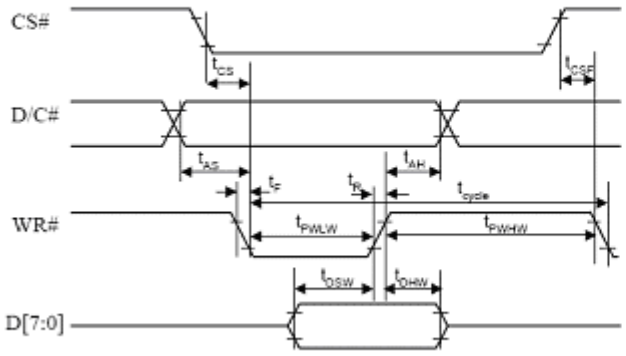
9.1 Timing Characteristics

8080 MPU Interface

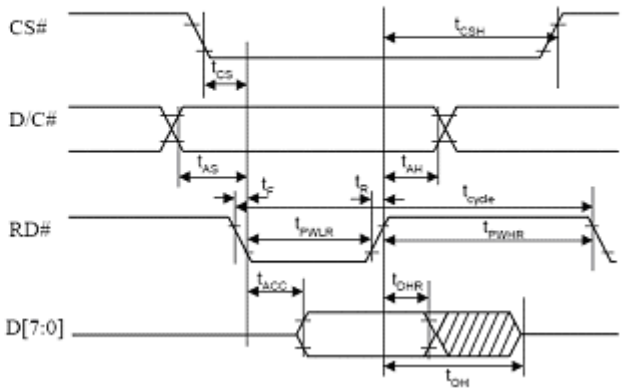
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	120	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

8080-series parallel interface characteristics (Form 1)

Write cycle (Form 1)

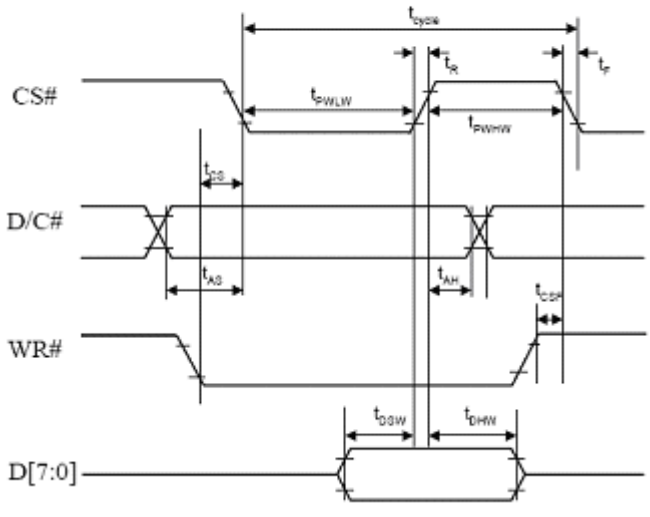


Read cycle (Form 1)

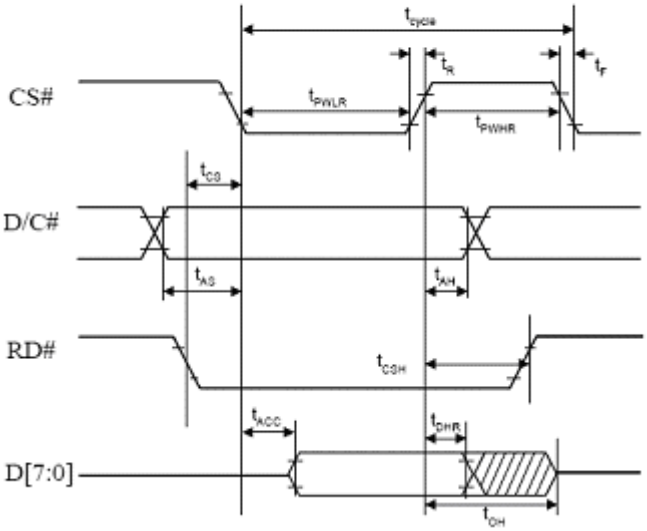


8080-series parallel interface characteristics (Form 2)

Write cycle (Form 2)



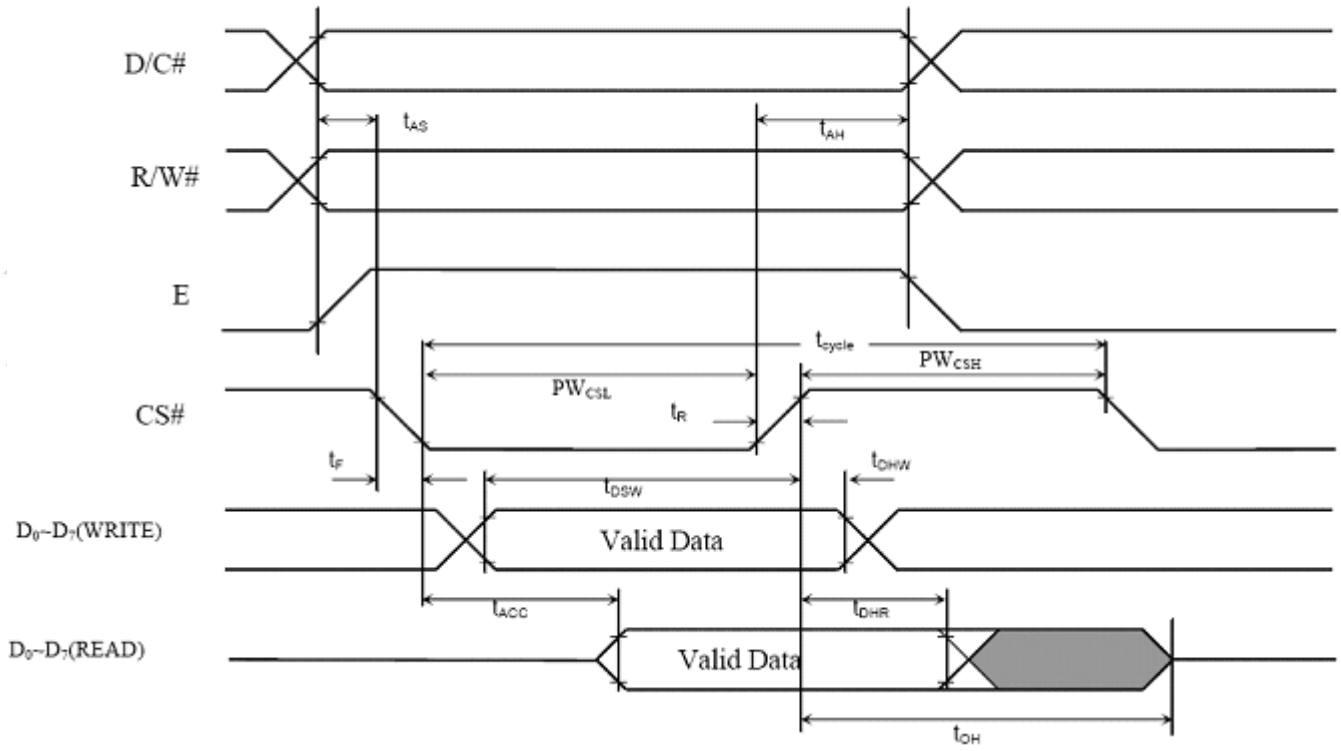
Read cycle (Form 2)



6800 MPU Interface

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

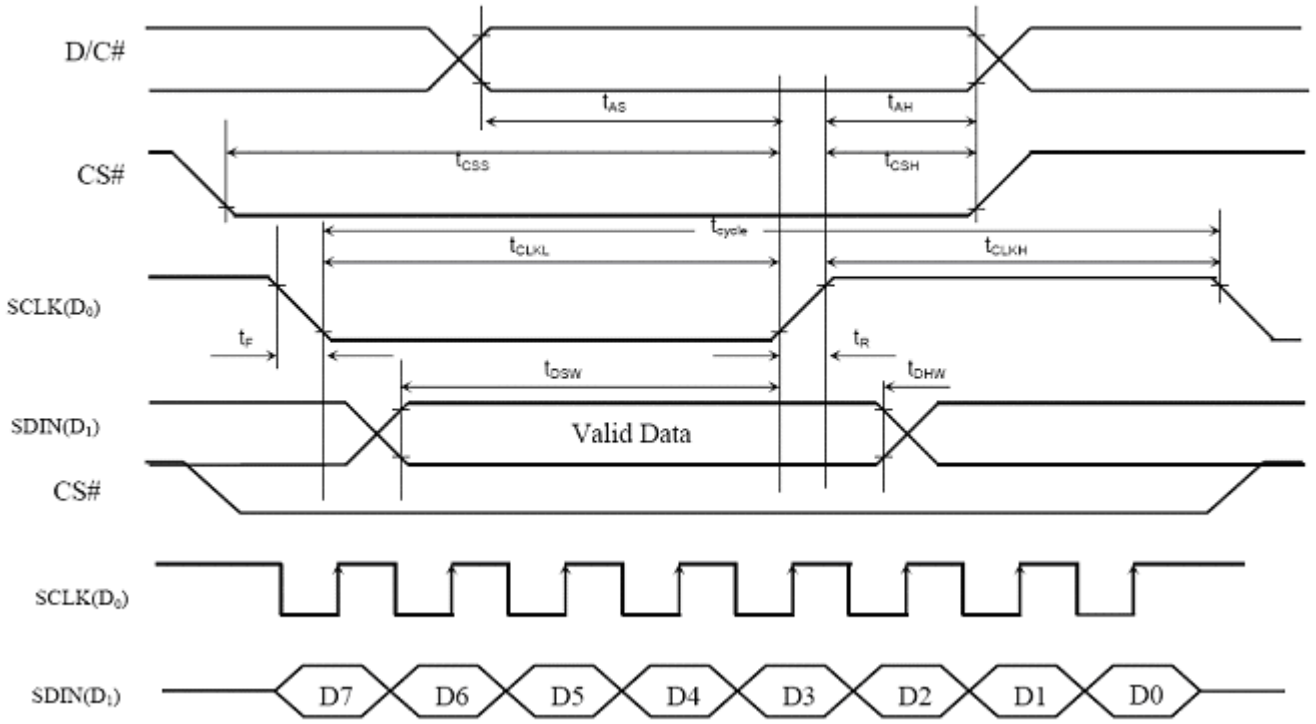
6800-series MPU Parallel Interface Characteristics



Serial Interface

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	100	-	-	ns
t_{DHW}	Write Data Hold Time	100	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Serial Interface Characteristics



9.2 Display Control Instruction

Command Table

(D/C# = 0, R/W# (WR#) = 0, E (RD#) = 1) unless specific setting is stated

Fundamental Command Table											
D/C	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0 0 0	15 A[5:0] B[5:0]	0 * *	0 * *	0 A_5 B_5	1 A_4 B_4	0 A_3 B_3	1 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Column Address	Second command A[5:0] sets the column start address from 0-63, POR = 00h Third command B[5:0] sets the column end address from 0-63, RESET = 3Fh
0 0 0	75 A[6:0] B[6:0]	0 * *	1 A_6 B_6	1 A_5 B_5	1 A_4 B_4	0 A_3 B_3	1 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Row address	Second command A[6:0]sets the row start address from 0-79, RESET = 00h Third command B[6:0] sets the row end address from 0-79, RESET = 4Fh
0 0	81 A[6:0]	1 *	0 A_6	0 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Contrast Current	Double byte command to select 1 out of 128 contrast steps. Contrast increases as level increase The level is set to 40h after RESET
0	84~86	1	0	0	0	0	1	X_1	X_0	Set Current Range	84h = Quarter Current Range (RESET) 85h = Half Current Range 86h = Full Current Range
0 0	A0 A[6:0]	1 *	0 A_6	1 A_5	0 A_4	0 A_3	0 A_2	0 A_1	0 A_0	Set Re-map	A[0]=0, Disable Column Address Re-map (RESET) A[0]=1, Enable Column Address Re-map A[1]=0, Disable Nibble Re-map (RESET) A[1]=1, Enable Nibble Re-map A[2]=0, Horizontal Address Increment (RESET) A[2]=1, Vertical Address Increment A[4]=0, Disable COM Re-map disable (RESET) A[4]=1, Enable COM Re-map A[5]=0, Reserved (RESET) A[5]=1, Reserved A[6]=0, Disable COM Split Odd Even (RESET) A[6]=1, Enable COM Split Odd Even
0 0	A1 A[6:0]	1 *	0 A_6	1 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Display Start Line	Set display RAM display start line register from 0-79 Display start line register is reset to 00h after RESET
0 0	A2 A[6:0]	1 *	0 A_6	1 A_5	0 A_4	0 A_3	0 A_2	1 A_1	0 A_0	Set Display Offset	Set vertical scroll by COM from 0-79 The value is reset to 00H after RESET
0	A4~A7	1	0	1	0	0	X_2	X_1	X_0	Set Display Mode	A4h = Normal Display (RESET) A5h = Entire Display ON,

Fundamental Command Table											
D/C	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
											all pixels turns ON in GS level 15 A6h = Entire Display OFF, all pixels turns OFF A 7h = Inverse Display
0 0	A8 A[6:0]	1 *	0 A_6	1 A_5	0 A_4	1 A_3	0 A_2	0 A_1	0 A_0	Set Multiplex Ratio	The next command determines multiplex ratio N from 16MUX-80MUX, A[6:0] = 15 represents 16MUX A[6:0] = 16 represents 17MUX : A[6:0] = 78 represents 79MUX A[6:0] = 79 represents 80MUX
0 0	AD A[1:0]	1 *	0 *	1 *	0 *	1 *	1 *	0 1	1 A_0	Set Master Configuration	A[0] = 0, Select external V_{CC} supply A[0] = 1, Reserved (RESET) **Note** (1) Bit A[0] **must be** set to 0b after RESET. (2) The setting will be activated after issuing Set Display ON command (AFh)
0	AE	1	0	1	0	1	1	1	0	Set Display OFF	AEh = Display OFF (Sleep mode) (RESET)
0	AF	1	0	1	0	1	1	1	1	Set Display ON	AFh = Display ON
0 0	B0 A[5:0]	1 *	0 *	1 A_5	1 A_4	0 A_3	0 A_2	0 A_1	0 A_0	Set Pre-charge Compensation Enable	A[5:0] = 08h (RESET) A[5:0] = 28h, Enable pre-charge compensation
0 0 0	B1 A[3:0] A[7:4]	1 * A_7	0 * A_6	1 * A_5	1 * A_4	0 A_3 *	0 A_2 *	0 A_1 *	1 A_0 *	Set Phase Length	A[3:0] = P1, phase 1 period of 1-15 DCLKs, RESET = 3DCLKS = 3h A[7:4] = P2, phase 2 period of 1-15 DCLKs, RESET = 5DCLKS = 5h Note (1) 0 DCLK is invalid in phase 1 & phase 2
0 0	B2 A[7:0]	1 A_7	0 A_6	1 A_5	1 A_4	0 A_3	0 A_2	1 A_1	0 A_0	Set Row Period (set frame frequency)	The next command sets the number of DCLKs, K, per row between 2-158 DCLKS RESET = 37DCLKS = 25h The K value should be set as K = P1+P2+GS15 pulse width (RESET: 3+5+29DCLKS)
0 0 0	B3 A[3:0] A[7:4]	1 * A_7	0 * A_6	1 * A_5	1 * A_4	0 A_3 *	0 A_2 *	1 A_1 *	1 A_0 *	Set Display Clock Divide Ratio / Oscillator Frequency	The lower nibble (A[3:0]) of the next command defines the divide ratio (D) of display clock (DCLK) Divide ratio (D)=A[3:0]+1 (A[3:0]RESET is 0001b, i.e. divide ratio (D) = 2)

Fundamental Command Table											
D/C	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
											The higher nibble (A[7:4]) of the next command sets the Oscillator Frequency Oscillator Frequency increases with the value of A[7:4] and vice versa Range: 0000b~1111b RESET= 0100b represents 655KHz, typical step value: 5% of previous value
0	B4	1	0	1	1	0	1	0	0	Set Pre-charge	A[2:0] = 0 (RESET)
0	A[2:0]	*	*	*	*	*	A_2	A_1	A_0	Compensation Level	A[2:0] = 3h, Recommended level
0	B8	1	0	1	1	1	0	0	0	Set Gray Scale Table	The next eight bytes of command set the gray scale level of GS1-15 as below:
0	A[2:0]	*	*	*	*	*	A_2	A_1	A_0		A[2:0] = Gray scale level of GS1, RESET=1
0	B[2:0]	*	*	*	*	*	B_2	B_1	B_0		B[2:0] = Gray scale level of GS2, RESET=1
0	B[6:4]	*	B_6	B_5	B_4	*	*	*	*		B[6:4] = Gray scale level of GS3, RESET=1
0	C[2:0]	*	*	*	*	*	C_2	C_1	C_0		C[2:0] = Gray scale level of GS4 RESET=1
0	C[6:4]	*	C_6	C_5	C_4	*	*	*	*		C[6:4] = Gray scale level of GS5, RESET=1
0	D[2:0]	*	*	*	*	*	D_2	D_1	D_0		D[2:0] = Gray scale level of GS6, RESET=1
0	D[6:4]	*	D_6	D_5	D_4	*	*	*	*		D[6:4] = Gray scale level of GS7, RESET=1
0	E[2:0]	*	*	*	*	*	E_2	E_1	E_0		E[2:0] = Gray scale level of GS8, RESET=1
0	E[6:4]	*	E_6	E_5	E_4	*	*	*	*		E[6:4] = Gray scale level of GS9, RESET=1
0	F[2:0]	*	*	*	*	*	F_2	F_1	F_0		F[2:0] = Gray scale level of GS10, RESET=1
0	F[6:4]	*	F_6	F_5	F_4	*	*	*	*		F[6:4] = Gray scale level of GS11, RESET=1
0	G[2:0]	*	*	*	*	*	G_2	G_1	G_0		G[2:0] = Gray scale level of GS12, RESET=1
0	G[6:4]	*	G_6	G_5	G_4	*	*	*	*		G[6:4] = Gray scale level of GS13, RESET=1
0	H[2:0]	*	*	*	*	*	H_2	H_1	H_0		H[2:0] = Gray scale level of GS14, RESET=1
0	H[6:4]	*	H_6	H_5	H_4	*	*	*	*		H[6:4] = Gray scale level of GS15, RESET=1
0	BC	1	0	1	1	1	1	0	0	Set Precharge Voltage	Second command A[7:0] sets the precharge voltage level, A[7:0] 1xxxxxxx connects to V_{COMH} (RESET) 001xxxxx 1.0 * V_{REF} 00000000 0.51* V_{REF} 00000001 0.52* V_{REF} ..... 00011111 0.84* V_{REF}
0	A[7:0]	A7	A6	A5	A4	A3	A2	A1	A0		
0	BE	1	0	1	1	1	1	1	0	Set V_{COMH} Voltage	Second command A[4:0] sets the V_{COMH} voltage level , A[4:0] 00000 0.51*V_{REF} 00001 0.52* V_{REF} ..... 11101 0.81* V_{REF} (RESET) 11110 0.82* V_{REF} 11111 0.84* V_{REF}
0	A[4 :0]	*	*	0	A4	A3	A2	A1	A0		
0	BF	1	0	1	1	1	1	1	1	Set Segment Low Voltage (VSL)	Second command A[3:0] sets the VSL voltage as follow: A[3:0] = 0010 kept VSL pin NC A[3:0] = 1110 (RESET) connect a capacitor between VSL pin and V_{SS}
0	A[3:0]	*	*	*	*	A_3	A_2	A_1	A_0		
0	E3	1	1	1	0	0	0	1	1	NOP	Command for No Operation

Graphic acceleration command

Set (GAC) (D/C# = 0, R/W#(WR#)= 0, E(RD#) = 1) unless specific setting is stated

Graphic acceleration command											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D2**	**D0**	**Command**	**Description**
0	23	0	0	1	0	0	0	1	1	Graphic Acceleration Command Options	A[0] = 0b: Disable Fill rectangle A[0] = 1b: Enable Fill rectangle (RESET) A[1] = 0b: Disable x-wrap(RESET) A[1] = 1b: Enable wrap around in x-direction during copying and scrolling A[4] = 0b: Disable reverse copy (RESET) A[4] = 1b: Enable reverse during copying.
0	A[4:0]	*	*	*	A_4	*	*	A_1	A_0		
0	24	0	0	1	0	0	1	0	0	Draw Rectangle	A[5:0]: Column Address of Start B[6:0]: Row Address of Start C[5:0]: Column Address of End D[6:0]: Row Address of End E[7:0]: Set Gray scale pattern E[7:0] This byte is divided into two nibbles. The most significant 4 bits represent the gray scale level of the left pixel of each group. The least significant 4 bits represent the gray scale level of the right pixel of each group. Please refer to Figure 33 for the gray scale pattern setting examples. **Note**: (1) $0 \le A < C \le 63$ (2) $0 \le B < D \le 79$
0	A[5:0]	*	*	A_5	A_4	A_3	A_2	A_1	A_0		
0	B[6:0]	*	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	C[5:0]	*	*	C_5	C_4	C_3	C_2	C_1	C_0		
0	D[6:0]	*	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
0	E[7:0]	E_7	E_6	E_5	E_4	E_3	E_2	E_1	E_0		
0	25	0	0	1	0	0	1	0	1	Copy	A[5:0]: Column Address of Start B[6:0]: Row Address of Start C[5:0]: Column Address of End D[6:0]: Row Address of End E[5:0]: Column Address of New Start F[6:0]: Row Address of New Start **Note**: (1) $0 \le A < C \le 63$ (2) $0 \le B < D \le 79$ (3) $0 \le E \le 63$ (4) $0 \le F \le 79$
0	A[5:0]	*	*	A_5	A_4	A_3	A_2	A_1	A_0		
0	B[6:0]	*	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	C[5:0]	*	*	C_5	C_4	C_3	C_2	C_1	C_0		
0	D[6:0]	*	D_6	D_5	D_4	D_3	D_2	D_1	D_0		
0	E[5:0]	*	*	E_5	E_4	E_3	E_2	E_1	E_0		
0	F[6:0]	*	F_6	F_5	F_4	F_3	F_2	F_1	F_0		

Graphic acceleration command											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D2**	**D0**	**Command**	**Description**
0	26	0	0	1	0	0	1	1	0	Horizontal Scroll	A[5:0]: 1~63 horizontal offset in number of 2~127 column 0 no horizontal scroll B[6:0]: 2~80 number of rows to be H-scrolled C[1:0]: scrolling time interval 00b 12 frames 01b 64 frames 10b 128 frames 11b 256 frames **Note:** (1) Scrolling operates during display ON. (2) The parameters should not be changed after scrolling is activated
0	A[5:0]	*	*	A_5	A_4	A_3	A_2	A_1	A_0		
0	B[6:0]	*	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	C[1:0]	*	*	*	*	*	*	C_1	C_0		
0	2E	0	0	1	0	1	1	1	0	Stop Moving	This command deactivates the scrolling action. **Note** (1) After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten.
0	2F	0	0	1	0	1	1	1	1	Start Moving	This command activates the scrolling function according to the setting done by Horizontal Scroll command 26h. **Note** (1) The "wrap around in x-direction" function must be enabled before scrolling start. i.e. Bit A{1} of command 23h must be set to 1b before issuing 2F command.

Read Command Table

(D/C#=0, R/W# (WR#)=1, E (RD#)=1 for 6800 or E (RD#)=0 for 8080)

$D_7D_6D_5D_4D_3D_2D_1$ D_0	Status Register Read	D7 = 0:reserved D7 = 1:reserved D6 = 0:indicates the display is ON D6 = 1:indicated the display is OFF D5 = 0:reserved D5 = 1:reserved D4 = 0:reserved D4 = 1:reserved

Note

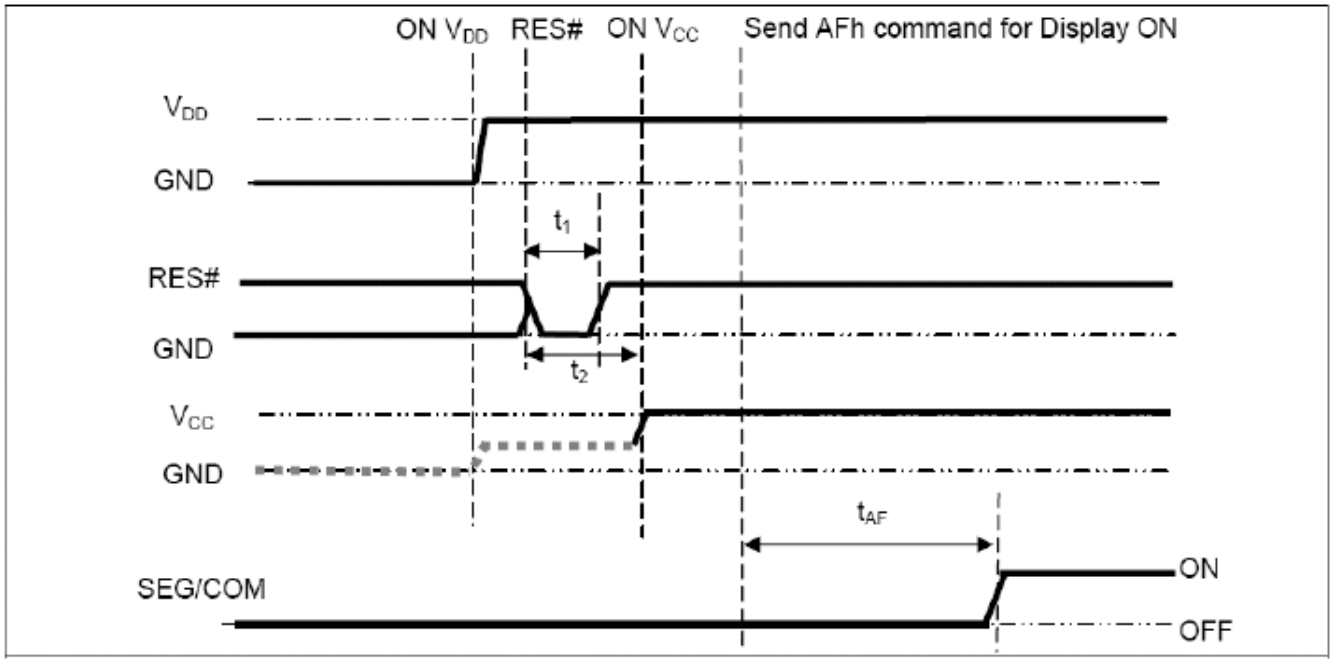
(1) Patterns other than that given in Command Table are prohibited to enter to the chip as a command; Otherwise, unexpected result will occur

9.3Power ON and OFF sequence& Application Circuit

9.3.1 POWER ON / OFF SEQUENCE

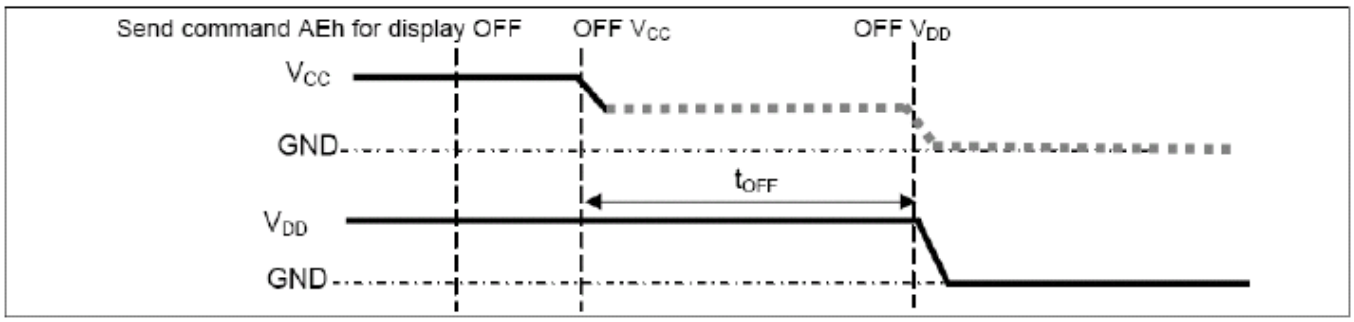
Power ON sequence:

1. Power ON V_{DD}.
2. After V_{DD} become stable, set RES# pin LOW (logic low) for at least 3us(t_1) and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 3us(t_2).Then Power ON V_{CC}.(1)
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM wil be ON after 100ms(t_{AF}).



Power OFF sequence:

1. Send command AEh for display OFF.
2. Wait until panel discharges completely.
3. Power OFF V_{CC}. (1), (2)
4. Wait for t_{OFF}. Power OFF V_{DD}. (where Minimum t_{OFF}=80ms, Typical t_{OFF}=100ms)

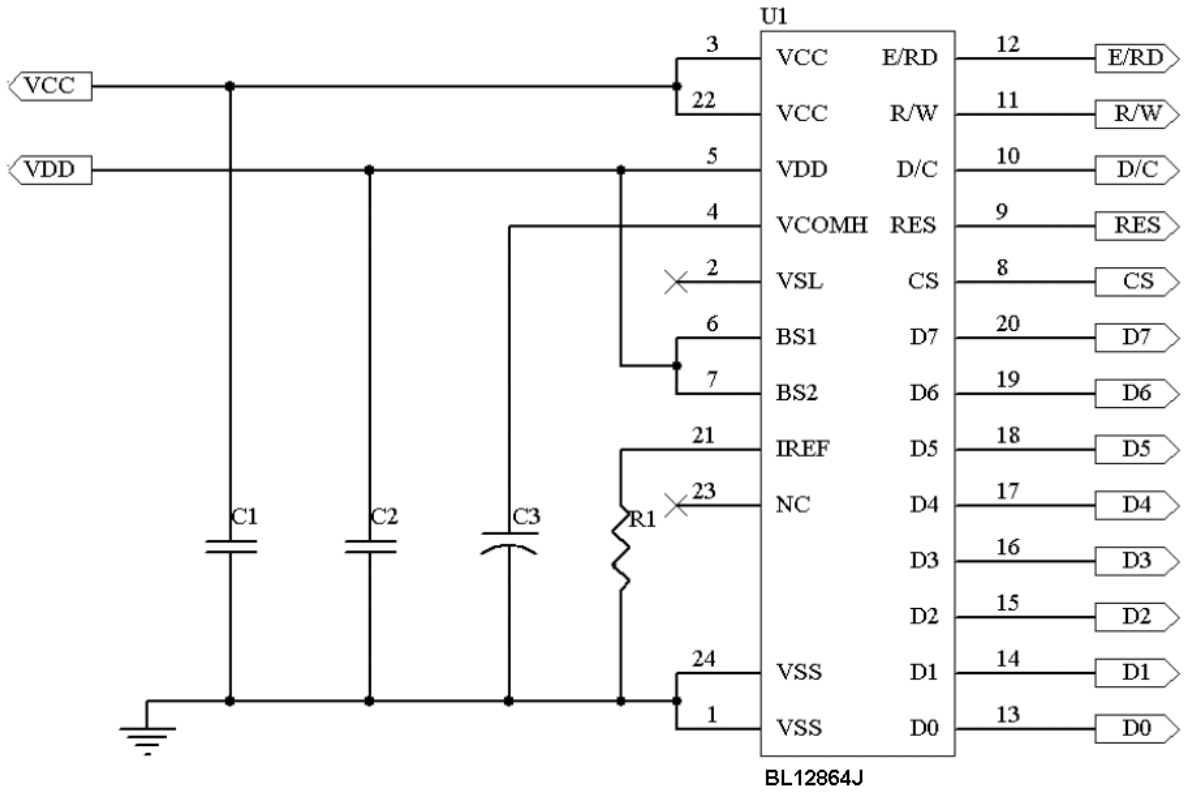


Note:

(1) Since an ESD protection circuit is connected between VDD and VCC,VCC becomes lower than VDD whenever VDD is ON and VCC is OFF as shown in the dotted line of VCC in above figures.

(2)VCC should be disabled when it is OFF.

9.3.2 Application circuit



Recommend Components:

C1: 2.2uF/25V (0805)

C2: 1uF/16V (0603)

C3: 4.7uF/25V (TANTALUM or Solid Tantalum 4.7uF/25V/A Case (Vishay 572D))

R1: 1M ohm/1% (0805)

Note: This circuit is for 8080 interface

10 Quality Assurance

10.1 Inspection conditions

1. The inspection and meaurement are performed under the following conditions,
2. unless otherwise specified.
3. Temperature: 25±5°C
4. Humidity: 50±10%R.H.
5. Distance between the panel and eyes of the inspector≧30cm

10.2 Inspection Parameters

Severity	Inspection Item	Defect	Remark
Major Defect	1. Panel	(1) Non-displaying	
		(2) Line defects	
		(3) Malfunction	
		(4) Glass cracked	
	2. Film	(1) Film dimension out of specification	Can not be assembled
	3. Dimension	(1) Outline dimension out of specification	
Minor Defect	1. Panel	(1) Glass scratch	Appearance defect
		(2) Glass cutting NG	
		(3) Glass chip	
	2. Polarizer	(1) Polarizer scratch	
		(2) Stains on surface	
		(3) Polarizer bubbles	
	3. Displaying	(1) Dim spot、Bright spot、dust	
	4. Film	(1) Damage (2) Foreign material	

<table>
<tr><th>Description</th><th>Criterion</th><th>AQL</th></tr>
<tr><td>1. Glass scratch</td><td>
<table>
<tr><th>Width (mm)
W</th><th>Length (mm)
L</th><th>number of pieces permitted</th></tr>
<tr><td>W≦0.03</td><td>Ignore</td><td>Ignore</td></tr>
<tr><td>0.03＜ W≦0.05</td><td>L≦3</td><td>3</td></tr>
<tr><td>0.05＜ W</td><td>------</td><td>None</td></tr>
<tr><td>beyond A.A.</td><td>------</td><td>Ignore</td></tr>
</table>
</td><td>Minor</td></tr>
<tr><td>2. Polarizer bubble</td><td>
<table>
<tr><th>Size</th><th>number of pieces permitted</th></tr>
<tr><td>Φ ≦0.2</td><td>Ignore</td></tr>
<tr><td>0.2＜Φ ≦0.5</td><td>2</td></tr>
<tr><td>0.5＜Φ</td><td>0</td></tr>
<tr><td>beyond A.A.</td><td>Ignore</td></tr>
</table>
</td><td>Minor</td></tr>
<tr><td>3. Dimming spot、
Lighting spot、
Dust</td><td>
<table>
<tr><th>average</th><th>number of</th></tr>
<tr><td>D ≦0.1</td><td>Ignore</td></tr>
<tr><td>0.1＜ D ≦0.15</td><td>2</td></tr>
<tr><td>0.15＜ D ≦0.2</td><td>1</td></tr>
<tr><td>0.2 ＜ D</td><td>0</td></tr>
<tr><td>beyond A.A.</td><td>Ignore</td></tr>
</table>
D=(long diameter + short diameter)/2.
Pixel off is not allowed.
</td><td>Minor</td></tr>
</table>

10.3 WARRANTY POLICY

Bolymin . Will provide one-year warranty for the products only if under specification operating conditions.

If there are functional defects found during the period of warranty, the defective products would be replaced on a one-to-one basis.

Bolymin would not be responsible for any direct/indirect liabilities consequential to any parties.

10.4 MTBF

10.4.1 .MTBF based on specific test condition is 40K hours.

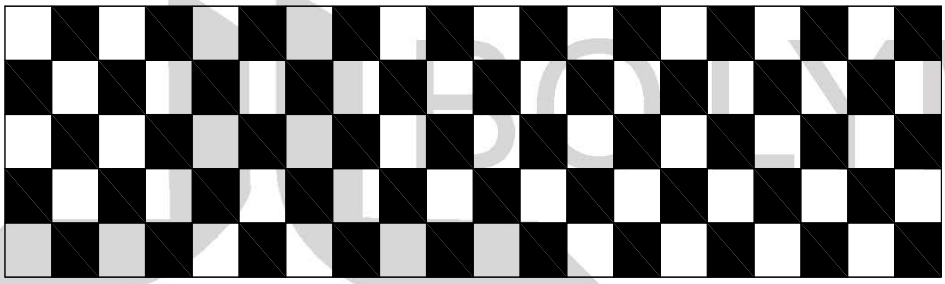
10.4.2 Test Condition:

10.4.2.1 Supply Voltage: Vcc=14V

10.4.2.2 Luminance: 100cd/m2

10.4.2.3 Operation temperature and humidity: 25 ℃ and 50%RH

10.4.2.4 Run-Patterns:



10.4.3 Test Criteria:

Luminace has decayed to less than 50% of the initial measured luminance.

11.Reliability

■**Content of Reliability Test**

NO.	Items.	Specification	Applicable Standard
1	High temp. (Non-operation)	85°C, 240hrs	——
2	High temp. (Operation)	70°C, 120hrs	——
3	Low temp. (Operation)	-40°C, 120hrs	——
4	High temp. / High. humidity (Operation)	65°C, 90%RH, 120hrs	——
5	Thermal shock(Non-operation)	-40°C ~85°C (-40°C /30min; transit /3min; 85°C /30min; transit /3min) 1cycle: 66min, 100 cycles.	——
6	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	——

Test and measurement conditions

1. All measurements shall not be started until the specimens attain to temperature stability.
2. All-pixels-on is used as operation test pattern.
3. The degradation of Polarizer are ignored for item 1 & 4 & 5.

Criteria

1. The function test is OK.
2. No observable defects.
3. Luminance: >50% of initial value.
4. Current consumption : within ±50% of initial value.

Reliability Test

Bolymin only guarantees the reliability of the panel under the test conditions and durations listed in the specification, and is not responsible for any test results that are conducted using more stringent conditions and/or with lengthened durations. Also, when the testing the panel in a chamber or oven, make sure they won't produce any condensation on the panel, especially on the electrical leads, before lighting on the panel to see if it passes the test. Also the panel should rest for about an hour at room temperature and pressure before the measurement, as indicated in the specification. Be aware that one should use fresh panel for each of the reliability test items listed in the specification, in other words, don't use the panels that were tested for subsequent tests.

12.Precautions for Handling

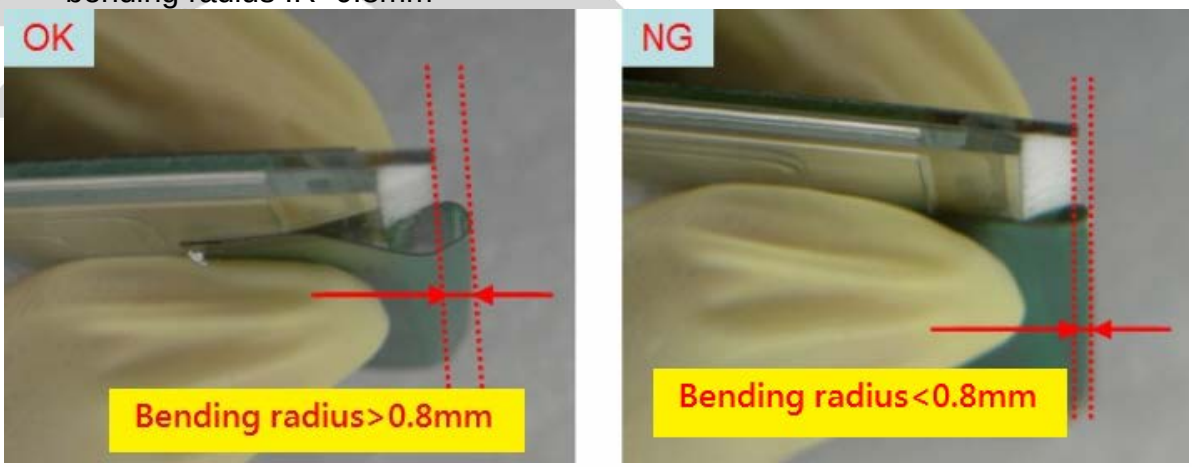
12.1 When handling the module, wear powder-free antistatic rubber finger cots, and be careful not to bend and twist it.

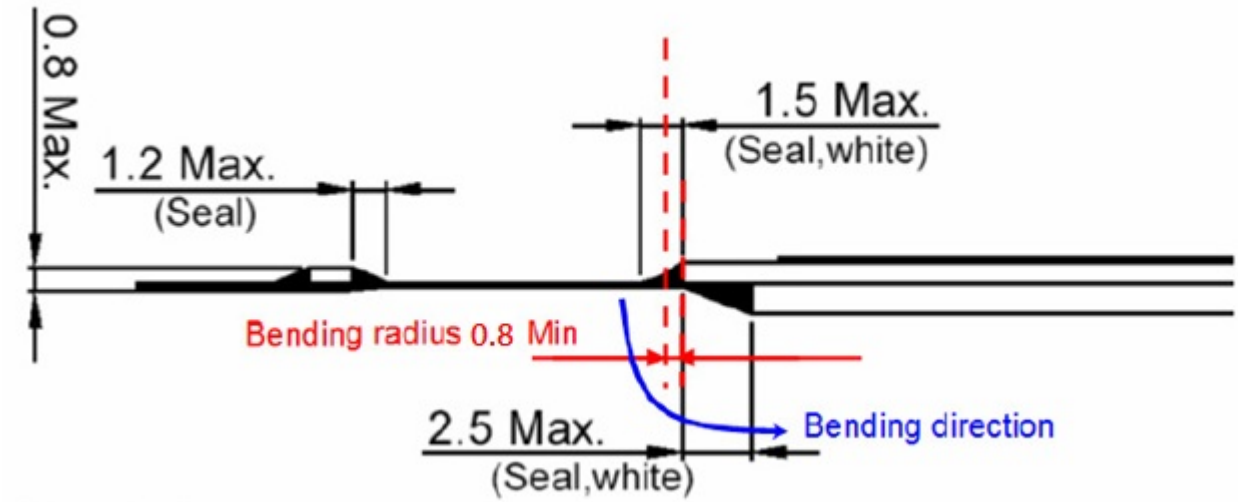
12.2 The OLED module is consisted of glass and film, and it should avoid pressure, strong impact, or being dropped from a height.

12.3 The OLED module is an electronic component and is subject to damage caused by Electro Static

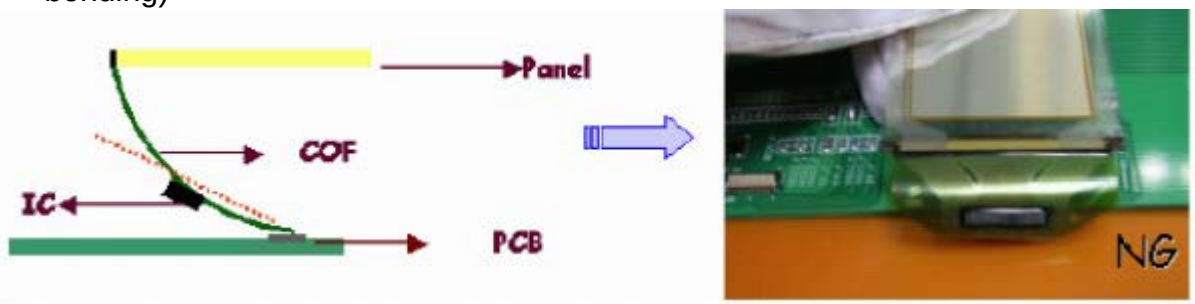
Discharge (ESD) and hence normal ESD precautions must be taken when handling it. Also, appropriate ESD protective environment must be administered and maintained in the production line. When handling and assembling the panel, wear an antistatic wrist strap with the alligator clip attached to the ground to prevent ESD damage on the panel. Also, ground the tools being used for panel assembly and make sure the working environment is not too dry to cause ESD problems. (See the photos below).

12.4 Please do not bend the film near the substrate glass.(this could cause film peeling and COF damage) and the peeling strength about 600g/cm, the bending <20times and the bending radius :R>0.8mm

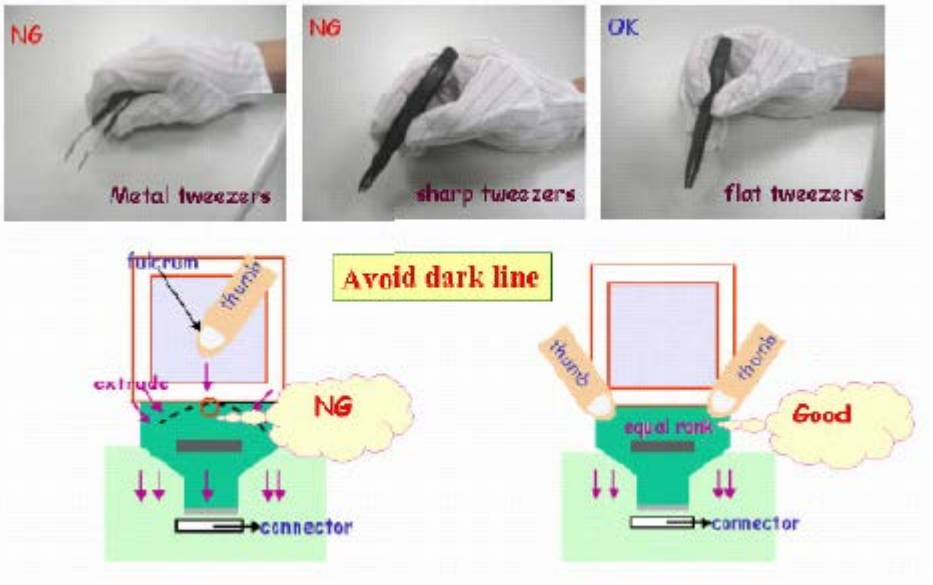




12.5 Avoid bending the film at IC bonding area.(>1.5mm)(this could damage the ILB bonding)



12.6 Use both thumbs to insert COF into the connector when assembling the panel. See the photo on the far right below for correct insertion of the film into the connector (one-handed insertion exerts uneven force on the film and could cause its breakage, photo on the left)



12.7 Do not wipe the pin of film with the dry or hard materials that will damage the surface. When cleaning the display surface, use soft cloth solvent and wipe gently (Recommend solvent: IPA, alcohol), and do not wipe the display with dry or hard materials that will damage the polarizer surface and do not use the solvent like: Water, Acetone, Aromatic

13. Precautions for Electrical

13.1. Design using the settings in the specification

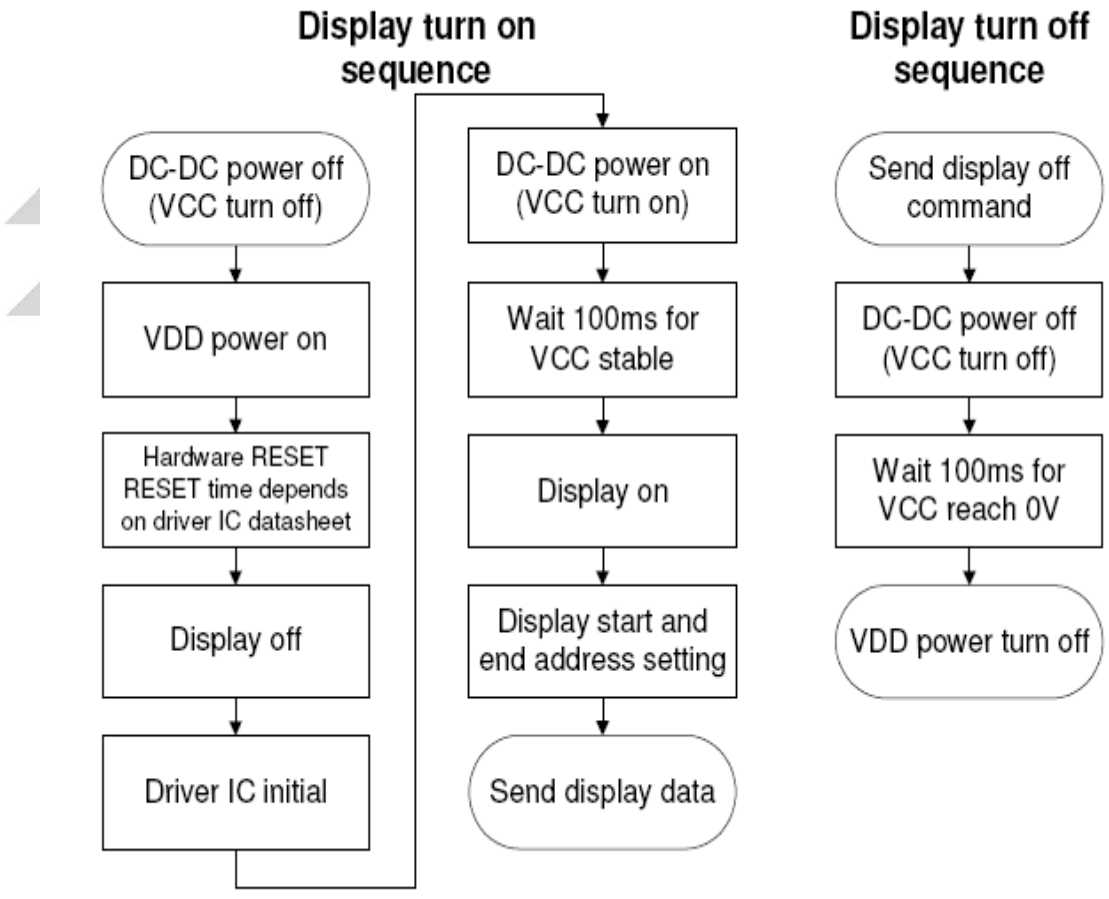
It is extremely important to design and operate the panel using the settings listed in the specification. This includes voltage, current, frame rate, duty cycle... etc. Operation of the OLED outside the specified range in the specification should be entirely avoided to ensure proper operation of the OLED.

13.2. Maximum Ratings

To ensure proper operation of the panel, never design the panel with parameters running over the maximum ratings listed in the specification. Also the logic voltages such as VIL and VIH have to be within the specified range in the specification to prevent any improper operation of the panel.

13.3 Power on/off procedure

Any operation that does not comply with the procedure could cause permanent damage of the IC and should be avoided. When the logic power is not on, do not activate any input signal. Abrupt shutdown of power to the module, while the OLED panel is on, could cause OLED panel malfunctioning.



13.4 Power savings

To save power consumption of the OLED, one can use partial display or sleep mode when the panel is not fully activated. Also, if possible, make maximum use of black background to save power. The OLED is a self-luminous device, and a particular pixel cluster or image can be lit on via software control, so power savings can be achieved by partial display or dimming down the luminance. Depending on the application, the user can choose among Ultra Bright Mode, Normal Operation Mode, and Sleeping Mode.

The power consumption is almost in direct proportion to the brightness of the panel, and also in direct proportion to the number of pixels lit on the panel, so the customer can save the power by the use of black background and Sleeping Mode. One benefit from using these design schemes is the extension of the OLED lifetime.

13.5 Residual Image (Image Sticking)

The OLED is a self-emissive device. As with other self-emissive device or displays consisting of self-emissive pixels, when a static image frozen for a long period of time is changed to another one with all-pixels-on background, residual image or image sticking is noticed by the human eye. Image sticking is due to the luminance difference or contrast between the pixels that were previously turned on and the pixels that are newly turned on. The time when image sticking happens depends on the luminance decay curve of the display. The slower the decay, the less prominent the image sticking is. It is strongly recommended that the user employ the following three strategies to minimize image sticking

13.5.1 Employ image scrolling or animation to even out the lit-on time of each and every pixel on the display, also could use sleeping mode for reduced the residual image and extend the power capacity.

13.5.2 Minimize the use of all-pixels-on or full white background in their application because when the panel is turned on full white, the image sticking from previously shown patterns is the most revealing. Black background is the best for power savings, greatest visibility, eye appealing, and dazzling displays

13.5.3 If in the reliability test when a static logo is used, change the pattern into its inverse (i.e., turn off the while pixels and turn on the previously unlit pixels) and freeze the inverse pattern as long as the original logo is used, so every pixel on the panel can be lit on for about the same time to minimize image sticking, caused by the differential turn-on time between the original and its reverse patterns

14. Precautions for Storage

Although the storage conditions and guarantee period are indicated in the specification, it is advisable to store the packed cartons or packages at 23℃±5℃,55%±10%RH, Do not store the OLED module under direct sunlight or UV light and for best panel performance, unpack the cartons and start the production with the panels within one months after the reception of them.