RTD2486AD-CG

Multi-Function Display Controller

Full Specification

Version 1.1
Last updated: 2015/11/21

1. Features

General
- Embedded 3 DDC with DDC1/2B/CI
- Zoom scaling up and down
- Embedded one MCU with SPI flash controller.
- It contains 4 ADCs in key pad application
- Require only one crystal to generate all timing.
- Programmable internal low-voltage-reset (LVR)
- High resolution 6 channels PWM output, and wide range selectable PWM frequency.
- Support input format up to FHD.
- Support 27MHz/24MHz/14.318MHz crystal type

Analog RGB Input Interface
- 1 Analog input supported
- Integrated 8-bit triple-channel 210MHz ADC/PLL
- Embedded programmable Schmitt trigger of HSYNC
- Support Sync-On-Green (SOG) and various kinds of composite sync modes
- On-chip high-performance hybrid PLLs
- High resolution true 64 phase ADC PLL
- YPbPr support up to HDTV 1080p resolution

DVI 1.0 Compliant Digital Input Interface with HDCP 1.1
- Single link on-chip TMDS receiver
- Adaptive algorithm for TMDS capability
- Data enable only mode support
- High-Bandwidth Digital Content Protection
- Enhanced Protection of HDCP secret key

DisplayPort 1.2 Digital Input Interface with HDCP 1.3
- Support 4 lanes digital input, each lanes speed up to 1.62Gbps and 2.7Gbps
- Support 6-bit, 8-bit, 10-bit and 12-bit color depth transport
- High-Bandwidth Digital Content Protection (HDCP 1.3)
- Capable of 8-channel I2S/SPDIF output in DP application

Embedded MCU
- Industrial standard 8051 core with external serial flash
- Low speed ADC for various application
- I2C Master or Slave hardware supported

Auto Detection /Auto Calibration
- Input format detection
- Compatibility with standard VESA mode and support user-defined mode
- Smart engine for Phase/Image position/Color calibration

Audio
- Output: IIS , SPDIF
- Embedded 2ch Audio DAC
- Embedded headphone amp

Scaling
- Fully programmable zoom ratios
- Independent horizontal/vertical scaling
- Advanced zoom algorithm provides high image quality
- Sharpness/Smooth filter enhancement
- Support non-linear scaling from 4:3 to 16:9 or 16:9 to 4:3

Color Processor
- True 10 bits color processing engine
- xvYCC supported
- sRGB compliance
- Advanced dithering logic for 18-bit panel color depth enhancement
- Dynamic overshoot-smear canceling engine
- Brightness and contrast control
- Programmable 10-bit gamma support
- Peaking/Coring function for video sharpness

VividColor™
- Independent color management (ICM)
- Dynamic contrast control (DCC)
- Precise color mapping (PCM)
- Image Adaptive Power Saving (IAPS)

Output Interface
- Fully programmable display timing generator
- Flexible data pair swapping for easier system design.
- Display clock supports up to186MHz (1920x1080@75Hz)
- LVDS -output interface on single PCB
- Support 8-bit LVDS output
- Spread-Spectrum DPLL to reduce EMI
- Fixed Last Line output for perfect panel capability

Embedded OSD

- Embedded 20K SRAM dynamically stores OSD command and fonts
- Support multi-color RAM font, 1, 2 and 4-bit per pixel
- 64 color palette
- Maximum 18 window with alpha-blending/
- gradient / gradient target color / gradient reversed color/ dynamic fade-in/fade-out, bordering/ shadow/3D window type
- Rotary 90,180,270 degree
- Independent row shadowing/bordering
- Programmable blinking effects for each character
- OSD-made internal pattern generator for factory mode
- Support 12x18~4x18 proportional font
- Hardware decompression for OSD font
- Support OSD scrolling
- Support 2 independent font based OSD

Power Supply

- 3.3V / 1.2V power supply
- Low standby current (<9mA)

2. Ordering Information

Part No.	VGA	DVI	HDMI	DP	HDCP	Audio DAC	OD	FRC	Max. Resolution	Output	PKG
RTD2486AD-CG	Yes (210MHz)	Yes	No	Yes	Yes	Yes	No	No	1920*1080	Dual-LVDS	LQFP128 (green package)

3. Chip Data Path Block Diagram

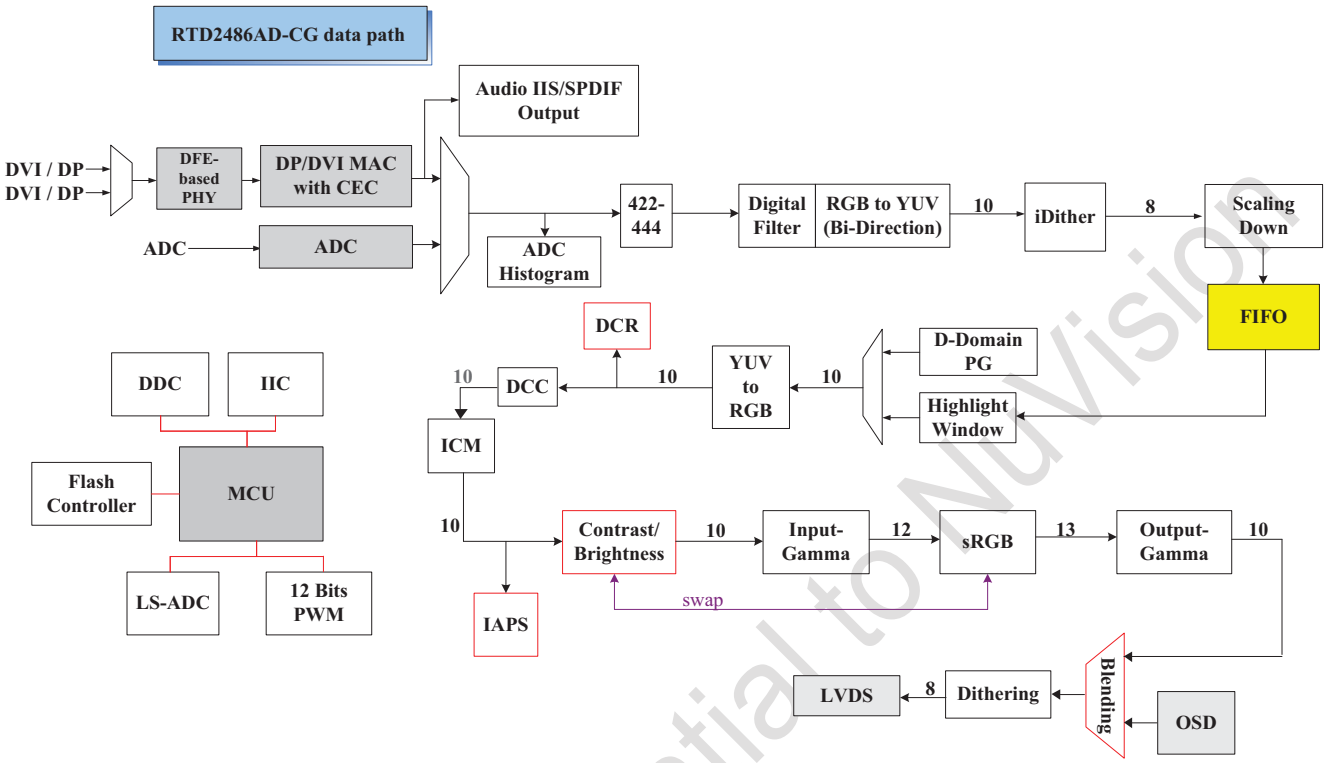
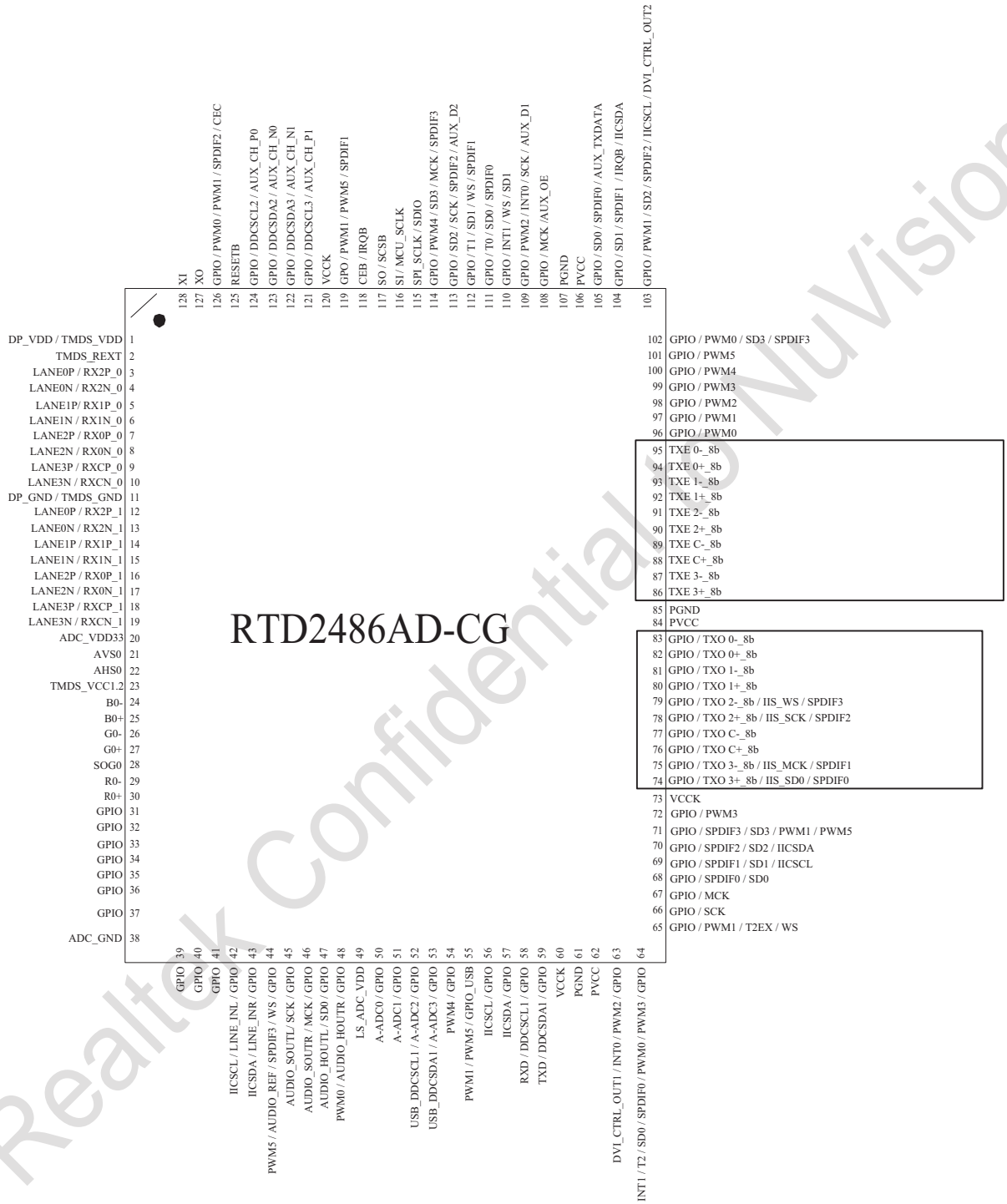


Figure1

4. Pin Diagram

128 Pin LQFP



(Pin 119 : Power on latch Pin)

(when AC Power On , Power on latch pin must be “High”)

Table of Pin Assignment

(I/O Legend: A = Analog, I = Input, O = Output, P = Power, G = Ground)

Name	I/O	Pin #	Description	Note
TMDS_VDD/DP_VDD	AP	1	TMDS power/Display Port Power	(3.3 V)
TMDS_REXT	AI	2	Impedance Match Reference Resistor For Scan mode,it should be pulled high Scan mode: SI[7:0] is assigned to {124~121,114~111} SO[7:0] is assigned to {110~108,105~101} SE is assigned to 100.	Ref value: 6.2 K ohm (Reference to VCC)
RX2P_0/LANE0P	AI	3	TMDS Differential signal Input/LANE0P	
RX2N_0/LANE0N	AI	4	TMDS Differential signal Input/LANE0N	
RX1P_0/LANE1P	AI	5	TMDS Differential signal Input/LANE1P	
RX1N_0/LANE1N	AI	6	TMDS Differential signal Input/LANE1N	
RX0P_0/LANE2P	AI	7	TMDS Differential signal Input/LANE2P	
RX0N_0/LANE2N	AI	8	TMDS Differential signal Input/LANE2N	
RXCP_0/LANE3P	AI	9	TMDS Differential signal Input/LANE3P	
RXCN_0/LANE3N	AI	10	TMDS Differential signal Input/LANE3N	
TMDS_GND/DP_GND	AG	11	TMDS ground/Display Port Ground	
RX2P_1/LANE0P	AI	12	TMDS Differential signal Input/LANE0P	
RX2N_1/LANE0N	AI	13	TMDS Differential signal Input/LANE0N	
RX1P_1/LANE1P	AI	14	TMDS Differential signal Input/LANE1P	
RX1N_1/LANE1N	AI	15	TMDS Differential signal Input/LANE1N	
RX0P_1/LANE2P	AI	16	TMDS Differential signal Input/LANE2P	
RX0N_1/LANE2N	AI	17	TMDS Differential signal Input/LANE2N	
RXCP_1/LANE3P	AI	18	TMDS Differential signal Input/LANE3P	
RXCN_1/LANE3N	AI	19	TMDS Differential signal Input/LANE3N	
ADC_VDD	AP	20	ADC Power	(3.3 V)
AVS0	I	21	ADC vertical sync input	5V tolerance even when power-off
AHS0	I	22	ADC horizontal sync input AVS0 and AHS0 could be used to select one of three scan chain. AHS0/AVS0: 2'b00: {i_chain[2:0], mcu_chain[1:0], vbi_chain[2:0]} 2'b01: d_chain 2'b10: vdec_chain Other are reserved	5V tolerance even when power-off
TMDS_VCC1.2/ DP_ VCC1.2	AP	23	TMDS power/Display Port Power	(1.2V)
B0-	AI	24	Negative BLUE analog input (Pb-)	
B0+	AI	25	Positive BLUE analog input (Pb+)	
G0-	AI	26	Negative GREEN analog input (Y-)	
G0+	AI	27	Positive GREEN analog input (Y+)	
SOG0	AI	28	Sync-On-Green	
R0-	AI	29	Negative RED analog input (Pr-)	
R0+	AI	30	Positive RED analog input (Pr+)	
GPIO	IO	31	MCU GPIO	3.3V tolerance
GPIO	IO	32	MCU GPIO	3.3V tolerance
GPIO	IO	33	MCU GPIO	3.3V tolerance
GPIO	IO	34	MCU GPIO	3.3V tolerance
GPIO	IO	35	MCU GPIO	3.3V tolerance

GPIO	IO	36	MCU GPIO	3.3V tolerance
GPIO	IO	37	MCU GPIO	3.3V tolerance
ADC_GND	AG	38	ADC ground	
GPIO	IO	39	MCU GPIO	5V tolerance even when power-off
GPIO	IO	40	MCU GPIO	5V tolerance even when power-off
GPIO	IO	41	MCU GPIO	5V tolerance even when power-off
GPIO/LINE_INL /IICSCL	IO	42	MCU GPIO/LINE-IN/ IIC BUS	3.3 V tolerance
GPIO/LINE_INR/ IICSDA	IO	43	MCU GPIO/LINE-IN/ IIC BUS	3.3 V tolerance
GPIO/PWM5/WS/ SPDIF3/AUDIO_REF	IO	44	MCU GPIO/PWM/IIS-WS/ SPDIF3/Audio Reference Resistance	3.3 V tolerance
GPIO/SCK/ AUDIO_SOUTL	IO	45	MCU GPIO/IIS-SCK/ Speaker Output	3.3 V tolerance
GPIO/MCK/AUDIO_SO UTR	IO	46	MCU GPIO/IIS-MCK/Speaker Output	3.3 V tolerance
GPIO/SD0/ AUDIO_HOUTL	IO	47	MCU GPIO /IIS-SD0/ Audio Headphone Output	3.3 V tolerance
GPIO/PWM0/AUDIO_H OUTR	IO	48	MCU GPIO /PWM/ Audio Headphone Output	3.3 V tolerance
LS_ADC_VDD	AP	49	Low Speed ADC POWER	(3.3V)
A-ADC0/GPIO	IO	50	8-bit MCU ADC Input/ MCU GPIO	5 V tolerance
A-ADC1/GPIO	IO	51	8-bit MCU ADC Input/ MCU GPIO	5V tolerance
A-ADC2/GPIO/ USB_DDCSCL1	IO	52	8-bit MCU ADC Input/MCU GPIO/ USB_DDCSCL1 When (Page 10, 0xD6[0] = 1) && (pin55 = 1), disable DDC function of pin 58, 59 and swap to pin 52, 53	5V tolerance
ADC3/GPIO/ USB_DDCSDA1	IO	53	8-bit MCU ADC Input/ MCU GPIO/USB_DDCSDA1 When (Page 10, 0xD6[0] = 1) && (pin55 = 1), disable DDC function of pin 58, 59 and swap to pin 52, 53	5V tolerance
GPIO/PWM4	IO	54	MCU GPIO/PWM	5V tolerance even when power-off
GPIO_USB/PWM1/ PWM5	IO	55	MCU GPIO_USB Ctrl/PWM	5V tolerance even when power-off
GPIO/IICSCL	IO	56	MCU GPIO/IIC BUS	5V tolerance even when power-off
GPIO/IICSDA	IO	57	MCU GPIO/IIC BUS	5V tolerance even when power-off
DDCSCL1/GPIO	IO	58	DDC1(Open drain I/O)/MCU GPIO	5V tolerance even when power-off
DDCSDA1/GPIO	IO	59	DDC1(Open drain I/O)/MCU GPIO	5V tolerance even when power-off
VCCK	P	60	Digital Power	(1.2V)
PGND	G	61	Pad ground	

PVCC	P	62	Pad power	(3.3V)
GPIO/PWM2/ DVI_CTRL_OUT1	IO	63	MCU GPIO/PWM/DVI Control Output	5V tolerance even when power-off
GPIO/PWM0/PWM3/ SD0/SPDIF0	IO	64	MCU GPIO/PWM/IIS-SD0/SPDIF0	5V tolerance even when power-off
GPIO/PWM1/WS	IO	65	MCU GPIO/PWM/IIS-WS	5V tolerance even when power-off
GPIO/SCK	IO	66	MCU GPIO/IIS-SCK	5V tolerance even when power-off
GPIO/MCK	IO	67	MCU GPIO/IIS-MCK	5V tolerance even when power-off
GPIO/SD0/SPDIF	IO	68	MCU GPIO/IIS-SD0/SPDIF0	5V tolerance even when power-off
GPIO/SD1/ SPDIF1/IICSCL	IO	69	MCU GPIO/IIS-SD1/SPDIF1/IIC BUS	5V tolerance even when power-off
GPIO/SD2/SPDIF2/ IICSDA	IO	70	MCU GPIO/IIS-SD2/SPDIF2/IIC BUS	5V tolerance even when power-off
GPIO/PWM1/PWM5/ SD3/SPDIF3	IO	71	MCU GPIO/PWM/IIS-SD3/SPDIF3	5V tolerance even when power-off
GPIO/PWM3	IO	72	MCU GPIO/PWM	5V tolerance even when power-off
VCCK	P	73	Digital Power	(1.2V)
TXO3+_8b/GPIO/IIS_SD 0/SPDIF0	IO	74	LVDS 8bit/MCU GPIO/IIS_SD0/SPDIF0	3.3 V tolerance
TXO3-_8b/GPIO/IIS_MC K/SPDIF1	IO	75	LVDS 8bit/MCU GPIO/IIS_MCK/SPDIF1	3.3 V tolerance
TXOC+_8b/GPIO	IO	76	LVDS 8bit/MCU GPIO	3.3 V tolerance
TXOC-_8b/GPIO	IO	77	LVDS 8bit/MCU GPIO	3.3 V tolerance
TXO2+_8b/GPIO/IIS_SC K/SPDIF2	IO	78	LVDS 8bit/MCU GPIO/IIS_SCK/SPDIF2	3.3 V tolerance
TXO2-_8b/GPIO/IIS_WS /SPDIF3	IO	79	LVDS 8bit/MCU GPIO/IIS_WS/SPDIF3	3.3 V tolerance
TXO1+_8b/GPIO	IO	80	LVDS 8bit/MCU GPIO	3.3 V tolerance
TXO1-_8b/GPIO	IO	81	LVDS 8bit/MCU GPIO	3.3 V tolerance
TXO0+_8b/GPIO	IO	82	LVDS 8bit/MCU GPIO	3.3 V tolerance
TXO0-_8b/GPIO	IO	83	LVDS 8bit/MCU GPIO	3.3 V tolerance
PVCC	P	84	Pad power	3.3V
PGND	G	85	Pad ground	
TXE3+_8b	O	86	LVDS 8bit	3.3 V tolerance
TXE3-_8b	O	87	LVDS 8bit	3.3 V tolerance
TXEC+_8b	O	88	LVDS 8bit	3.3 V tolerance
TXEC-_8b	O	89	LVDS 8bit	3.3 V tolerance
TXE2+_8b	O	90	LVDS 8bit	3.3 V tolerance
TXE2-_8b	O	91	LVDS 8bit	3.3 V tolerance
TXE1+_8b	O	92	LVDS 8bit	3.3 V tolerance
TXE1-_8b	O	93	LVDS 8bit	3.3 V tolerance
TXE0+_8b	O	94	LVDS 8bit	3.3 V tolerance
TXE0-_8b	O	95	LVDS 8bit	3.3 V tolerance
GPIO/PWM0	IO	96	MCU GPIO/PWM	5V tolerance
GPIO/PWM1	IO	97	MCU GPIO/PWM	5V tolerance
GPIO/PWM2	IO	98	MCU GPIO/PWM	5V tolerance

GPIO/PWM3	IO	99	MCU GPIO/PWM	5V tolerance
GPIO/PWM4	IO	100	MCU GPIO/PWM	5V tolerance even when power-off
GPIO/PWM5	IO	101	MCU GPIO/PWM	5V tolerance even when power-off
GPIO/PWM0/SD3/SPDIF3	IO	102	MCU GPIO/PWM/IIS-SD3/SPDIF3	5V tolerance even when power-off
GPIO/PWM1/SD2/ SPDIF2/ DVI_CTRL_OUT2/ IICSCL	IO	103	MCU GPIO/PWM/IIS-SD2/SPDIF2/ DVI Control Output/IICSCL	5V tolerance even when power-off (GPIO open-drain)
GPIO/SD1/SPDIF1/ IRQB/IICSDA/	IO	104	MCU GPIO/IIS-SD1/SPDIF1/ IRQ Bar/IICSDA	5V tolerance even when power-off
GPIO/SD0/SPDIF0/ AUX_TXDATA	IO	105	MCU GPIO/IIS-SD0/SPDIF0/ AUX_TXDATA	5V tolerance even when power-off
PVCC	P	106	Pad 3.3V power	3.3V
PGND	G	107	Pad 3.3V GND	
GPIO/MCK/ AUX_OE	IO	108	MCU GPIO/IIS-MCK/AUX_OE	5V tolerance even when power-off
GPIO/PWM2/SCK/ AUX_D1	IO	109	MCU GPIO/PWM/IIS-SCK/ AUX_D1	5V tolerance even when power-off
GPIO/WS/SD1	IO	110	MCU GPIO/IIS-WS/IIS-SD1	5V tolerance even when power-off
GPIO/SD0/ SPDIF0	IO	111	MCU GPIO/IIS-SD0/SPDIF0	5V tolerance even when power-off
GPIO/SD1/WS/SPDIF1	IO	112	MCU GPIO/IIS-SD1/IIS-WS/SPDIF1	5V tolerance even when power-off
GPIO/SD2/SCK/SPDIF2/ AUX_D2	IO	113	MCU GPIO/IIS-SD2/IIS-SCK/ SPDIF2/AUX_D2	5V tolerance even when power-off
GPIO/PWM4/SD3/MCK/ SPDIF3	IO	114	MCU GPIO/PWM/IIS-SD3/ IIS-MCK/SPDIF3	5V tolerance even when power-off
SPI_SCLK/SDIO	IO	115	SPI flash serial clock /external MCU serial control I/F data in	3.3 V tolerance
SI/MCU_SCLK	IO	116	SPI flash serial data input /external MCU serial control I/F clock	3.3 V tolerance
SO/SCSB	IO	117	SPI flash serial data output /external MCU serial control I/F chip select	3.3 V tolerance
CEB/IRQB	IO	118	SPI flash chip enable bar/IRQ Bar Note:It should be pulled down to 0 v or pulled up to 3.3 v in order to designate the MCU type(Internal MCU(3.3 volts) or External MCU(0 volts)).	3.3 V tolerance
GPO/PWM1/PWM5/ SPDIF1	IO	119	MCU GPO/PWM/SPDIF1 **(Power on latch Pin .)** **(when AC Power On , Power on latch Pin must be "High")**	5V tolerance even when power-off

VCCK	P	120	Digital 1.2V Power	1.2V
DDCSCL3/GPIO/ AUX_CH_P1	IO	121	DDC3(Open drain I/O)/MCU GPIO/ DP AUX_CH_P1	5V tolerance even when power-off
DDCSDA3/GPIO/ AUX_CH_N1	IO	122	DDC3(Open drain I/O)/MCU GPIO/ DP AUX_CH_N1	5V tolerance even when power-off
DDCSDA2/GPIO/ AUX_CH_N0	IO	123	DDC2(Open drain I/O)/MCU GPIO/ DP AUX_CH_N0	5V tolerance even when power-off
DDCSCL2/GPIO/ AUX_CH_P0	IO	124	DDC2(Open drain I/O)/MCU GPIO/ DP AUX_CH_P0	5V tolerance even when power-off (GPIO open-drain)
RESETB	I	125	Chip Reset Bar	Low active; 5V tolerance even when power-off
GPIO/PMW0/PWM1/SP DIF2/CEC	I/O	126	MCU GPIO/PWM/SPDIF2/CEC	5V tolerance
XO	AO	127	Crystal Output	
XI	AI	128	Crystal Input	

MCU GPIO Assignment

PIN No.	MCU GPIO Name	PIN No.	MCU GPIO Name	PIN No.	MCU GPIO Name
31	PD.7	70	P1.6	122	P7.2
32	PD.6	71	P1.7	123	P7.1
33	PD.5	72	PC.2	124	P7.0
34	PD.4	74	P9.0	126	PC.0
35	PD.3	75	P9.1		
36	PD.2	76	P9.2		
37	PD.1	77	P9.3		
39	PD.0	78	P9.4		
40	PC.4	79	PA.0		
41	PB.7	80	PA.1		
42	PB.6	81	PA.2		
43	PB.5	82	PA.3		
44	PB4	83	PA.4		
45	PB.3	94	P5.0 (removed)		
46	PB.2	95	P5.1 (removed)		
47	PB.1	96	P5.2		
48	PB.0	97	P5.3		
50	P6.0	98	P5.4		
51	P6.1	99	P5.5		
52	P6.2	100	P5.6		
53	P6.3	101	P5.7		
54	P6.4	102	P7.6		
55	P6.5	103	P7.5		
56	P6.6	104	P7.4		
57	P6.7	105	P8.0		
58	P3.0/RXD(I/O)	108	P8.1/CLKO1(O)		
59	P3.1/TXD(O)	109	P3.2/INT0(I)		
63	PC.3 /INT0(I)	110	P3.3/INT1(I)		
64	P1.0/T2(I) /INT1(I)	111	P3.4/T0		
65	P1.1/T2EX(I)	112	P3.5(BS)/T1		
66	P1.2/CLKO2(O)	113	P3.6		
67	P1.3	114	P3.7		
68	P1.4	119	PC.1		
69	P1.5	121	P7.3		