TITLE : MV270QHM-NF2

Product Specification

Ver.P2

BEIJING BOE Display TECHNOLOGY CO. LTD

REVISION HISTORY

(●) Preliminary specification
( ) Final specification

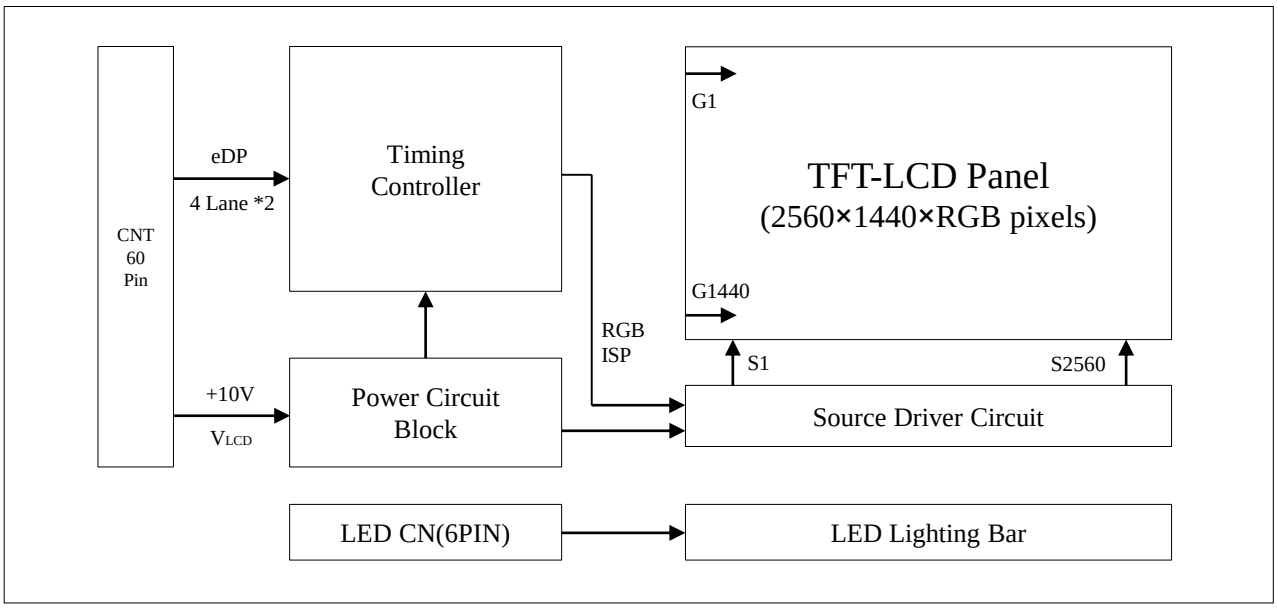
Revision No.	Page	Description of changes	Date	Prepared
Rev.P0		Preliminary Specification	Jan.08.2021	Tian Ming
Rev.P1	8	Add Backlight LED inimum voltage & Current	Feb.25.2021	Tian Ming
Rev.P2	18	Vsync Period & Vertical blank	Mar.03.2021	Tian Ming

Contents

1.0 GENERAL DESCRIPTION

1.1 Introduction

MV270QHM-NF2 is a color active matrix TFT LCD module using amorphous silicon TFT's (Thin Film Transistors) as an active switching devices. This module has a 27 inch diagonally measured active area with QHD resolutions (2560 horizontal by 1440 vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical stripe and this module can display 1.07G colors. The TFT-LCD panel used for this module is adapted for a low reflection and higher color type.



1.2 Features

- 2*4 Lanes eDP Interface with 5.4Gbps Link Rates
- High-speed response
- 10-bit (8+FRC) color depth, display 1.07G colors
- High luminance and contrast ratio, low reflection and wide viewing angle
- DE (Data Enable) only
- RoHS/Halogen Free
- CEC/CEL2 compliant
- Gamma Correction
- Reverse type
- Compatible with sRGB Matching Ratio 99% typ.
- Compatible with Low Blue Light with TUV certificate

1.3 Application

- Desktop Type of PC & Workstation Use
- Slim-Size Display for Stand-alone Monitor
- Display Terminals for Control System
- Monitors for Process Controller

1.4 General Specification

The followings are general specifications at the model MV270QHM-NF2.

<Table 1. General Specifications>

Parameter	Specification	Unit	Remarks
Active area	596.736(H) × 335.664(V)	mm	
Number of pixels	2560(H) ×1440(V)	pixels	
Pixel pitch	0.2331(H) x 0.2331(V)	mm	
Pixel arrangement	RGB Vertical stripe	-	
Display colors	1.07G	colors	
Display mode	Normally Black	-	
Dimensional outline	608.8(H) x 355.1(V)× 15.2(D) typ	mm	Detail refer to drawing
Weight	2260	g	
Surface Treatment	Anti-glare, 3H	-	
Back-light	Down edge side 1-LED Light bar Type	-	

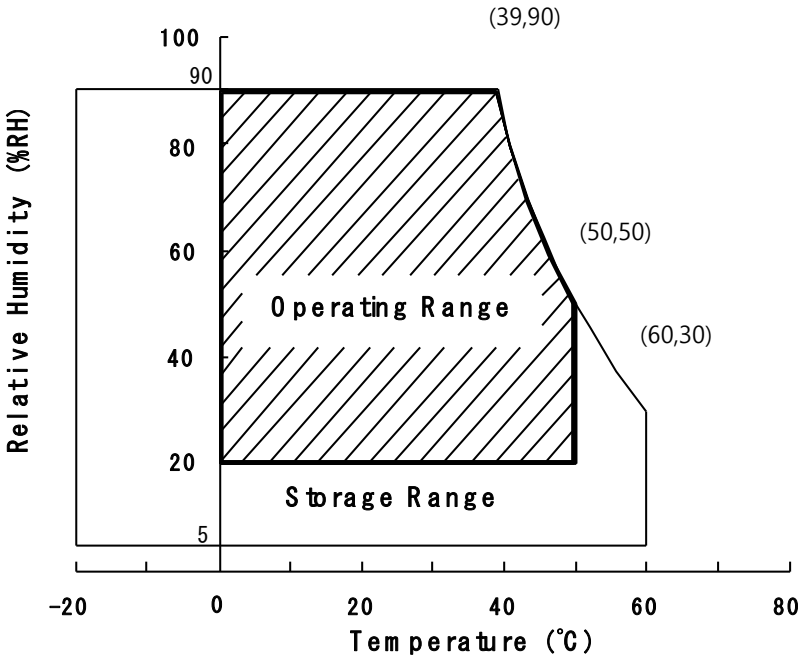
2.0 ABSOLUTE MAXIMUM RATINGS

The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit. The operational and non-operational maximum voltage and current values are listed in Table 2.

< Table 2. Absolute Maximum Ratings> [VSS=GND=0V]

Parameter	Symbol	Min.	Max.	Unit	Remarks
Power Supply Voltage	V_{DD}	-0.3	11.0	V	Ta = 25 ℃
Logic Supply Voltage	V_{IN}	VSS-0.3	V_{DD}+0.3	V	
Operating Temperature	T_{OP}	0	+50	℃	1)
Storage Temperature	T_{ST}	-20	+60	℃	1)

Note : 1) Temperature and relative humidity range are shown in the figure below.
Wet bulb temperature should be 39 ^{O}C max. and no condensation of water.



3.0 ELECTRICAL SPECIFICATIONS

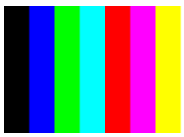
3.1 Electrical Specifications

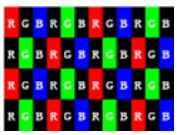
[Ta =25±2 ℃]

< Table 3. Electrical specifications >

Parameter		Min.	Typ.	Max.	Unit	Remarks
Power Supply Voltage	V_{DD}	9.5	10.0	10.5	V	**Note1**
Power Supply Current	I_{DD}	-	1000	1800	mA	
In-Rush Current	I_{RUSH}	-	2.0	6.0	A	**Note 2**
Permissible Input Ripple Voltage	V_{RF}	-	-	300	mV	**V_{DD} = 10.0V**
High Level Differential Input Threshold Voltage	V_{IH}	-	-	+100	mV	
Low Level Differential Input Threshold Voltage	V_{IL}	-100	-	-	mV	
Differential input voltage	$\|V_{ID}\|$	200	-	600	mV	
Differential input common mode voltage	Vcm	1.0	1.2	1.5	V	
LED Voltage	V_L	-	3.0	3.2	V	
LED Channel Voltage	V_L	-	27	28.8	V	
LED Channel Current	I_L	-	130	136	mA	
LED Lifetime		30,000	-	-	Hrs	I_L=130 mA
Power Consumption	P_D	-	10	18	W	165Hz
	P_{BL}	-	28.08	31.33	W	I_L=130mA, **Note 3**
	P_{total}	-	38.08	49.33	W	

Notes : 1. The supply voltage is measured and specified at the interface connector of LCM.
The current draw and power consumption specified is for VDD=10.0V, Frame rate=165Hz. Test Pattern of power supply current
a) Typ : Color Bar pattern
b) Max : Skip subpixel pattern





2. Duration of rush current is about 2 ms and rising time of VDD is 520 μs ± 20 %
3. Calculated value for reference (VL × IL) ×4(channel) excluding driver loss. (LED Light bar: 9S8P)

3.2 Backlight Unit

<Table4. LED Backlight Unit (@320nit min/@400nit typ)>

Parameter		Min.	Typ.	Max.	Unit	Remarks
LED Light Bar Input Voltage Per Input Pin	VPIN	25.2	27	28.8	V	Duty 100%
LED Light Bar Input Current Per Input Pin	IPIN	124	130	136	mA	Note1,2,
LED Power Consumption	PBL	25.0	28.08	31.34	W	Note 3
LED Life-Time	-	30,000	-	-	Hrs	Note 4

LED bar consists of 72LED packages,8 strings(parallel)*9packages(serial)
Note1: There are one light bar ,and the specified current is input LED chip 100% duty current
Note2: The sense current of each input pin is 130mA
Note3: PBL=8 Input pins*VP_{IN} ×IP_{IN}
Note4: The lifetime is determined as the time at which luminance of LED become 50% of the initial brightness or not normal lighting at IPIN=130mA on condition of continuous operating at 25 ±2 ℃

<Table5. LED Backlight Unit (≥@450nit typ.)>

Parameter		Min.	Typ.	Max.	Unit	Remarks
LED Light Bar Input Voltage Per Input Pin	VPIN	25.2	27	28.8	V	Duty 100%
LED Light Bar Input Current Per Input Pin	IPIN	139	146	153	mA	Note 1
MDL peak brightness	-	-	450	-	nit	

4.0 OPTICAL SPECIFICATION

4.1 Overview

The test of Optical specifications shall be measured in a dark room (ambient luminance ≤ 1 lux and temperature = 25±2°C) with the equipment of Luminance meter system (Goniometer system and TOPCONE PR730) and test unit shall be located at an approximate distance 50cm from the LCD surface at a viewing angle of θ and Φ equal to 0°. We refer to $\theta_{Ø=0}$ (=θ_3) as the 3 o'clock direction (the "right"), $\theta_{Ø=90}$ (= θ_{12}) as the 12 o'clock direction ("upward"), $\theta_{Ø=180}$ (= θ_9) as the 9 o'clock direction ("left") and $\theta_{Ø=270}$(= θ_6) as the 6 o'clock direction ("bottom"). While scanning θ and/or Ø, the center of the measuring spot on the Display surface shall stay fixed. The measurement shall be executed after 30 minutes warm-up period. VDD shall be 10.0V +/-10% at 25°C. Optimum viewing angle direction is 6 'clock.

4.2 Optical Specifications

[VDD = 10.0V, Frame rate = 60Hz, Clock = 120.8MHz, I_{BL} = 1040mA, Ta =25±2 °C]

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle range	Horizontal	Θ_3	CR > 10	85	89	-	Deg.	Note 1
		Θ_9		85	89	-	Deg.	
	Vertical	Θ_{12}		85	89	-	Deg.	
		Θ_6		85	89	-	Deg.	
Luminance Contrast ratio		CR	Θ = 0° (Center) Normal Viewing Angle	700	1000			Note 2
Luminance of White		Y_w		320	400	-	cd/m^2	Note 3
White luminance uniformity		ΔY		75	-	-	%	Note 4
Reproduction of color	White	W_x		0.283	0.313	0.343	-	Note 5
		W_y		0.299	0.329	0.359	-	
	Red	R_x		0.630	0.660	0.690	-	
		R_y		0.305	0.335	0.365	-	
	Green	G_x		0.279	0.309	0.339	-	
		G_y		0.589	0.619	0.649	-	
	Blue	B_x		0.111	0.141	0.171	-	
		B_y		0.019	0.049	0.079	-	
Response Time	GTG	T_g		-	5.x	11	ms	Note 6
Cross Talk		CT		-	-	2.0	%	Note 7

Note :

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface.
2. Contrast measurements shall be made at viewing angle of θ= 0° and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. (See FIGURE 1 shown in Appendix) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. Center Luminance of white is defined as the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in FIGURE 2 for a total of the measurements per display.
4. The White luminance uniformity on LCD surface is then expressed as :
   ΔY = (Minimum Luminance of 9points / Maximum Luminance of 9points) * 100
   (See FIGURE 2 shown in Appendix).
5. The color chromaticity coordinates specified in Table 5. shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.
6. Response time Tg is the average time required for display transition by switching the input signal as below table and is based on Frame rate fV =165 Hz to optimize.
   Each time in below table is defined as appendix Figure 3and shall be measured by switching the input signal for "any level of gray(bright)"and "any level of gray(dark)".

Measured Response Time		Target				
		0	63	127	191	255
Start	0					
	63					
	127					
	191					
	255					

7. Cross-Talk of one area of the LCD surface by another shall be measured by comparing the luminance (Y_A) of a 25mm diameter area, with all display pixels set to a gray level, to the luminance (Y_B) of that same area when any adjacent area is driven dark. (See FIGURE 4 shown in Appendix).

5.0 INTERFACE CONNECTION.

5.1 Electrical Interface Connection

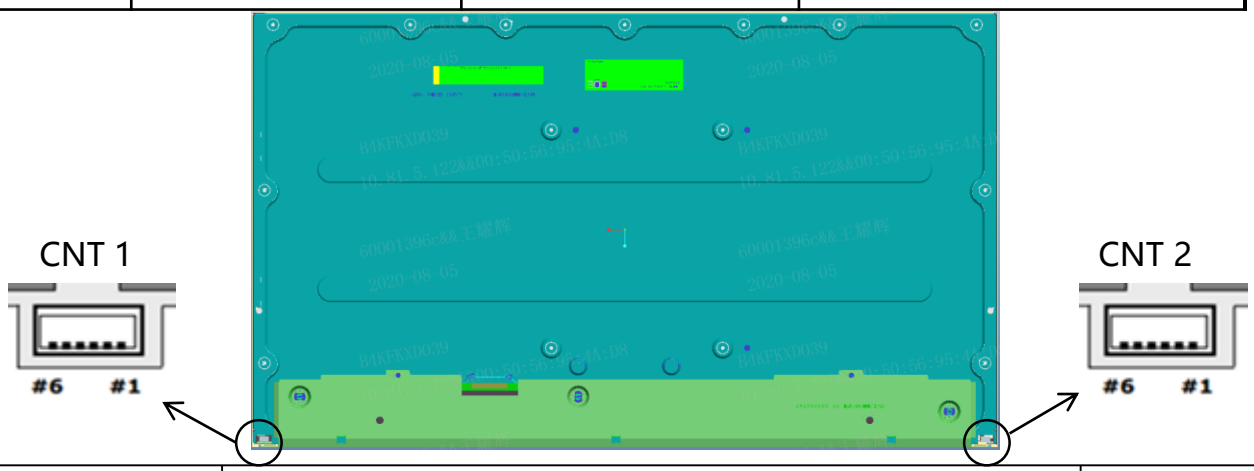
5.1.1 LED Light Bar

LED connector：10035WS-H06D manufactured by YEONHO or 3712K-Q06M-00R manufactured by Entery or EQUIVALENT

< Table 5. LED Light Bar>

	Pin No	Symbol	Description
CNT1	1	IRLED1	LED current sense for string1
	2	IRLED2	LED current sense for string2
	3	VLED	LED power supply
	4	VLED	LED power supply
	5	IRLED3	LED current sense for string3
	6	IRLED4	LED current sense for string4

	Pin No	Symbol	Description
CNT2	1	IRLED1	LED current sense for string1
	2	IRLED2	LED current sense for string2
	3	VLED	LED power supply
	4	VLED	LED power supply
	5	IRLED3	LED current sense for string3
	6	IRLED4	LED current sense for string4



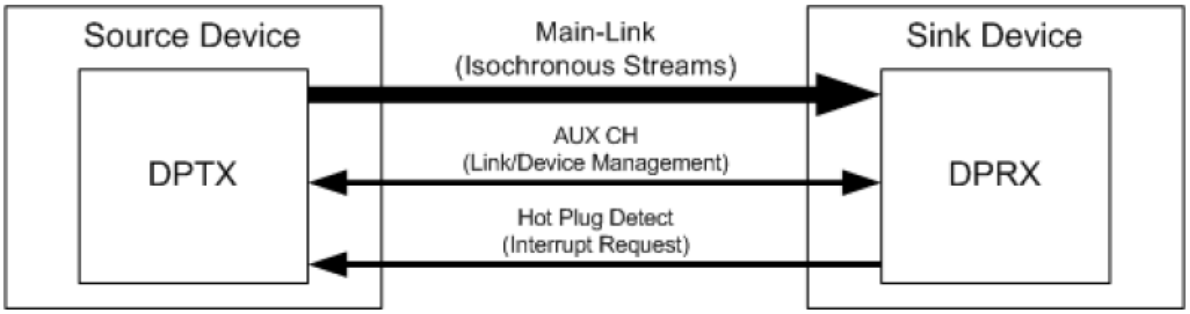
5.2 Electrical Interface Connection

- CN1 Module Side Connector : 20525-060E-01 or Equivalent

No.	Symbol	Description	No.	Symbol	Description
1	GND	Ground	31	DP0_L1_N	Master Component Signal for Main Link 1
2	VDD	Power Supply +10.0V	32	GND	Ground
3	VDD	Power Supply +10.0V	33	DP0_L2_P	Master True Signal for Main Link 2
4	VDD	Power Supply +10.0V	34	DP0_L2_N	Master Component Signal for Main Link 2
5	VDD	Power Supply +10.0V	35	GND	Ground
6	VDD	Power Supply +10.0V	36	DP0_L3_P	Master True Signal for Main Link 3
7	VDD	Power Supply +10.0V	37	DP0_L3_N	Master Component Signal for Main Link 3
8	VDD	Power Supply +10.0V	38	GND	Ground
9	VDD	Power Supply +10.0V	39	DP1_L0_P	Slave True Signal for Main Link 0
10	GND	Ground	40	DP1_L0_N	Slave Component Signal for Main Link 0
11	GND	Ground	41	GND	Ground
12	GND	Ground	42	DP1_L1_P	Slave True Signal for Main Link 1
13	GND	Ground	43	DP1_L1_N	Slave Component Signal for Main Link 1
14	GND	Ground	44	GND	Ground
15	GND	Ground	45	DP1_L2_P	Slave True Signal for Main Link 2
16	GND	Ground	46	DP1_L2_N	Slave Component Signal for Main Link 2
17	GND	Ground	47	GND	Ground
18	GND	Ground	48	DP1_L3_P	Slave True Signal for Main Link 3
19	NC	No Connection (I2C serial interface for LCM)	49	DP1_L3_N	Slave Component Signal for Main Link 3
20	NC	No Connection (I2C serial interface for LCM)	50	GND	Ground
21	DP0_HPD	Master Hot Plug Detect Signal	51	DP1_AUX_P	Slave True Signal for Auxiliary Channel
22	DP1_HPD	Slave Hot Plug Detect Signal	52	DP1_AUX_N	Slave Component Signal for Auxiliary Channel
23	GND	Ground	53	GND	Ground
24	DP0_AUX_P	Master True Signal for Auxiliary Channel	54	NC	No Connection
25	DP0_AUX_N	Master Component Signal for Auxiliary Channel	55	NC	No Connection
26	GND	Ground	56	NC	No Connection
27	DP0_L0_P	Master True Signal for Main Link 0	57	GND	Ground
28	DP0_L0_N	Master Component Signal for Main Link 0	58	NC	No Connection
29	GND	Ground	59	GND	Ground
30	DP0_L1_P	Master True Signal for Main Link 1	60	NC	No Connection

5.3 eDP Interface

- eDP Data Transport Channels



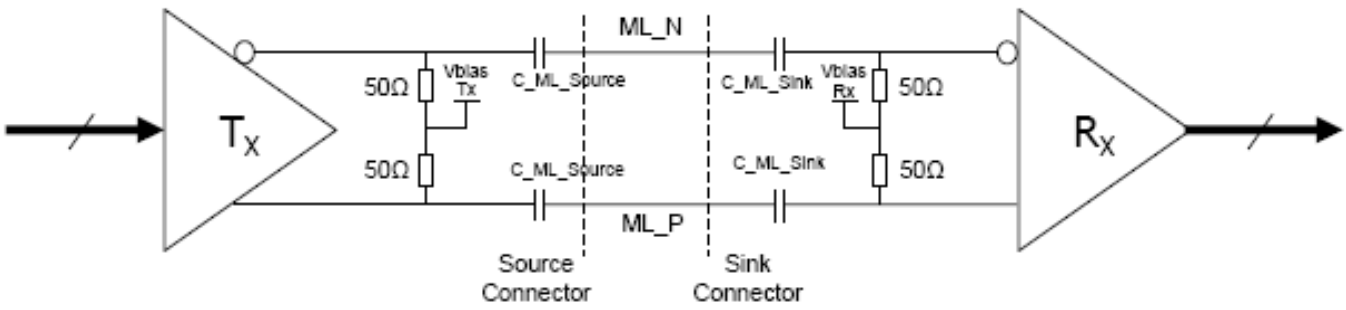
eDP Data Transport Channels

- The TCON supports 4 lane 8 bit input eDP architecture. The data mapping is shown as below：

Lane 0	Lane 1	Lane 2	Lane 3
R0-7:0	R1-7:0	R2-7:0	R3-7:0
G0-7:0	G1-7:0	G2-7:0	G3-7:0
B0-7:0	B1-7:0	B2-7:0	B3-7:0
R4-7:0	R5-7:0	R6-7:0	R7-7:0
G4-7:0	G5-7:0	G6-7:0	G7-7:0
B4-7:0	B5-7:0	B6-7:0	B7-7:0
R8-7:0	R9-7:0	R10-7:0	R11-7:0
G8-7:0	G9-7:0	G10-7:0	G11-7:0
B8-7:0	B9-7:0	B10-7:0	B11-7:0

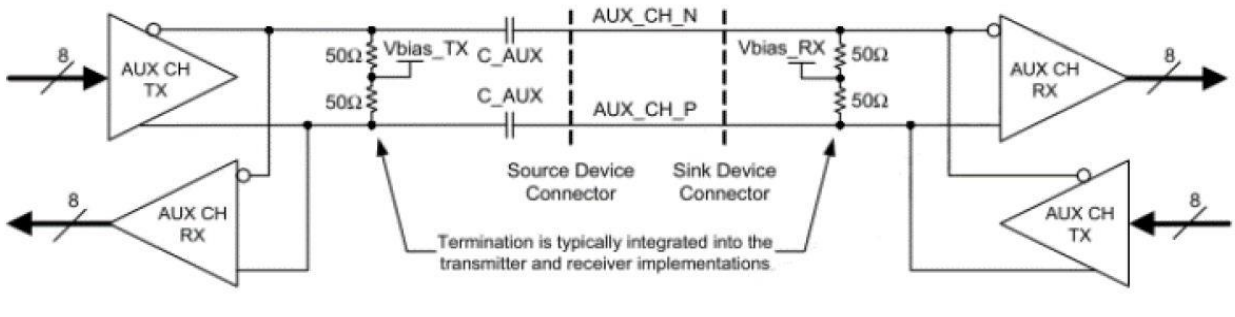
8bit RGB to a 4-Lane Main-Link Mapping

5.3.1 eDP Main Link Signal



Parameter	Symbol	Min	Typ	Max	Unit	Notes
Unit Interval for high bit rate2(5.4Gbps/lane)	UI-HBR2	-	185	-	ps	
Link Clock Down Spreading	Amplitude	0	-	0.5	%	
	Frequency	30	-	33	kHz	TBD
Differential peak-to-peak input voltage at package pins	$V_{RX-DIFFp-p}$	-	-	1.38	V	
EYE width at Sink side connector	$T_{RX-EYE-CONN}$	0.25	-	-	UI	TBD
Lane-to-Lane skew	$L_{Rx-SKEWINTER\_PAIR}$	-	-	1250	-	TBD
Lane intra-pair skew	$L_{Rx-SKEWINTER\_PAIR}$	-	-	50	ps	
AC Coupling Capacitor	C_{SOURCE_ML}	75	-	265	nF	Source side

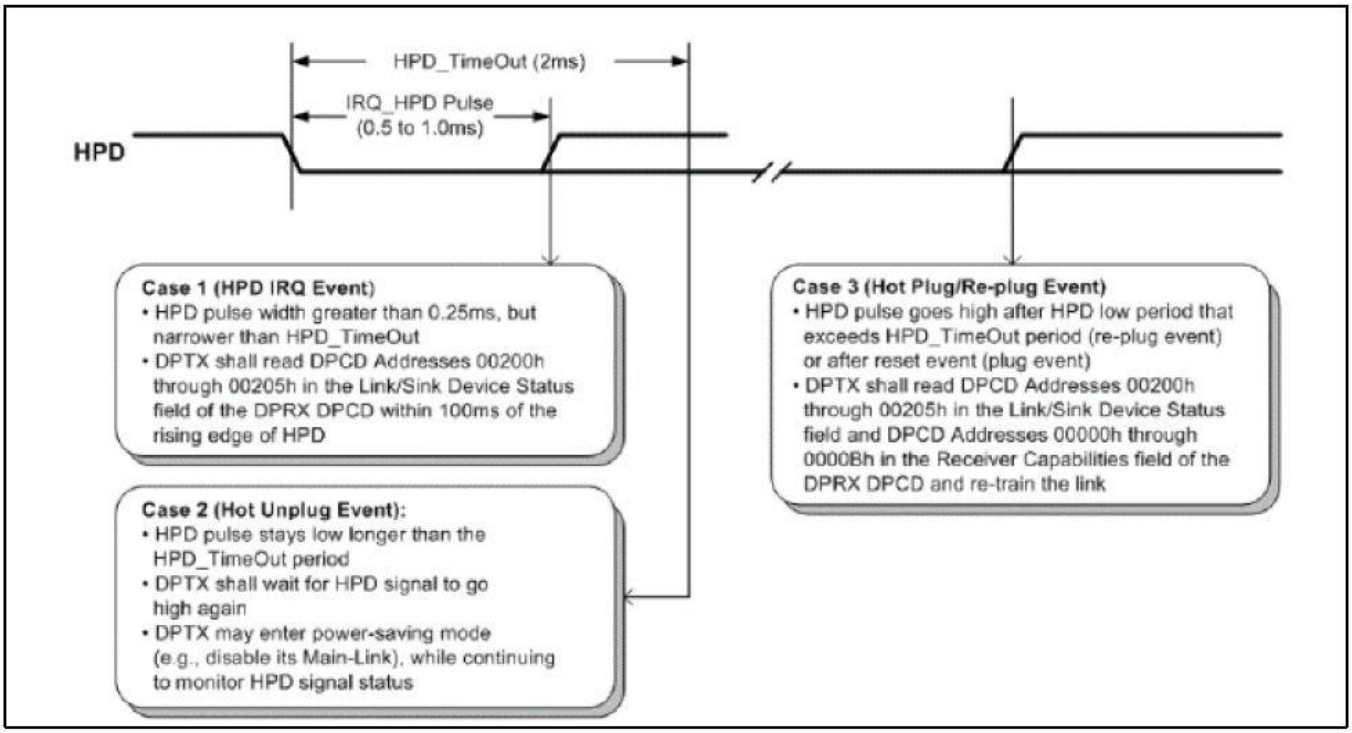
5.3.2 eDP AUX Channel Signal



Recommended eDP AUX Channel Differential Pair

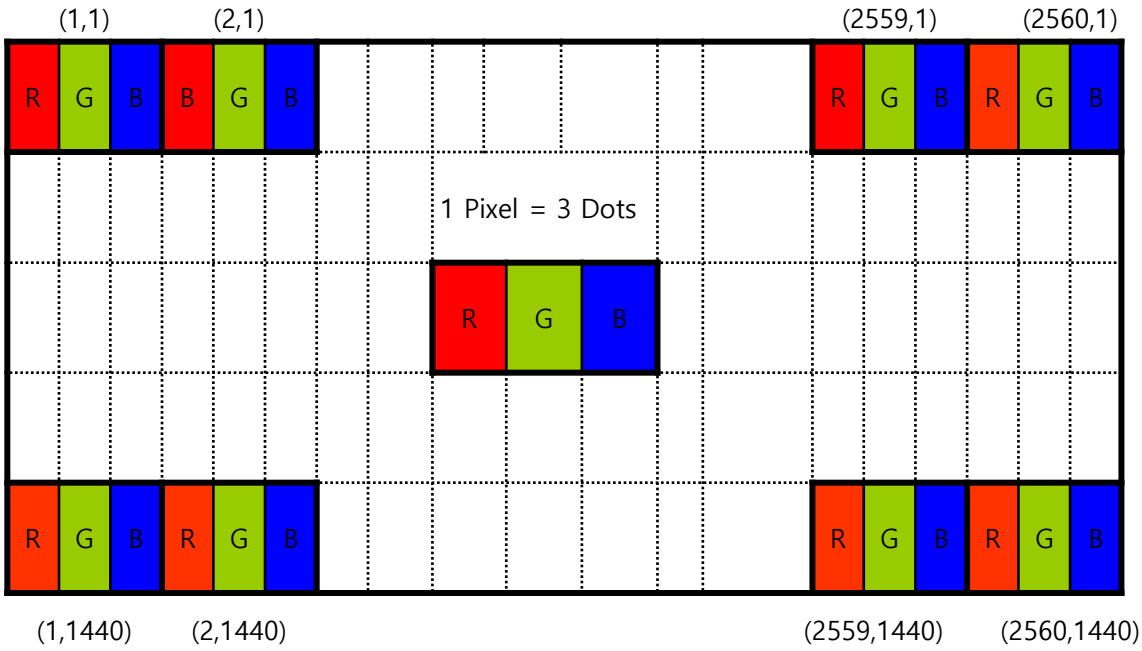
Parameter	Symbol	Min	Typ	Max	Unit	Notes
AUX Unit Interval	UI	0.4	-	0.6	μs	
AUX Jitter at Tx IC Package Pins	T_{jitter}	-	-	0.04	UI	
AUX Jitter at Rx IC Package Pins		-	-	0.05	UI	
AUX Peak-to-peak voltage at Connecto r Pins of Receiving	$V_{AUX-DIFFP-P}$	0.27	-	1.36	V	
AUX Peak-to-peak voltage at Connector Pins of Transmitting		0.29	-	1.38	V	
AUX DC common mode voltage	V_{AUX-CM_RX}	0	-	2.0	V	
	V_{AUX-CM_TX}	0	-	2.0	V	
AUX AC Coupling Capacitor	C_{SOURCE_ML}	75	-	200	nF	

5.3.3 eDP HPD Signal



Parameter	Symbol	Min	Typ	Max	Unit	Notes
HPD Voltage	HPD	2.25	-	3.6	V	Sink side Driving
HOT Plug Detection Threshold		2.0	-	-	V	Source side Detecting
HOT Unplug Detection Threshold		-	-	0.8	V	
HPD_IRQ Pulse Width	HPD_IRQ	0.5	-	1.0	ms	
HPD_TimeOut	–	2.0	-	-	ms	HPD Unplug Event

5.4 Data Input Format



Display Position of Input Data (V-H)

5.5 Back-light Interface Connection

LED connector： 10035WS-H06D manufactured by YEONHO or 3712K-Q06M-00R manufactured by Entery or EQUIVALENT

Pin	Function
1	Channel 1 Current Feedback
2	Channel 2 Current Feedback
3	LED Power Supply
4	LED Power Supply
5	Channel3 Current Feedback
6	Channel4 Current Feedback

6.0 SIGNAL TIMING SPECIFICATION

6.1 The MV270QHM-NF2 is operated by the DE only.

Item	Symbols		Min	Typ	Max	Unit	Note
DCLK	Period	tCLK	2.81	7.72	9.64	ns	
	Frequency	-	103.7	129.6	360.9	MHz	
Hsync	Period	tHP	1400	1440	1480	tCLK	
	Horizontal Valid	tHV		1280		tCLK	
	Horizontal Blank	tHB	120	160	200		
	Frequency	fH	72.0	90.0	247.5	KHz	
Vsync	Period	tVP	1480	1500	5370	tHP	
	Vertical Valid	tVV		1440		tHP	
	Vertical Blank	tVB	40	60	3930	tHP	
	Frequency	fV	48	60	165	Hz	2)

Note 1 : 1). This DCLK range at last line of V-blanking should be set in 0~XXX.

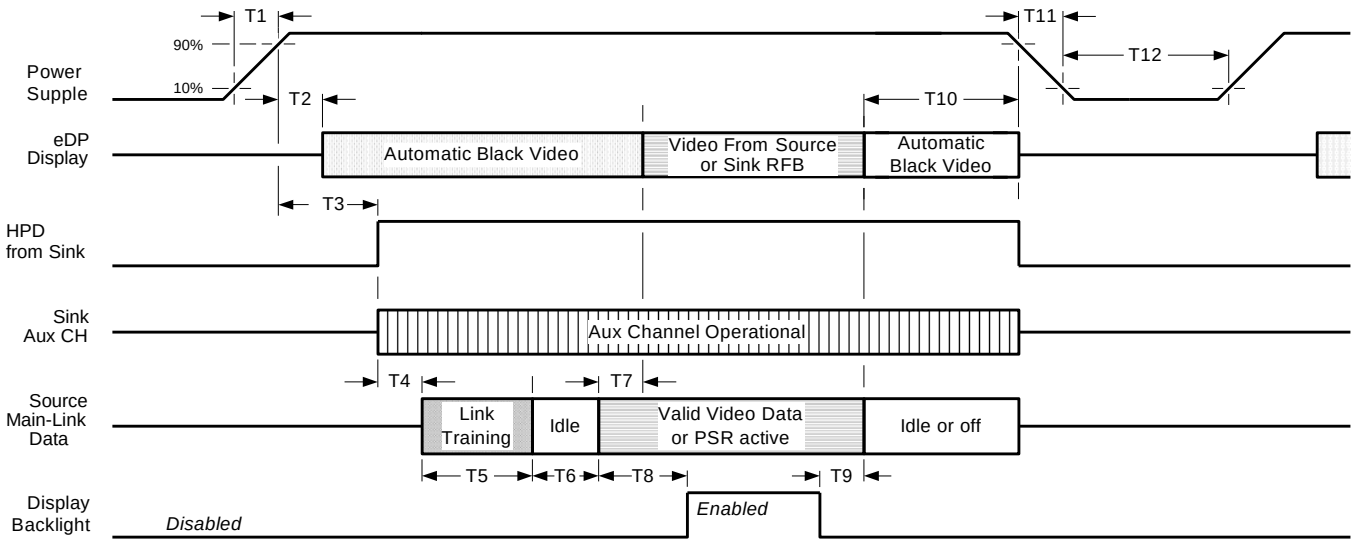
2). The Vsync Frequency maximum can reach XXHz when the resolution is applied @ 1152*900, 1280*1024.

7.0 INPUT SIGNALS, BASIC DISPLAY COLORS & GRAY SCALE OF COLORS

Color & Gray Scale		RED DATA										GREEN DATA										BLUE DATA									
		R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Green	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Red	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale of RED	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	↑										↑										↑									
	▽	↓										↓										↓									
	Brighter	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	▽	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale of GREEN	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	Darker	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	△	↑										↑										↑									
	▽	↓										↓										↓									
	Brighter	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0
	▽	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
Gray Scale of BLUE	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Darker	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	△	↑										↑										↑									
	▽	↓										↓										↓									
	Brighter	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1
	▽	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
Gray Scale of WHITE	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1
	Darker	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0
	△	↑										↑										↑									
	▽	↓										↓										↓									
	Brighter	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	0	1
	▽	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

8.0 POWER SEQUENCE

To prevent a latch-up or DC operation of the LCD module, the power on/off sequence shall be as shown in below.



Timing Parameter	Description	Required By	Limits		Notes
			Min	Max	
T1	Power rail rise time, 10% to 90%	Source	0.5ms	10ms	
T2	Delay from Power Supple to automatic Black Video generation	Sink	0ms	120ms	Automatic Black Video generation prevents display noise until valid video data is received from the Source
T3	Delay from Power Supple to HPD high	Sink	0ms	120ms	Sink AUX Channel must be operational upon HPD high
T4	Delay from HPD high to link training initialization	Source	-	-	Allows for the Source to read Link capability and initialize
T5	Link training duration	Source	-	-	Dependant on the Source link training protocol
T6	Link idle	Source	-	-	Min accounts for required BS-Idle Pattern. Max allows for Source frame synchronization.

8.0 POWER SEQUENCE

To prevent a latch-up or DC operation of the LCD module, the power on/off sequence shall be as shown in below.

T7	Delay from valid video data from Source to video on display	Sink	0ms	50ms	Max value allows for the Sink to validate video data and timing. At the end of T7, the Sink will indicate the detection of valid video data by setting the SINK_STATUS bit to logic 1 (DPCD 00205h, bit 0), and the Sink will no longer generate automatic Black Video.
T8	Delay from valid video data from Source to backlight enable	Source	-	-	The Source must assure display video is stable
T9	Delay from backlight disable to end of valid video data	Source	-	-	The Source must assure backlight is no longer illuminated. At the end of T9, the Sink will indicate the detection of no valid video data by setting the SINK_STATUS bit to logic 0 (DPCD 00205h, bit 0), and the Sink will automatically display Black Video.
T10	Delay from end of valid video data from Source to power off	Source	0ms	500ms	
T11	Power rail fall time, 90 to 10%	Source	-	10ms	
T12	Power off time	Source	500ms	-	

Notes:

1. When the power supply VDD is 0V, keep the level of input signals on the low or keep high impedance.
2. Do not keep the interface signal high impedance when power is on.
3. Back Light must be turn on after power for logic and interface signal are valid.
4. T11 decreases smoothly, there is none re-bouncing voltage.

9.0 MECHANICAL CHARACTERISTICS

9.1 Dimensional Requirements

FIGURE 5 (located in Appendix) shows mechanical outlines for the model MV270QHM-N40. Other parameters are shown in Table 8.

<Table 8. Dimensional Parameters>

Parameter	Specification	Unit
Dimensional outline	608.8(H) x 355.3(V)× 9.3(D) typ	mm
Weight	TBD	Kg
Active area	596.736(H) × 335.664(V)	mm
Pixel pitch	0.2331H) x 0.2331(V)	mm
Number of pixels	2560(H) ×1440(V)(1 pixel = R + G + B dots)	pixels
Back-light	Down edge side 1-LED Light bar Type	

9.2 Mounting

See FIGURE 5 .（shown in Appendix）

9.3 Anti-Glare and Polarizer Hardness.

The surface of the LCD has an anti-glare coating to minimize reflection and a coating to reduce scratching.

9.4 Light Leakage

There shall not be visible light from the back-lighting system around the edges of the screen as seen from a distance 50cm from the screen with an overhead light level of 350lux.

10.0 RELIABLITY TEST

The Reliability test items and its conditions are shown in below.

<Table 9. Reliability Test Parameters >

No	Test Items	Conditions	
1	High temperature storage test	Ta = 60 ℃, 240 hrs	
2	Low temperature storage test	Ta = -20 ℃, 240 hrs	
3	High temperature & high humidity operation test	Ta = 50 ℃, 80%RH, 240hrs	
4	High temperature operation test	Ta = 50 ℃, 240hrs	
5	Low temperature operation test	Ta = 0℃, 240hrs	
6	Thermal shock	Ta = -20 ℃ ↔ 60 ℃ (0.5 hr), 100 cycle	
7	Vibration test (non-operating)	Frequency	Random,10 ~ 300 Hz, 30 min/Axis
		Gravity\ AMP	1.5 Grms
		Period	X, Y, Z 30 min
8	Shock test (non-operating)	Gravity	50G
		Pulse width	11msec, sine wave
		Direction	±X, ±Y, ±Z Once for each
9	Electro-static discharge test	Air : 150 pF, 330Ω, 15 KV Contact : 150 pF, 330Ω, 8 KV	

11.0 HANDLING & CAUTIONS

(1) Cautions when taking out the module
- Pick the pouch only, when taking out module from a shipping package.

(2) Cautions for handling the module
- As the electrostatic discharges may break the LCD module, handle the LCD module with care. Peel a protection sheet off from the LCD panel surface as slowly as possible.
- As the LCD panel and back - light element are made from fragile glass material, impulse and pressure to the LCD module should be avoided.
- As the surface of the polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.
- Do not pull the interface connector in or out while the LCD module is operating.
- Put the module display side down on a flat horizontal plane.
- Handle connectors and cables with care.

(3) Cautions for the operation
- When the module is operating, do not lose CLK, ENAB signals. If any one of these signals is lost, the LCD panel would be damaged.
- Obey the supply voltage sequence. If wrong sequence is applied, the module would be damaged.

(4) Cautions for the atmosphere
- Dew drop atmosphere should be avoided.
- Do not store and/or operate the LCD module in a high temperature and/or humidity atmosphere. Storage in an electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.

(5) Cautions for the module characteristics
- Do not apply fixed pattern data signal to the LCD module at product aging.
- Applying fixed pattern for a long time may cause image sticking.

(6) Other cautions
- Do not disassemble and/or re-assemble LCD module.
- Do not re-adjust variable resistor or switch etc.
- When returning the module for repair or etc., Please pack the module not to be broken. We recommend to use the original shipping packages.

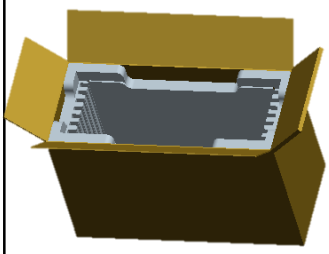
12.0 PRODUCT SERIAL NUMBER

1	2	3	4	5	6	7
X X	X	X	X X	X	X X X X	X X X X X X X

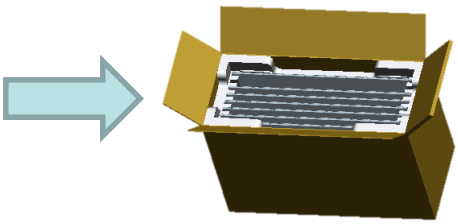
1. Control Number
2. Rank / Grade
3. Line Classification
4. Year (2001 : 01, 2002 : 02, …)
5. Month (1,2,3, … , 9, X, Y, Z)
6. Internal Use
7. Serial Number

13.0 Packing

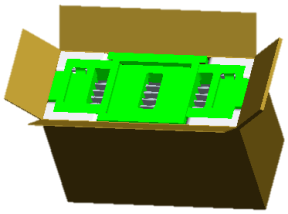
13.1 Packing Order



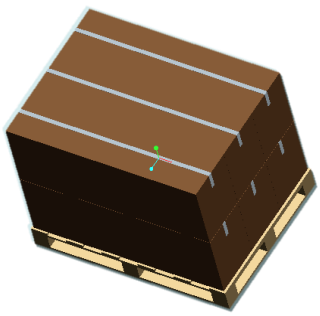
Put 1 EPO bottom into the inner box.



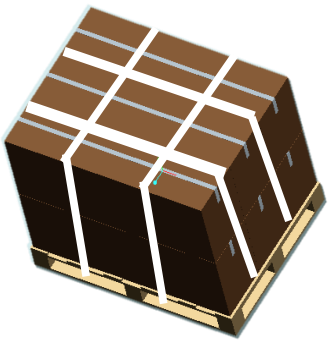
Put each module into a PE bag.
Insert 7Pcs MDL into each box.



Put 1 EPO cover in and seal the box.



Put the boxes on the pallet (12ea boxes per ballet)



Place paper corners and wrap film around the boxes.
Pack with 4 packing belts.

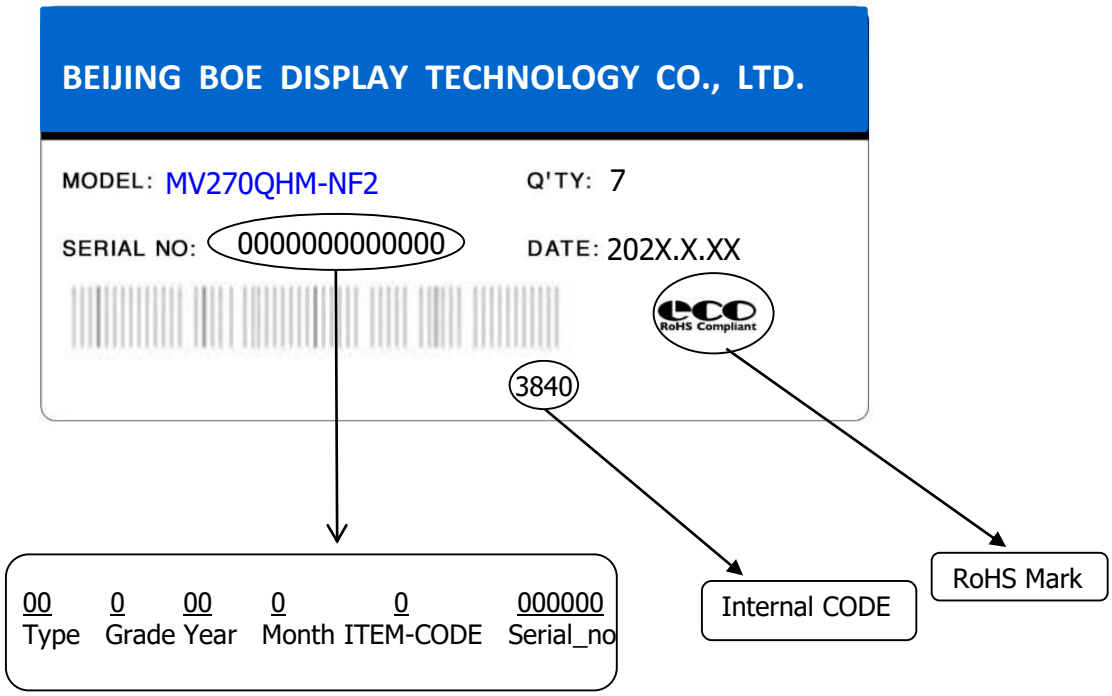
13.2 Packing Specification and Note

- Box Dimension : 687mm(L) × 289mm(W) × 461mm(H)
- Package Quantity in one Box : 7 pcs

13.3 Box label

- Label Size : 110 mm (L) × 55 mm (W)
- Contents

  Model : MV270QHM-NF2
  Q`ty : Module 7Q`ty in one box
  Serial No. : Box Serial No. See next page for detail description.
  Date : Packing Date
  FG Code : FG Code of Product



14.0 APPENDIX

Figure 1. Measurement Set Up

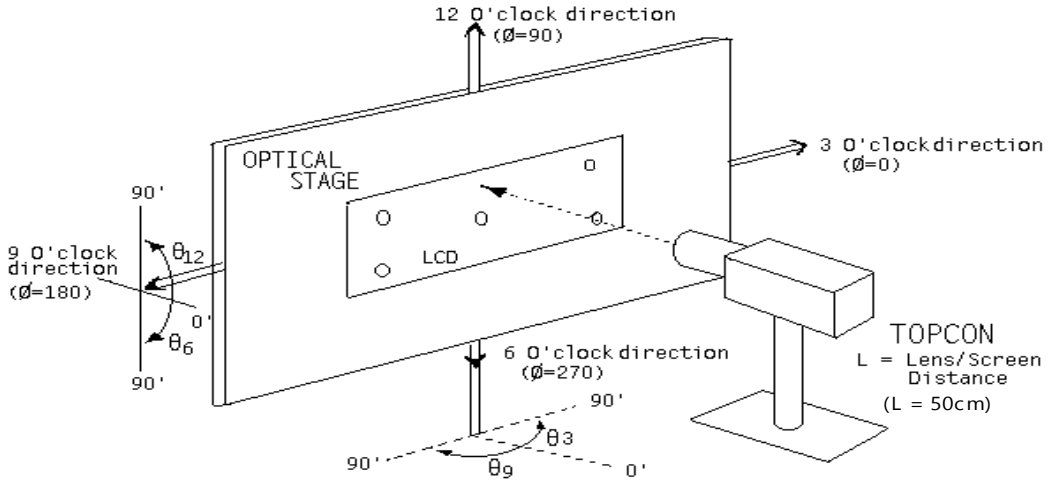


Figure 2. White Luminance and Uniformity Measurement Locations (9 points)

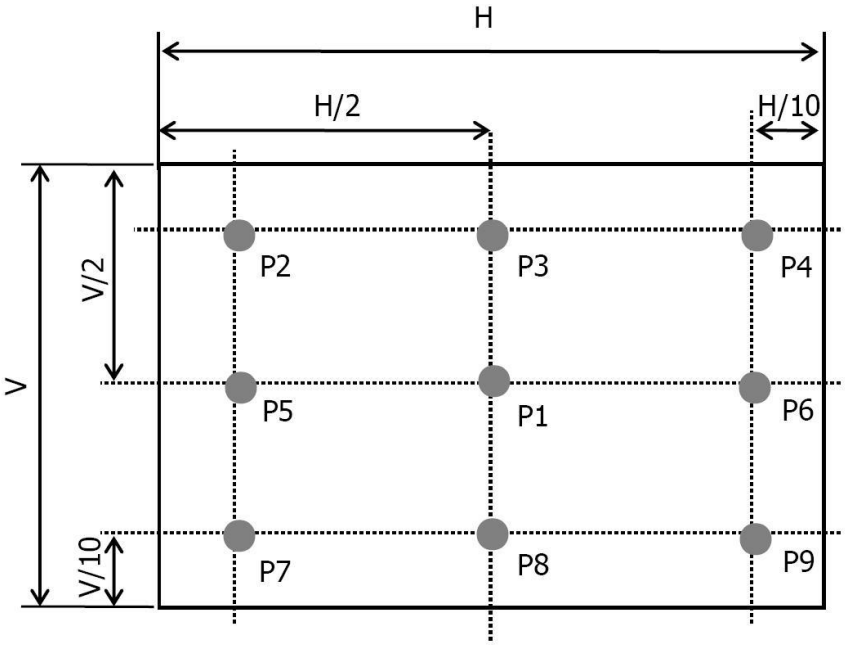
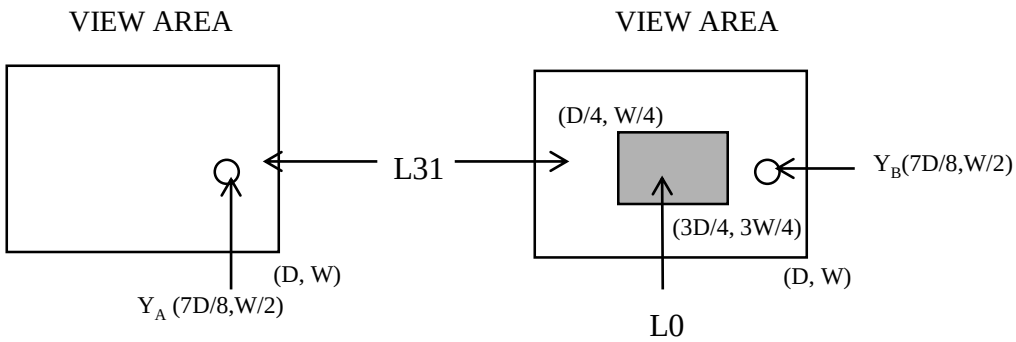


Figure 3. Response Time Testing

Measured Response Time		Target				
		0	63	127	191	255
Start	0					
	63					
	127					
	191					
	255					

Figure 4. Cross Modulation Test Description



$$\text{Cross-Talk (\%)} = \left| \frac{Y_B - Y_A}{Y_A} \right| \times 100$$

Where: Y_A = Initial luminance of measured area (cd/m^2)
Y_B = Subsequent luminance of measured area (cd/m^2)
The location measured will be exactly the same in both patterns

Figure 5. TFT-LCD Module Outline Dimensions (Front view)

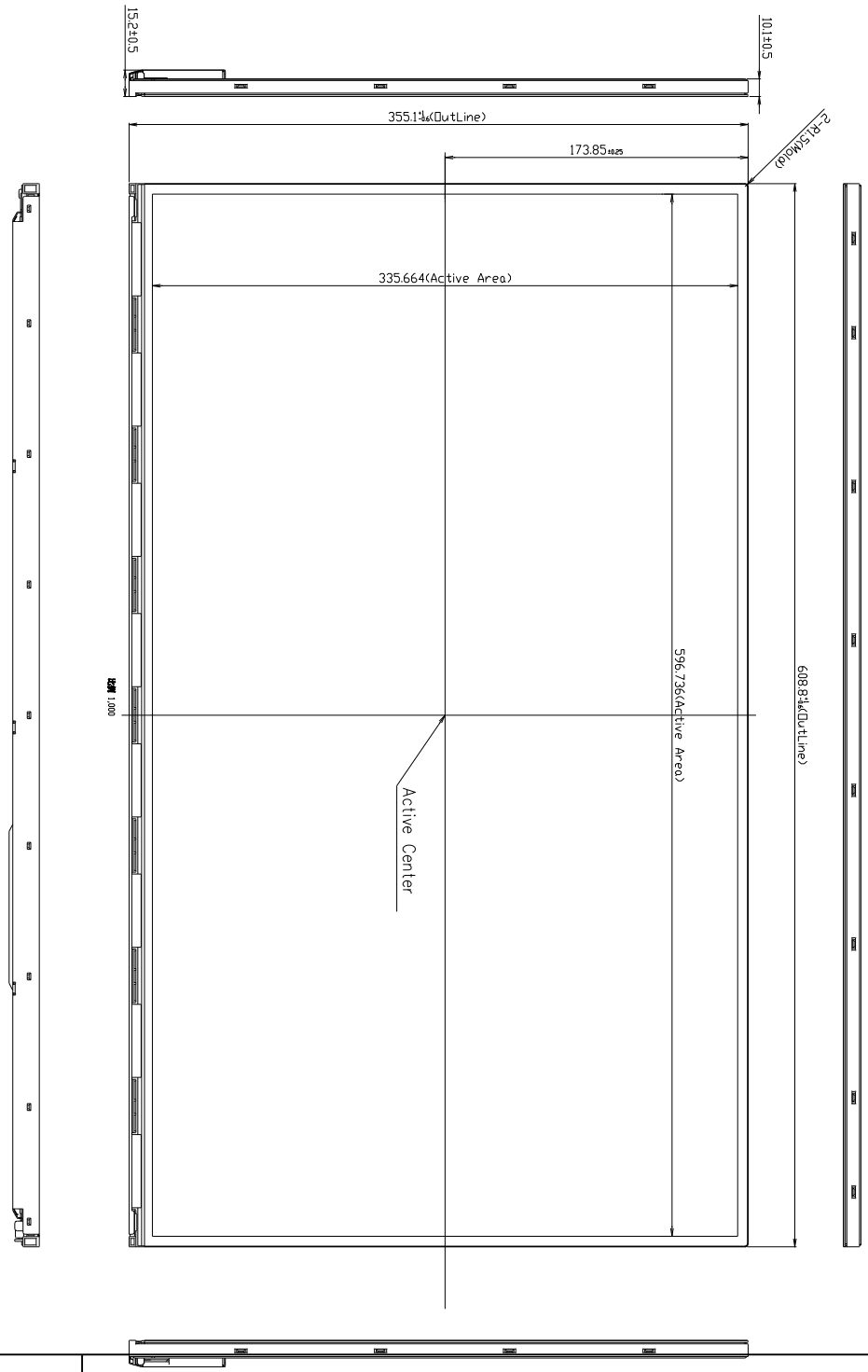


Figure 6. TFT-LCD Module Outline Dimensions (Rear view)