1.8 cm(Type 0.71) Active Matrix Color OLED Panel Module

1. Overview/Application

VX071FHP-NH2/VX071FHM-NH2 is a 0.71 inch diagonal, FHD resolution(1920 x1080), active matrix color OLED (Organic Light Emitting Display)panel module based on single crystal silicon backplane . The pixel circuits and driving IC are integrated on the silicon backplane to get the compact size and very low power consumption..

(Potential applications: Virtual Reality application（AR/VR）, Head mounted displays, Near-Eye Displays etc.)

2. Features

- Small-size, high resolution 0.71” FHD Display PPI=3135
- AP Operated Resolution 1920 x 1080 up to 90Hz
- Full color mode , 16.7M colors
- Fast response
- Thin and light in weight
- Color enhancement
- High contrast
- IR compensation with 2D
- Idle mode for save power
- Scan direction selection, up or down
- Interface，Support MIPI only or MIPI+I2C

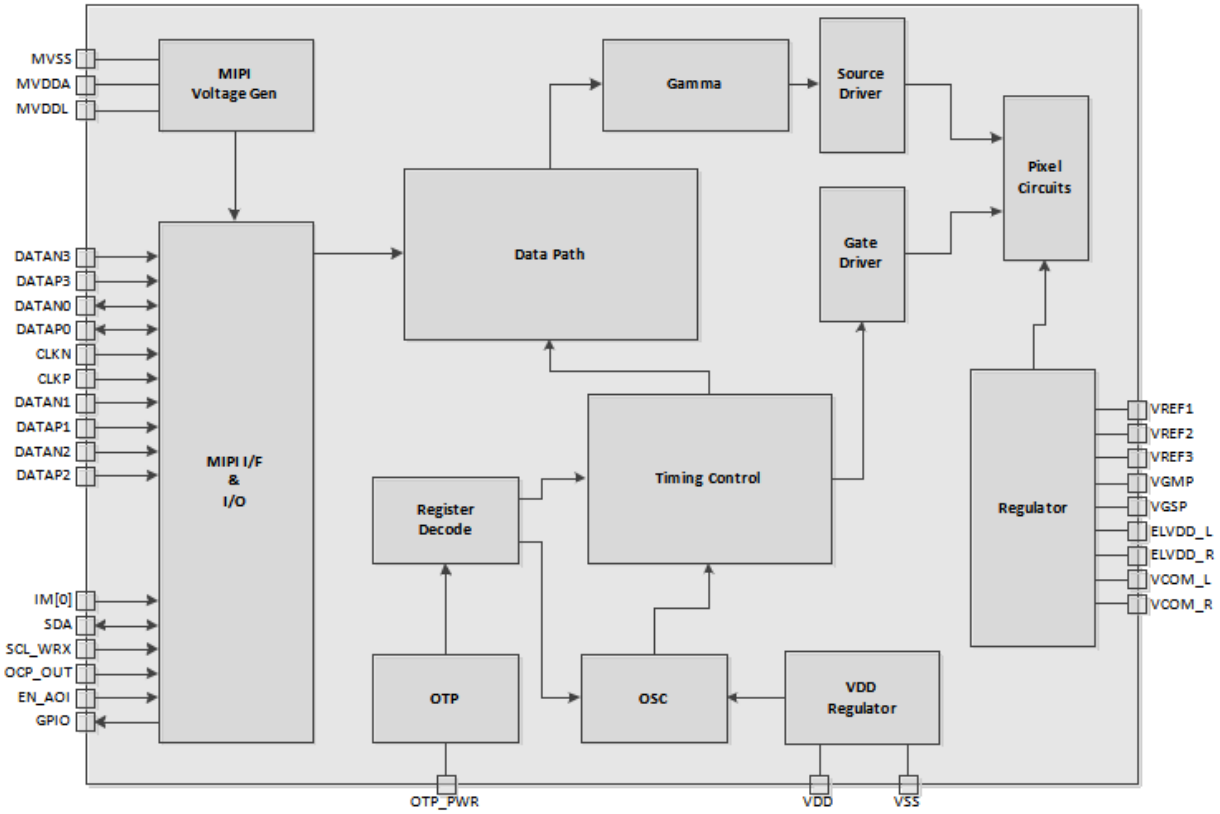
  Support VESA-DSC in-chip decoder (3X and 3.75X compression ratio)

  Support scaling up 1.33x (1440x810 to 1920 x 1080) and 1.5x (1280x720 to 1920 x 1080)
- Sequential/Global emission

3. Module Structure

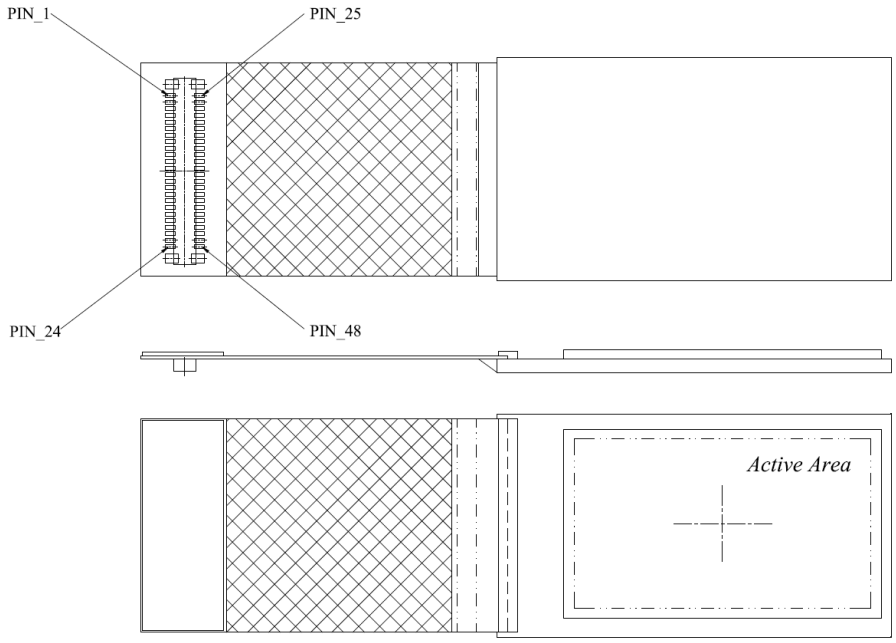
- Active matrix color OLED display with on-chip driver based on single crystal silicon transistors

4. System Block Diagram

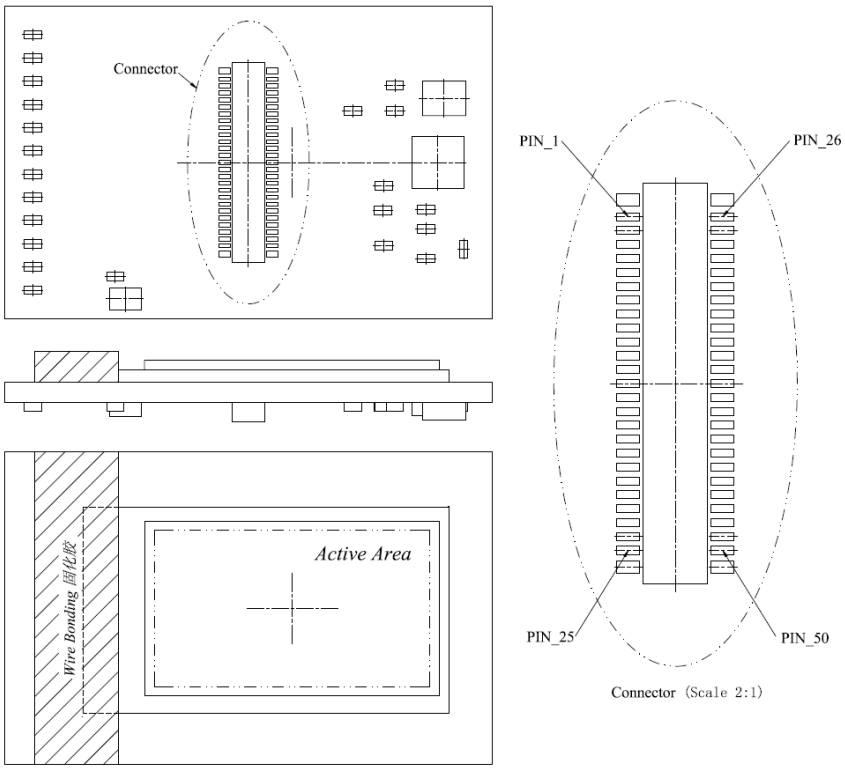


5. Pin Description

5.1 Pin Assignment



- **FPC module**



PCB module

5.2 Pin description of FPC Module

PIN No. (FPC Side)	Symbol	Type	Description
1	GND	Power Supply	Circuit ground
2	OCP_OUT	Output	Over current protect flag
3	AVEE	Power Supply	Power supply for OLED cell，Connect a capacitor for stabilization
4	AVEE	Power Supply	Power supply for OLED cell，Connect a capacitor for stabilization
5	AVDD	Power Supply	Power supply for OLED cell，Connect a capacitor for stabilization
6	AVDD	Power Supply	Power supply for OLED cell，Connect a capacitor for stabilization
7	GND	Power Supply	Circuit ground
8	ELVDD	Output	Power supply for OLED cell，Connect a capacitor for stabilization
9	ELVDD	Output	Power supply for OLED cell，Connect a capacitor for stabilization
10	GND	Power Supply	Circuit ground
11	VREF2	Output	VREF voltage，Connect a capacitor for stabilization
12	VREF3	Output	VREF voltage，Connect a capacitor for stabilization
13	VGMP	Output	Gamma top voltage，Connect a capacitor for stabilization
14	VGSP	Output	Gamma bottom voltage，Connect a capacitor for stabilization
15	VREF1	Output	VREF voltage，Connect a capacitor for stabilization
16	GND	Power Supply	Circuit ground
17	DVDD	Output	Internal system Power，Connect a capacitor for stabilization
18	DVDD	Output	Internal system Power，Connect a capacitor for stabilization
19	VDDI	Power Supply	External power supply（1.8V for digital system power）
20	VDDI	Power Supply	External power supply（1.8V for digital system power）
21	VCOM	Output	Power supply for OLED cell，Connect a capacitor for stabilization

<table>
<tr><td>22</td><td>VCOM</td><td>Output</td><td>Power supply for OLED cell，Connect a capacitor for stabilization</td></tr>
<tr><td>23</td><td>GND</td><td>Power Supply</td><td>Circuit ground</td></tr>
<tr><td>24</td><td>TEST PIN1</td><td>Input</td><td>Test pin (no connect, floating)</td></tr>
<tr><td>25</td><td>TEST PIN2</td><td>Input</td><td>Test pin (connect to GND)</td></tr>
<tr><td>26</td><td>SDA</td><td>Input/ Output</td><td>Bi-direction data PIN in I2C I/F
If this pin is not used, please connect to VDDI</td></tr>
<tr><td>27</td><td>SCL_WRX</td><td>Input</td><td>Synchronous clock signal in I2C I/F.
If this pin is not used, please connect to VDDI</td></tr>
<tr><td>28</td><td>TEST PIN3</td><td>Input</td><td>Test pin (no connect, floating)</td></tr>
<tr><td>29</td><td>IM [0]</td><td>Input</td><td>Use to select the Interface type.
<table>
<tr><th>IM [0]</th><th>Command Execute</th><th>Image Write</th></tr>
<tr><td>0</td><td>MIPI</td><td>MIPI</td></tr>
<tr><td>1</td><td>I2C/MIPI</td><td>MIPI</td></tr>
</table></td></tr>
<tr><td>30</td><td>RESX</td><td>Input</td><td>This signal will reset the device and must be applied to properly initialize the chip，
Signal is active low</td></tr>
<tr><td>31</td><td>MVDDL</td><td>Output</td><td>Internal system Power，Connect a capacitor for stabilization</td></tr>
<tr><td>32</td><td>MVDDA</td><td>Output</td><td>Internal system Power，Connect a capacitor for stabilization</td></tr>
<tr><td>33</td><td>GND</td><td>Power Supply</td><td>Circuit ground</td></tr>
<tr><td>34</td><td>DATAP2</td><td>Input</td><td>Differential small amplitude signal of MIPI data input</td></tr>
<tr><td>35</td><td>DATAN2</td><td>Input</td><td>Differential small amplitude signal of MIPI data input</td></tr>
<tr><td>36</td><td>GND</td><td>Input</td><td>Circuit ground for MIPI</td></tr>
<tr><td>37</td><td>DATAP1</td><td>Input</td><td>Differential small amplitude signal of MIPI data input</td></tr>
<tr><td>38</td><td>DATAN1</td><td>Input</td><td>Differential small amplitude signal of MIPI data input</td></tr>
<tr><td>39</td><td>GND</td><td>Input</td><td>Circuit ground for MIPI</td></tr>
<tr><td>40</td><td>CLKP</td><td>Input</td><td>MIPI CLK</td></tr>
<tr><td>41</td><td>CLKN</td><td>Input</td><td>MIPI CLK</td></tr>
<tr><td>42</td><td>GND</td><td>Input</td><td>Circuit ground for MIPI</td></tr>
<tr><td>43</td><td>DATAP0</td><td>Input/ Output</td><td>Differential small amplitude signal of MIPI data input</td></tr>
<tr><td>44</td><td>DATAN0</td><td>Input/ Output</td><td>Differential small amplitude signal of MIPI data input</td></tr>
<tr><td>45</td><td>GND</td><td>Input</td><td>Circuit ground for MIPI</td></tr>
<tr><td>46</td><td>DATAP3</td><td>Input</td><td>Differential small amplitude signal of MIPI data input</td></tr>
<tr><td>47</td><td>DATAN3</td><td>Input</td><td>Differential small amplitude signal of MIPI data input</td></tr>
<tr><td>48</td><td>GND</td><td>Input</td><td>Circuit ground</td></tr>
</table>

5.3 Pin description of PCB Module

<table>
<tr><th>PIN No.
(PCB Side)</th><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td>1</td><td>GND</td><td>Power Supply</td><td>Circuit ground</td></tr>
<tr><td>2</td><td>GND</td><td>Power Supply</td><td>Circuit ground</td></tr>
<tr><td>3</td><td>GND</td><td>Power Supply</td><td>Circuit ground</td></tr>
<tr><td>4</td><td>OCP_OUT</td><td>Output</td><td>Over current protect flag</td></tr>
<tr><td>5</td><td>GND</td><td>Power Supply</td><td>Circuit ground</td></tr>
<tr><td>6</td><td>GND</td><td>Power Supply</td><td>Circuit ground</td></tr>
<tr><td>7</td><td>DATAP2</td><td>Input</td><td>Differential small amplitude signal of MIPI data input</td></tr>
<tr><td>8</td><td>DATAN2</td><td>Input</td><td>Differential small amplitude signal of MIPI data input</td></tr>
<tr><td>9</td><td>GND</td><td>Input</td><td>Circuit ground for MIPI</td></tr>
<tr><td>10</td><td>DATAP1</td><td>Input</td><td>Differential small amplitude signal of MIPI data input</td></tr>
<tr><td>11</td><td>DATAN1</td><td>Input</td><td>Differential small amplitude signal of MIPI data input</td></tr>
<tr><td>12</td><td>GND</td><td>Input</td><td>Circuit ground for MIPI</td></tr>
<tr><td>13</td><td>CLKP</td><td>Input</td><td>MIPI CLK</td></tr>
<tr><td>14</td><td>CLKN</td><td>Input</td><td>MIPI CLK</td></tr>
<tr><td>15</td><td>GND</td><td>Input</td><td>Circuit ground for MIPI</td></tr>
<tr><td>16</td><td>DATAP0</td><td>Input/ Output</td><td>Differential small amplitude signal of MIPI data input</td></tr>
<tr><td>17</td><td>DATAN0</td><td>Input/ Output</td><td>Differential small amplitude signal of MIPI data input</td></tr>
<tr><td>18</td><td>GND</td><td>Input</td><td>Circuit ground for MIPI</td></tr>
<tr><td>19</td><td>DATAP3</td><td>Input</td><td>Differential small amplitude signal of MIPI data input</td></tr>
<tr><td>20</td><td>DATAN3</td><td>Input</td><td>Differential small amplitude signal of MIPI data input</td></tr>
<tr><td>21</td><td>GND</td><td>Input</td><td>Circuit ground</td></tr>
<tr><td>22</td><td>GND</td><td>Power Supply</td><td>Circuit ground</td></tr>
<tr><td>23</td><td>GND</td><td>Power Supply</td><td>Circuit ground</td></tr>
<tr><td>24</td><td>TEST PIN1</td><td>Input</td><td>Test pin (no connect, floating)</td></tr>
<tr><td>25</td><td>GND</td><td>Power Supply</td><td>Circuit ground</td></tr>
<tr><td>26</td><td>GND</td><td>Power Supply</td><td>Circuit ground</td></tr>
<tr><td>27</td><td>TEST PIN2</td><td>Input</td><td>Test pin (connect to GND)</td></tr>
<tr><td>28</td><td>SDA</td><td>Input/ Output</td><td>Bi-direction data PIN in I2C I/F
If this pin is not used, please connect to VDDI</td></tr>
<tr><td>29</td><td>SCL_WRX</td><td>Input</td><td>Synchronous clock signal in I2C I/F.
If this pin is not used, please connect to VDDI</td></tr>
<tr><td>30</td><td>TEST PIN3</td><td>Input</td><td>Test pin (no connect, floating)</td></tr>
<tr><td>31</td><td>IM [0]</td><td>Input</td><td>Use to select the Interface type.
<table>
<tr><th>IM [0]</th><th>Command Execute</th><th>Image Write</th></tr>
<tr><td>0</td><td>MIPI</td><td>MIPI</td></tr>
<tr><td>1</td><td>I2C/MIPI</td><td>MIPI</td></tr>
</table></td></tr>
<tr><td>32</td><td>RESX</td><td>Input</td><td>This signal will reset the device and must be applied to properly initialize the chip,
Signal is active low</td></tr>
<tr><td>33</td><td>TEST PIN4</td><td>Input</td><td>Test pin (connect to VIN)</td></tr>
<tr><td>34</td><td>TEST PIN5</td><td>Input/Output</td><td>Test pin (no connect, floating)</td></tr>
<tr><td>35</td><td>TEST PIN6</td><td>Input</td><td>Test pin (no connect, floating)</td></tr>
</table>

36	GND	Power Supply	Circuit ground
37	GND	Power Supply	Circuit ground
38	GND	Power Supply	Circuit ground
39	GND	Power Supply	Circuit ground
40	GND	Power Supply	Circuit ground
41	GND	Power Supply	Circuit ground
42	GND	Power Supply	Circuit ground
43	VDDI	Power Supply	External power supply（1.8V for digital system power）
44	VDDI	Power Supply	External power supply（1.8V for digital system power）
45	VDDI	Power Supply	External power supply（1.8V for digital system power）
46	VIN	Power Supply	External power supply（2.7V~5.5V for power IC）
47	VIN	Power Supply	External power supply（2.7V~5.5V for power IC）
48	VIN	Power Supply	External power supply（2.7V~5.5V for power IC）
49	VIN	Power Supply	External power supply（2.7V~5.5V for power IC）
50	TEST PIN7	Input	Test pin (no connect, floating)

5.4 Interface

0.71" Micro OLED supports MIPI interface and inter-integrated circuit interface(I2C). MIPI or I2C is selected by IM0, the detail interface selection by IM0 pin and shows in below table.

IM0	Command Execute	Image Write
0	MIPI	MIPI
1	I2C	MIPI

5.4.1 IIC Interface

The I2C-bus is for bi-directional, two-line communication between different ICs or modules. The two lines are the Serial Data Line(I2C_SDA) and Serial Clock Line(I2C_SCL). Both lines must be connected to a positive power supply via pull-up resistors. Data transfer can be initiated only when the bus is not busy. The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. The master generates all clock pulses, including the acknowledge ninth clock pulse.

5.4.1.1 I2C-Bus Protocol

Before any data is transmitted on the I2C-bus, the device which should response is addressed first. There are several slave addresses can be selected by MCU. The slave addressing is always carried out with the first byte transmitted after the START procedure.

Definition

-Transmitter: The device which sends the data to the bus.

-Receiver: The device which receives the data from the bus.

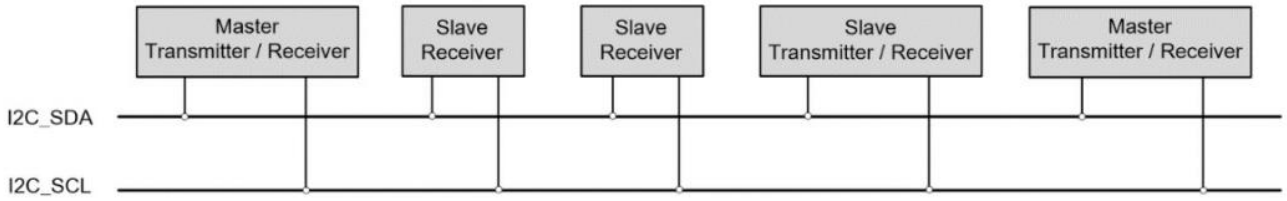
-Master: The device which initiates a transfer, generates clock signals and terminates a transfer.

-Slave: The device addressed by a master.

-Multi-master: More than one master can attempt to control the bus at the same time without corrupting the message.

-Arbitration: Procedure to ensure that. If more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted.

-Synchronization: Procedure to synchronize the clock signals of two or more devices.



5.4.1.2 Write Sequence

0.71" Micro OLED supports register write sequence via I2C-bus transfer. The register writing supports single register write mode. The detailed transfer sequences are illustrated and described as below.

(1) Data transfer for register writing should follow the format shown as below.

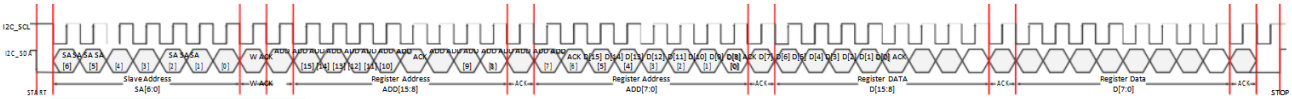
(2)After the START condition, a slave address is sent. R/$\overline{W}$ bit is setting to "0" for Write.

(3)The slave issues an ACK to the master.

(4)8-bits register address transfer first then transfer the register data parameter.

(5)A data transfer is always terminated by a STOP condition.

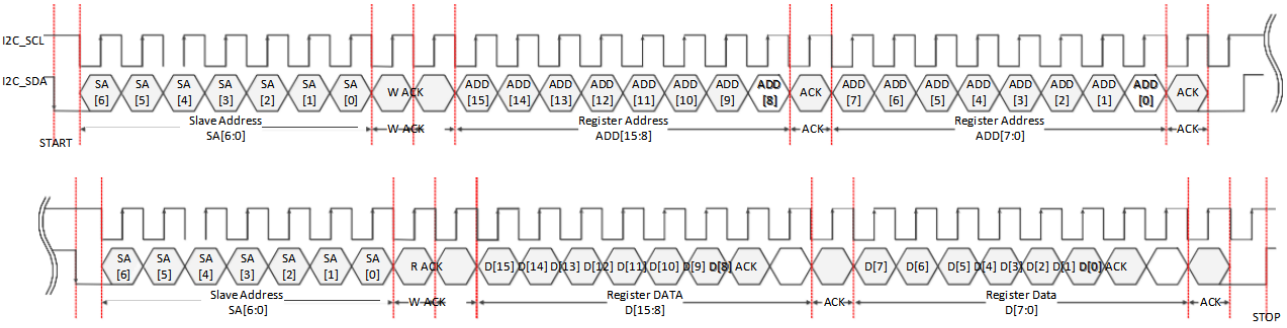
(6) The chip SA[6:0]=100_1100.



W : Write Bit, W=" 0 "here.
ACK : Acknowledge Bit, ACK=" 0 " here
SA[6:0] : Slave Address.
ADD[15:0] : Register Address.
D[15:0] : : Register Data.

5.4.1.3 Read Sequence

0.71" Micro OLED supports register read sequence via I2C-bus transfer. The register reading supports single register read mode. The register data reading transfer are shown as below.



W : Write Bit, W=" 0 " here.
R : Read Bit, R=" 1 " here.
ACK : Acknowledge Bit, ACK=" 0 " here
SA[6:0] : Slave Address.
ADD[15:0] : Read Register Address.
D[15:0] : : Read Register Return Data.

5.4.2 MIPI Interface

Display serial interface(DSI) specifies the interface between a host processor and a peripheral such as a display module. It builds on existing MIPI Alliance specification by adoption pixel formats and command set. The detail Lane configuration for DPHY is listed below.

There are one Clock Lane and 1~4 Data Lane. The configuration for DPHY between host and 0.71" Micro OLED shows as the table below.

Lane Pair	Available Operation Mode	
Clock Lane	Unidirectional Lane	Forward High-Speed Clock Escape Mode (ULPS only)
Data Lane 0	Bi-directional Lane	Forward High-Speed Data Bi-directional Escape Mode Bi-directional LPDT
Data Lane 1	Unidirectional Lane	Forward High-Speed Data No LPDT Escape Mode (ULPM only)
Data Lane 2	Unidirectional Lane	Forward High-Speed Data No LPDT Escape Mode (ULPM only)
Data Lane 3	Unidirectional Lane	Forward High-Speed Data No LPDT Escape Mode (ULPM only)

5.4.2.1 Packet Footer for Long Packets

The Packet Footer for Long Packets is a checksum value which is calculated from the Data Payload in the Long Packet. The checksum is using a 16-bit Cyclic Redundancy Check(CRC) with a generator polynomial of x^16 + x^12 + x^5 + x^0. The Receiver will calculate checksum value from received Data Payload and compare this CRC value with the Packet Footer sent by transmitter. If calculated CRC values equal to Packet Footer, the received Data Payload are correct. The CRC implementation is presented as the following.

5.4.2.2 Packet Pixel Stream Format

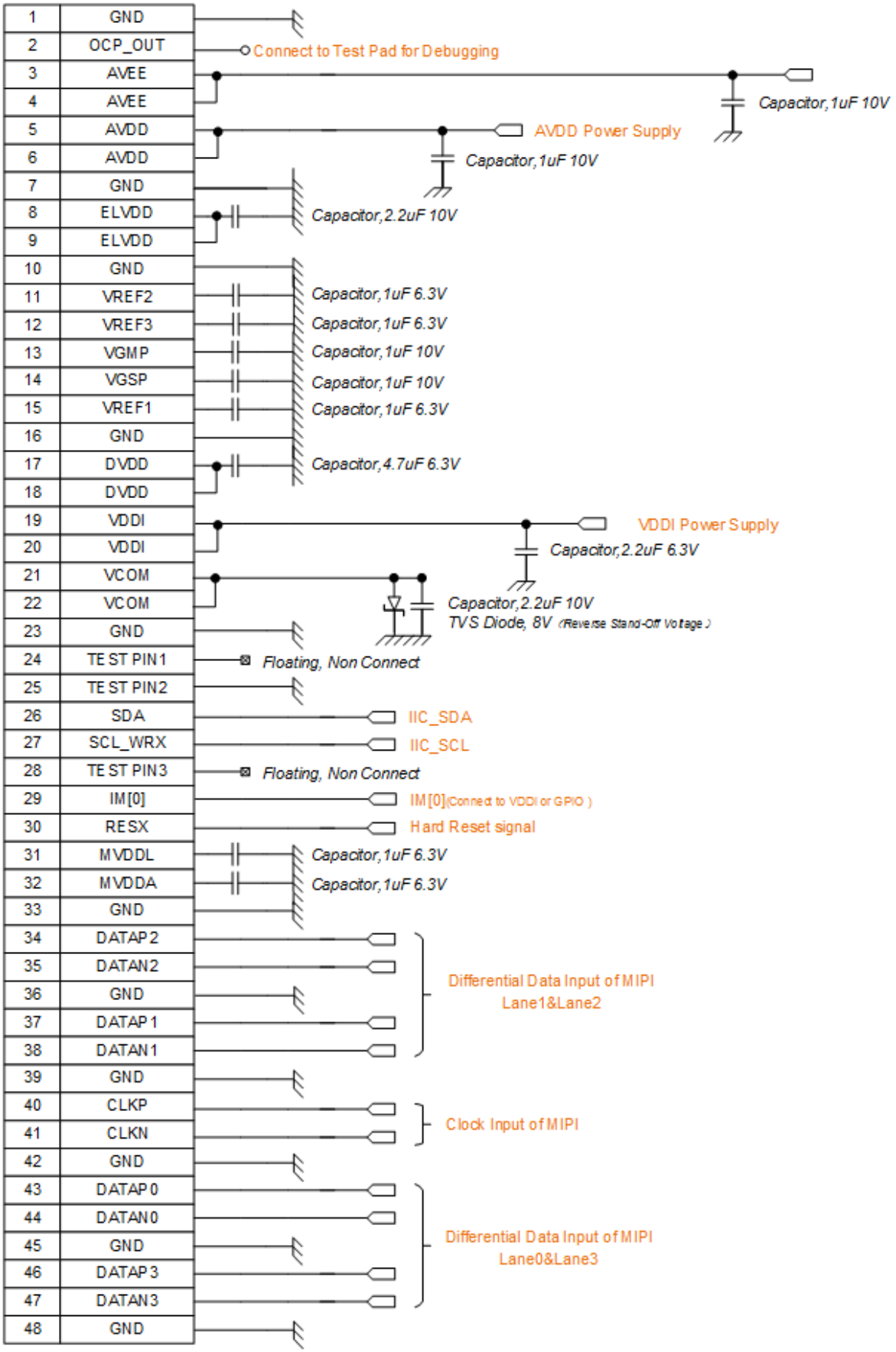
There are 4 packet pixel stream format: 16-bit RGB 5-6-5, 18-bit RGB 6-6-6, loosely packed 18- bit RGB 6-6-6 and 24-bit RGB 8-8-8. The Data Type for these pixel stream format are shown as the table below.

Data Type(hex)	Data Type(binary)	Description	Packet Size
0x0E	00 1110	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	Long
0x1E	01 1110	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
0x2E	10 1110	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
0x3E	11 1110	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	Long

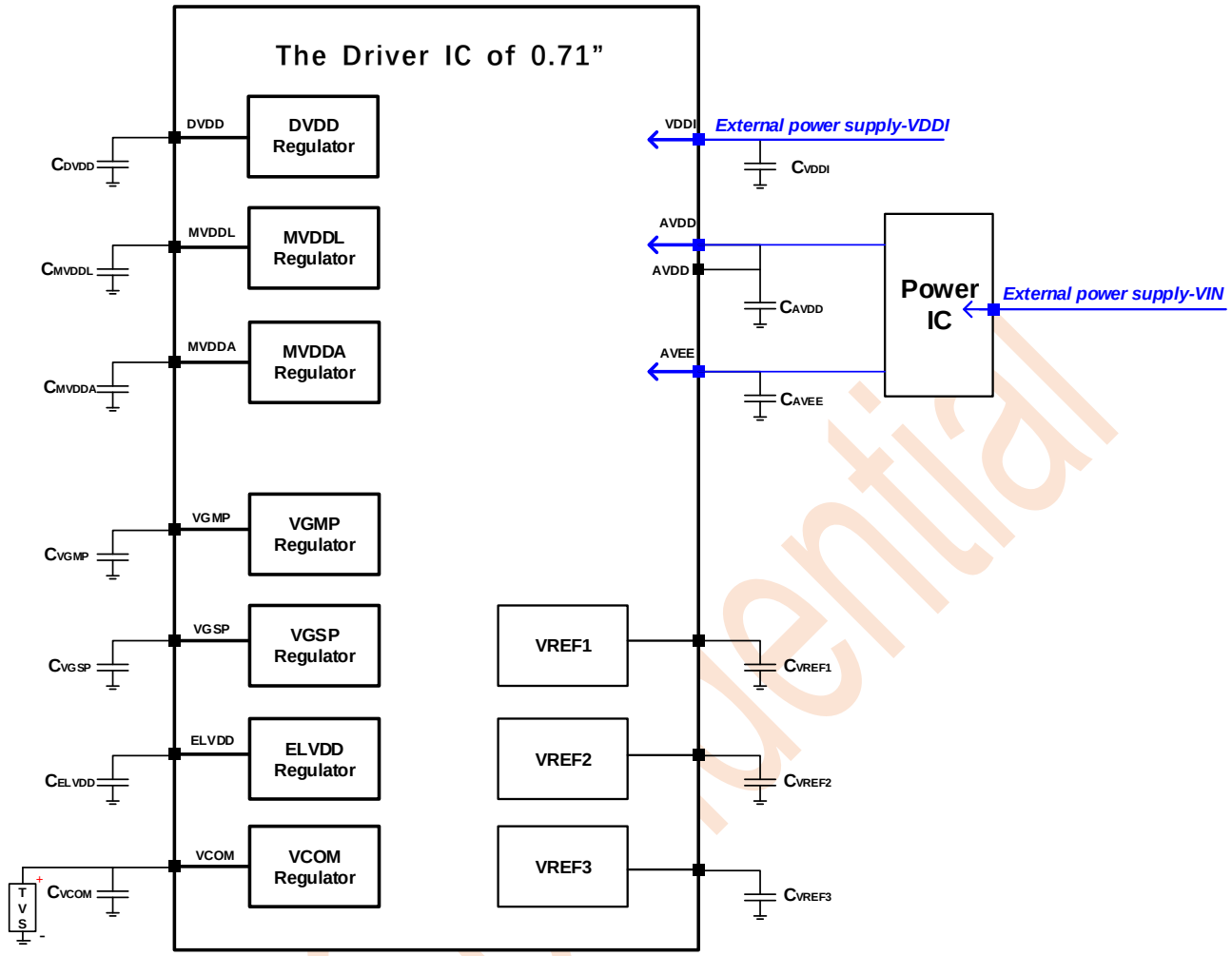
Note: 0.71" Micro OLED only support 24-bit RGB pixel stream format

5.5 Peripheral Circuit

FPC Module



Mounting the capacitor for each power supply to ensure that the panel display normally.



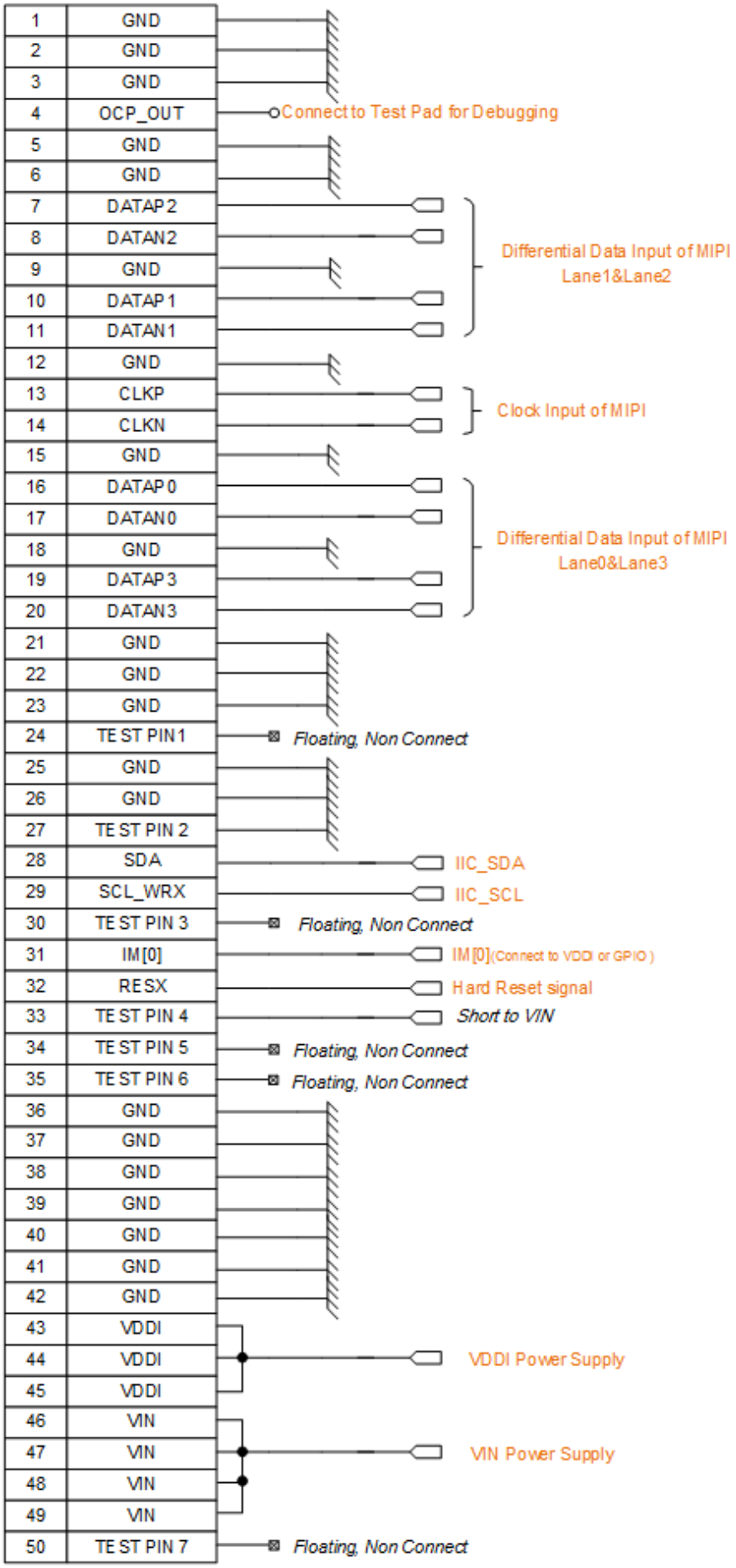
Notes:

No.	Signal Name	Typical Value	Maximum Rated Voltage	Note
1	VDDI	Cap, 2.2uF	6.3V	
2	AVDD	Cap, 1.0uF	10V	
3	ELVDD	Cap, 2.2uF	10V	
4	AVEE	Cap, 1.0uF	10V	
5	DVDD	Cap, 4.7uF	6.3V	
6	MVDDA	Cap, 1uF	6.3V	
7	MVDDL	Cap, 1uF	6.3V	
8	VGMP	Cap, 1uF	10V	
9	VGSP	Cap, 1uF	10V	
10	VREF1	Cap, 1uF	6.3V	
11	VREF2	Cap, 1uF	6.3V	
12	VREF3	Cap, 1uF	6.3V	
13	VCOM	Cap, 2.2uF TVS	10V	

(1) There are totally 13 capacitors and 1 Schottky diode.

(2) The Schottky diode is placed between VCOM and ground, and the anode connect to Vcom, the cathode connect to GND.

PCB Module



6. Absolute Maximum Ratings

The absolute maximum rating is listed on the below table. When the VTOS6203 is used beyond the absolute maximum ratings, it may be permanently damaged. It is strongly recommended use the driver IC within the following specified limits for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the driver IC will malfunction and cause poor reliability.

Item	Symbol	Value	Unit
Power Supply Voltage (1)	VDDI	5.5	V
Power Supply Voltage (2)	AVDD-AVSS	6.6	V
	AVEE-AVSS	6.6	V
Power Supply Voltage in AOI mode	VDDI	1.65	V
	AVDD-AVSS	6.6	V
	AVEE-AVSS	6.6	V
MIPI Differential Input	CLKP,CLKN DATAP0,DATAN0 DATAP1,DATAN1 DATAP2,DATAN2 DATAP3,DATAN3	1.32	V
Input Voltage of Interface	Vin	-0.3 ~ VDDI+0.3	V
Output Voltage of Interface	Vo	-0.3 ~ VDDI+0.3	V
Operating temperature	Topr	-30 ~ 70	°C
Storage temperature	Tstg	-45 ~ 90	°C

Note:

1. The environment temperature is not a RA test temperature.

7. Electrical Characteristics

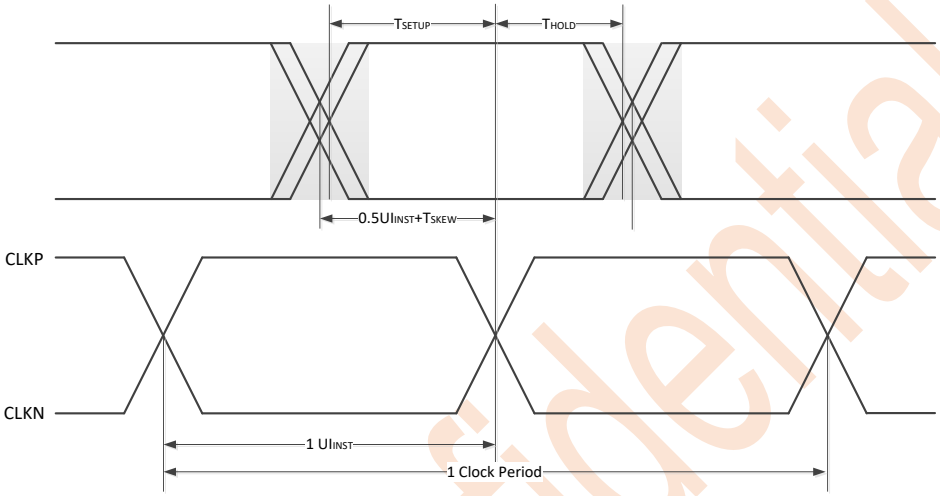
7.1 DC Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power & Operation Voltage/Current						
VIN Input Level (PCB MDL)	VIN Voltage	-	2.7	5.0	5.5	V
	VIN Loading Current	Driving current≥ Loading current			300	mA
AVDD Input Level (FPC MDL)	AVDD Voltage	-	5.5	6.0	6.5	V
	AVDD Loading Current	Driving current≥ Loading current	-	-	260	mA
AVEE Input Level (FPC MDL)	AVEE Voltage	-	-5.5	6.0	-6.5	V
	AVEE Loading Current	Driving current≥ Loading current	-	-	260	mA
VDDI Input Level	VDDI Voltage	-		1.8		V
	VDDI Loading Current	Driving current≥ Loading current	-	-	200	mA
MIPI I/O Power Supply	MVDD	-	-	1.2	-	V

7.2 AC Characteristics

7.2.1 MIPI High Speed Mode Characteristics

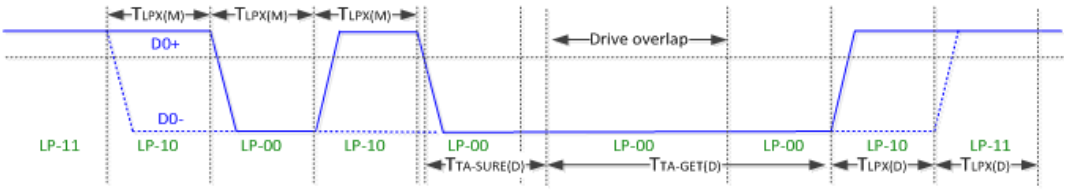
Parameter	Symbol	Min	Typ.	Max	Unit
UI instantaneous	UIINST	1	-	3	ns
T Data to Clock Skew	TSKEW	-0.15	-	0.15	UIHS
RX Data to Clock Setup Time Tolerance	TSETUP	0.15	-	-	UIHS
RX Data to Clock Hold Time Tolerance	THOLD	0.15	-	-	UIHS



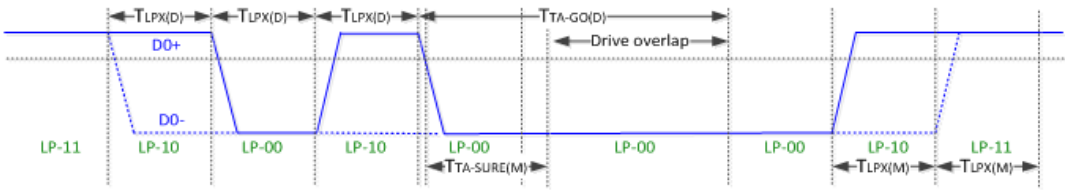
7.2.2 MIPI Low Power Mode Characteristics

Parameter	Description	Min	Typ.	Max	Unit
$T_{LPX(M)}$	Transmitted length of any Low-Power state period (MCU to display module)	50	-	-	ns
$T_{LPX(D)}$	Transmitted length of any Low-Power state period (display module to MCU)	50	-	-	ns
$T_{TA-SURE}$	Time that the new transmitter waits after the LP-10 state before transmitting the Bridge state(LP-00) during a Link Turnaround	T_{LPX}	-	$2*T_{LPX}$	
T_{TA-GET}	Time that the new transmitter drives the Bridge state(LP-00) after accepting control during a Link Turnaround	$5*T_{LPX}$			
T_{TA-GO}	Time that the transmitter drives the Bridge state(LP-00) before releasing control during a Link Turnaround	$4*T_{LPX}$			

- Bus Turnaround from MPU to display module



- Bus Turnaround from display module to MPU



7.2.3 MIPI Video Timing Specification.

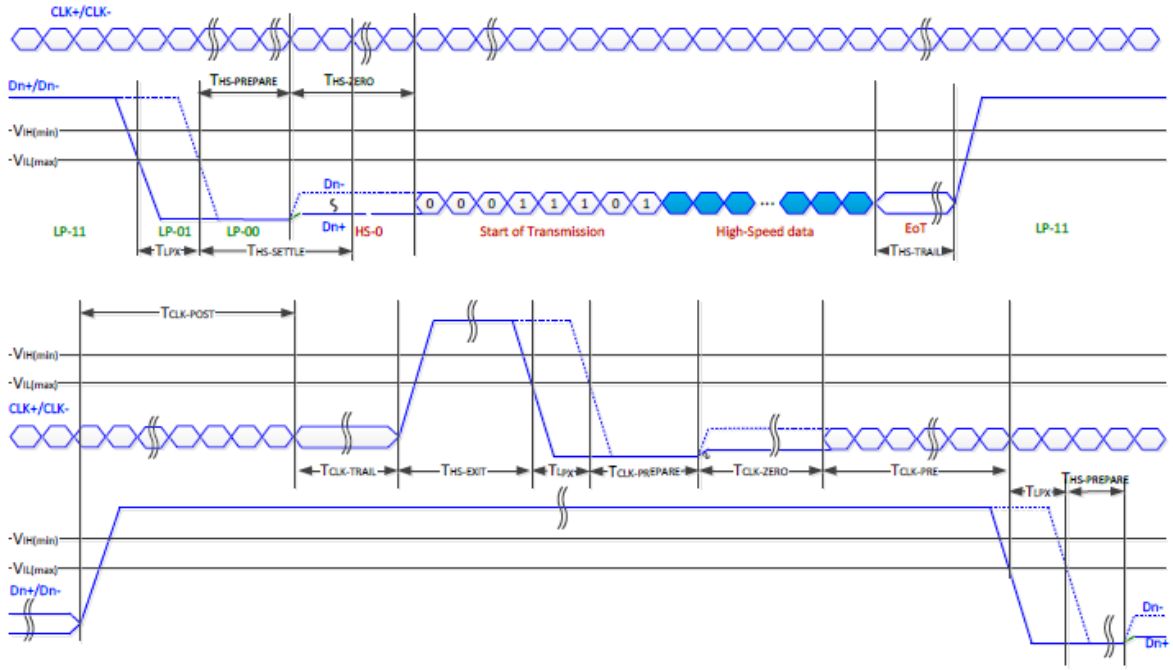
1920×1080@60Hz					
H	Hsync	32	V	Vsync	4
	HBP	72		VBP	8
	Hactive	1920		Vactive	1080
	HFP	56		VFP	8
Pclk （MHz）	955.47				
Recommended configuration of MIPI					
D-PHY V1.2 DSI 1.01	CLK Mode: Discontinue Mode				
	MIPI Lane: 4 Lanes@60Hz				
	Video Mode: Burst Mode				
	HS Speed: 80Mbps ~ 1.0Gbps per Lane				
	LP Speed: 10Mbps（max）				
	General Packet Structure：DCS Mode .Data Type of Packet：0x39 or 0x05				

※This parameter is a typical example illustrating the display timing. BOE cannot assume responsibility for any problems arising out of the use of the circuit.

7.2.4 High Speed Mode Operation Timing Characteristics

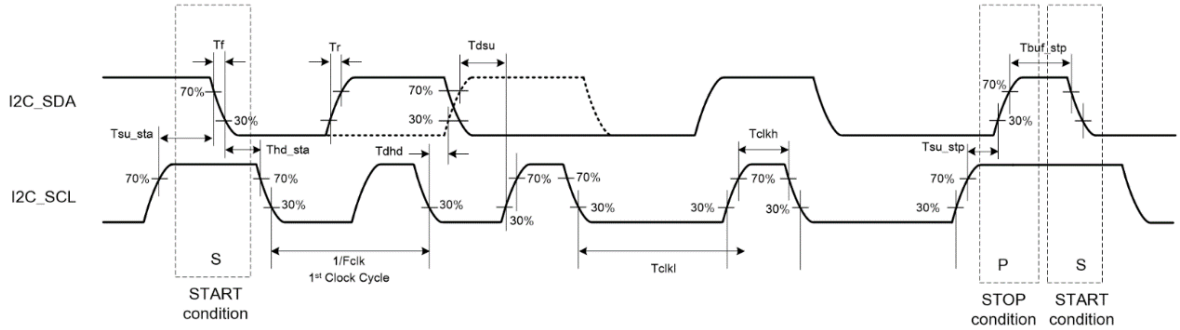
Parameter	Description	Min	Typ.	Max	Unit
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of $T_{HS-TRAIL}$ to the beginning of $T_{CLK-TRAIL}$	60ns+52*UI	-	-	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode	8	-	-	UI
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	38	-	95	ns
$T_{CLK-SETTLE}$	Time interval during which the HS receiver should ignore any Clock Lane HS transitions, starting from the beginning of $T_{CLK-PREPARE}$	95	-	300	ns
$T_{CLK-TERM\_EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$	-	-	38	ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst	60	-	-	ns
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock	300	-	-	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst	100	-	-	ns
T_{D-TERM_EN}	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$	-	-	35ns+4*UI	ns
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40ns+4*UI	-	85ns+6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence	145ns+10*UI	-	-	ns

$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of $T_{HS-PREPARE}$. The HS receiver shall ignore any Data Lane transitions before the minimum value, and the HS receiver shall respond to any Data Lane transitions after the maximum value.	85ns+6* UI		145ns+1 0*UI	ns



7.2.5 I2C Interface Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
I2C Clock Frequency	Fclk	-	-	400	kHz
I2C Clock Low	Tclkl	1300	-	-	ns
I2C Clock High	Tclkh	600	-	-	ns
I2C Data Rising Time	Tdr	-	-	300	ns
I2C Data Falling Time	Tdf	-	-	300	ns
I2C Data Setup Time	Tdsu	100	-	-	ns
I2C Data Hold Time	Tdhd	-	-	TBD	ns
I2C Setup Time (Start Condition)	Tsu_sta	600	-	-	ns
I2C Hold Time (Start Condition)	Thd_sta	600	-	-	ns
I2C Setup Time (Stop Condition)	Tsu_stp	600	-	-	ns
I2C Bus Free Time (Stop Condition)	Tbuf_stp	1300	-	-	ns

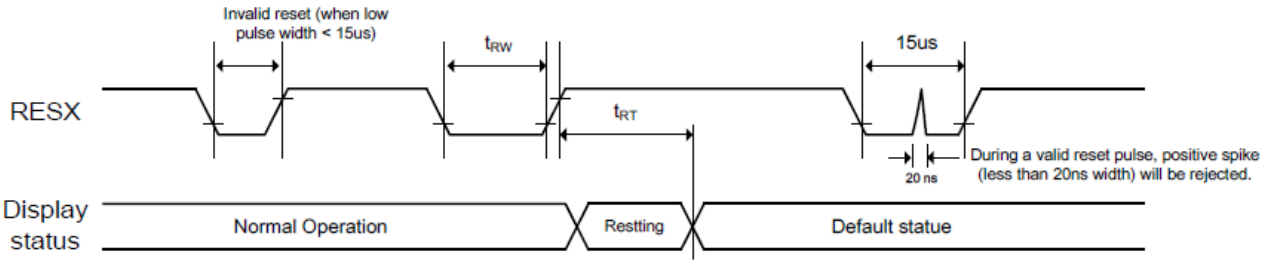


Notes:

No.	ITEM	Description	Note
1	Slave address	0x4C	
2	Pull-up resistor	4.7KΩ@100Kbps	
3	Read bit	Setting “1” for write	
4	Write bit	Setting “0” for write	
5	Start condition	SDA is setting from “1” to “0” when SCL is “1”	
6	Stop condition	SDA is setting from “0” to “1” when SCL is “1”	

7.2.6 Rest Timing Characteristics

When Reset happens in Sleep-out mode, the driver IC will enter blanking sequence with the maximum time 120 msec. Then driver IC will remain in blanking state and return IC’s default state. During reset complete time (t_{RT}), data in OTP will be re-loaded and latched to internal registers. This data re-load is done every time when there is an H/W reset and completes within 20 msec after the rising edge of RESX. Therefore, it is necessary to wait at least 20 msec after releasing the RESX before sending commands. Moreover, the Sleep-out command cannot be sent in 120 msec. Spike (less than 20ns width) Rejection can also be applied during a valid reset pulse.



Reset time @ VDDI=1.65V to 1.95V, AVSS=VSS=MVSS=0V, Ta=-40°C to 85°C

Signal	Symbol	Parameter	Min.	Typ.	Max.	Unit	Description
RESX	t_{RW}	Reset low pulse width	15			us	
	t_{RT}	Reset Complete time			20	ms	When reset applied at sleep-in mode
					120	ms	When reset applied at sleep-out mode

7.3 Power Consumption

Item		Symbol	Condition	Typ.		Unit
				200cd/m²	300cd/m²	
FPC MDL	AVDD power consumption	AVDD	- Tpnl = 40°C	110	160	mW
	AVEE power consumption	AVEE		165	215	mW
	VDDI Input Level	VDDI		75	75	mW
	Total	Total power		340	450	mW

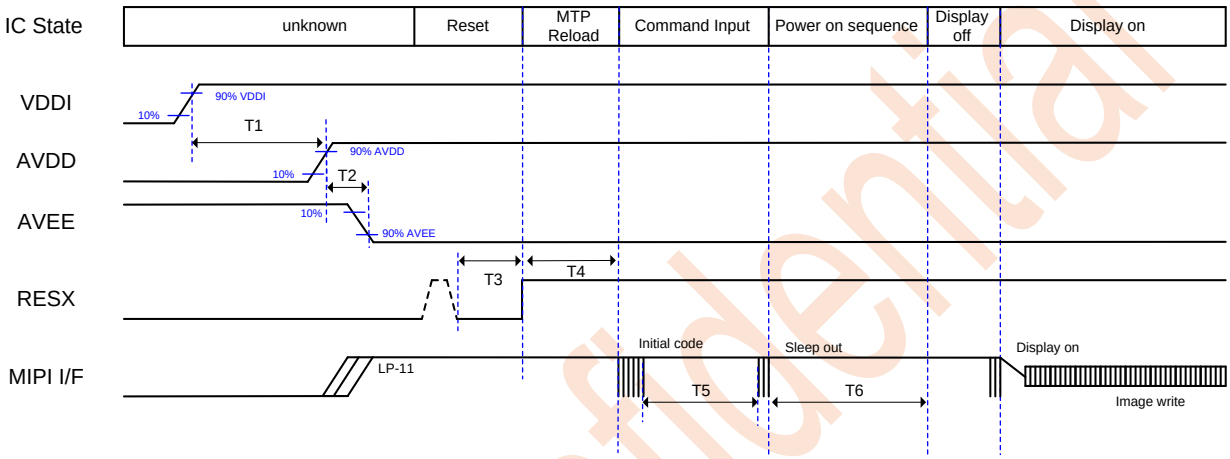
PCB MDL	VIN power consumption	VIN	- Tpnl = 40°C	345	495	mW
	VDDI Input Level	VDDI		75	75	mW
	Total	Total power		420	570	mW

Note: All white raster display, clock frequency=148.5MHz, frame rate=60Hz, resolution= 1920 x 1080

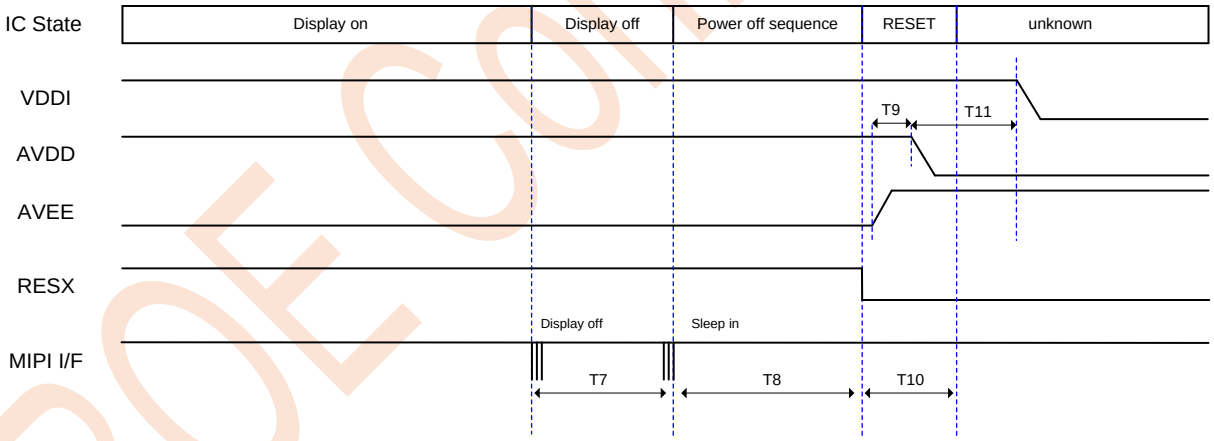
8. Power Supply Sequence

8.1 Power On/Off Sequence

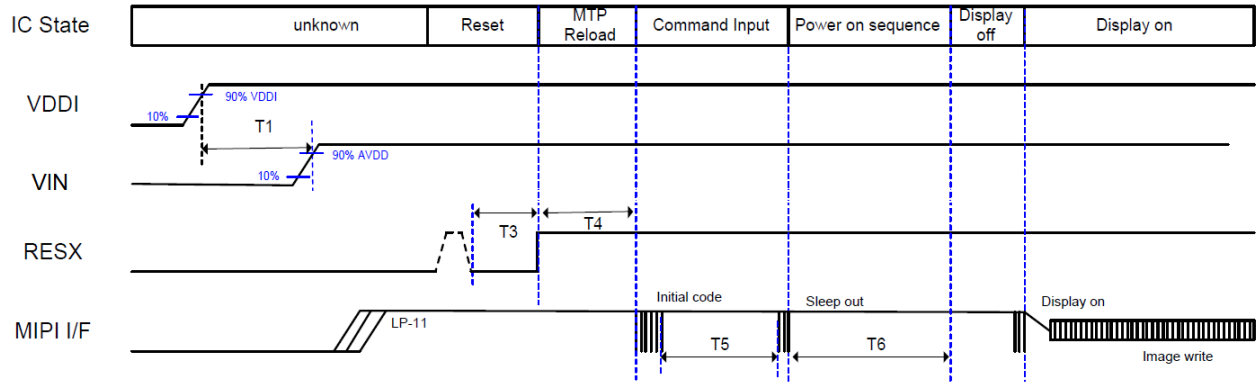
Power on sequence of FPC MDL



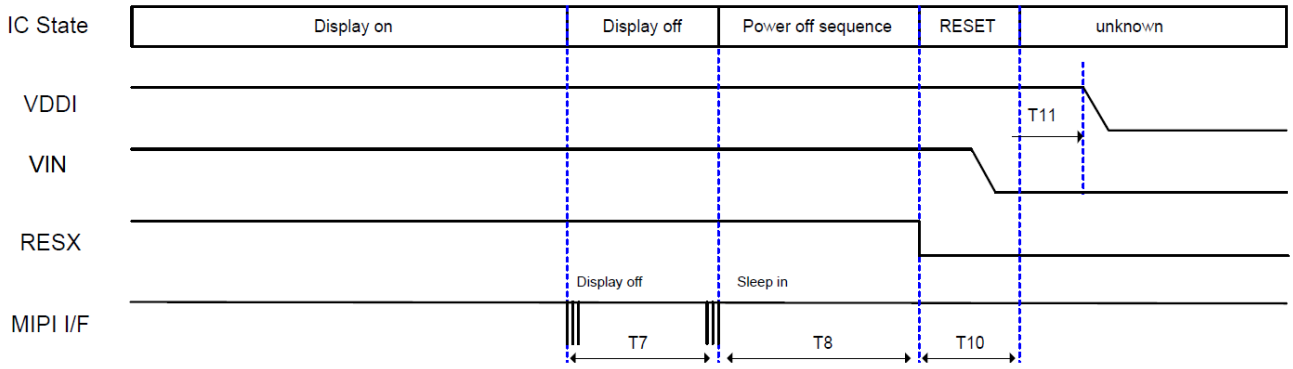
Power off sequence of FPC MDL



Power on sequence of PCB MDL



Power off sequence of PCB MDL



Symbol	Min.	Typ.	Max.	Unit	Description
T1	1	-	-	ms	Power on time between AVDD and VDDI
T2	1	-	-	ms	Power on time between AVDD and AVEE
T3	1	-	-	ms	Effective hardware reset period
T4	20	-	-	ms	MTP reload time
T5	0	-	-	ms	The time is between initial code finished and sleep-out command
T6	2	-	8	VS	Power on sequence, the period can be modified
T7	1	-	-	VS	Blanking region
T8	-	1	-	VS	Power off sequence, the period can be modified
T9	1	-	-	ms	Power off time between AVEE and AVDD
T10	1	-	-	ms	Effective hardware reset period
T11	1	-	-	ms	Power off time between AVEE and VDDI

9. Description of Function

9.1 Display Mode

9.1.1 Power Mode

ITEM	Code value
Sleep In	0x10
Sleep Out	0x11
Display On	0x29
Display Off	0x28

9.1.2 Idle Mode

ITEM	Code value
Idle On	0x39(Default value)
Idle Off	0x38

9.1.3 BIST Mode

Register setting：

◆ BIST On/Off Control (C4h)

<table>
<tr><td rowspan="2">Instruction</td><td rowspan="2">R/W</td><td colspan="2">Address name</td><td colspan="9">Parameter</td></tr>
<tr><td>MIPI</td><td>Other</td><td>D15-D8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td rowspan="4">BISTONOFF</td><td rowspan="4">R/W</td><td rowspan="4">C4h</td><td>C400h</td><td>-</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>C401h</td><td>-</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>C402h</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>BION1</td></tr>
<tr><td>C403h</td><td>-</td><td>BION2</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to control BIST function (Free Run mode).
BIST function enable step:
1. Enter Sleep-In(10h) mode.
2. Setting PATENICYC[1:0] and BISTPATEN[11:0] to control the display cycle time and pattern.
3. Setting BION1=”1” and BION2=”1”, the driver IC will start to run the BIST function.
BIST function disable step:
1. Setting BION1=”0” and BION2=”0”,the driver IC will return to normal function.
2. Sending MIPI video data and enter Sleep-Out(11h) mode for normal display.</td></tr>
<tr><td>Restriction</td><td colspan="12">-</td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><td>Status</td><td colspan="2">Default Value</td></tr><tr><td rowspan="4">Power On Sequence</td><td>C400h</td><td>AAh</td></tr><tr><td>C401h</td><td>55h</td></tr><tr><td>C402h</td><td>00h</td></tr><tr><td>C403h</td><td>00h</td></tr></table></td></tr>
</table>

◆ BIST CTRL (C5h)

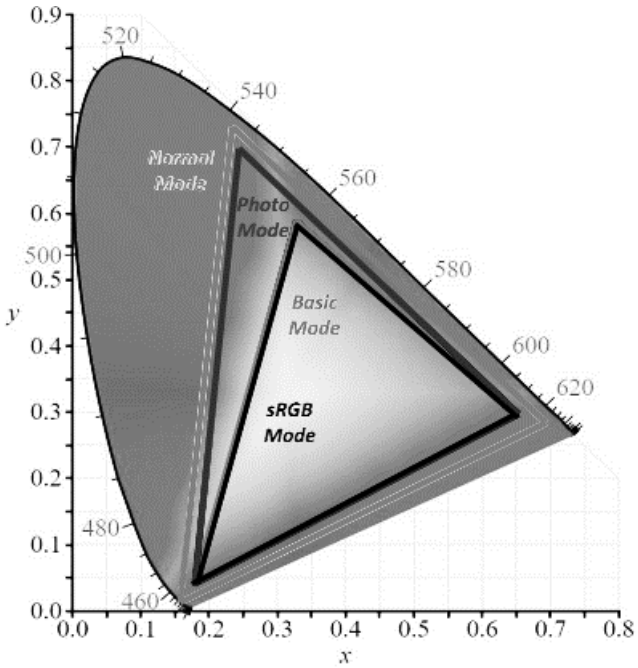
<table>
<tr><th rowspan="2">Instruction</th><th rowspan="2">R/W</th><th colspan="2">Address name</th><th colspan="9">Parameter</th></tr>
<tr><th>MIPI</th><th>I2C</th><th>D15-D8</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td rowspan="3">BISTSET</td><td rowspan="3">R/W</td><td rowspan="3">C5h</td><td>C500h</td><td>-</td><td>0</td><td>0</td><td colspan="2">PATENICYC[1:0]</td><td colspan="4">BISTPATEN[11:8]</td></tr>
<tr><td>C501h</td><td>-</td><td colspan="8">BISTPATEN[7:0]</td></tr>
<tr><td>C502h</td><td>-</td><td colspan="8">GRAY_LEVEL[7:0]</td></tr>
<tr><td>escription</td><td colspan="11">
This command is used to set the display pattern in BIST function.
PATENICYC[1:0] : Cycle time between each display pattern.
<table>
<tr><th>PATENICYC[1:0]</th><th>Pattern cycle time</th></tr>
<tr><td>0h</td><td>256 Frame</td></tr>
<tr><td>1h</td><td>512 Frame</td></tr>
<tr><td>2h</td><td>1024 Frame</td></tr>
<tr><td>3h</td><td>2048 Frame</td></tr>
</table>
BISTPATEN[11:0] : Select the display pattern in BIST function.
<table>
<tr><th>BISTPATEN[9:0]</th><th>Description</th></tr>
<tr><td>BISTPATEN[0]</td><td>Red pattern.</td></tr>
<tr><td>BISTPATEN[1]</td><td>Green pattern.</td></tr>
<tr><td>BISTPATEN[2]</td><td>Blue pattern.</td></tr>
<tr><td>BISTPATEN[3]</td><td>Black pattern.</td></tr>
<tr><td>BISTPATEN[4]</td><td>Gray Level pattern. (Set by BIST_GRAY_LEVEL[7:0])</td></tr>
<tr><td>BISTPATEN[5]</td><td>Vertical Gradation pattern.</td></tr>
<tr><td>BISTPATEN[6]</td><td>Horizontal Gradation pattern.</td></tr>
<tr><td>BISTPATEN[7]</td><td>Color Bar pattern.</td></tr>
<tr><td>BISTPATEN[8]</td><td>Crosstalk with boundary pattern.</td></tr>
<tr><td>BISTPATEN[11]</td><td>Reserved</td></tr>
</table>
Note1: the patterns which the bit number of BISTPATEN[9:0] is set to “1” will display and change automatically.
Note2: When BISTPATEN[11:0]=12’h000, display pattern will be black pattern.

GRAY_LEVEL[7:0] : Set the gray level when BISTPATEN[4]=”1” in BIST function.
<table>
<tr><th>GRAY_LEVEL[7:0]</th><th>Description</th></tr>
<tr><td>0h</td><td>Gray Level : 00h</td></tr>
<tr><td>1h</td><td>Gray Level : 01h</td></tr>
<tr><td>2h</td><td>Gray Level : 02h</td></tr>
<tr><td>:</td><td>:</td></tr>
<tr><td>FDh</td><td>Gray Level : FDh</td></tr>
<tr><td>FEh</td><td>Gray Level : FEh</td></tr>
<tr><td>FFh</td><td>Gray Level : FFh</td></tr>
</table>
</td></tr>
<tr><td>Restriction</td><td colspan="11">-</td></tr>
<tr><td>Default</td><td colspan="11">
<table>
<tr><th>Status</th><th colspan="2">Default Value</th></tr>
<tr><td rowspan="3">Power On Sequence</td><td>C500h</td><td>00h</td></tr>
<tr><td>C501h</td><td>08h</td></tr>
<tr><td>C502h</td><td>FFh</td></tr>
</table>
</td></tr>
</table>

9.2 Image Enhancement

9.2.1 Gamut Mapping—Selectable Color Mode with Different Gamut

◆ 0.71” Micro OLED support Normal Mode/Photo Mode/ Basic Mode (sRGB Mode).



◆ Register Setting

Gamut mapping (57 CMD1).

5700H	GAMUT										
Instruction	R/W	Address name		Parameter							
		MIPI	I2C	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
GAMUT	R/W	57h	5700h	-	-	-	-	-	-	-	GAMUT_SEL [1:0]	
Description	This command sets the control of gamut mapping.											

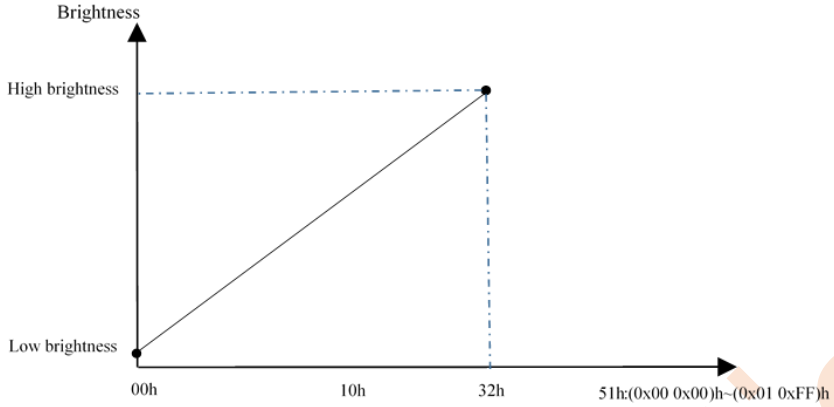
Bit	Symbol	Description	Comment
2bit	GAMUT_SEL[1:0]	Gamut mapping control	0h= Gamut mapping 0 —Normal Mode 1h= Gamut mapping 1—Photo Mode 2h= Gamut mapping 2—Basic Mode

Restriction	-

Default	Status	Default Value	
	Power On Sequence	5700h	00h

9.4 Brightness Control(BC) Functions

This function adjusts the gamma parameter according to the register 51h and 53h setting to adjust the luminance.



◆ Register setting

White Display Brightness(51h CMD1).

5100H	WRDISBV											
Instruction	R/W	Address		Parameter								
		MIPI	Other	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
WRDISBV	W	51h	5100h	-	DBV[7:0]							
			5101h	-	-	-	-	-	-	-	-	DBV [8]
Description	This command is used to adjust brightness.											
Restriction	-											
Default	Status	Default Value										
	Power On Sequence	5100h	00h									
		5101h	00h									

White CTRL Display (53h CMD1)

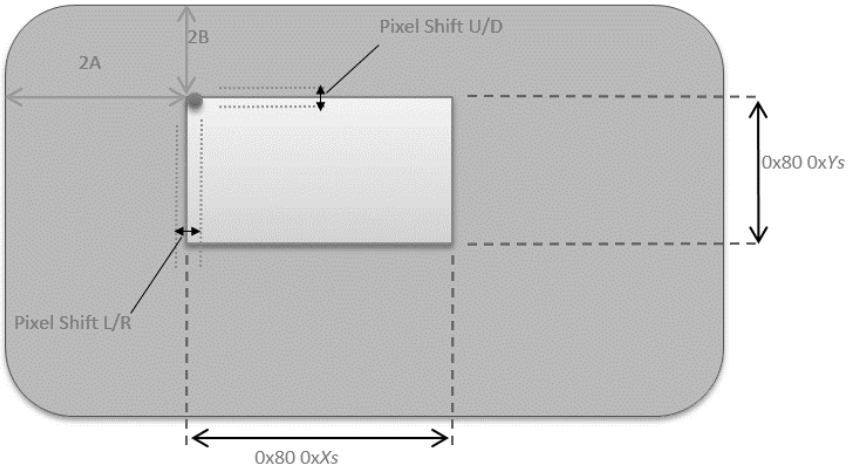
5300H	WRCTRLD											
Instruction	R/W	Address		Parameter								
		MIPI	I2C	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
WRCTRLD	W	53h	5300h	-	-	-	D5	-	D3	D2	-	-
Description	This command is used to set brightness control and display diming control.											

Bit	Symbol	Description	Comment
D5	BCTRL	Brightness control	1= Brightness control enable 0= Brightness control disable
D3	DD_BC	Display dimming control	1= Display dimming control enable 0= Display dimming control disable
D2	DD_TC	Temperature index dimming control	1=Temperature dimming control enable 0=Temperature dimming control disable

Restriction			
Default	Status	Default Value	
	Power On Sequence	5300h	00h

9.5 Display Active-Area(AA) Control

ITEM	Description	Code 值
Resolution	X-direction: Support 4N, N=160~480 Y-direction: support 4M, M=120~270	CMD1：0x80 (NC[7:0] NL[7:0])
Active-Area(AA) control	Display start pointer	Xs：CMD1：0x2A Ys：CMD1：0x2B
	Pixel shift： ±16pixel/step=1pixel	CMD2 Page0：0xB4



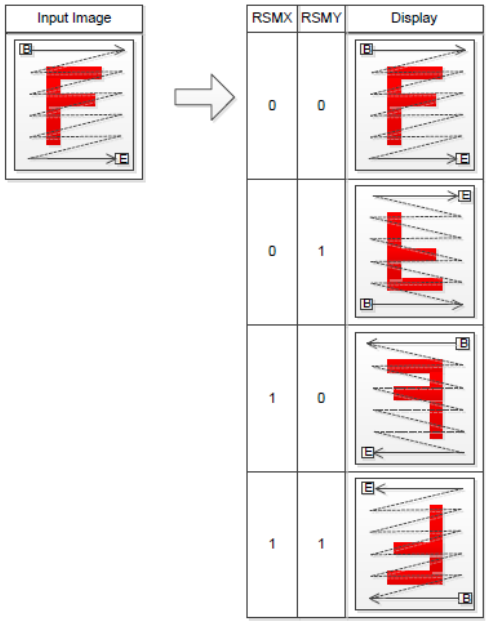
Scan direction selection

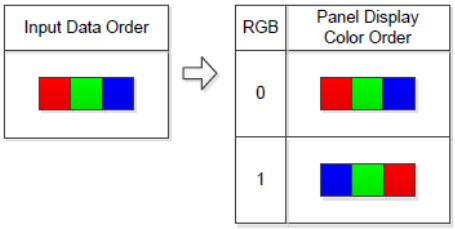
5300H	WRCTRLD											
Instruction	R/W	Address		Parameter								
		MIPI	I2C	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
WRCTRLD	W	36h	3600h	-	-	-	-	-	RGB	-	RSMX	RSMY

Description

This command set scan direction of source and gate and data order.

Bit	Symbol	Description	Comment
D3	RGB	Color Order of sub-pixel of true RGB type	1=BGR 0=RGB
D1	RSMX	Horizontal Flip	1=Normal Display 0=Horizontal Flip
D0	RSMY	Vertical Flip	1= Normal Display 0= Vertical Flip





Restriction	

Default

Status	Default Value	
Power On Sequence	5300h	00h

10. Optical Characteristics

10.1 Optical Characteristics

Item			Specification..
White Brightness (255 Level)	Standard		300±20% cd/m²
White Uniformity 9 Point	White (255 Level)		>85%
View Angle (White)	Lum.Decay(50%)		-45°~45°
	Color Shift(Δu'v'<0.025)		-40°~40°
Contrast	CR		>10000:1
Color Coordinate	Red	CIE-x	0.63±0.05
		CIE-y	0.34±0.05
	Green	CIE-x	0.27±0.05
		CIE-y	0.61±0.05
	Blue	CIE-x	0.15±0.05
		CIE-y	0.09±0.05
	White	CIE-x	0.31±0.05
		CIE-y	0.33±0.05
Color Gamut(NTSC)			>65%
Color Temperature			>5000K

Notes:

1. The brightness of the product will be measured after 5 minutes of stabilization for the white screen at room temperature.

2. The formula of the brightness uniformity at 9 points of the white screen is Uniformity=1-(Max. -Min.)/(Ave.), and the Max., Min. and Ave. represent the maximum, minimum and average of the brightness of 9 points, respectively.

10.2 Measurement System · Measurement Method

The luminance and chromaticity are measured in Measurement System A shown below.

Measurement temperature: Tpnl = 40 ℃

Measurement point: One point on the screen center

All white display: All RGB signal data is set to High.

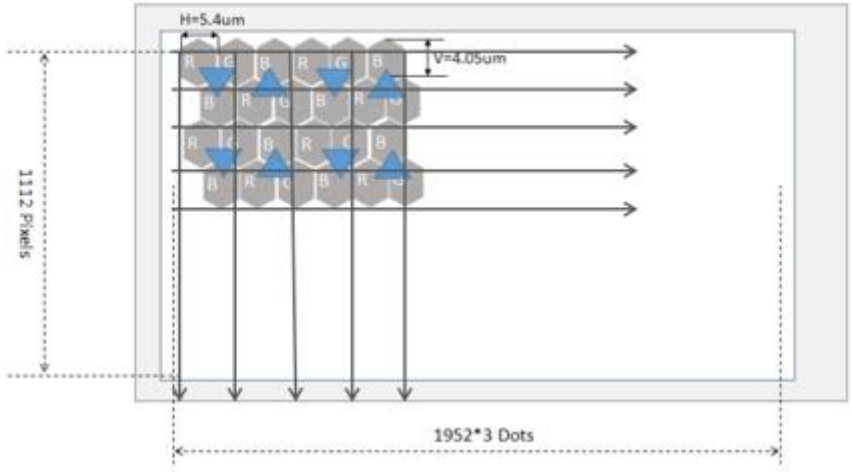
All black display: All RGB signal data is set to Low.

Luminance and chromaticity: Measure the luminance and chromaticity in all white display in Measurement System A.

Contrast: Measure the luminance in all white display (@ : 300cd/m²) and all black display in Measurement System A, and substitute them into the formula below.

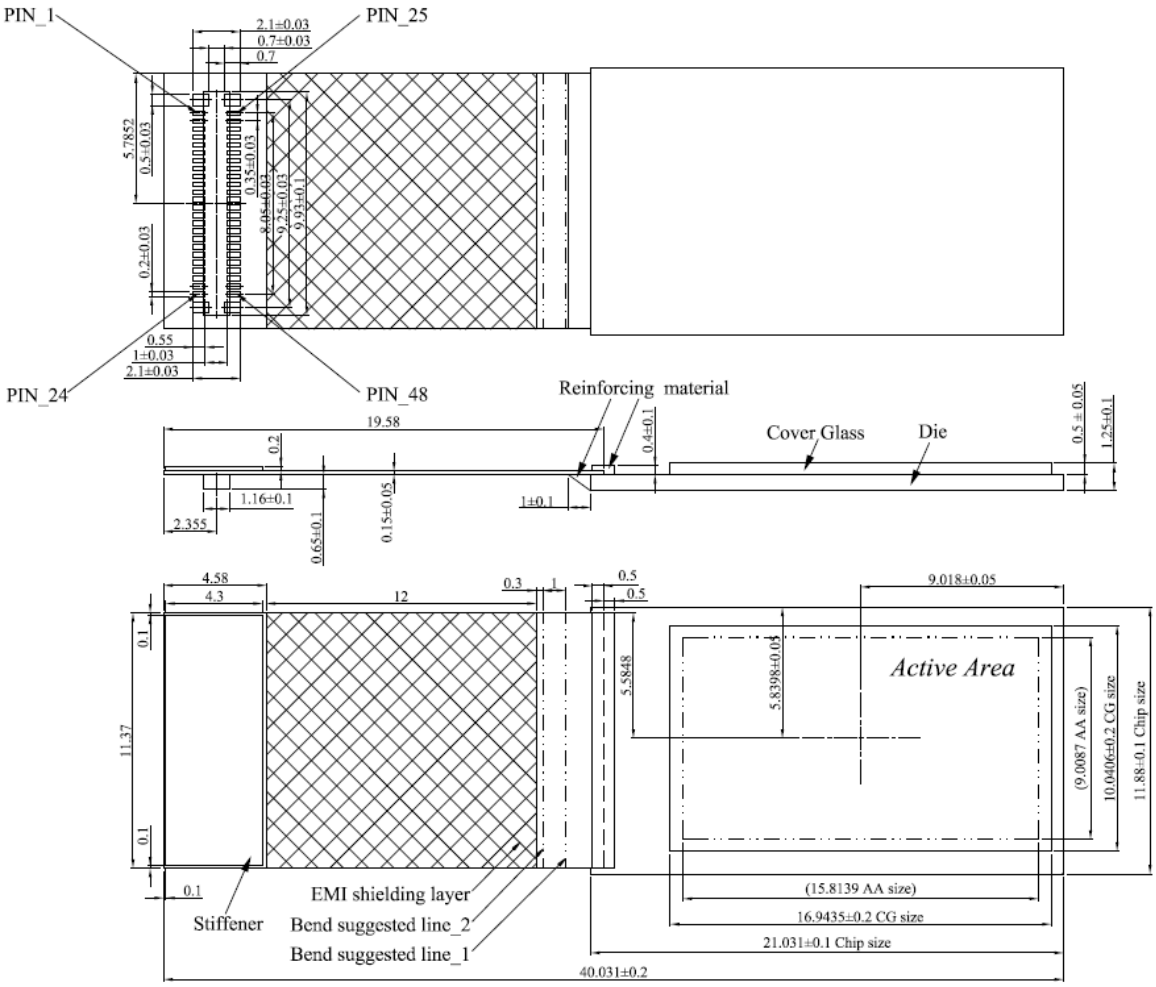
Contrast = Luminance in all white display/Luminance in all black display

11. Pixel Alignment



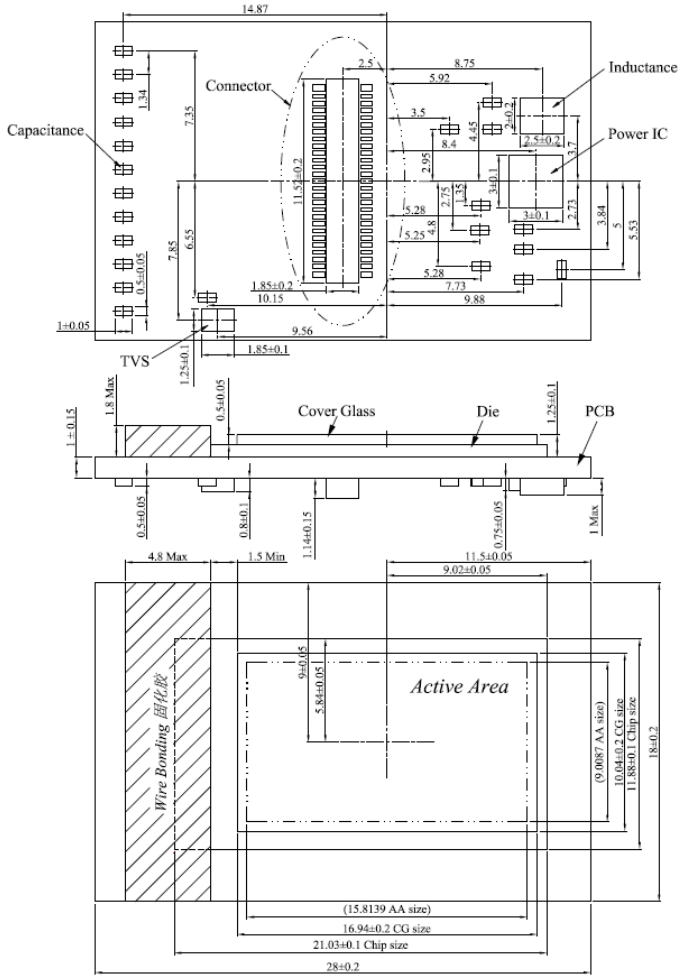
12. Package Outline

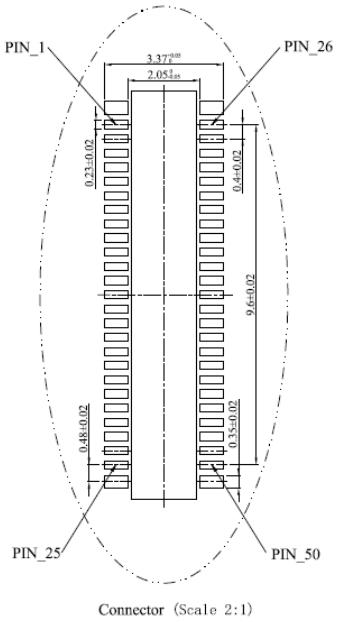
12.1 FPC Module(Unit：mm)



Notes:
1. Undeclared tolerance: ±0.1mm;
2. Weight:0.8±0.1g;
3. Connector model:GB35R-48P-H08-E10000;
4. Corresponding connector model:GB35R-48S-H08-E10000.

12.2 PCB Module(Unit：mm)





Notes:
1. Undeclared tolerance:±0.1mm;
2. Weight:2.2±0.1g;
3. Connector model:DF40C-50DP-0.4V(51);
4. Corresponding connector model:DF40C-50DS-0.4V(51).

Note:

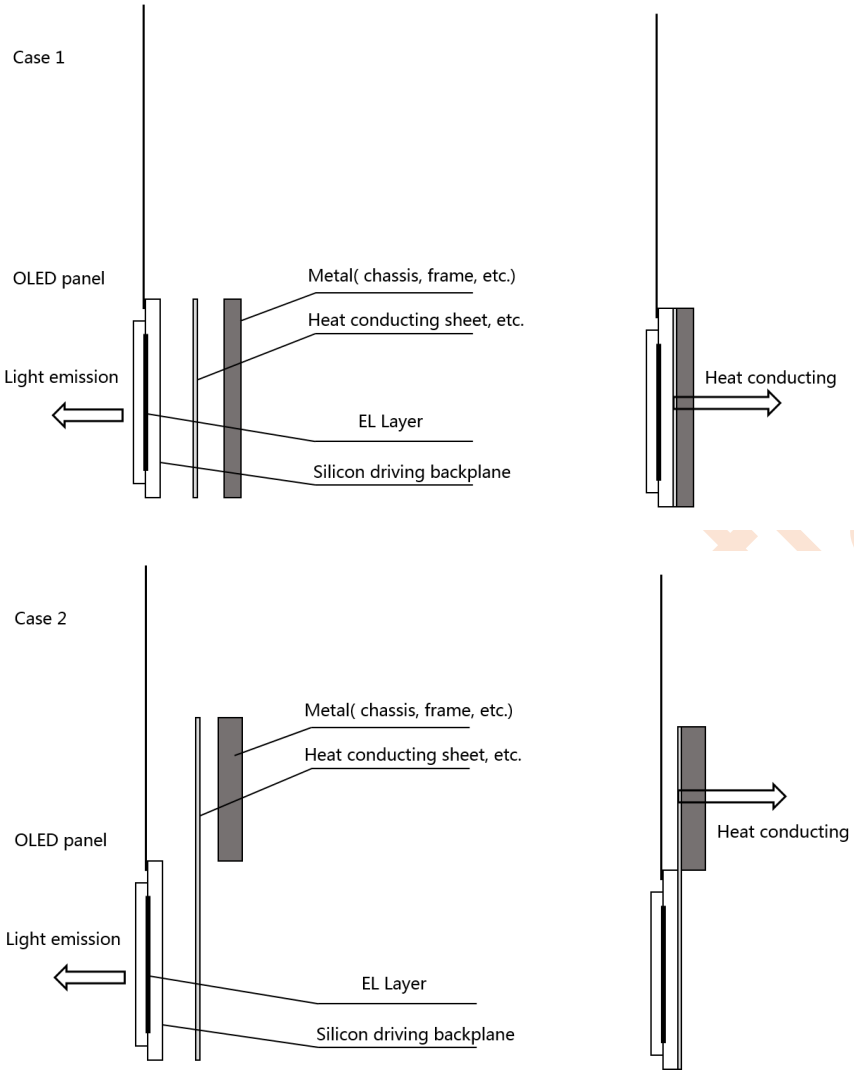
1.时 The FPC bending Angle ≤ 180° and FPC bending radius ≥ R2 mm.

13. Recommended Items

13.1 Suppression of the Panel Temperature

Temperature of organic EL panel tends to rise due to power consumption (heat generation) by the EL emission layer and the integrated silicon drive circuit. The temperature rise may cause luminance rise at initial state, or luminance drop by over time.

The temperature change in panel can be suppressed by establishing a thermal connection between panel rear surface (silicon substrate surface) and metal (chassis, frame, metal structure, etc.) at panel mount area, and the heat conducting sheet size can be changed, So highly recommend the heat conductive sheet between them as show in below.In order to ensure the normal operation of the screen, the heat dissipation must be done to ensure that the scre en temperature < 60 ℃.



14. Notes on Handling

14.1 Static charge prevention

Be sure to take the following protective measures. Organic EL panels are easily damaged by static charges.

(1) Use non-chargeable gloves or handle with bare hands.

(2) Use a wrist strap connecting ground when handling.

(3) Do not touch any electrodes on the panel.

(4) Wear non-chargeable clothes and conductive shoes.

(5) Install grounded conductive mats on the working floor and working table.

(6) Keep the panel away from any charged materials.

14.2 Protection from dust and dirt

(7) Operate in a clean environment.

(8) Do not touch the panel surface. The surface is easily scratched.

When cleaning on panel surface, use a clean-room wiper with isopropyl alcohol. Be careful not to leave stains on the surface.

(9) Use ionized air to blow dust off the panel surface.

14.3 Others

(10) Not hold FPC (Flexible Printed Circuit) , not twist the FPC, not bend FPC because connection area between the FPC and panel is easily broken by mechanical stress.

(11) The minimum fold radius of the FPC is 1.0 mm, So, do not fold the FPC less than 1.0mm radius.

(12) Do not drop the module.

(13) Do not twist or bend the module .

(14) Keep the module away from heat sources.

(15) Not be close the module to water or other solvents.

(16) Do not store or use the module at high temperatures or high humidity circumstance, as the circumstance may affect module specifications.

(17) When disposing of this, regard it as industrial waste and please comply with related regulations.

(18) Do not store or use the panel in reactive chemical substance (including alcohol) environments, as these may affect the specifications.