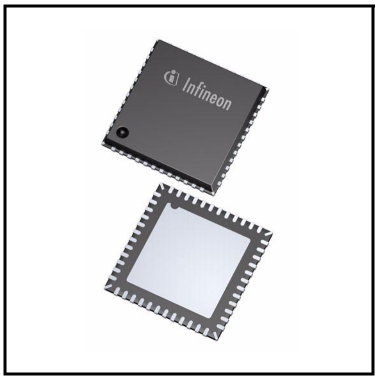
TLE92108-232QX

Multiple MOSFET Driver IC



1 Overview

Features

- Eight half-bridge gate drivers for external N-channel MOSFETs
- Control of reverse battery protection MOSFET
- Adaptive MOSFET gate control
  - Improved electromagnetic emission
  - Reduced switching losses in PWM mode
- 24-bit Serial Peripheral Interface
- Two current sense amplifiers with configurable gain
  - High-side and low-side capable for protection and diagnosis
- Drain-source monitoring for short circuit detection
- Overtemperature warning and shutdown
- Timeout watchdog
- Detailed off-state diagnostic (open load, short circuit to battery or short circuit to GND) via SPI
- Three PWM inputs
  - High-side and low-side PWM capable
  - Active free-wheeling
  - Up to 25 kHz PWM frequency
- Low current consumption in sleep mode
- Configurable low-side 1-4 brake with short circuit detection in sleep mode and normal mode
- Configurable VS overvoltage detection in sleep mode
- Leadless power package with support of optical lead tip inspection
- Green Product (RoHS compliant)
- AEC Qualified

Potential applications

- Seat control and extended functions (steering column adjustment, gas pedal adjustment)
- Power lift gate
- Central door lock
- Body control module (cargo cover, washer pump, window lift, rear wiper ...)

Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

Description

The TLE92108-232QX is a Multi-MOSFET driver IC dedicated to control up to sixteen n-channel MOSFETs. It includes eight half-bridges for DC motor control applications such as automotive power seat control or other applications.

A 24-bit Serial Peripheral Interface (SPI) is used to configure the TLE92108-232QX and to control the half-bridges. It also allows the read out of the status registers for diagnostic purpose.

The TLE92108-232QX offers a wide range of diagnostic features such as the monitoring of the supply voltage, the charge pump voltage, temperature warning and over-temperature shutdown. Each gate driver monitors independently its external MOSFET drain-source voltage for fault conditions.

The device is housed in a VQFN-48 with exposed pad supporting lead tip inspection. The package provides a good thermal performance and minimizes the required PCB space.

Type	Package	Marking
TLE92108-232QX	PG-VQFN-48	TLE92108-232QX

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2 Block diagram

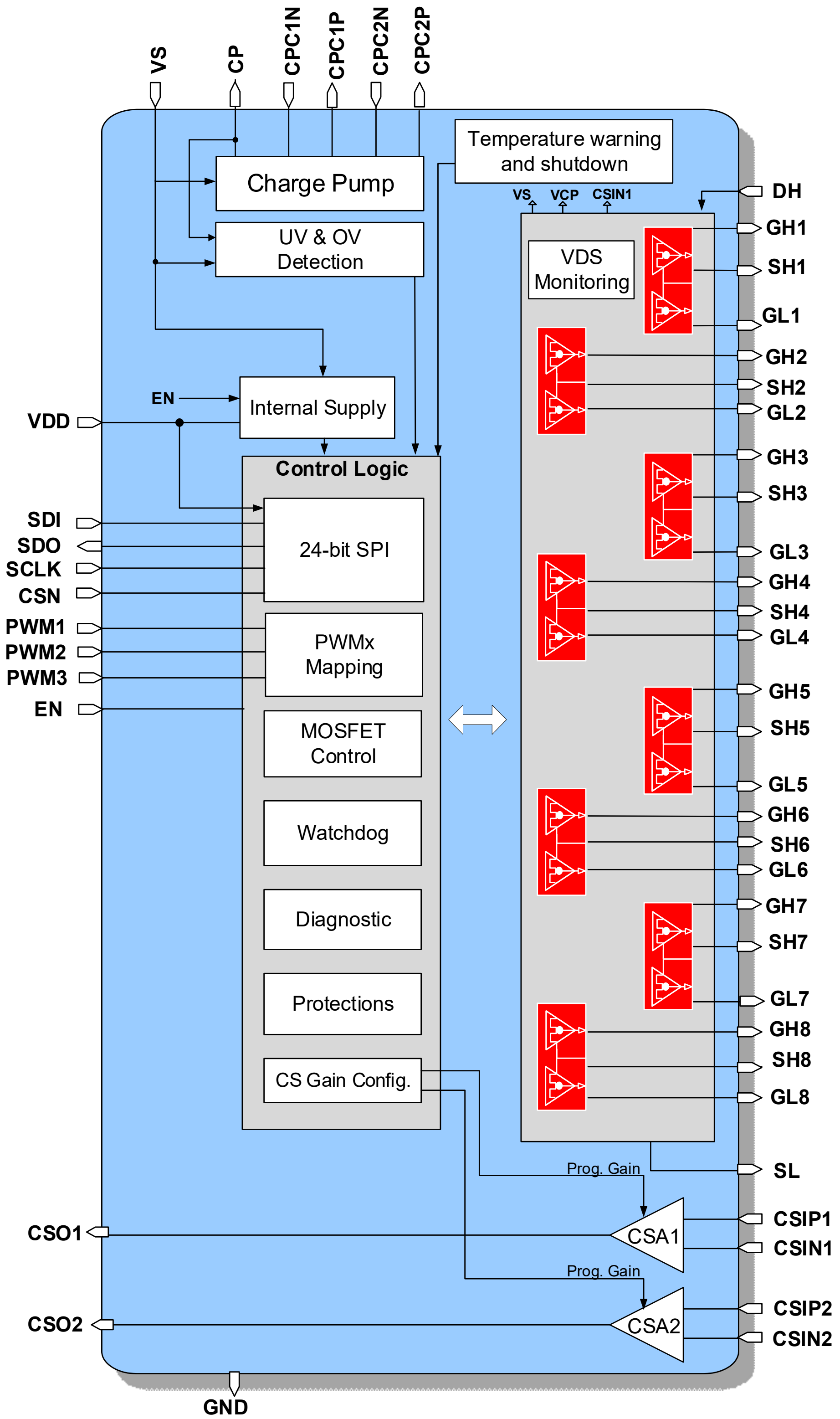


Figure 1 Block diagram

2.1 Voltage and current definition

Figure 2 shows terms used in this datasheet, with associated convention for positive value.

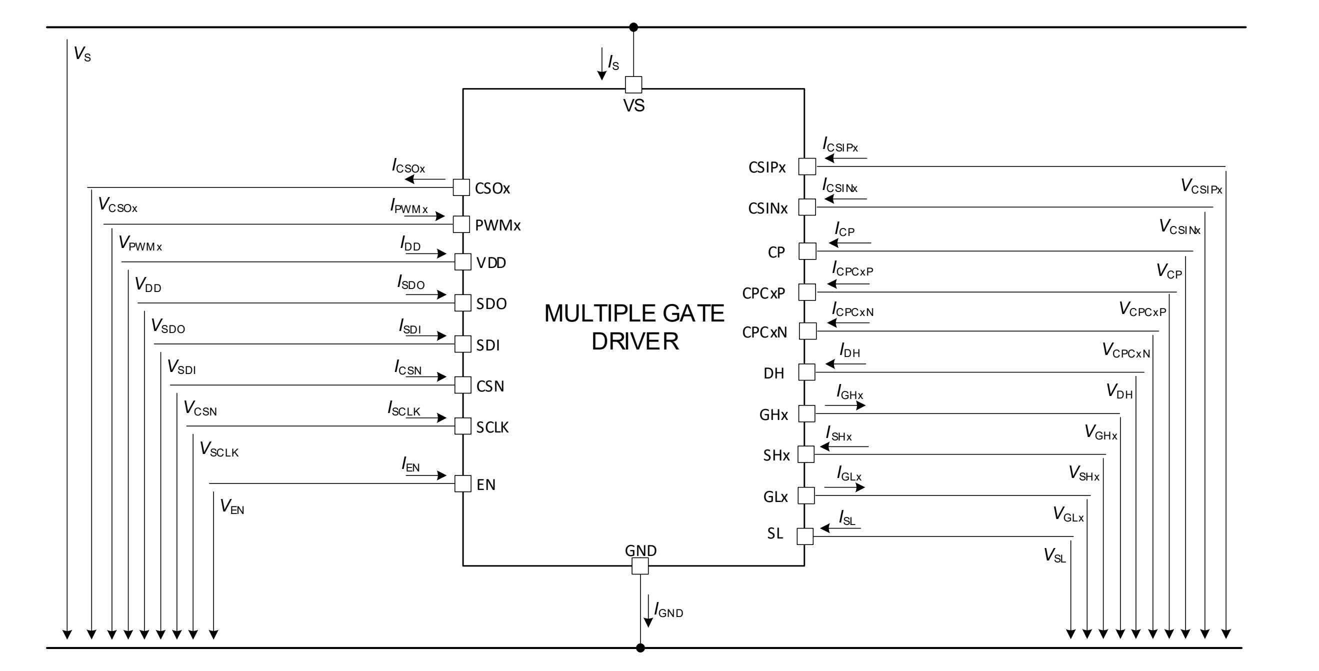


Figure 2 Voltage and current definition

3 Pin configuration

3.1 Pin assignment

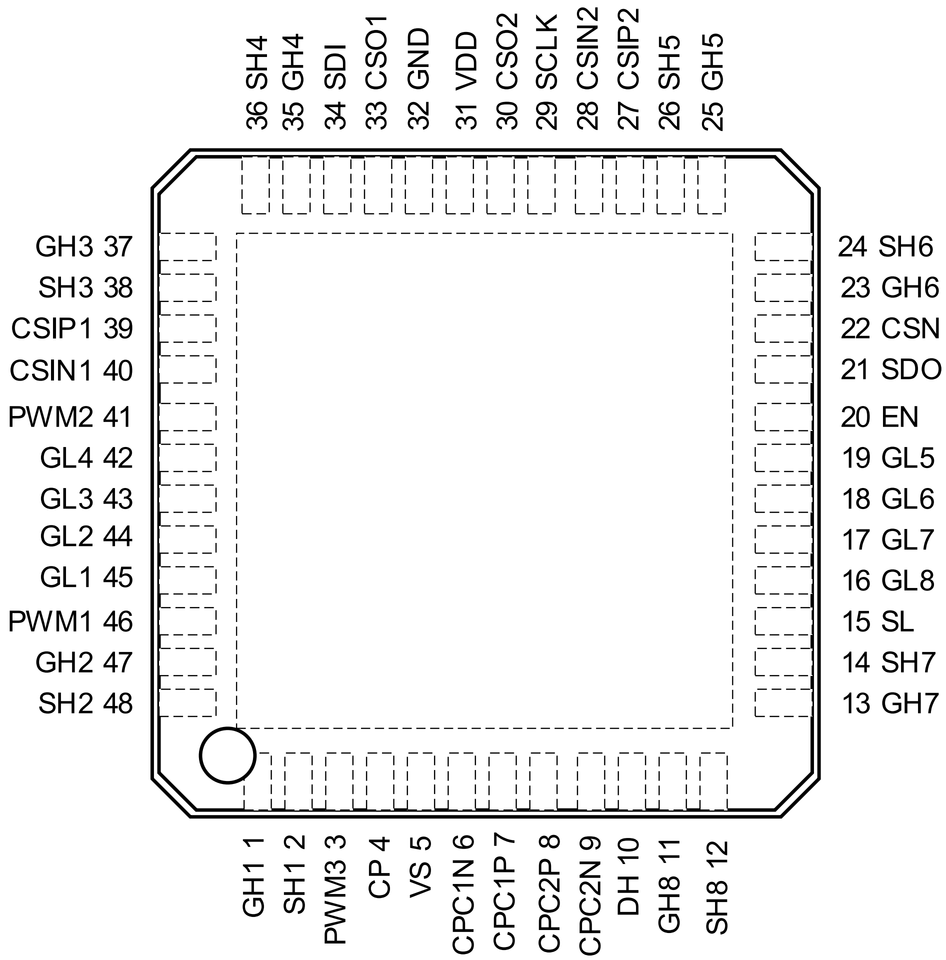


Figure 3 Pin configuration TLE92108-232QX

3.2 Pin definitions and functions

Table 1 Pin configuration TLE92108-232QX

Pin	Symbol	Function
1	GH1	**Gate high-side 1** Analog I/O pin to turn on/off high-side MOSFET 1. Connect to the gate of high-side MOSFET 1.
2	SH1	**Source high-side 1** Connection to source of high-side MOSFET 1.
3	PWM3	**PWM input 3**
4	CP	**Charge Pump Output**
5	VS	**Supply Voltage** Device supply voltage. Connect this pin to the supply (battery) voltage with a reverse battery protection circuit.
6	CPC1N	**Negative connection to Charge Pump Capacitor 1**
7	CPC1P	**Positive connection to Charge Pump Capacitor 1**
8	CPC2P	**Positive connection to Charge Pump Capacitor 2**
9	CPC2N	**Negative connection to Charge Pump Capacitor 2**
10	DH	**Drain input for high-sides** Input for the drains of high-side MOSFETs. Refer to **Chapter 7.3**.
11	GH8	**Gate high-side 8**
12	SH8	**Source high-side 8**
13	GH7	**Gate high-side 7**
14	SH7	**Source high-side 7**
15	SL	**Source low-side** Common connection to the source of the low-side MOSFETs.
16	GL8	**Gate low-side 8**
17	GL7	**Gate low-side 7**
18	GL6	**Gate low-side 6**
19	GL5	**Gate low-side 5**
20	EN	**Enable input** with internal pull-down
21	SDO	**Serial Data Output**
22	CSN	**Chip Select Not** with internal pull-up
23	GH6	**Gate high-side 6**
24	SH6	**Source high-side 6**
25	GH5	**Gate high-side 5**
26	SH5	**Source high-side 5**
27	CSIP2	**Non-Inverting input of the Current Sense Amplifier 2**
28	CSIN2	**Inverting input of the Current Sense Amplifier 2**
29	SCLK	**Serial Clock Input** with internal pull-down
30	CSO2	**Current Sense Amplifier Output 2**

Table 1 Pin configuration TLE92108-232QX

Pin	Symbol	Function
31	VDD	**Logic supply**
32	GND	**Ground connection**
33	CSO1	**Current Sense Amplifier Output1**
34	SDI	**Serial Data Input** with internal pull-down
35	GH4	**Gate high-side 4**
36	SH4	**Source high-side 4**
37	GH3	**Gate high-side 3**
38	SH3	**Source high-side 3**
39	CSIP1	**Non-inverting input of the Current Sense Amplifier 1**
40	CSIN1	**Inverting input of the Current Sense Amplifier 1** . This pin can be used as reference for the high-side MOSFET drain if CSA1 is configured as high-side. Refer to **Chapter 7.3**
41	PWM2	**PWM input 2**
42	GL4	**Gate low-side 4**
43	GL3	**Gate low-side 3**
44	GL2	**Gate low-side 2**
45	GL1	**Gate low-side 1**
46	PWM1	**PWM input 1**
47	GH2	**Gate high-side 2**
48	SH2	**Source high-side 2**
	E.P.	**Exposed pad** For cooling purpose only, do not use as electrical GND[1].

1) The exposed pad at the bottom of the package allows better power dissipation from TLE92108-232QX via the PCB. The exposed pad must be left floating or connected to GND (recommended) for best EMC and thermal performance.

4 General product characteristics

4.1 Absolute maximum ratings

Table 2 Absolute maximum ratings[1)]

T_j = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Voltages							
Supply voltage	V_S	-0.3	–	40	V	–	P_4.1.1
PWM input voltages (PWMx)	V_{PWMx}	-0.3	–	V_{DD} + 0.3	V	$\|I\|$< 10 mA	P_4.1.2
Logic input voltages (SDI, SCLK, CSN, EN)	V_{SDI}, V_{SCLK}, V_{CSN}, V_{EN}	-0.3	–	V_{DD} + 0.3	V	$\|I\|$< 10 mA	P_4.1.3
Voltage range and SDO	V_{SDO}	-0.3	–	V_{DD} + 0.3	V	$\|I\|$< 10 mA	P_4.1.4
Voltage range at CSIPx and CSINx	V_{CSIP}, V_{CSIN}	-8.0	–	40	V	–	P_4.1.5
Differential input voltage range CSIPx - CSINx	$V_{CSIDiff}$	-8.0	–	8.0	V	–	P_4.1.21
Voltage range at DH	V_{DH}	-0.3	–	40	V	–	P_4.1.6
Voltage range at SL	V_{SL}	-8.0	–	6.0	V	–	P_4.1.7
Voltage range at SHx	V_{SH}	-8.0	–	48	V	–	P_4.1.8
Voltage range at GHx	V_{GH}	-8.0	–	48	V	–	P_4.1.9
Voltage range at GLx	V_{GL}	-8.0	–	24	V	–	P_4.1.10
Voltage difference between GLx and SL	V_{GS_LS}	-0.3	–	16	V	–	P_4.1.11
Voltage difference between GHx and SHx	V_{GS_HS}	-1.0	–	16	V	[2)]	P_4.1.23
Voltage range at charge pump pins CP	V_{CP}	V_S-0.3	–	V_S+15	V	–	P_4.1.12
Voltage range at charge pump pins CPC1N, CPC1P, CPC2N, CPC2P	V_{CPCx}	V_{CP}-0.3	–	V_{CP}+0.3	V	–	P_4.1.22
Logic supply voltage	V_{DD}	-0.3	–	5.5	V	–	P_4.1.13
Voltage at CSOx	V_{CSOx}	-0.3	–	V_{DD} + 0.3	V	–	P_4.1.14
Temperatures							
Junction temperature	T_j	-40	–	150	°C	–	
Storage temperature	T_{stg}	-55	–	150	°C	–	P_4.1.16

Table 2 Absolute maximum ratings[1)] (cont'd)

T_j = -40°C to 150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
ESD susceptibility							
ESD susceptibility all pins	$V_{ESDHBM1}$	-2	–	2	kV	HBM[3)]	P_4.1.17
ESD susceptibility of VS and DH pins versus GND	$V_{ESDHBM2}$	-4	–	4	kV	HBM[3)]	P_4.1.18
ESD susceptibility all pins	$V_{ESDCDM1}$	-500	–	500	V	CDM[4)]	P_4.1.19
ESD susceptibility pin corner pins	$V_{ESDCDM2}$	-750	–	750	V	CDM[4)]	P_4.1.20

1) Not subject to production test, specified by design.
2) V_{GS_GH} may be between -1.0 and -0.3V only if the current injected into SHx is below 4 mA
3) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5 kΩ, 100 pF).
4) ESD susceptibility, Charged Device Model "CDM" according JEDEC JESD22-C101.

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

4.2 Functional range

Table 3 Functional range

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply voltage range for normal operation	$V_{S(nor)}$	6.0	–	28	V	–	P_4.2.1
Extended supply voltage range	$V_{S(ext)}$	5.5	–	6	V	[1)] Parameter deviations possible	P_4.2.7
Extended supply voltage range	$V_{S(ext)}$	28	–	V_{SOV_OFF2} (max)	V	[1)] Parameter deviations possible	P_4.2.2
Supply voltage transients slew rate	dV_S/dt	-10	–	10	V/µs	[1)]	P_4.2.3
Logic supply voltage	V_{DD}	3.0	–	5.5	V	–	P_4.2.4
SPI logic input voltage	V_{SDI}, V_{SCLK}, V_{CSN}	0	–	V_{DD}	V	–	P_4.2.5
Junction temperature	T_j	-40	–	150	°C	–	P_4.2.6

1) Not subject to production test, specified by design.

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

4.3 Thermal resistance

Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to ***www.jedec.org***.

Table 4 Thermal resistance

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Junction to case	R_{thJC}	–	4.4	–	K/W	[1]	
Junction to ambient	R_{thJA}	–	27	–	K/W	[1][2]	

1) Not subject to production test, specified by design.

2) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 inner copper layers (2 × 70 mm Cu, 2 × 35 mm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

5 General description

5.1 Power supply

The Multiple MOSFET Driver IC requires two power supplies: V_S and V_{DD}.

V_{DD} supplies the I/O buffers (including the SPI pins) and the internal voltage regulator for the logic. V_{DD} allows the flexibility of a 3.3 V or a 5.0 V logic interface.

V_S supplies the charge pump for the MOSFET gate drivers. The V_S pin must be connected to the battery through a reverse battery protection.

Both supplies are separated so that the information stored in the logic remains intact in the event of voltage drop on V_S. V_{DD} and V_S should be decoupled with ceramic capacitors connected close to the supply and ground planes.

5.2 Operation modes

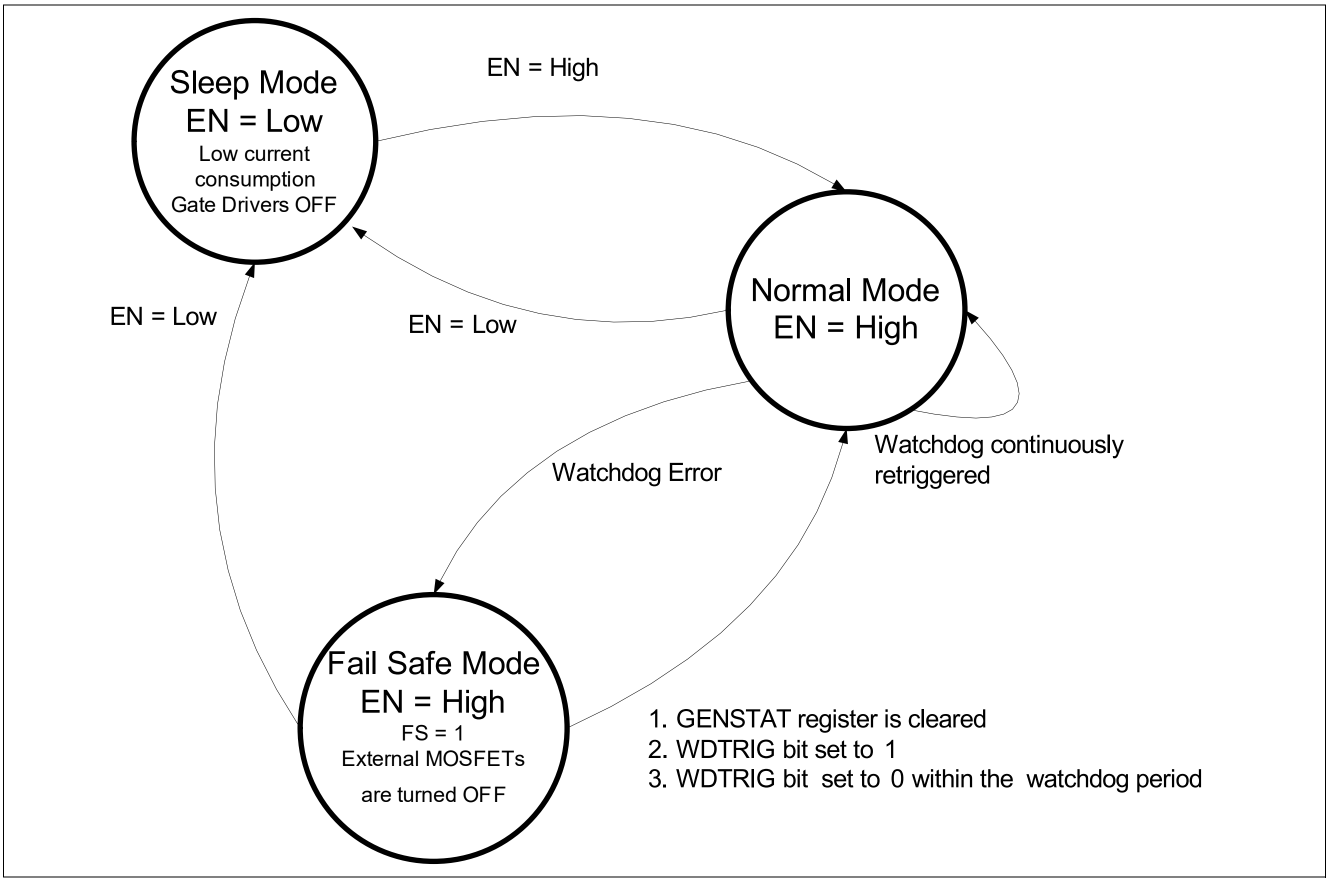


Figure 4 State diagram

Note: The state diagram is valid for V_S and V_{DD} within the nominal operating range. For V_S and V_{DD} outside of the nominal range, refer to ***Chapter 7.8****, respectively* ***Chapter 5.2.2****.*

5.2.1 Normal mode

The TLE92108-232QX enters Normal Mode by setting EN pin to High and waiting for the SPI setup time t_{SET_SPI}. In normal mode, the MOSFET gate drivers are enabled and can be configured through the SPI interface, provided that the voltages applied to V_{DD} and V_S are within the operating range. The watchdog must be retriggered correctly in order to stay in Normal Mode (see **Chapter 7.10**).

5.2.2 Sleep mode

The Multiple MOSFET Driver IC enters Sleep Mode by setting EN pin to Low. The transition to the sleep mode is delayed by $\mathbf{t_{DSLEEP}}$[1] (max tCCP of active half-bridges + 3 µs) in order to actively turn-off the external MOSFETs. In this mode, the internal regulator and the internal circuitry are deactivated, and the SPI registers are reset.
The current consumption of V_{DD} is reduced to $\mathbf{I_{DD\_Q}}$. The current consumption of V_S is reduced to $\mathbf{I_{SQ}}$ or $\mathbf{I_{SQ}}$ + $\mathbf{I_{SQ\_BRAKE}}$.

The V_S current consumption is $\mathbf{I_{SQ}}$ if:

- **PASS_MOD** = 00_B and **PASS_VDS** = 0_B while entering sleep mode
- and V_S never drops below $\mathbf{V_{SLEEP\_SET}}$ after entering sleep mode

The V_S current consumption is $\mathbf{I_{SQ}}$ + $\mathbf{I_{SQ\_BRAKE}}$ if:

- **PASS_MOD** = 01_B, 10_B, 11_B or **PASS_VDS** = 1_B while entering sleep mode
- or V_S has recovered from a voltage below $\mathbf{V_{SLEEP\_SET}}$ (i.e. V_S has ramped up from a voltage below $\mathbf{V_{SLEEP\_SET}}$ or V_S has dropped below $\mathbf{V_{SLEEP\_SET}}$)

The internal resistors R_{GGND} between GHx/GLx and GND are activated to discharge the gate of the external MOSFETs.

Note: If EN is set to Low for a duration shorter than ($\mathbf{t_{ENL\_FILT}}$, 8 µs max.), and EN is set to High again, then device does not go in sleep mode and the registers are not reset. The half-bridges are reactivated according to the settings of the control registers when EN is High.

5.2.3 Fail Safe Mode

In case of watchdog error (see **Chapter 7.10**), the device enters Fail Safe Mode, FS bit is set (see **Global status byte**) and the external MOSFETs are actively discharged with the static discharge current (**Chapter 6.2**) during the max. configured tHBxCCP active (**Chapter 7.5.1**). Then the bridge driver is set to passive mode (the passive discharge path is activated,**Chapter 6.4**, all external MOSFETs are latched off, and the charge pump is deactivated). To resume Normal Mode the microcontroller must execute the following sequence[2]:

1. Clear **GENSTAT** register.
2. Write WDTRIG bit to 1 (**GENCTRL1**) within the watchdog period.
3. Write WDTRIG bit to 0 within the watchdog period[3].

In fail safe mode, the control registers are frozen to their default value, at the exception of **WDTRIG**, **CCSO**, **PASS_VDS**, **PASS_MOD**, **CSA1L**, **CSA2L**. Any write command (except for WDTRIG bit) or clear command (except for GENSTAT) will be discarded in this mode and sets SPIE bit (**Global status byte**).

A clear command to **GENSTAT** in fail safe mode does not reset any failure flag reported by this status register.

1) SPI Frames are ignored during $\mathbf{t_{DSLEEP}}$.
2) The exit sequence must be strictly followed to leave fail safe mode. If a SPI frame not belonging to the sequence is added, then the device stays in fail safe mode and the microcontroller must restart the complete sequence to enter normal mode.
3) During Fail Safe Mode, the charge pump is deactivated and **CPUV** is set. Therefore, recovering from Fail Safe Mode, **GENSTAT** must be cleared again at the end of the Fail Safe exit sequence to re-activate of the gate drivers.

The control and status registers can be read in this mode before the start of the exit sequence without SPIE bit being set.

5.3 Reset behavior

The following events trigger a Power On Reset:

V_{DD} undervoltage reset:

If $V_{DD} < V_{DD\ PoffR}$ the digital block is deactivated and the outputs are switched off. The digital block is reset once $V_{DD} > V_{DD\ POR}$. Then NPOR bit (negated power-on reset bit, see **Global status byte**) is reset to 0 to report the reset condition.

Reset on EN pin:

If the EN pin is pulled low, the logic content is reset and the device enters sleep mode. Once the device enters Normal Mode (after t_{SET_SPI} with EN = high and $V_{DD} > V_{DD\ POR}$), the NPOR bit is reset to 0 to report the reset condition.

NPOR is set to 1 when **GENSTAT** is cleared.

5.4 Charge pump

A dual-stage charge pump supplies the gate drivers for the high-side and low-side MOSFETs. It requires three external capacitors connected between CPC1N and CPC1P, CPC2N and CPC2P, VS and CP.

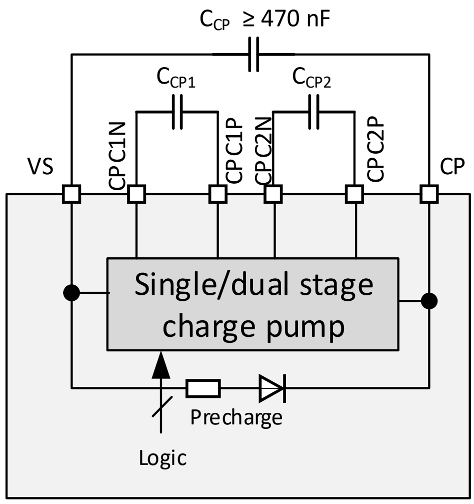


Figure 5 Charge pump

CPSTGA = 0 (default, see **GENCTRL2**), the device operates with the dual-stage charge pump.

If CPSTGA = 1 (**GENCTRL2**), the device switches automatically to single-stage or dual-stage charge pump automatically:

- If $V_S > V_{CPSO\ DS}$: the TLE92108-232QX switches from a dual-stage to a single-stage charge pump.
- If $V_S < V_{CPSO\ SD}$: the TLE92108-232QX switches from single-stage to dual-stage charge pump.

The operation with the single-stage charge pump reduces the current consumption from the VS pin.

5.5 Frequency modulation

A modulation of the charge pump frequency can be activated to reduce the peak emission. The modulation frequency can be selected based on the resolution bandwidth of the peak detector during EMC testing.

The modulation frequency is set by the control bit FMODE in **GENCTRL1**

- FMODE = 0: No modulation.
- FMODE = 1: Modulation frequency = 15.6 kHz (default).

5.6 Electrical characteristics

5.6.1 Electrical characteristics: supply

Table 5 Electrical characteristics: supply

V_S = 6.0 V to 18 V if VSOVTH = 0, V_S = 6.0 V to 28 V if VSOVTH = 1; V_{DD} = 3.0 V to 5.5 V, T_j = -40°C to 150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Current consumption, EN = LOW)							
Supply quiescent current	I_{SQ}	–	2	5	µA	T_j < 85°C, V_S= 13.5 V **PASS_MOD**=00_B, **PASS_VDS**=0_B	P_5.5.1
Supply quiescent current	I_{SQ2}	–	5	7	µA	T_j < 85°C, V_S< 25 V **PASS_MOD**=00_B,**PASS_VDS**=0_B	P_5.5.61
Additional supply quiescent current, brake enabled	I_{SQ_BRAKE}	–	5	7.5	µA	T_j < 85°C, V_S = 13.5 V [1] **PASS_MOD**=01_B or 10_Bor 11_B or **PASS_VDS**=1_B	P_5.5.60
Logic Supply quiescent current	I_{DD_Q}	–	1	3	µA	T_j < 85°C	P_5.5.3
Total quiescent current	$I_{DD\_Q} + I_{SQ}$	–	3	8	µA	T_j < 85°C, V_S= 13.5 V **PASS_MOD**=00_B, **PASS_VDS**	P_5.5.5
EN Low filter time	t_{DSLEEP}	–	–	Max. tCCP + 3 µs	µs	[2][3]**BD_PASS** = 0	P_5.5.49
EN Low filter time	t_{ENL_FILT}	1	–	8	µs	[2]	P_5.5.51
VS for LS1-4 setting	V_{SLEEP_SET}	–	–	5.5	V		P_5.5.63
Current consumption, EN = HIGH							
Supply current	I_{S1}	–	45	55	mA	HBxVDSTH = 001_B, **BD_PASS** = 0, I_{CP} = 0 mA	P_5.5.6
Supply current	I_{S2}	–	83	100	mA	8 V < V_S < 28 V HBxVDSTH = 001_B, **BD_PASS** = 0, I_{CP} = -12 mA, dual stage CP	P_5.5.7

Table 5 Electrical characteristics: supply (cont'd)

V_S = 6.0 V to 18 V if VSOVTH = 0, V_S = 6.0 V to 28 V if VSOVTH = 1; V_{DD} = 3.0 V to 5.5 V, T_j = -40°C to 150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Supply current	I_{S3}	–	55	70	mA	18 V < V_S < 28 V HBxVDSTH = 001_B, **BD_PASS** = 0, I_{CP} = -12 mA[2], single stage CP	P_5.5.56
Supply current	I_{S4}	–	55	70	mA	V_S = 6 V, HBxVDSTH = 001_B, **BD_PASS** = 0, I_{CP} = - 6 mA[2]	P_5.5.57
Supply current	$I_{S\_BD\_PASS}$	–	10	20	mA	HBxMODE=00_B, **BD_PASS** = 1	P_5.5.54
Logic supply current	I_{DD1}	–	3	4	mA	SPI not active, CSA1 and CSA2 off, all I_{PDDiag} off, **BD_PASS**=0	P_5.5.8
Logic supply current	I_{DD2}	–	3	3.8	mA	[4] Additional VDD current per CSA on, VCSOx = 4.5 V, LS shunt, **CCSO** = 1 CSAxL = 0, I_{PDDiag} off	P_5.5.52
Logic supply current	I_{DD3}	–	2	2.8	mA	[4] Additional VDD current per CSA on, **CCSO** = 0, VCSOx = 4.5 V, LS shunt, CSAxL = 0, I_{PDDiag} off	P_5.5.55
Logic supply current	I_{DD4}	–	6	7	mA	[5] Additional VDD current per CSA on, VCSOx = 4.5 V, HS shunt, **VSOVTH** = 1 CSAxL = 1, I_{PDDiag} off	P_5.5.58
Logic supply current	I_{DD5}	–	4.2	5.2	mA	[5] Additional VDD current per CSA on, **VSOVTH** = 0, VCSOx = 4.5 V, HS shunt, CSAxL = 1, I_{PDDiag} off	P_5.5.59

Table 5 Electrical characteristics: supply (cont'd)

V_S = 6.0 V to 18 V if VSOVTH = 0, V_S = 6.0 V to 28 V if VSOVTH = 1; V_{DD} = 3.0 V to 5.5 V, T_j = -40°C to 150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Additional logic supply current pull-down	I_{DD_PDDiag}	–	1.5	2	mA	Additional VDD current when all I_{PDDiag} are on	P_5.5.53
VS with active bridge driver (BD_PASS = 0)							
UV switch ON voltage	$V_{SUV\ ON}$	–	–	5.5	V	V_S increasing	P_5.5.11
UV switch OFF voltage	$V_{SUV\ OFF}$	4.0	4.5	5.0	V	V_S decreasing	P_5.5.12
UV ON/OFF hysteresis	$V_{SUV\ HY}$	–	0.5	–	V	$V_{SUV\ ON}$ - $V_{SUV\ OFF}$ 2)	P_5.5.13
OV switch OFF voltage VSOVTH = 0	$V_{SOV\ OFF1}$	19	–	21	V	V_S increasing	P_5.5.14
OV switch ON voltage VSOVTH = 0	$V_{SOV\ ON1}$	18	–	20	V	V_S decreasing	P_5.5.15
OV switch OFF voltage VSOVTH = 1	$V_{SOV\ OFF2}$	29	–	31	V	V_S increasing	P_5.5.16
OV switch ON voltage VSOVTH = 1	$V_{SOV\ ON2}$	28	–	30	V	V_S decreasing	P_5.5.17
OV ON/OFF hysteresis	$V_{SOV\ HY}$	–	1	–	V	$V_{SUV\ ON}$ - $V_{SUV\ OFF}$ 2)	P_5.5.18
VS undervoltage filter time	t_{VSUV_FILT}	7	10	13	µs	1)	P_5.5.47
VS overvoltage filter time	t_{VSOV_FILT}	7	10	13	µs	2)	P_5.5.48
CP turn-off delay after VS overvoltage detection	t_{D_CPVSOV}	12.8	16	19.2	µs	2)	P_5.5.50
VDD							
V_{DD} Power-On-Reset	$V_{DD\ POR}$	2.40	2.60	2.80	V	V_{DD} increasing	P_5.5.19
V_{DD} Power-Off-Reset	$V_{DD\ POffR}$	2.30	2.50	2.70	V	V_{DD} decreasing	P_5.5.20
V_{DD} Power-On-Reset Hysteresis	$V_{DD\ POR\ HY}$	–	0.1	–	V	$V_{DD\ POR}$ - $V_{DD\ POffR}$ 2)	P_5.5.21

1) Additional quiescent current if VS drops below **V_{SLEEP_SET}**.
2) Not subject to production test, specified by design.
3) Max. cross-current protection time of the active half-bridges.
4) Parameter independent of **VSOVTH**.
5) Parameter independent of **CCSO**.

5.6.2 Electrical characteristics: logic inputs PWMx, EN

Table 6 Electrical characteristics: PWMx, EN

V_S = 6.0 V to 18 V if VSOVTH = 0, V_S = 6.0 V to 28 V if VSOVTH = 1; V_{DD} = 3.0 V to 5.5 V, T_j = -40°C to 150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
EN high voltage	V_{ENH}	0.7 × V_{DD}	–	–	V	–	P_5.5.22
EN low voltage	V_{ENL}	–	–	0.3 × V_{DD}	V	–	P_5.5.23
EN hysteresis	V_{ENHY}	–	0.12 × V_{DD}	–	V	1)	P_5.5.24
EN pull-down resistor	R_{PD_EN}	30	40	50	kΩ	–	P_5.5.25
PWMx high voltage	V_{PWMH}	0.7 × V_{DD}	–	–	V	–	P_5.5.26
PWMx low voltage	V_{PWML}	–	–	0.3 × V_{DD}	V	–	P_5.5.27
PWMx hysteresis	V_{PWMHY}	–	0.12 × V_{DD}	–	V	1)	P_5.5.28
PWMx pull-down resistor	R_{PD_PWMx}	30	40	50	kΩ	–	P_5.5.29

1) Not subject to production test, specified by design.

5.6.3 Electrical characteristics charge pump

Table 7 Electrical characteristics: charge pump

V_S = 6.0 V to 18 V if VSOVTH = 0, V_S = 6.0 V to 28 V if VSOVTH = 1; V_{DD} = 3.0 V to 5.5 V, T_j = -40°C to 150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Charge Pump Frequency	f_{CP}	–	250	–	kHz	3)	P_5.5.30
Output Voltage VCP vs. VS	V_{CPmin}	8.5	–	–	V	V_S = 6 V, I_{CP} = - 6 mA	P_5.5.31
Regulated output voltage VCP vs. VS, CPSTGA = 0	V_{CP1}	11	15	17	V	8 V < V_S < 28 V, I_{CP} = - 12 mA	P_5.5.32
Regulated output voltage VCP vs. VS, CPSTGA = 1	V_{CP2}	12	15	17	V	18 V < V_S < 28 V, I_{CP} = - 12 mA	P_5.5.41
Turn-on time, CPSTGA = 0	t_{ON_VCP1}	10	40	80	µs	8 V < V_S < 28 V (25%)1)2)3)4)	P_5.5.34
Rise time, CPSTGA = 0	t_{RISE_VCP1}	10	60	100	µs	8 V < V_S < 28 V (25%-75%)1)2)3)4)	P_5.5.35
Turn-on time, CPSTGA = 1	t_{ON_VCP2}	10	40	80	µs	18 V < V_S < 28 V (25%)1)2)3)5)	P_5.5.36

Table 7 Electrical characteristics: charge pump

V_S = 6.0 V to 18 V if VSOVTH = 0, V_S = 6.0 V to 28 V if VSOVTH = 1; V_{DD} = 3.0 V to 5.5 V, T_j = -40°C to 150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
Rise time, CPSTGA = 1	t_{RISE_VCP2}	10	60	100	µs	18 V < V_S < 28 V (25%-75%)[1)2)3)5)]	P_5.5.37
Charge Pump Undervoltage (referred to VS)	V_{CPUV1}	5.5	6	6.5	V	**CPUVTH** = 0, VCP falling	P_5.5.38
Charge Pump Undervoltage (referred to VS)	V_{CPUV2}	7	7.5	8	V	**CPUVTH** = 1, VCP falling	P_5.5.42
Automatic switch over dual to single stage charge pump	$V_{CPSO\ DS}$	16	17	18	V	**CPSTGA** = 1	P_5.5.43
Automatic switch over single to dual stage charge pump	$V_{CPSO\ SD}$	15.5	16.5	17.5	V	**CPSTGA** = 1	P_5.5.44
Charge pump switch over hysteresis	$V_{CPSO\ HY}$	–	0.5	–	V	[3)] **CPSTGA** = 1, $V_{CPSO\ DS}$ - $V_{CPSO\ SD}$	P_5.5.45
Charge Pump Undervoltage Filter Time	t_{CPUV}	51	64	77	µs	[3)]	P_5.5.39
Charge pump minimum output current	I_{CPOC1}	–	–	-12	mA	[2)3)4)] V_S = 13.5 V; **CPSTGA** = 0	
Charge pump minimum output current	I_{CPOC2}	–	–	-12	mA	[2)3)5)] V_S = 18 V; **CPSTGA** = 1	

1) Parameter dependent on the capacitance C_{CP}.
2) C_{CPC1} = C_{CPC2} = 220 nF, C_{CP} = 470 nF, I_{CP} = 0 mA.
3) Not subject to production test, specified by design.
4) Dual stage charge pump.
5) Single stage charge pump.

6 Floating gate drivers

The TLE92108-231QX integrates sixteen floating gate drivers capable of controlling a wide range of n-channel MOSFETs. They are configured as eight high-sides and low-sides, building eight half-bridges.

The gate driver are current controlled, allowing a regulation of the MOSFET switching times.

For more information, please contact your sales partner for the datasheet including the complete device description.

7 Protections and diagnostics

The TLE92108-232QX integrates comprehensive diagnostic and protection functions.

For more information, please contact your sales partner for the datasheet including the complete device description.

8 Serial Peripheral Interface - SPI

The 24-bit Serial Peripheral Interface (SPI) enables the communication between the microcontroller and the TLE92108-232QX. It allows to configure and control the device, and to read out the status registers for diagnostic purpose.The MOSFET driver IC acts as a SPI-slave while the microcontroller acts as a SPI-master.

The interface has a serial data input pin (SDI) to transfer data to the device, a serial data output pin (SDO) for reading data back from the device, and a serial clock pin (SCLK) for clocking data into and out of the device. A chip select pin (CSN) enables or disables the serial interface.

The SPI frame starts with the falling edge of CSN. During the falling edge of CSN, SCLK must be low (Clock Polarity CPOL = 0). Received data on SDI are shifted in on the falling edge of SCLK. Transmitted data by SDO are shifted out on the rising edge of SCLK (Clock Phase CPHA = 1). Refer to **Figure 7**.

The Most Significant Bit (MSB, bit 23) is shifted in/out first.

Write and clear commands are executed at the rising edge of CSN.

The SPI protocol supports both independent slave selection and daisy chain configurations.

8.1 SPI protocol with independent slave selection

With individual slave selection, the microcontroller controls the CSN pin of each SPI slave individually (**Figure 6**).

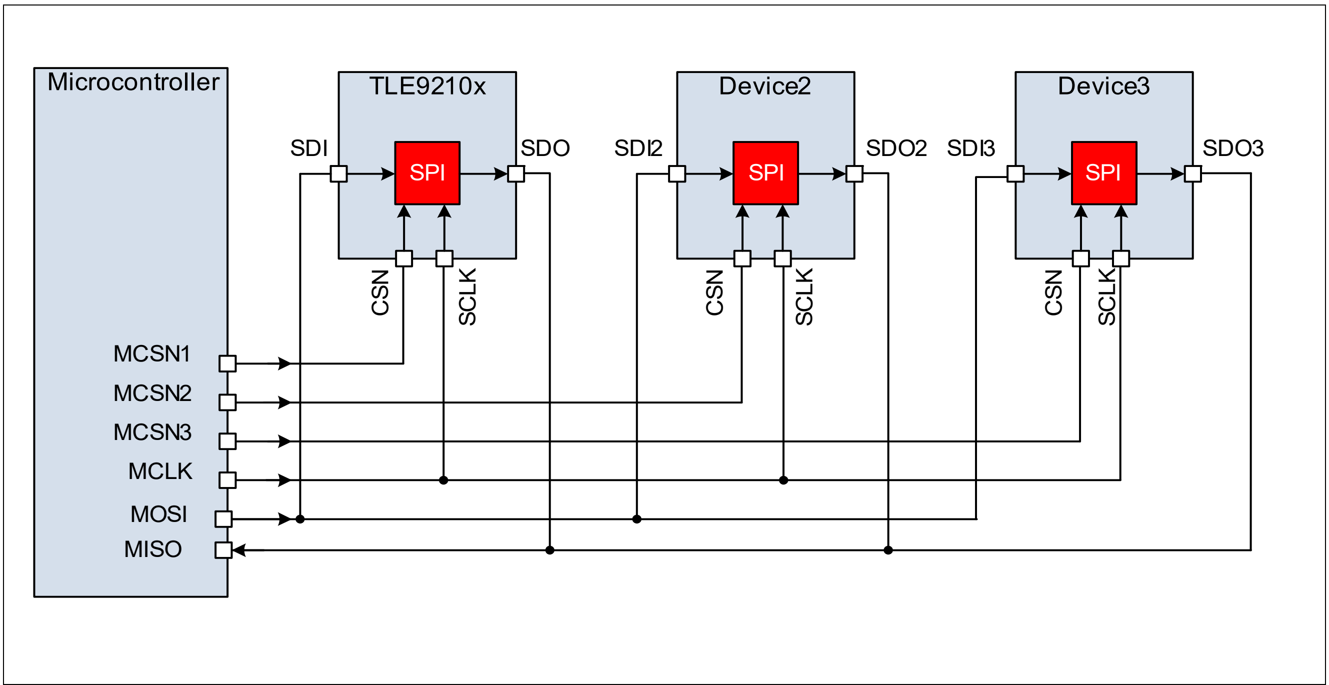


Figure 6 Individual slave selection with three slave devices

A SPI communication consists of 24-bit frame (**Figure 7**):

- SDI receives one address byte followed by two data bytes.
- SDO transmits the Global Error Flag and the Global Status Byte followed by two response bytes.

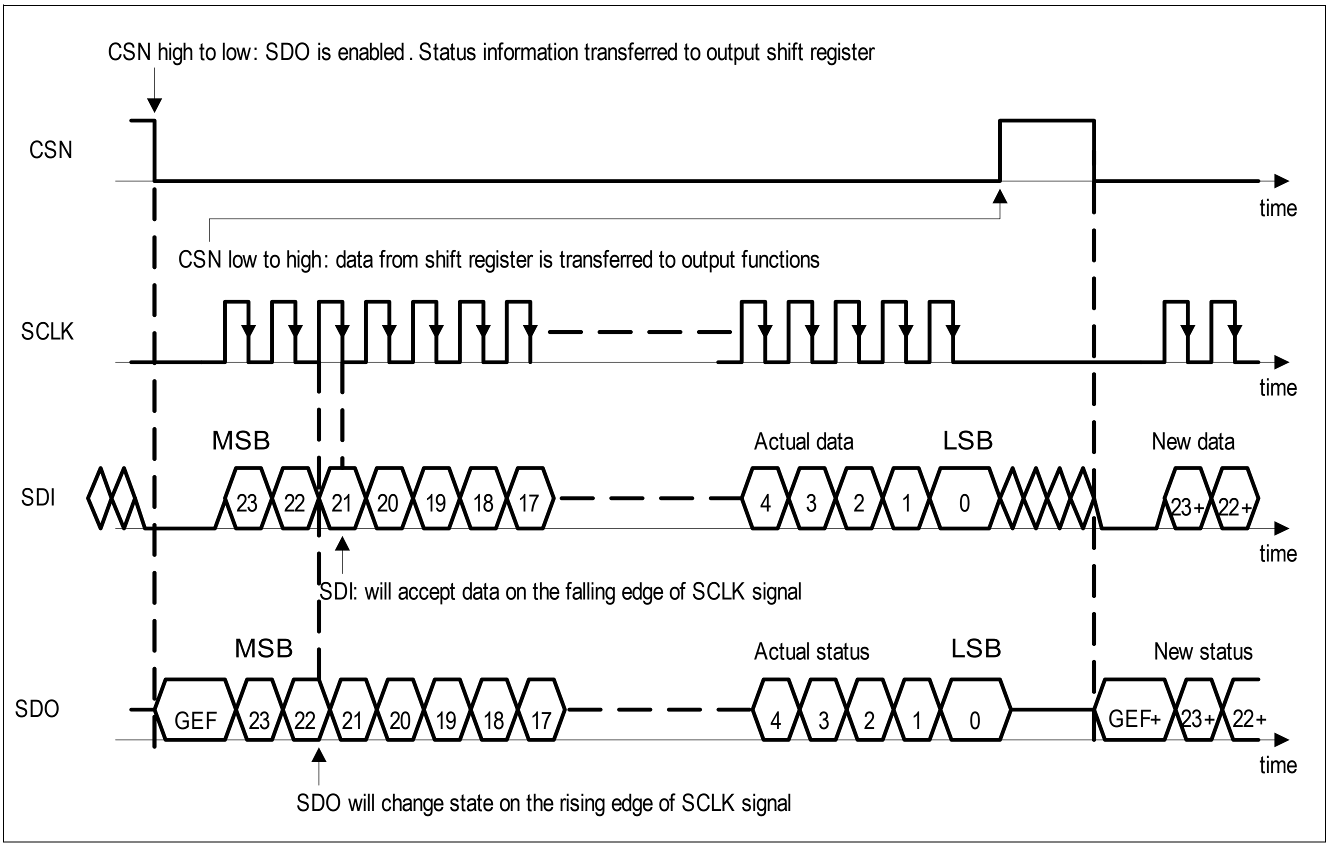


Figure 7 SPI Data Transfer

The MSB of the address byte must be set to '1'.

The address byte specifies (see **Figure 8**):

- the target register (A[4:0])
- the type of operation:
  - For control registers:
  - Read only: OP bit[1] = '0'
  - Read and write: OP bit = '1'
  - For status registers:
  - Read only: OP bit = '0'
  - Read and clear: OP bit = '1'

With individual slave selection, the Last Address Byte Token (LABT) must be set to '1'.

In-frame response

The SPI protocol incorporates an in-frame response: The content of the addressed register is shifted out by SDO within the same SPI frame. This feature reduces the SPI bus load during the read out of the control or status registers.

1) OP bit is the least significant bit of the address byte, see **Figure 8**

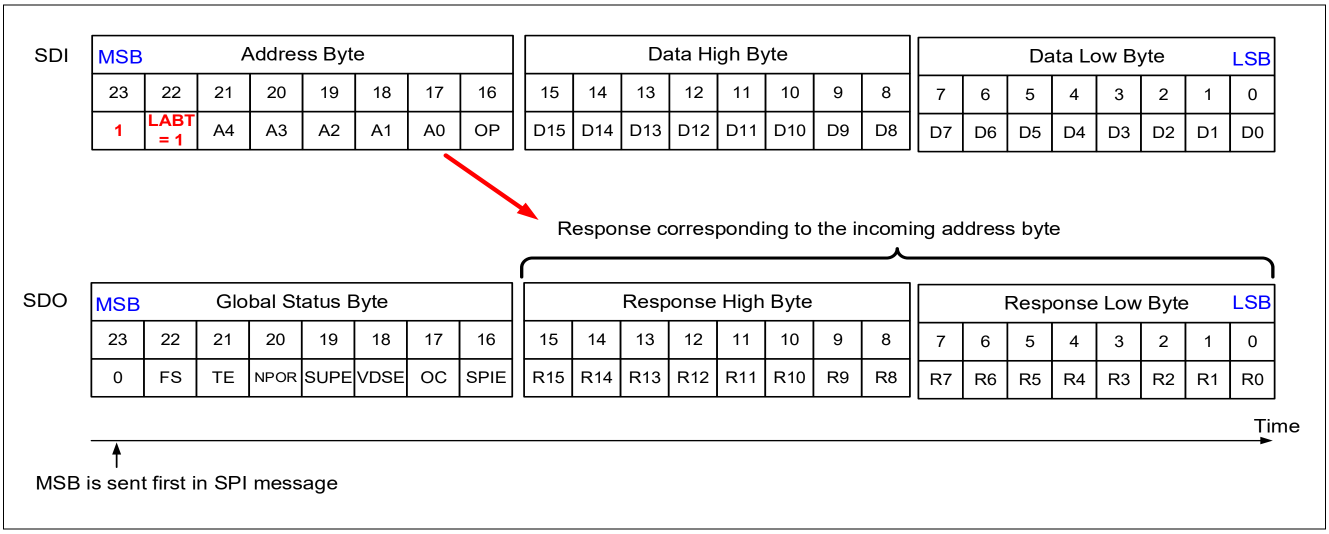


Figure 8 In-frame response with individual slave selection

8.2 Global Error Flag (GEF)

The Global Error Flag (GEF) is reported on SDO between the CSN falling edge and the first SCLK rising edge. GEF is set if a fault condition is detected or if the device comes from a Power On Reset (POR). It is therefore possible to have a quick device diagnostic without any SPI clock pulse (**Figure 9**).

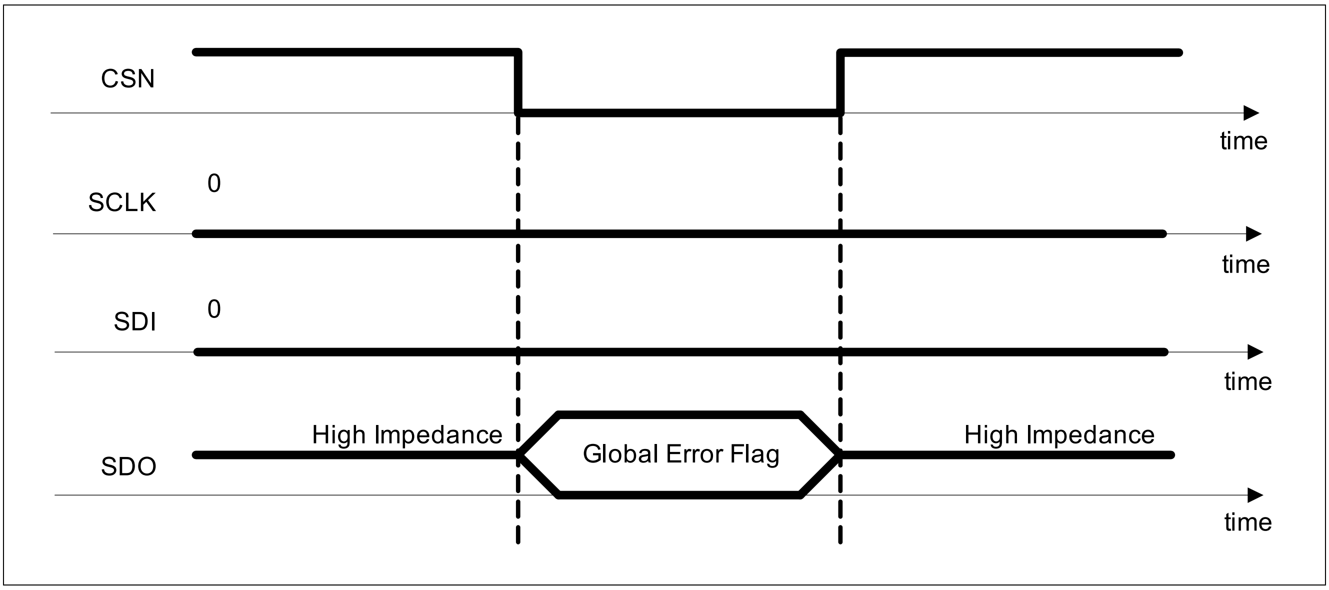


Figure 9 GEF - Diagnostic with 0-clock cycle

8.3 Global status byte

The SDO shifts out during the first eight SCLK cycles the Global Status Byte. This register provides an overview of the device status. The following error conditions are reported in this byte:

- Fail Safe (FS bit).
- Temperature error (TE bit): logical OR combination between Thermal Warning (**TW**) and Thermal shutdown (**TSD**).
- **Negated** Power ON Reset (NPOR bit, refer to **Chapter 5.3** for reset conditions).

- Supply Error (SUPE bit): logical OR combination between VS undervoltage shutdown (**VSUV**), VS overvoltage shutdown (**VSOV**) and charge pump undervoltage (**CPUV**).
- VDS monitoring Error (VDSE bit): logical OR combination between the bits of the **DSOV** register.
- Overcurrent (OC bit): logical OR combination between OC1 and OC2 status bits (**GENSTAT** register).
- SPI protocol Error (SPIE bit).

*Note: The Global Error Flag is a logic OR combination of every bit of the Global Status Byte and of TDREGx: GEF = (FS) OR (TE) OR (**NOT(NPOR)**) OR (SUPE) OR (VDSE) OR (OC) OR (SPIE) OR **(NOT(TDREGx) AND (PWMx_EN =1) AND (NOT (MSKTDREG)))**, x = 1 ... 3.*

The following table shows how failures are reported in the Global Status Byte and the error Flag:

Table 8 Failure reported in the global status byte and global error flag

Type of Error	Failure reported in the Global Status Byte	Global Error Flag
Fail safe	FS = 1	1
Thermal error	TE = 1	1
Power ON reset	**NPOR = 0**	1
Supply error	SUPE = 1	1
Drain source voltage monitoring	VDSE = 1	1
Overcurrent	OC = 1	1
SPI protocol error	SPIE = 1	1
TDREGx, x = 1 ... 3[1] (see **GENSTAT**)	-	1 if MSKTDREG = 0[2] 0 if MSKTDREG = 1[2]
No error and no power ON reset	SPIE = 0 OC = 0 VDSE = 0 SUPE= 0 **NPOR = 1** TE = 0 FS = 0 TDREGx = 0,	0

1) See status register **GENSTAT**.
2) See control register **GENCTRL2**.

Note: The default value (after Power ON Reset) of NPOR is 0, therefore the default value of GEF is 1.

In fail safe mode, the control registers are frozen to their default value, with the exception of the WDTRIG bit (refer to **Chapter 5.2.3**). Any write access (except for WDTRIG bit) in fail safe mode will be discarded and the SPIE bit will set.

8.4 SPI error detection

The SPI incorporates an error flag in the Global Status Byte (SPIE) to supervise and preserve the data integrity. If an SPI protocol error is detected during a given frame, the SPIE bit is set in the next SPI communication.

The SPIE bit is set in the following error conditions:

- The number of SCLK clock pulses received when CSN is Low is (protocol error):
  - not zero
  - or less than 24
  - or more than 24 but not a multiple of 8
- The microcontroller sends an SPI command to an unused address (protocol error).
- A clock polarity error is detected (see **Figure 10** Case 2 and Case 3): the incoming clock signal was High during CSN rising or falling edges (protocol error).
- No address byte or no last address byte are detected (protocol error).
- In daisy chain: the microcontroller does not send in sequence the first address byte until the last address byte (i.e. with gaps between two address bytes). In this case, the SDO signal is set to '0' during the remaining part of the SPI frame[1)], in order to prevent other devices from executing wrong commands (protocol error).
- A clear command to address 0x1F (Device ID register, Offset address = 0x1F).
- The same half-bridge is allocated to several activated PWM channels.
- Any write or clear command received in fail safe mode and not belonging to the exit sequence (refer to **Chapter 5.2.3**).

Note: SPI commands to activate a half-bridge mapped to several PWM channels are ignored.

In fail safe mode, the control registers may not be accessed, except for writing WDTRIG. An invalid write command in this mode sets the SPIE bit.

For a correct SPI communication:

- SCLK must be Low for a minimum t_{BEF} before CSN falling edge and t_{lead} after CSN falling edge.
- SCLK must be Low for a minimum t_{lag} before CSN rising edge and t_{BEH} after CSN rising edge.

1) Provided that the SPI frame has a correct polarity

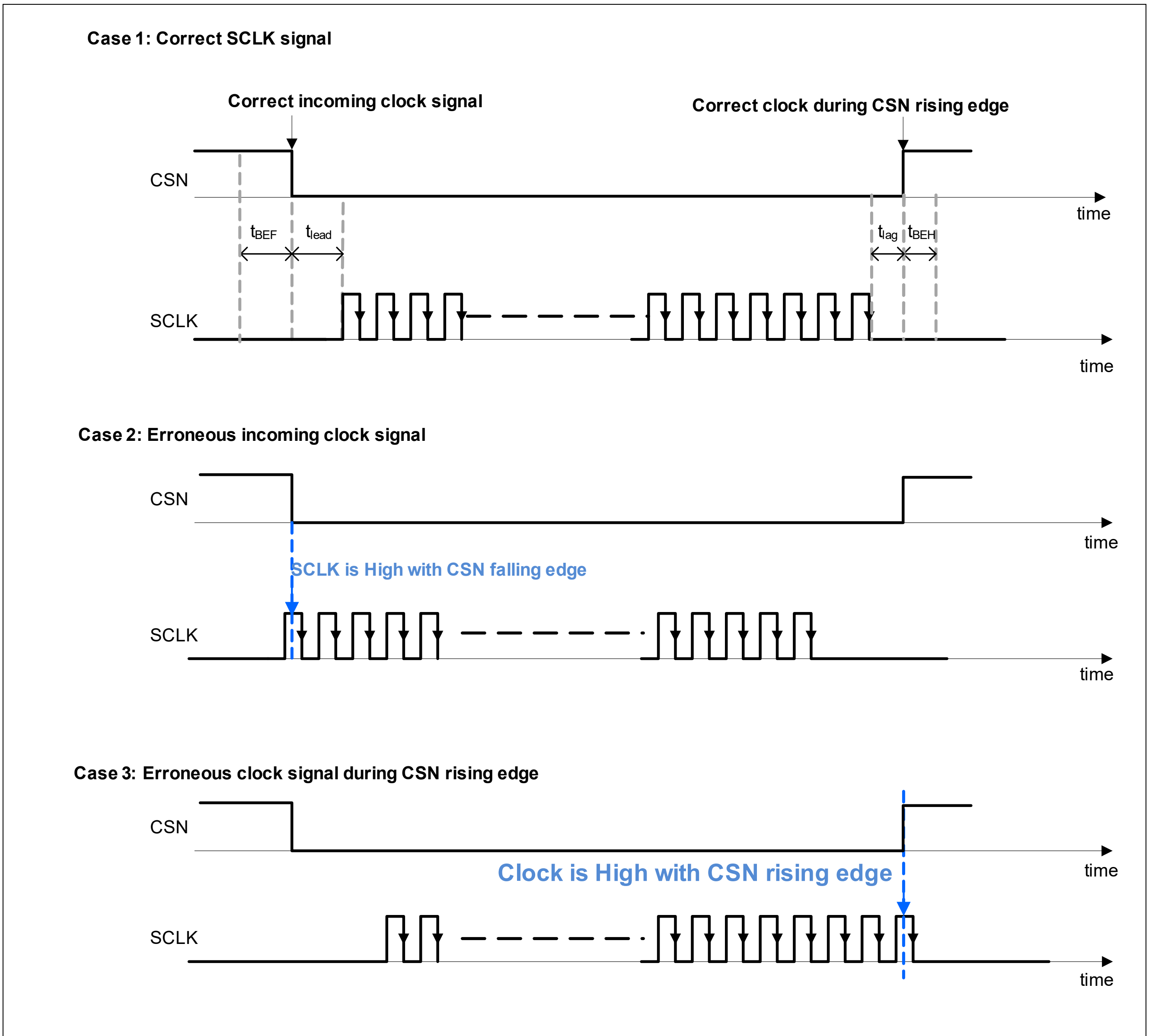


Figure 10 Clock polarity error

The reset condition of the SPIE bit depends on the cause of error:

- In normal mode:
  - The microcontroller must clear **HBVOUT_PWMERR** if one half-bridge has been allocated to several PWM channels.
  - The microcontroller must send a correct SPI frame for the other errors reported by SPIE.
- If SPIE has been set in fail safe mode, the device must enter normal mode first.

8.5 Daisy chain

In daisy chain configuration the master output / slave input (noted MOSI) is connected to a slave SDI. The first slave SDO is connected to the next slave SDI in the chain. The SDO of the final in the chain is connected to the master input / slave output (noted MISO). In daisy chain configuration, the microcontroller MCSN is connected to all the slave CSN inputs (**Figure 11**).

To support daisy chain configurations, the TLE92108-232QX accepts SPI frames with more than 24 bits, provided that the number of bits is a multiple of 8, and the structure of the address byte is respected.

In daisy chain, the TLE92108-232QX works as follows:

1. The TLE92108-232QX operates as a 8-bit shift register until it receives the first address byte. This first received address byte is considered by the device as its own address byte.
2. The TLE92108-232QX copies directly SDI to SDO until the last address byte is detected.
3. The TLE92108-232QX shifts out the response high byte and low byte corresponding to the address byte.
4. After the last address byte, the TLE92108-232QX operates as a 16-bit shift register until the end of the SPI frame.

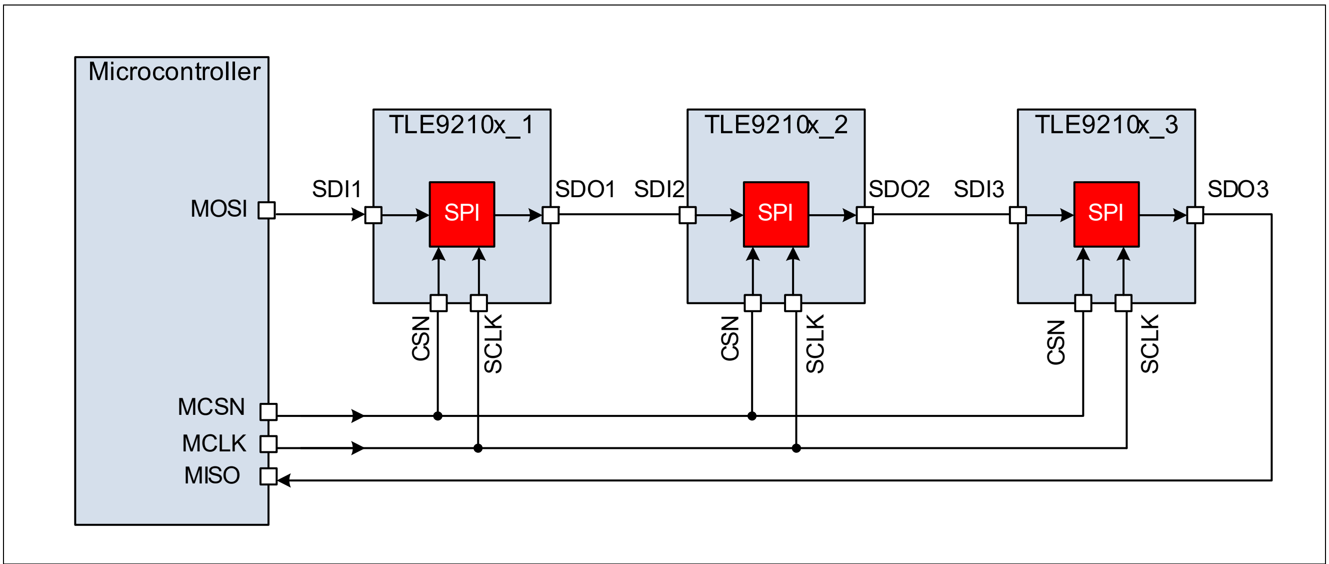


Figure 11 Daisy chain configuration with three TLE9210x devices

In daisy chain configuration (**Figure 11**), the microcontroller must send the address and data bytes in the following order (**Figure 12**):

1. The address bytes altogether are sent first:
   - Address byte 1 (for TLE9210x_1) is sent first, followed by address byte 2 (for TLE9210x_2), followed by address byte 3 (for TLE9210x_3).
   - The LABT bit of the last address byte must be ‘1’, while the LABT bit of all the other address bytes must be ‘0’.
2. The data bytes are sent altogether **in reverse order** once the address bytes are transmitted:
   - The data high byte for the TLE9210x_3 is sent first followed by the data low byte for the TLE9210x_3.
   - Then the data high byte for the TLE9210x_2 is sent followed by the data low byte for the TLE9210x_2.
   - Then the data high byte for the TLE9210x_1 is sent followed by the data low byte for the TLE9210x_1.

The Master Input / Slave Output (MISO), which is connected to SDO of the last device in the daisy chain, receives:

1. A logic OR combination of all Global Error Flags (GEF) at the beginning of the SPI frame, between CSN falling edge and the first SCLK rising edge.
2. The Global Status Byte of each TLE9210x **in reverse order**:

- The Global Status Byte 3 (GSB3) corresponding to the TLE9210x_3 is received first, followed by GSB2 (corresponding to the TLE9210x_2), and finally the GSB1 (corresponding to the TLE9210x_1) is received.

3. The response of each TLE9210x **in reverse order**:
   - The response high byte of the TLE9210x_3 is received first followed by the response low byte of the TLE9210x_3.
   - Then the response high byte of the TLE9210x_2 is received followed by the response low byte of the TLE9210x_2.
   - Then the response high byte of the TLE9210x_1 is received followed by the response low byte of the TLE9210x_1.

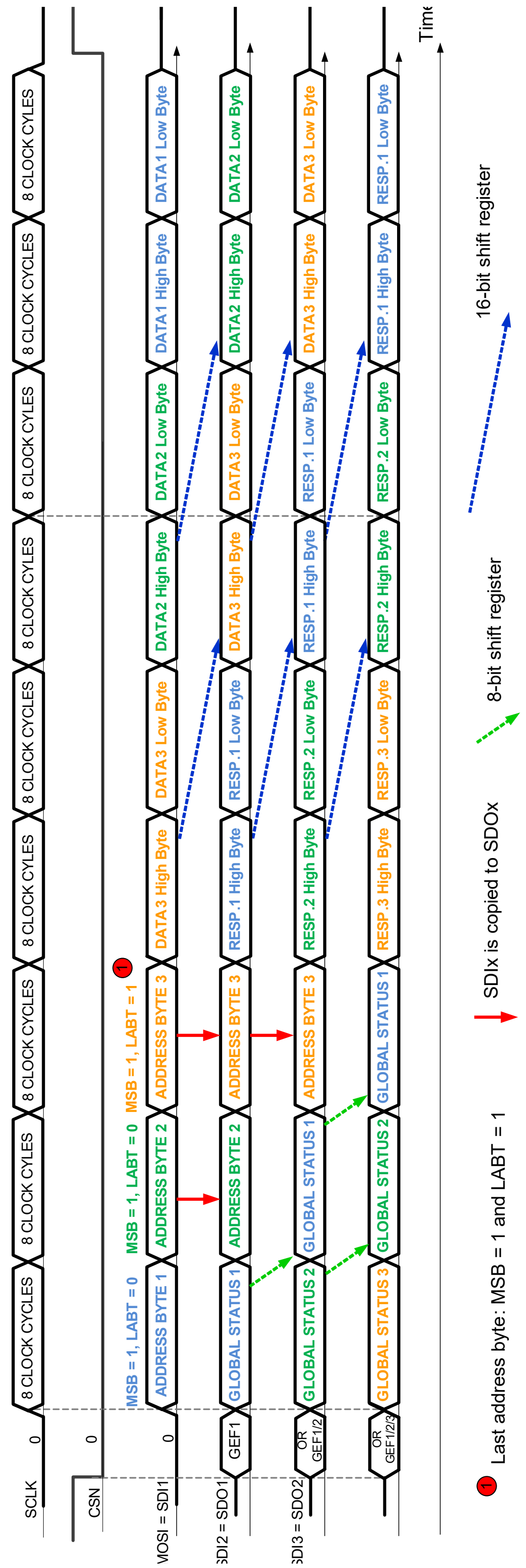


Figure 12 SPI Frame in daisy chain configuration with three TLE9210x devices

8.6 SPI electrical characteristics: timings

Table 9 Electrical characteristics: SPI interface

V_S = 6.0 V to 18 V if VSOVTH = 0, V_S = 6.0 V to 28 V if VSOVTH = 1; V_{DD} = 3.0 V to 5.5 V, T_j = -40°C to 150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
SPI frequency							
Maximum SPI frequency	$f_{SPI,max}$	–	–	4		1)	P_8.6.1
Delay from EN rising edge to first SPI frame							
SPI interface setup time[2)]	t_{SET_SPI}	–	–	150	µs	1)	P_8.6.32
SPI interface, logic inputs SDI, SCLK, CSN							
High input voltage threshold	V_{IH}	0.7 x V_{DD}	–	–	V		P_8.6.2
Low input voltage threshold	V_{IL}	–	–	0.3 x V_{DD}	V		P_8.6.3
Hysteresis of input voltage	V_{IHY}	–	0.12 x V_{DD}	–	V	1)	P_8.6.4
Pull up resistor at pin CSN	R_{PU_CSN}	20	40	80	kΩ	V_{CSN} = 0.7 x V_{DD}	P_8.6.5
Pull down resistor at pin SDI, SCLK	R_{PD_SDI}, R_{PD_SCLK}	20	40	80	kΩ	V_{SDI}, V_{SCLK} = 0.2 x V_{DD}	P_8.6.6
Input capacitance at pin CSN, SDI or SCLK	C_I	–	10	–	pF	1) 0 V < V_{DD} < 5.5 V	P_8.6.7
Input interface, logic outputs SDO							
H-output voltage level	V_{SDOH}	0.8 x V_{DD}	–	–	V	I_{SDOH} = -1.6 mA	P_8.6.8
L-output voltage level	V_{SDOL}	–	–	0.2 x V_{DD}	V	I_{SDOL} = 1.6 mA	P_8.6.9
Tri-state Leakage Current	I_{SDOLK}	-10	–	10	µA	1) V_{CSN} = V_{DD}; 0 V < V_{SDO} < V_{DD}	P_8.6.10
Tri-state input capacitance	C_{SDO}	–	10	15	pF	1)	P_8.6.11
Data input timing. See Figure 6							
SCLK Period	t_{pCLK}	250	–	–	ns	1)	P_8.6.12
SCLK High Time	t_{SCLKH}	0.45 x t_{pCLK}	–	0.55 x t_{pCLK}	ns	1)	P_8.6.13
SCLK Low Time	t_{SCLKL}	0.45 x t_{pCLK}	–	0.55 x t_{pCLK}	ns	1)	P_8.6.14
SCLK Low before CSN Low	t_{BEF}	125	–	–	ns	1)	P_8.6.15
CSN Setup Time	t_{lead}	250	–	–	ns	1)	P_8.6.16
SCLK Setup Time	t_{lag}	250	–	–	ns	1)	P_8.6.17
SCLK Low after CSN High	t_{BEH}	125	–	–	ns	1)	P_8.6.18
SDI Setup Time	t_{SDI_setup}	100	–	–	ns	1)	P_8.6.19

Table 9 Electrical characteristics: SPI interface (cont'd)

V_S = 6.0 V to 18 V if VSOVTH = 0, V_S = 6.0 V to 28 V if VSOVTH = 1; V_{DD} = 3.0 V to 5.5 V, T_j = -40°C to 150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition	Number
		Min.	Typ.	Max.			
SDI Hold Time	t_{SDI_hold}	50	–	–	ns	1)	P_8.6.20
Input Signal Rise Time at pin SDI, SCLK, CSN	t_{rIN}	–	–	50	ns	1)	P_8.6.21
Input Signal Fall Time at pin SDI, SCLK, CSN	t_{fIN}	–	–	50	ns	1)	P_8.6.22
Delay time from EN falling edge to standby mode	t_{DMODE}	–	–	6	µs	1)	P_8.6.23
Minimum CSN High Time	t_{CSNH}	3	–	–	µs	1)	P_8.6.24
Data output timing. See Figure 7.							
SDO Rise Time	t_{rSDO}	–	30	80	ns	1) C_{load} = 100 pF	P_8.6.25
SDO Fall Time	t_{fSDO}	–	30	80	ns	1) C_{load} = 100 pF	P_8.6.26
SDO Enable Time after CSN falling edge	t_{ENSDO}	–	–	50	ns	1) Low Impedance	P_8.6.27
SDO Disable Time after CSN rising edge	t_{DISSDO}	–	–	50	ns	1) High Impedance	P_8.6.28
Duty cycle of incoming clock at SCLK	$duty_{SCLK}$	45	–	55	%	1)	P_8.6.29
SDO Valid Time for V_{DD} = 5V	t_{VASDO5}	–	–	50	ns	1) $V_{SDO} < 0.2 \times V_{DD}$ $V_{SDO} > 0.8 \times V_{DD}$ C_{load} = 100 pF	P_8.6.31

1) Not subject to production test, specified by design

2) Delay required between EN rising edge and the moment when the device can accept SPI commands

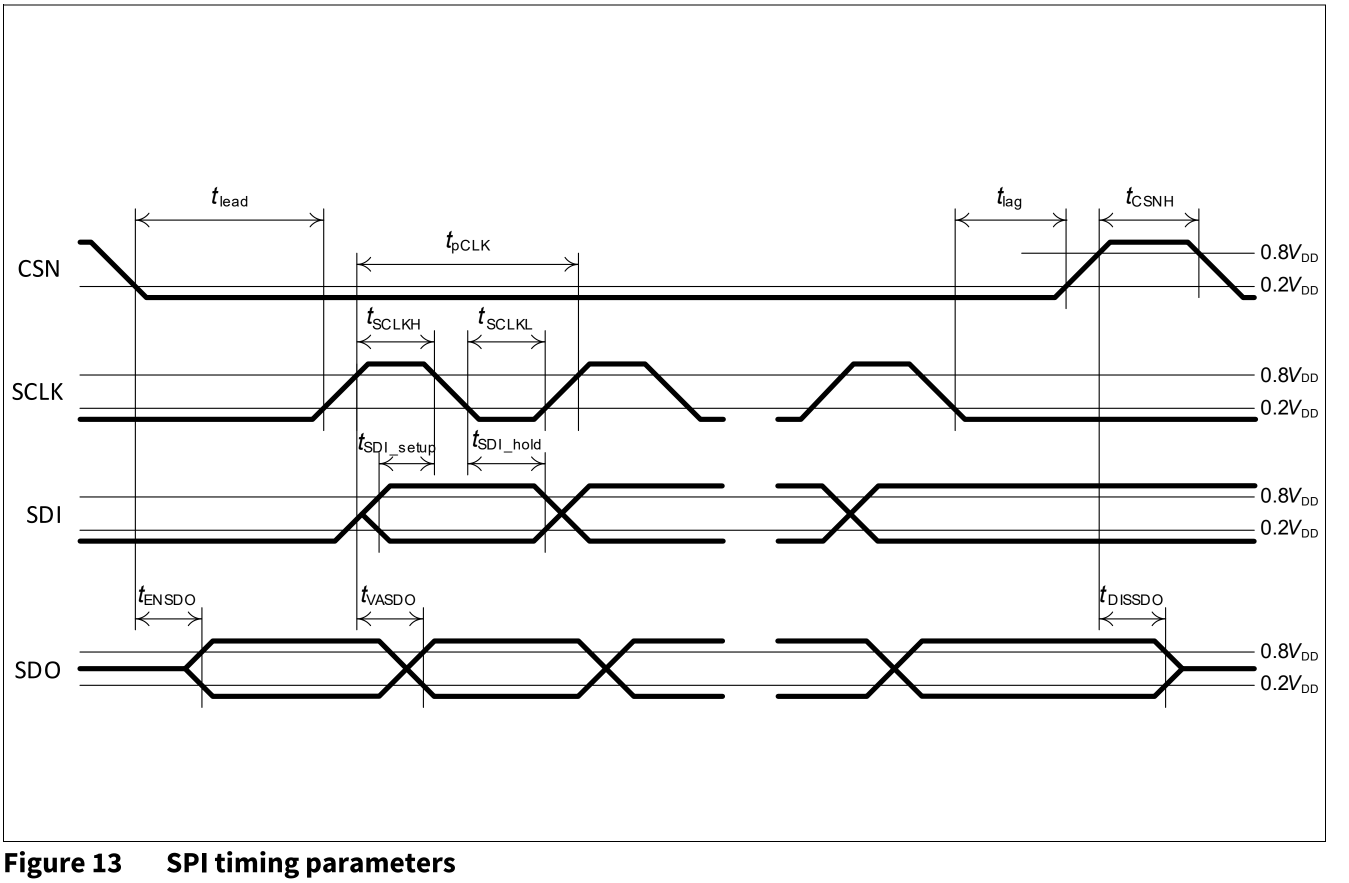


Figure 13 SPI timing parameters

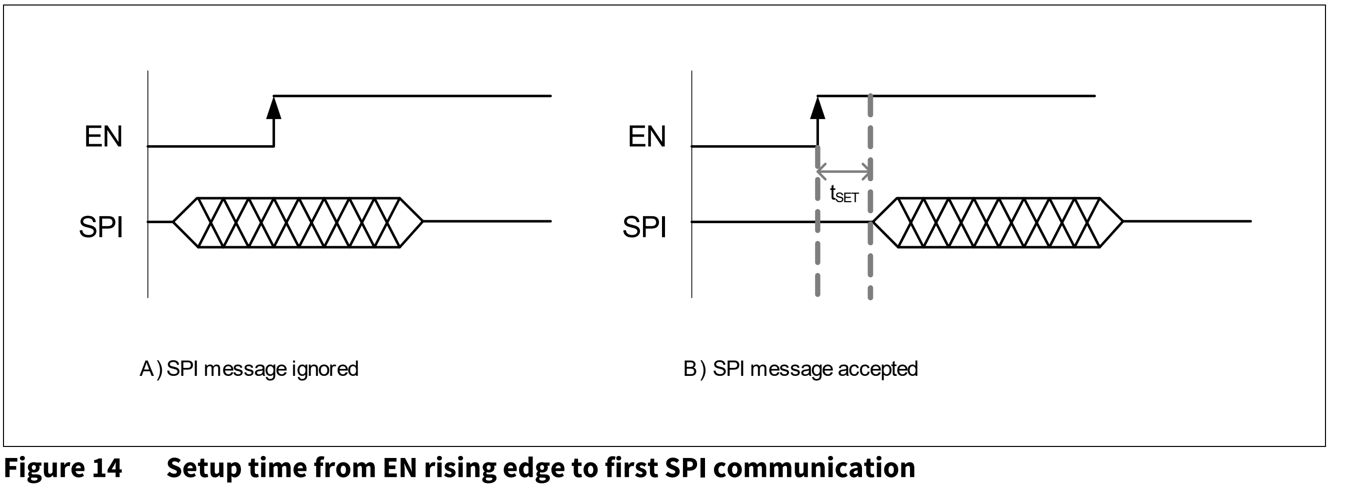


Figure 14 Setup time from EN rising edge to first SPI communication

9 Register specification

For more information, please contact your sales partner for the datasheet including the complete device description.

10 Application information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

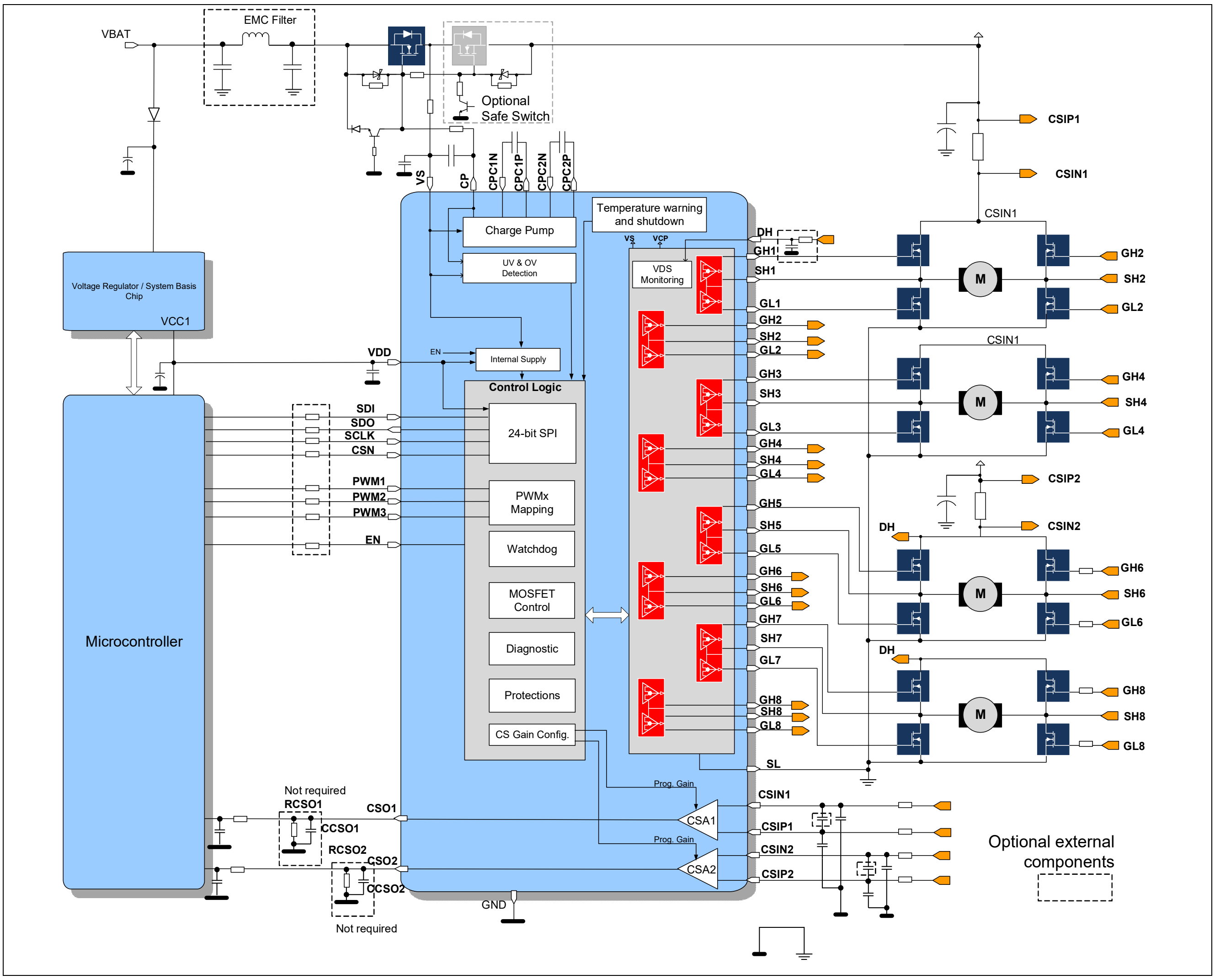


Figure 15 Application diagram TLE92108-232QX

Note: This is a simplified example of an application circuit. The function must be verified in the real application.

The charge pump buffer capacitor between VS and CP must have a capacitance equal or higher than 470 nF for a stable operation. A higher capacitance can be used to reduce the voltage ripples caused by the charge of the gate of the external MOSFETs during PWM operation.

The flying capacitors between CPC1N/CPC1P and CPC2N/CPC2P must be as close as possible to the TLE92108-232QX.

The decoupling capacitors between VS/GND and VDD/GND must be as close as possible to the TLE92108-232QX and short PCB tracks to the GND plane.

A resistor (RCSOx) and a capacitor (CCSOx) can be placed (not mandatory) at the output of the current sense amplifiers.

The device does not need any resistor at the output of the current sense amplifiers. However, if a resistor is used by the application, RCSOx must be higher than 1 kΩ. This resistor causes additional current consumption from VDD, which is not taken into account in the electrical characteristics of the datasheet.

CCSOx must be between 10 pF and 400 pF. For a fast reaction time of the CSA output, it is recommended to keep CCSOx to 10 pF.

If a filter is used at the inputs of the current sense amplifier, the serial resistor may not exceed 5 Ω.

It is possible that the MOSFET gate voltage goes below the source voltage during the commutation of a half-bridge. This depends on the stray inductances at the drain and the source of the MOSFET, the speed of the commutation and the ratio between the MOSFET Gate-Source and Gate-Drain capacitances.

If $V_{GATE} - V_{SOURCE} < -0.6$ V, a series resistor (e.g. 4.7 Ω) in series to GHx and GLx are recommended to limit current delivered by the gate driver during the commutation.

Shunt resistor in the motor phase

When the shunt resistor is placed in the motor phase, it is highly recommended to apply the PWM to the half-bridge which is not connected to the shunt resistor (**Figure 16**). This avoids a high common mode swing at the inputs of the current sense amplifier.

The drain-source monitoring of the monitoring of the drain-source overvoltage of the high-side MOSFETs must be set to DH - VSHx. Refer to **VDS1**, **VDS2**, HBxD bits.

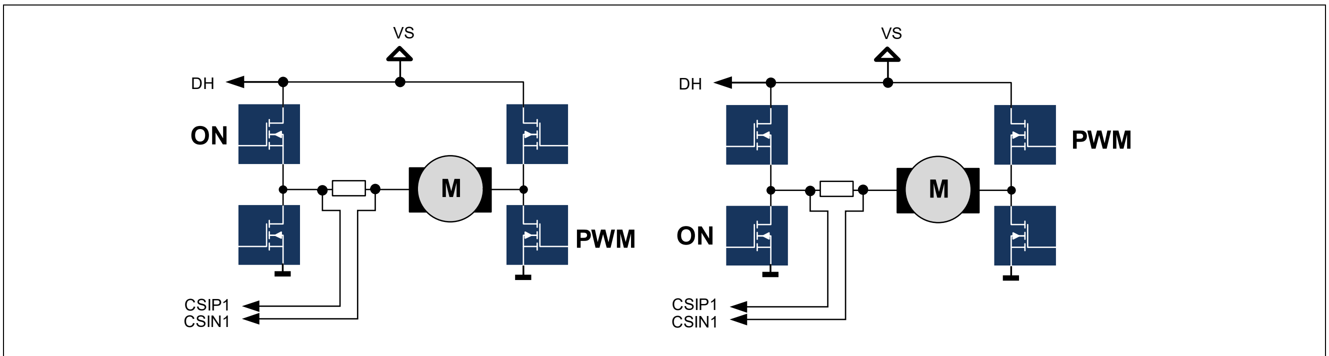
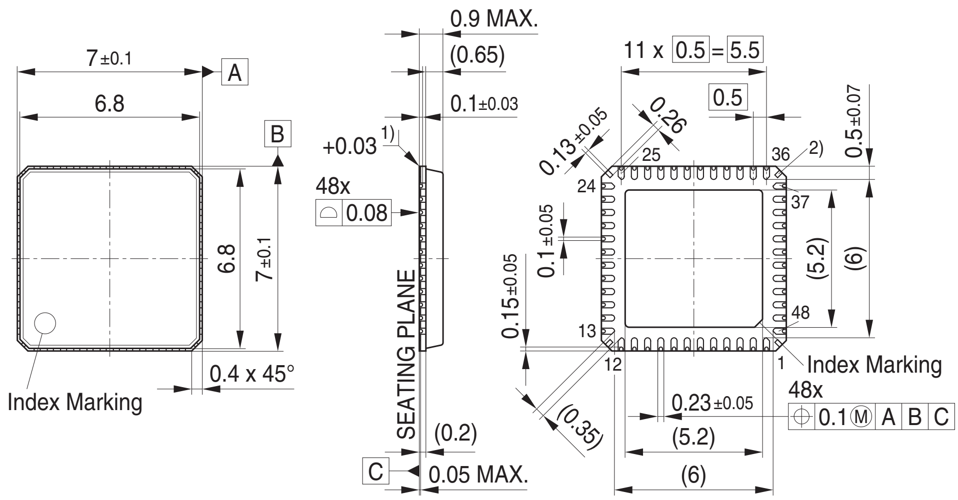


Figure 16 PWM with Shunt resistance in the motor phase

For a proper off-state diagnostic for with the shunt resistor in the motor phase, the corresponding current sense amplifier (CSA) must be deactivated. Otherwise, the activated CSA draws current from its inputs, preventing the internal pull-up source to set the SHx pin to high.

11 Package outlines



1) Vertical burr 0.03 max., all sides
2) These four metal areas have exposed diepad potential

PG-VQFN-48-29, -31-PO V05

Figure 17 **PG-VQFN-48**[1)]

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

1) Dimmensions in mm

12 Revision History

Revision	Date	Changes
1.0	2019-08-29	First release

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Document reference