



Product Specification

T215HVN05.1

AU OPTRONICS CORPORATION

(V) Preliminary Specification

() Final Specification

Module	21.5" Color TFT-LCD
Model Name	T215HVN05.1 open cell

Customer	Date	Approved by	Date
_____	_____	<u>Howard Lee</u>	<u>Aug. 23, 2017</u>
Approved by		Prepared by	Date
_____	_____	<u>Kevin Su</u>	<u>Aug.21, 2017</u>
		AU Optronics corporation	

Contents

1 Handling Precautions	4
2 General Description	5
2.1 Display Characteristics	5
2.2 Absolute Maximum Rating of Environment.....	5
2.3 Optical Characteristics.....	6
3 TFT-LCD Module	12
3.1 Block Diagram.....	12
3.2 Interface Connection.....	13
3.2.1 Connector Type	13
3.2.2 Connector Pin Assignment.....	13
3.3 Electrical Characteristics.....	15
3.3.1 Absolute Maximum Rating.....	15
3.3.2 Recommended Operating Condition.....	15
3.3.3 Input control signal threshold voltage definition	16
3.3.4 Write Protection mode selection.....	16
3.3.5 Input equivalent impedance	16
3.4 Signal Characteristics	16
3.4.1 LCD Pixel Format	16
3.4.2 LVDS Data Format.....	16
3.4.3 Color versus Input Data.....	18
3.4.4 LVDS Specification	19
3.4.5 Input Timing Specification.....	21
3.4.6 Input Timing Diagram	22
3.4.7 I2C Electrical Characteristics.....	23
3.5 Power ON/OFF Sequence	24
3.6 Vcom adjustment flow.....	25
4 Reliability Test.....	28
5 Shipping Label.....	29
6 Mechanical Characteristic	錯誤! 尚未定義書籤。
7 Packing Specification	31
7.1 Packing Flow	31
7.2 Pallet and Shipment information.....	32



Product Specification

T215HVN05.1

AU OPTRONICS CORPORATION

Record of Revision

Version	Date	Page	Old description	New Description	Remark
0.0	2017/08/23			Preliminary spec	

1 Handling Precautions

- 1) Since polarizer is easily damaged, do not touch or press the surface of polarizer with hand.
- 2) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 3) When the cell surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 4) Since the cell is made of glass, it may break or crack if dropped or bumped on hard surface.
- 5) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 6) Do not press or pat the panel surface by fingers, hand or tooling.
- 7) Please handle TFT cell with care. The FPCs can only sustain for quite limited stress.
- 8) The cell package tray is packed in clean room. Please do pack & unpack it in clean room.
- 9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT cell.
- 10) Pls avoid touching COF position while you are doing mechanical design.
- 11) When storing modules as spares for a long time, the following precaution is necessary: Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5℃ and 35℃ at normal humidity.
- 12) Do not apply the same pattern for a long time, it will enhance relevant defect.
- 13) If the product will be used under extreme conditions such as under high temperature, humidity, display patterns or the operation time etc., it is strongly recommended to contact AUO for the advice about the application of engineering. Otherwise, its reliability and the function may not be guaranteed. Extreme conditions are commonly found at airports, transit stations, banks, stock markets, and controlling systems.
- 14) Module designer should apply adequate thermal solutions to keep the electrical components surface temperature under control limit (ex: Source Driver IC 100℃ , Components on T-con PCB 85℃) Operations over the temperature can cause damages or decrease of lifetime.



2 General Description

This specification applies to the 21.5 inch wide Color a-Si TFT-LCD Module T215HVN05.1. The display supports the Full HD - 1920(H) x 1080(V) screen format and 16.7M colors (RGB 6-bits+Hi-FRC). The input interface is Dual channel LVDS.

2.1 Display Characteristics

The following items are characteristics summary on the table under 25℃ condition:

ITEMS	Unit	SPECIFICATIONS	
Screen Diagonal	[mm]	546.21 (21.50")	
Active Area	[mm]	476.064 (H) x 267.786 (V)	
Pixels H x V	-	1920(x3) x 1080	
Pixel Pitch	[um]	247.95 (per one triad) ×247.95	
Pixel Arrangement	-	R.G.B. Vertical Stripe	
Display Mode	-	VA Mode, Normally Black	
Response Time	[msec]	18 (Typ., on/off)	
Power Consumption	[Watt]	LCD module : PDD (Typ.)=3.5W@ White pattern,Fv=60Hz Backlight unit : PBLU (Typ.)=9.86 @Is=50mA	
Weight	[Grams]	TBD	
Electrical Interface	-	Dual channel LVDS	
Support Color	-	16.7M colors (RGB 6-bits +Hi-FRC)	
Surface Treatment	-	Anti-Glare , 3H	
Temperature Range Operating Storage (Shipping)	[°C]	0 to +50 -20 to +60	
Cell transmittance	[%]	3.60 (Typ.) 3.06 (Min)	Base on AUO LED Backlight
Cell thickness	[mm]	1.41 (Thickness of polarizer(upper) film:0.20mm ; polarizer(down) 0.21mm)	

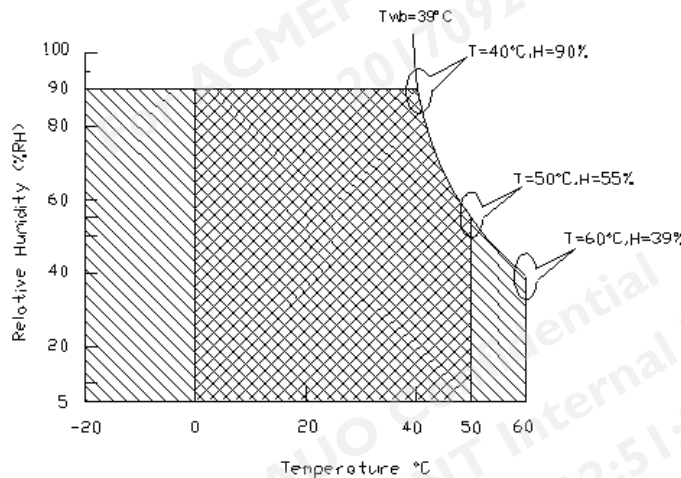
2.2 Absolute Maximum Rating of Environment

Permanent damage may occur if exceeding the following maximum rating.

Symbol	Description	Min.	Max.	Unit	Remark
TOP	Operating Temperature	0	+50	[°C]	Note 2-1
TGS	Glass surface temperature (operation)	0	+65	[°C]	Note 2-1 Function judged only
HOP	Operation Humidity	5	90	[%RH]	Note 2-1
TST	Storage Temperature	-20	+60	[°C]	
HST	Storage Humidity	5	90	[%RH]	

Note 2-1: Temperature and relative humidity range are shown as the below figure.

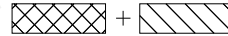
1. 90% RH Max ($T_a \leq 39^\circ\text{C}$)
2. Max wet-bulb temperature at 39°C or less. ($T_a \leq 39^\circ\text{C}$)
3. No condensation



Operating Range



Storage Range



2.3 Optical Characteristics

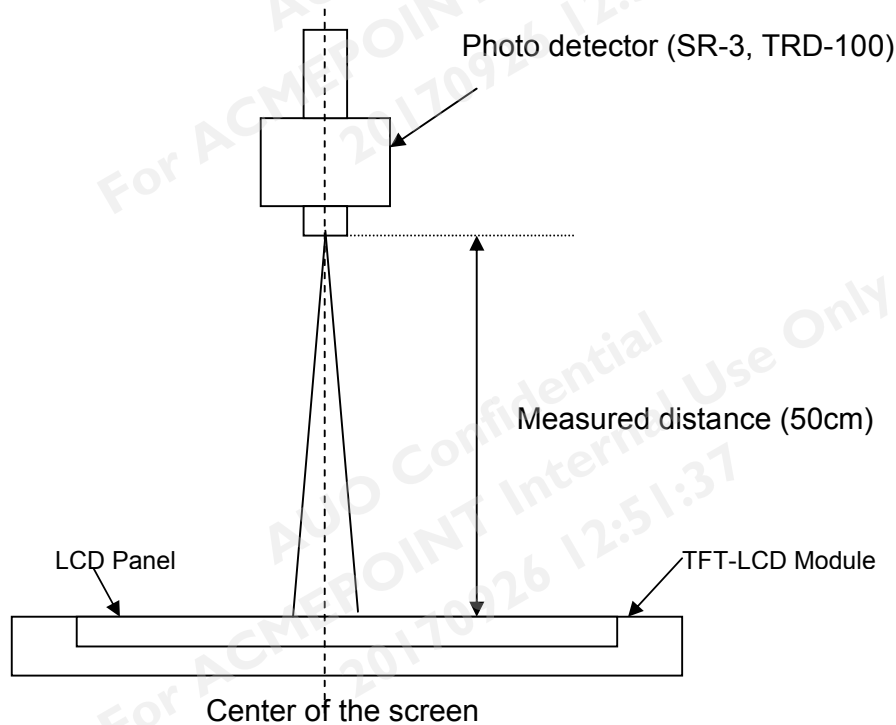
The optical characteristics are measured on the following test condition.

Test Condition:

1. Equipment setup: Please refer to **Note 2-2**.
2. Panel Lighting time: 30 minutes
3. VDD=5.0V, Fv=60Hz, Is=65mA, Ta=25℃

Symbol	Description		Min	Typ.	Max	Unit	Remark
CR	Contrast Ratio (Center of screen)		2000	3000	-	-	Note 2-3 Base on AUO LED Backlight
θ_R	Horizontal Viewing Angle (CR=10)	Right	75	89	-	[degree]	Note 2-4 By SR-3 (Base on AUO backlight design)
θ_L		Left	75	89	-		
Φ_H	Vertical Viewing Angle (CR=10)	Up	75	89	-		
Φ_L		Down	75	89	-		
θ_R	Horizontal Viewing Angle (CR=5)	Right	75	89	-		
θ_L		Left	75	89	-		
Φ_H	Vertical Viewing Angle (CR=5)	Up	75	89	-		
Φ_L		Down	75	89	-		
T_R	Response Time	Rising Time	-	13	28	[msec]	Note 2-5 By TRD-100
T_F		Falling Time	-	5	8		
-		Rising + Falling	-	18	36		
T_{GTG}	Response Time	Gray To Gray	-	28	-	[msec]	Note 2-5 By TRD-100
R_x	Color Coordinates (CIE 1931)	Red x	0.627	0.657	0.687		Base on C light
R_y		Red y	0.305	0.335	0.365		
G_x		Green x	0.288	0.318	0.348		
G_y		Green y	0.604	0.634	0.664		
B_x		Blue x	0.124	0.154	0.184		
B_y		Blue y	0.034	0.064	0.094		
W_x		White x	0.283	0.313	0.343		
W_y		White y	0.299	0.329	0.359		
CT	Crosstalk		-	-	2.0	[%]	Note 2-6 By SR-3
F_{dB}	Flicker (Center of screen)		-	-	-20	[dB]	Note 2-7 By SR-3

Note 2-2: Equipment setup :



Note 2-3: Contrast Ratio Measurement

Definition:

$$\text{Contrast Ratio} = \frac{\text{Luminance of White pattern}}{\text{Luminance of Black pattern}}$$

a. Measured position: Center of screen (P5) & perpendicular to the screen

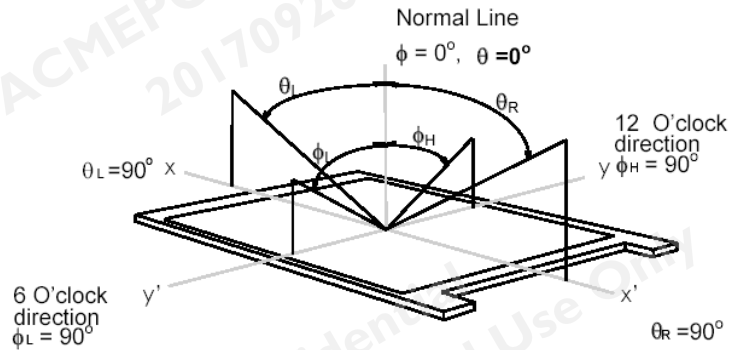
($\theta = \Phi = 0^\circ$)

Note 2-4: Viewing angle measurement

Definition: The angle at which the contrast ratio is greater than 10 & 5 .

a. Horizontal view angle: Divide to left & right (θ_L & θ_R)

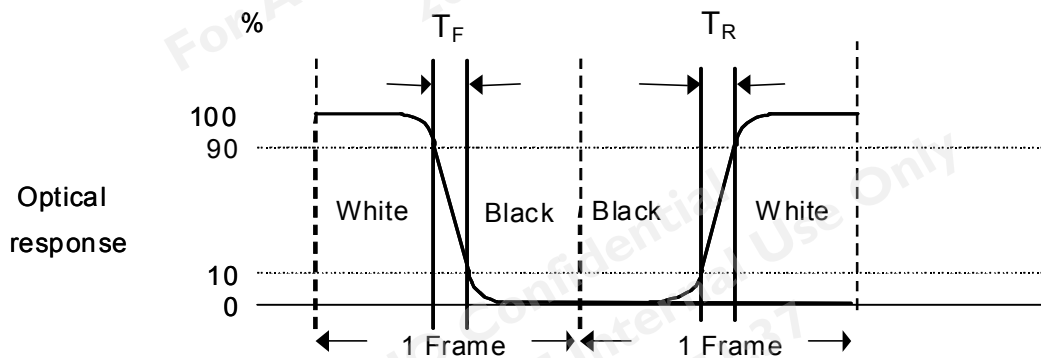
Vertical view angle: Divide to up & down (Φ_H & Φ_L)



Note 2-5: Response measurement

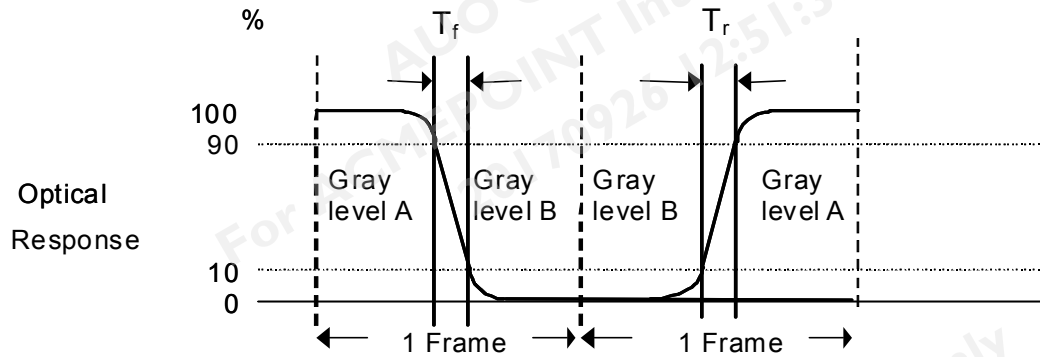
time

The output signals of photo detector are measured when the input signals are changed from "Black" to "White" (rising time, T_R), and from "White" to "Black" (falling time, T_F), respectively. The response time is interval between the 10% and 90% of optical response. (Black & White color definition: Please refer section 3.4.3)



Note 2-5: Response time measurement

The output signals of photo detector are measured when the input signals are changed from "Gray level A" to "Gray level B" (falling time, T_F), and from "Gray level B" to "Gray level A" (rising time, T_R), respectively. The response time is interval between the 10% and 90% of optical response.



The gray to gray response time is defined as the following table.

Gray Level to Gray Level		Target gray level				
		L0	L63	L127	L191	L255
Start gray level	L0					
	L63					
	L127					
	L191					
	L255					

■ T_{GTG_typ} is the total average time at rising time and falling time of gray to gray.

Note 2-6: Crosstalk measurement

Definition:

$$CT = \text{Max.} (CT_H, CT_V);$$

Where

a. Maximum Horizontal Crosstalk :

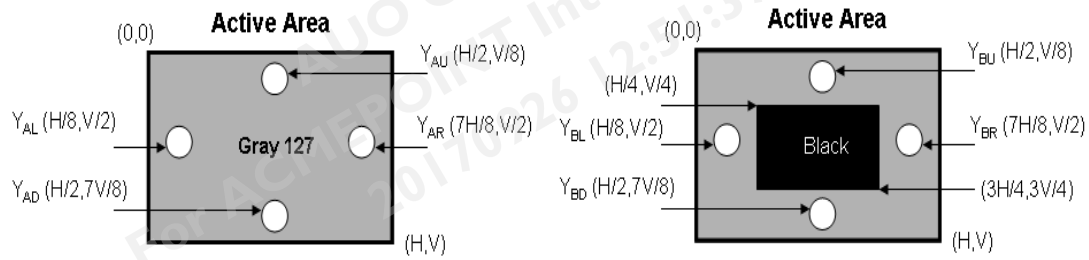
$$CT_H = \text{Max.} (|Y_{BL} - Y_{AL}| / Y_{AL} \times 100\%, |Y_{BR} - Y_{AR}| / Y_{AR} \times 100\%);$$

Maximum Vertical Crosstalk:

$$CT_V = \text{Max.} (|Y_{BU} - Y_{AU}| / Y_{AU} \times 100\%, |Y_{BD} - Y_{AD}| / Y_{AD} \times 100\%);$$

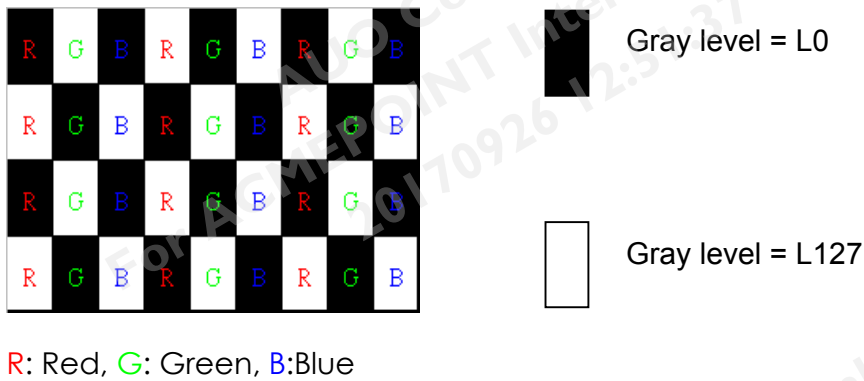
b. $Y_{AU}, Y_{AD}, Y_{AL}, Y_{AR}$ = Luminance of measured location without Black pattern

$Y_{BU}, Y_{BD}, Y_{BL}, Y_{BR}$ = Luminance of measured location with Black pattern



Note 2-7: Flicker measurement

a. Test pattern: It is listed as following.

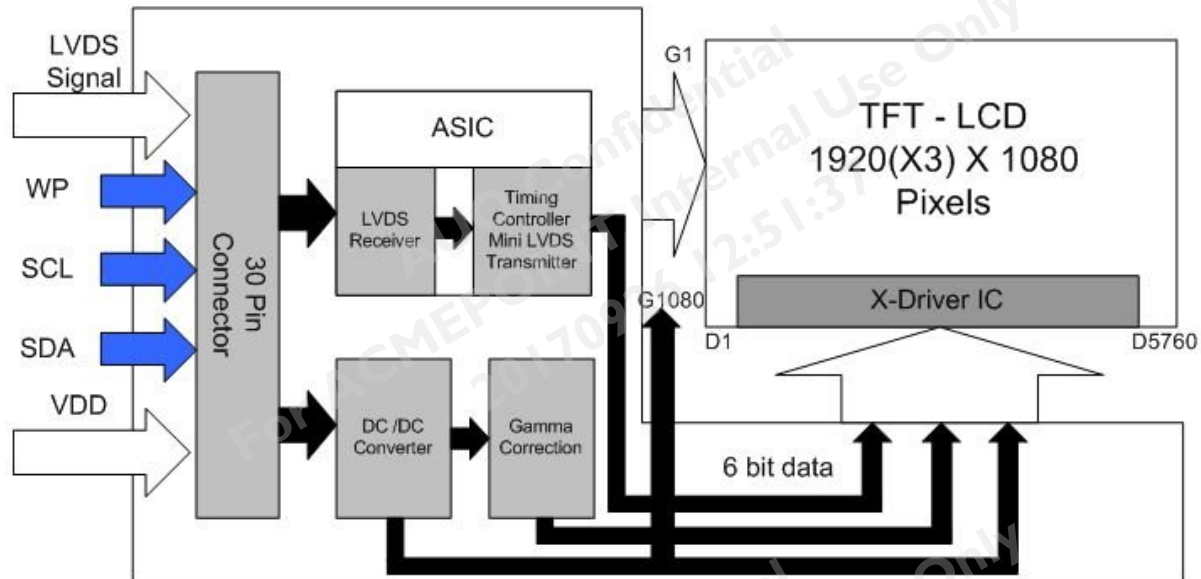


b. Measured position: Center of screen & perpendicular to the screen

3 TFT-LCD Module

3.1 Block Diagram

The following shows the block diagram of the 21.5 inch Color TFT-LCD Module.



3.2 Interface Connection

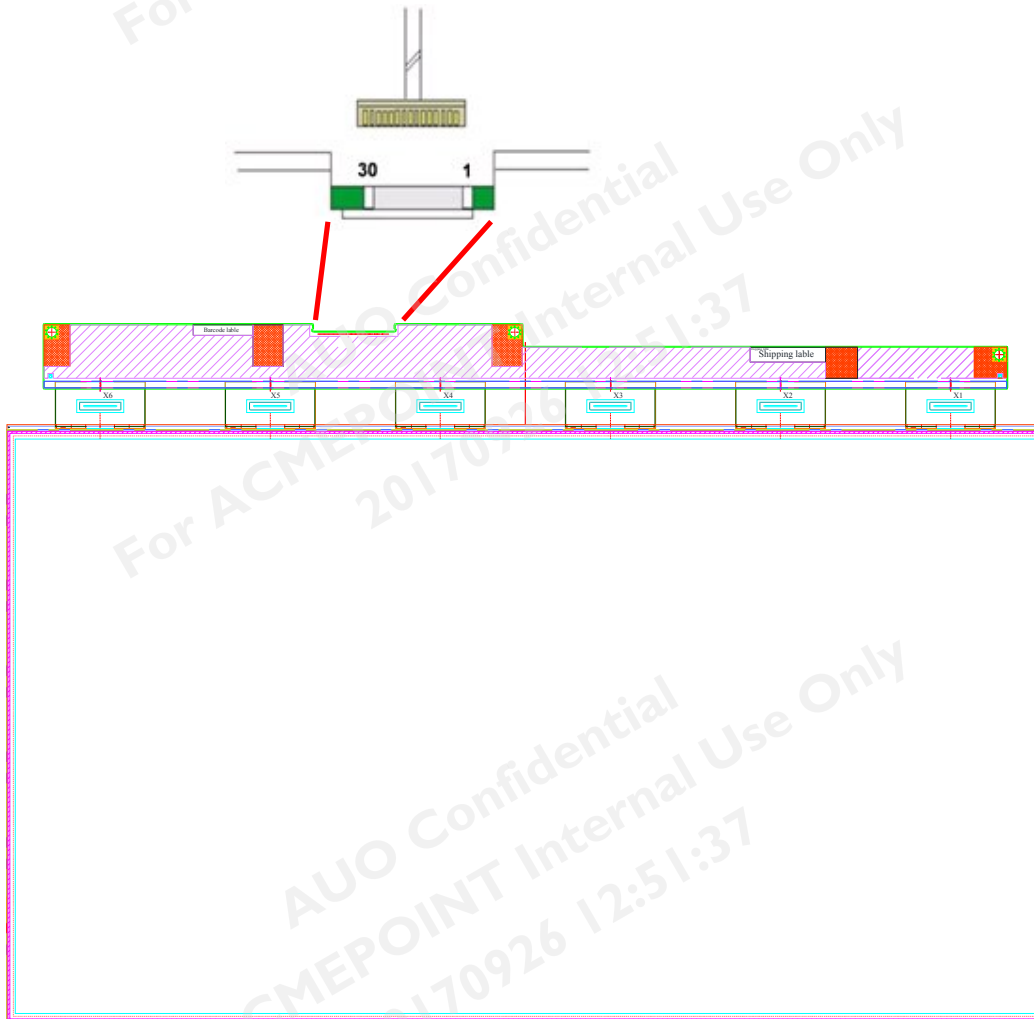
3.2.1 Connector Type

TFT-LCD Connector	Manufacturer	P-TWO	STM
	Part Number	187034-3009	MSBKT2407P30HB
Mating Connector	Manufacturer	JAE or Compatible	
	Part Number	FI-X30HL (Locked Type)	

3.2.2 Connector Pin Assignment

PIN #	Symbol	Description	Remark
1	RxO0-	Negative LVDS differential data input (Odd data)	
2	RxO0+	Positive LVDS differential data input (Odd data)	
3	RxO1-	Negative LVDS differential data input (Odd data)	
4	RxO1+	Positive LVDS differential data input (Odd data)	
5	RxO2-	Negative LVDS differential data input (Odd data)	
6	RxO2+	Positive LVDS differential data input (Odd data)	
7	GND	Ground	
8	RxOCLK-	Negative LVDS differential clock input (Odd clock)	
9	RxOCLK+	Positive LVDS differential clock input (Odd clock)	
10	RxO3-	Negative LVDS differential data input (Odd data)	
11	RxO3+	Positive LVDS differential data input (Odd data)	
12	RxE0-	Negative LVDS differential data input (Even data)	
13	RxE0+	Positive LVDS differential data input (Even data)	
14	GND	Ground	
15	RxE1-	Negative LVDS differential data input (Even data)	
16	RxE1+	Positive LVDS differential data input (Even data)	
17	GND	Ground	
18	RxE2-	Negative LVDS differential data input (Even data)	
19	RxE2+	Positive LVDS differential data input (Even data)	
20	RxECLK-	Negative LVDS differential clock input (Even clock)	
21	RxECLK+	Positive LVDS differential clock input (Even clock)	
22	RxE3-	Negative LVDS differential data input (Even data)	
23	RxE3+	Positive LVDS differential data input (Even data)	
24	WP	Digital-Vcom write protection	
25	NC	No connection (for AUO test only. Do not connect)	
26	SCL	I2C-Compatible Serial-Clock Input for Vcom	

27	SDA	I2C-Compatible Serial-Data Input / Output for	
28	VDD	Power Supply Input Voltage	
29	VDD	Power Supply Input Voltage	
30	VDD	Power Supply Input Voltage	



3.3 Electrical Characteristics

3.3.1 Absolute Maximum Rating

Permanent damage may occur if exceeding the following maximum rating.

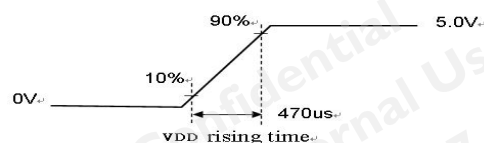
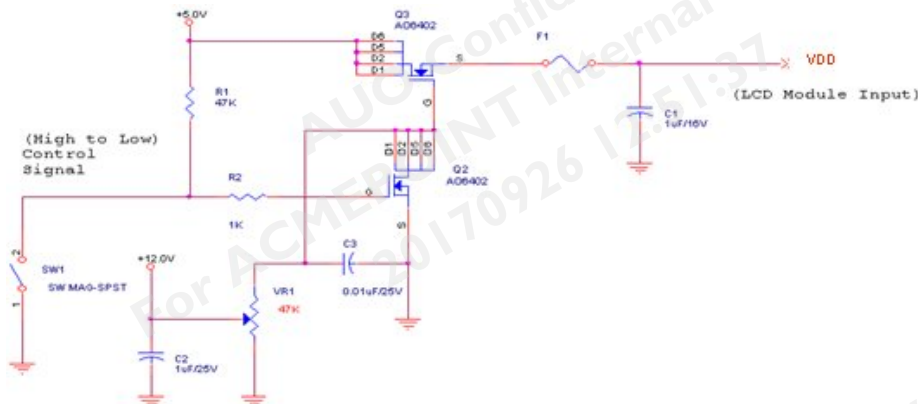
Symbol	Description	Min	Max	Unit	Remark
VDD	Power Supply Input Voltage	GND-0.3	6.0	[Volt]	Ta=25℃
SCL,SDA,WP	I2C input Voltage	GND-0.3	4.0	[Volt]	Ta=25℃

3.3.2 Recommended Operating Condition

Symbol	Description	Min	Typ	Max	Unit	Remark
VDD	Power supply Input voltage	4.5	5.0	5.5	[Volt]	
IDD	Power supply Input Current (RMS)	-	TBD	TBD	[A]	VDD= 5.0V, White Pattern, Fv=60Hz
			TBD	TBD	[A]	VDD= 5.0V, White Pattern , Fv=75Hz
PDD	VDD Power Consumption	-	TBD	TBD	[Watt]	VDD= 5.0V, White Pattern , Fv=60Hz
			TBD	TBD	[Watt]	VDD= 5.0V, White Pattern , Fv=75Hz
IRush	Inrush Current	-	-	3.0	[A]	Note 3-1
VDDrp	Allowable VDD Ripple Voltage	-	-	500	[mV]	VDD= 5.0V, White Pattern , Fv=75Hz

Note 3-1: Inrush Current measurement:

Test circuit:



The duration of VDD rising time: 470us.

3.3.3 Input control signal threshold voltage definition

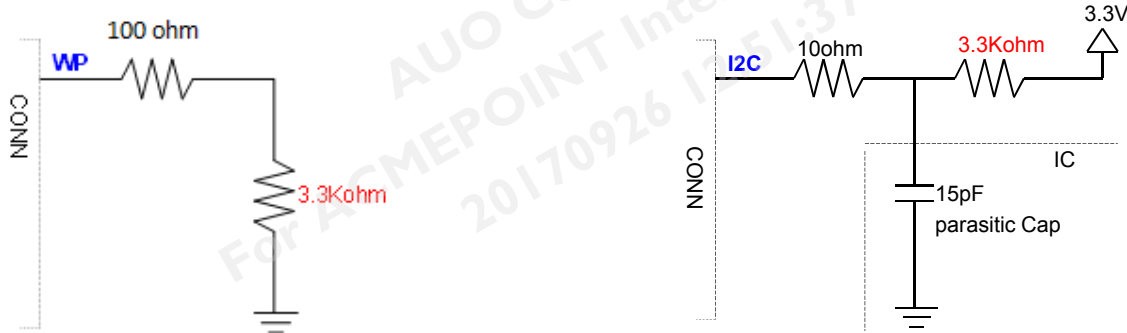
Item	Symbol	Min.	Typ.	Max.	Unit
Input High Threshold Voltage	V _{IH}	2.7	-	3.6	V
Input Low Threshold Voltage	V _{IL}	0	-	0.6	V

3.3.4 Write Protection mode selection

WP	Note
L or OPEN	Protection
H	Writable

3.3.5 Input equivalent impedance

1. Input equivalent impedance of WP pin 2. Input equivalent impedance of SDA/SCL pin

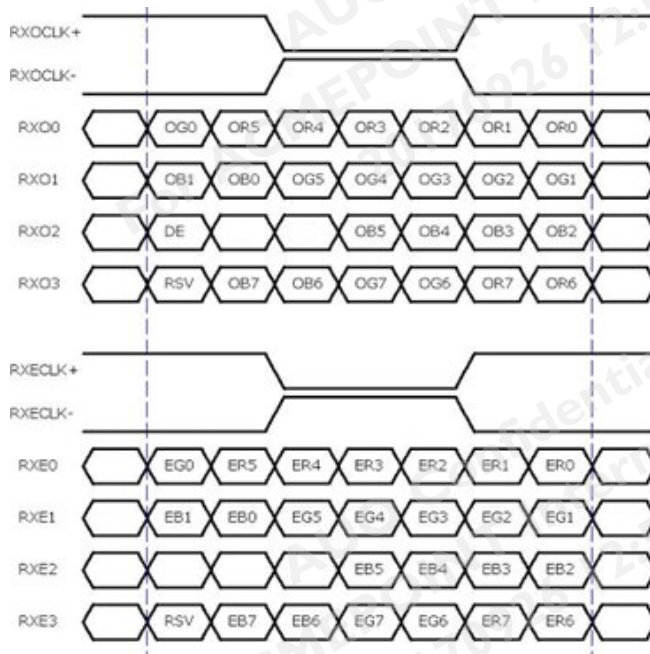


3.4 Signal Characteristics

3.4.1 LCD Pixel Format

	1			2															1919			1920			
1st Line	R	G	B	R	G	B	.	.	.	.	.	.	.	.	.	.	R	G	B	R	G	B	R	G	B
	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
1080 Line	R	G	B	R	G	B	.	.	.	.	.	.	.	.	.	.	R	G	B	R	G	B	R	G	B

3.4.2 LVDS Data Format



8 Bit Color Bit Order			
MSB	R7	G7	B7
	R6	G6	B6
	R5	G5	B5
	R4	G4	B4
	R3	G3	B3
	R2	G2	B2
	R1	G1	B1
LSB	R0	G0	B0

Note 3-2:

- O = "Odd Pixel Data" E = "Even Pixel Data"
- Refer to 3.4.1 LCD pixel format, the 1st data is 1 (Odd Pixel Data), the 2nd data is 2 (Even Pixel Data) and the last data is 1920 (Even Pixel Data).

3.4.3 Color versus Input Data

The following table is for color versus input data (8bit). The higher the gray level, the brighter the color.

Color	Gray Level	Color Input Data																										Remark
		RED data (MSB :R7, LSB :R0)								GREEN data (MSB :G7, LSB :G0)								BLUE data (MSB :B7, LSB :B0)										
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0			
Black	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
White	-	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1			
Gray 127	-	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1			
Red	L0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Black		
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:			
	L255	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
Green	L0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Black		
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:			
	L255	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0			
Blue	L0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Black		
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:			
	L255	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1			

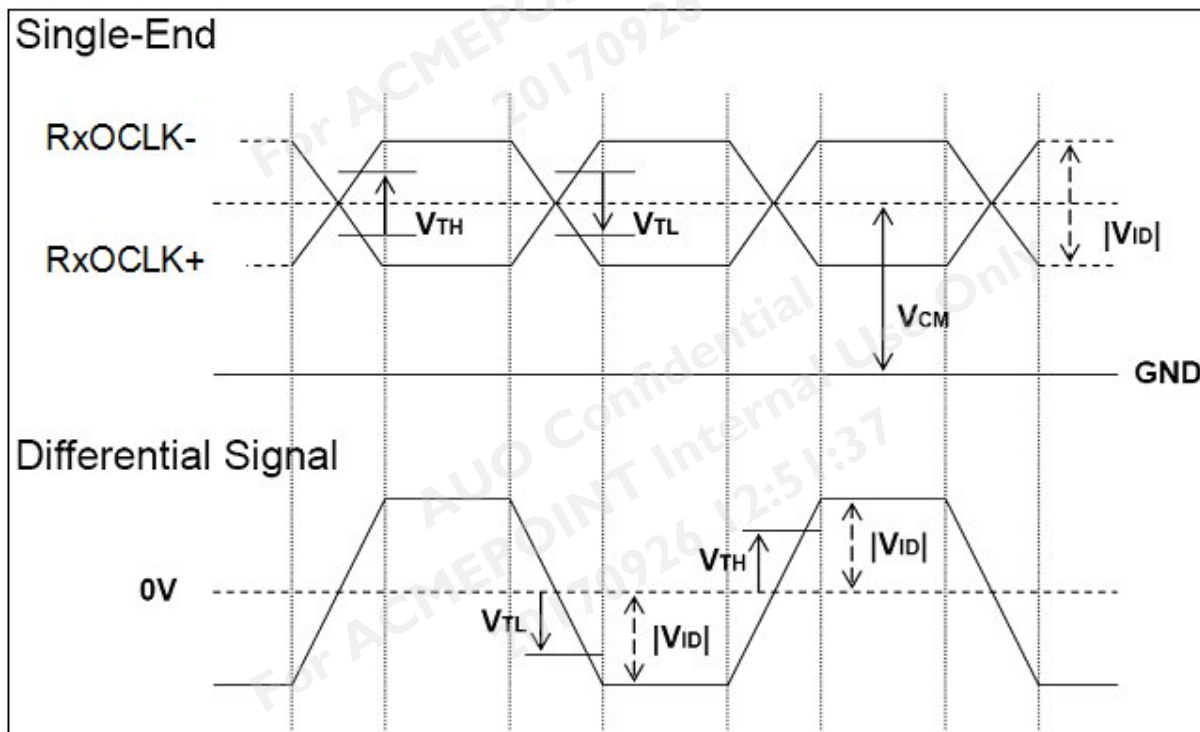
3.4.4 LVDS Specification

a. DC Characteristics:

Symbol	Description	Min	Typ	Max	Units	Condition
V_{TH}	LVDS Differential Input High Threshold	-	-	+100	[mV]	$V_{CM} = 1.2V$
V_{TL}	LVDS Differential Input Low Threshold	-100	-	-	[mV]	$V_{CM} = 1.2V$
$ V_{ID} $	LVDS Differential Input Voltage	100	-	600	[mV]	
V_{CM}	LVDS Common Mode Voltage	+1.0	+1.2	+1.5	[V]	$V_{TH} - V_{TL} = 200mV$

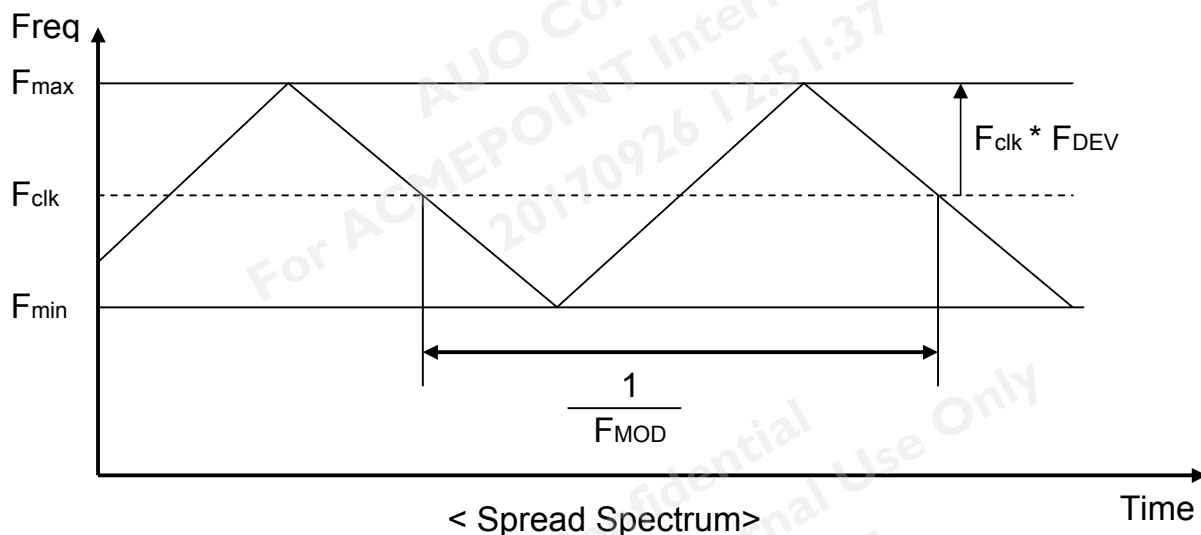
LVDS Signal Waveform:

Use RxOCLK- & RxOCLK+ as example.



b. AC Characteristics:

Symbol	Description	Min	Max	Unit	Remark
F_{DEV}	Maximum deviation of input clock frequency during Spread Spectrum	-	± 3	%	
F_{MOD}	Maximum modulation frequency of input clock during Spread Spectrum	-	200	KHz	



F_{clk} : LVDS Clock Frequency

3.4.5 Input Timing Specification

It only support DE mode, and the input timing are shown as the following table.

Symbol	Description		Min.	Typ.	Max.	Unit	Remark
Tv	Vertical Section	Period	1094	1130	3000	Th	
Tdisp (v)		Active	1080	1080	1080	Th	
Tblk (v)		Blanking	14	50	1920	Th	
Fv		Frequency	30	60	76	Hz	Note 3-3
Th	Horizontal Section	Period	1000	1050	1678	Tclk	
Tdisp (h)		Active	960	960	960	Tclk	
Tblk (h)		Blanking	40	90	718	Tclk	
Fh		Frequency	40.0	67.8	90.0	KHz	Note 3-4
Tclk	LVDS Clock	Period	11.2	14.0	25.0	ns	1/Fclk
Fclk		Frequency	40.0	71.2	90.0	MHz	Note 3-5

Note 3-3: The optimal Vertical Frequency is 50~76 Hz for best picture quality

Note 3-4: The equation is listed as following. Please don't exceed the above recommended value.

$$Fh (\text{Min.}) = Fclk (\text{Min.}) / Th (\text{Min.});$$

$$Fh (\text{Typ.}) = Fclk (\text{Typ.}) / Th (\text{Typ.});$$

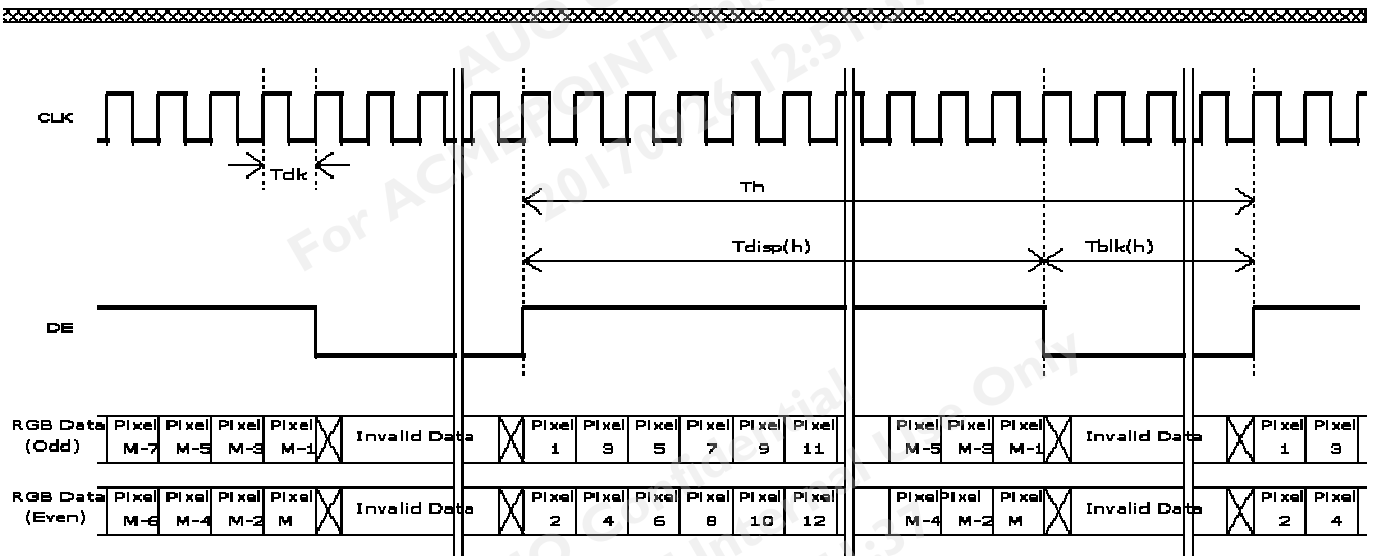
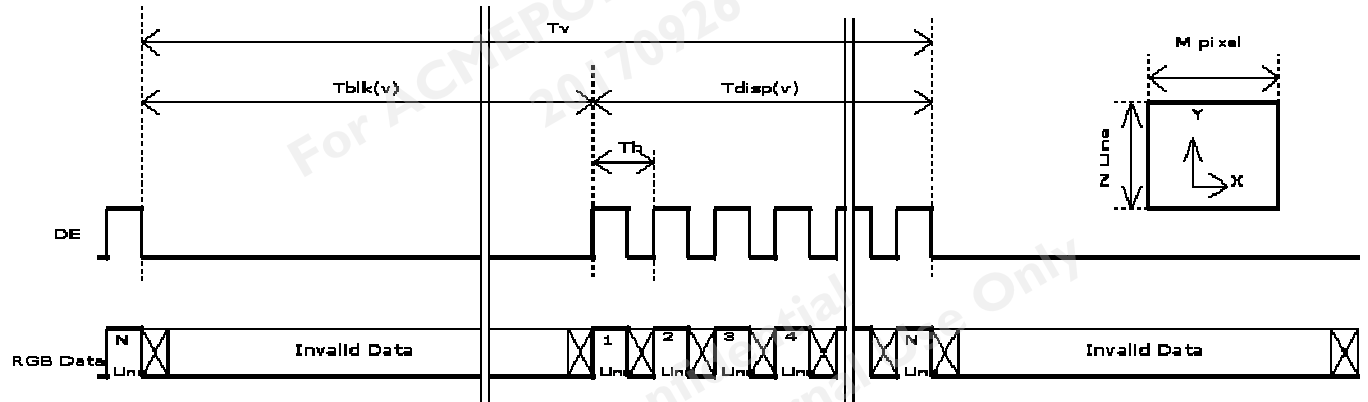
$$Fh (\text{Max.}) = Fclk (\text{Max.}) / Th (\text{Min.});$$

Note 3-5: The equation is listed as following. Please don't exceed the above recommended value.

$$Fclk (\text{Typ.}) = Fv (\text{Typ.}) \times Th (\text{Typ.}) \times Tv (\text{Typ.});$$

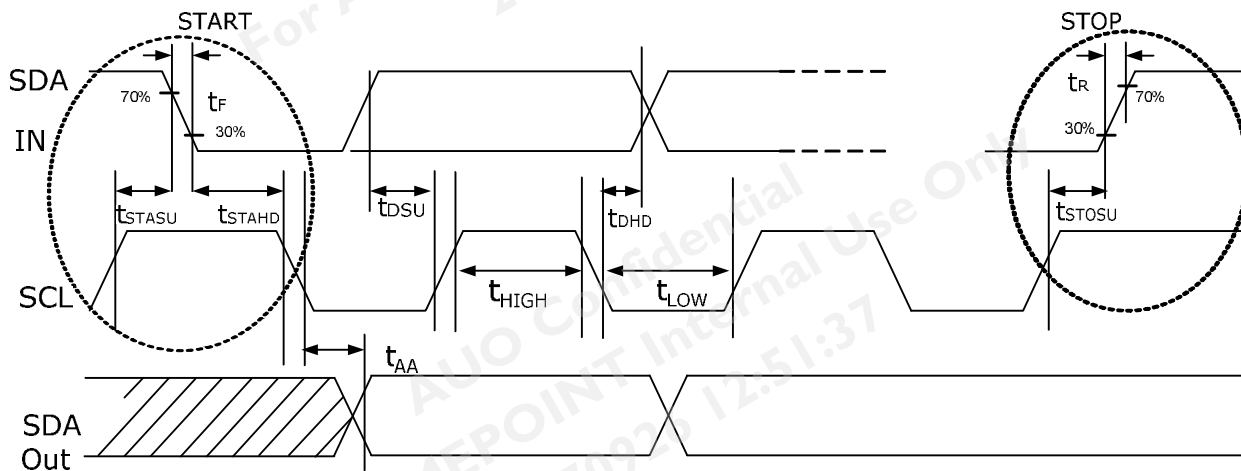
$$Fclk (\text{Max.}) = Fv (\text{Max.}) \times Th (\text{Typ.}) \times Tv (\text{Typ.});$$

3.4.6 Input Timing Diagram



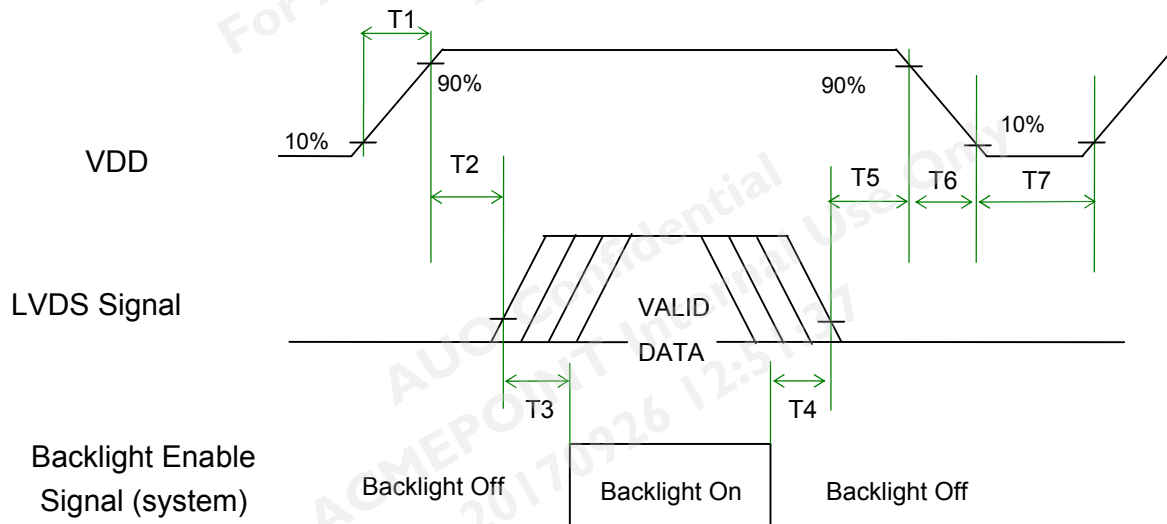
3.4.7 I2C Electrical Characteristics (VDD=5V, VSDA/VSCL=3.3V, TA=25°C)

	Parameter	Symbol	Min.	Typ.	Max	Unit
I2C	SCL clock frequency	fSCL	-	-	350	kHz
	Clock Pulse Width Low	tLOW	1.85	-	-	us
	Clock Pulse Width High	tHIGH	0.4	-	-	us
	Clock Low to Data Output Valid	tAA	1.76	-	-	us
	Start Setup Time	tSTASU	0.6	-	-	us
	Start Hold Time	tSTAHD	0.6	-	-	us
	Stop Setup Time	tSTOSU	0.6	-	-	us
	Data In Setup Time	tDSU	0.1	-	-	us
	Data In Hold Time	tDHD	0	-	-	us
	SCL/SDA Rise Time	tR	-	-	0.3	us
	SCL/SDA Fall Time	tF	-	-	0.3	us



3.5 Power ON/OFF Sequence

VDD power, LVDS signal and backlight on/off sequence are as following. LVDS signals from any system shall be Hi-Z state when VDD is off.



Power Sequence Timing

Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
T1	0.5	-	10	[ms]	
T2	0	-	50	[ms]	
T3	500	-	-	[ms]	
T4	100	-	-	[ms]	
T5	0	-	50	[ms]	Note 3-5 Note 3-6
T6	0	-	200		Note 3-6 Note 3-7
T7	1000	-	-	[ms]	

Note 3-5 : Recommend setting T5 = 0ms to avoid electronic noise when VDD is off.

Note 3-6 : During T5 and T6 period , please keep the level of input LVDS signals with Hi-Z state.

Note 3-7 : Voltage of VDD must decay smoothly after power-off. (customer system decide this value)

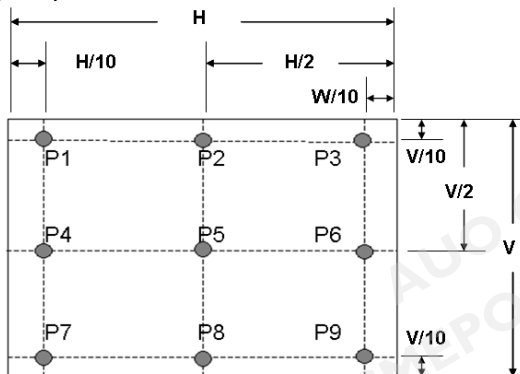
3.6 Vcom adjustment flow

A. Flicker Pattern

2L+1 (1V) L127

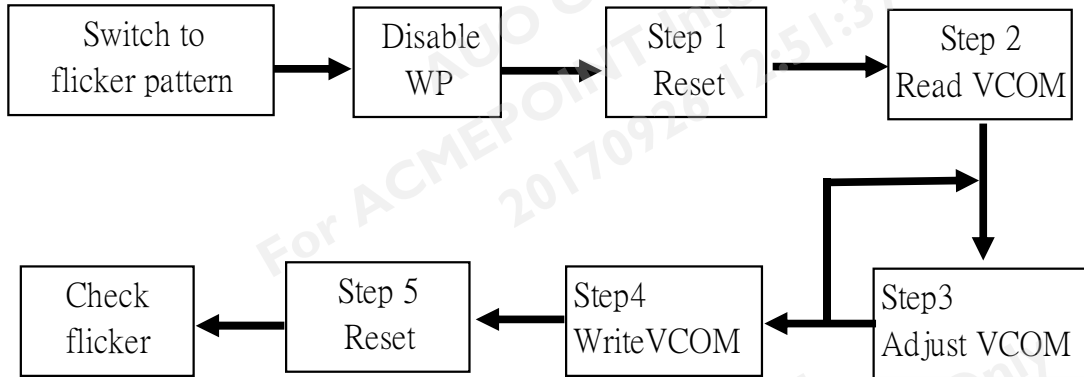


B. Vcom is optimization when minimized flicker phenomenon of location P5 (as below figure)



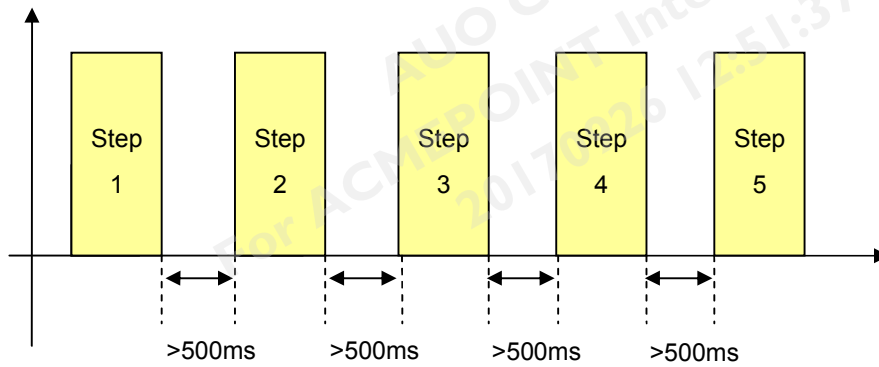
C. Tuning Step

VCOM I2C Tuning Step



D. Interval of Step to Step

VCOM I2C Tuning Step



E. I2C Protocol Define

DVCOM IC address (slave) : 1110100 (0x74)

Step1 Reset Command

Start	Slave Address							W R	ACK	Index Address 0								ACK	Control Byte								ACK	Stop		
	1	1	1	0	1	0	0	0		0	0	0	0	0	0	0	0		0	0	0	0	0	1	0	0			1	0
	0xE8							0x00								0x12														
	Device Address + W							Control Address								Reset + OUT_EN														

Step2 Read Vcom Command

Start	Slave Address							W	R	ACK	Index Address 0								ACK	Start	Slave Address							W	R	ACK	VCOM data						ACK	Stop
	1	1	1	0	1	0	0	0	0		0	0	0	0	0	1	1	1			1	0	1	0	0	1	X	X	X		X	X	X					
	0xE8							0x01										0xE9							0~127													
	Device Address + W							VCOM Address										Device Address + R							DATA													



Step3 Adjust Vcom Command

Start	Slave Address							W R	ACK	Index Address 1							ACK	VCOM data							ACK	Stop								
	1	1	1	0	1	0	0	0		0	0	0	0	0	0	0		0	0	0	0	0	0	X			X	X	X	X	X	X	N	A
	0xE8							0x01							0~127																			
	Device Address + W							VCOM Address							VCOM Value																			

Step4 Write Vcom Command

Start	Slave Address							W R	ACK	Index Address 0							ACK	Control Byte							ACK	Stop		
	1	1	1	0	1	0	0	0		0	0	0	0	0	0	0		0	0	0	0	0	1	0			1	0
	0xE8							0x00							0x0A													
	Device Address + W							Control Address							Write DAC to NVM													

Step5 Reset Command

Start	Slave Address							W R	ACK	Index Address 0							ACK	Control Byte							ACK	Stop		
	1	1	1	0	1	0	0	0		0	0	0	0	0	0	0		0	0	0	0	1	0	0			1	0
	0xE8							0x00							0x12													
	Device Address + W							Control Address							Reset + OUT_EN													



4 Reliability Test

AUO reliability test items are listed as following table. (Bare Panel only)

Items	Condition	Remark
Temperature Humidity Bias (THB)	Ta= 50□, 80%RH, 300hours	
High Temperature Operation (HTO)	Ta= 50□, 50%RH, 300hours	
Low Temperature Operation (LTO)	Ta= 0□, 300hours	
High Temperature Storage (HTS)	Ta= 60□, 300hours	
Low Temperature Storage (LTS)	Ta= -20□, 300hours	
Thermal Shock Test (TST)	-20□/30min, 60□/30min, 100 cycles	Note 4-1

Note 4-1: a. A cycle of rapid temperature change consists of varying the temperature from -20□ to 60□, and back again. Power is not applied during the test.
b. After finish temperature cycling, the unit is placed in normal room ambient for at least 4 hours before power on.



5 Shipping Label

5.1 Small Shipping Label

The label is on the PCBA as shown below :



5.2 Run Card Label

The label is on the panel as shown below :

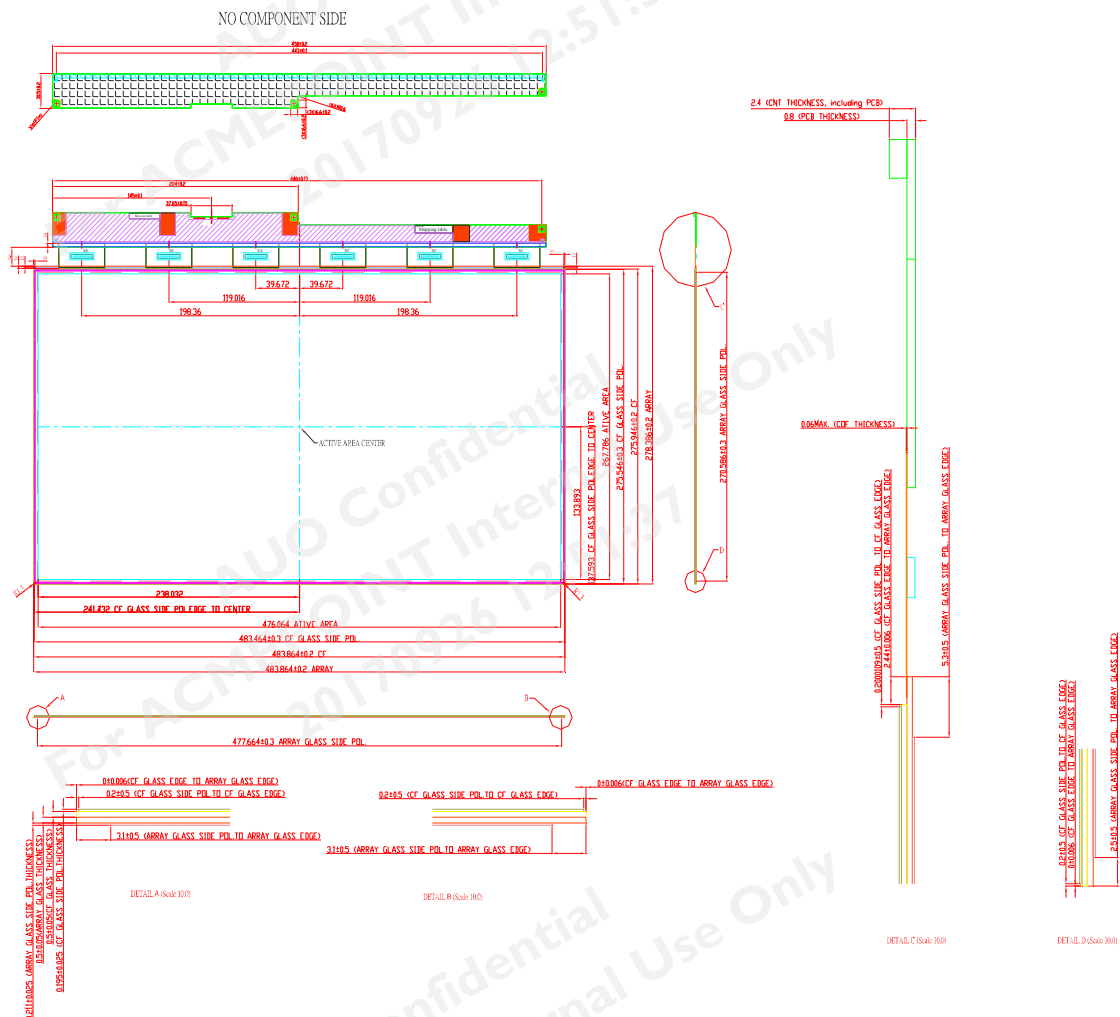
T215HVN05-x/xx		xx:xxxxxxxxxx	Remark : X	
0				SKD
S/N	xxxxxxxxxxxx (xxxxx)		Z	P N V
XXXXX	XXXXX	XXXXX		
XXXXX	XXXXX	XXXXX		
XXXXX	XXXXX	XXXXX		
XXXXX	XXXXX	XXXXX		



Product Specification

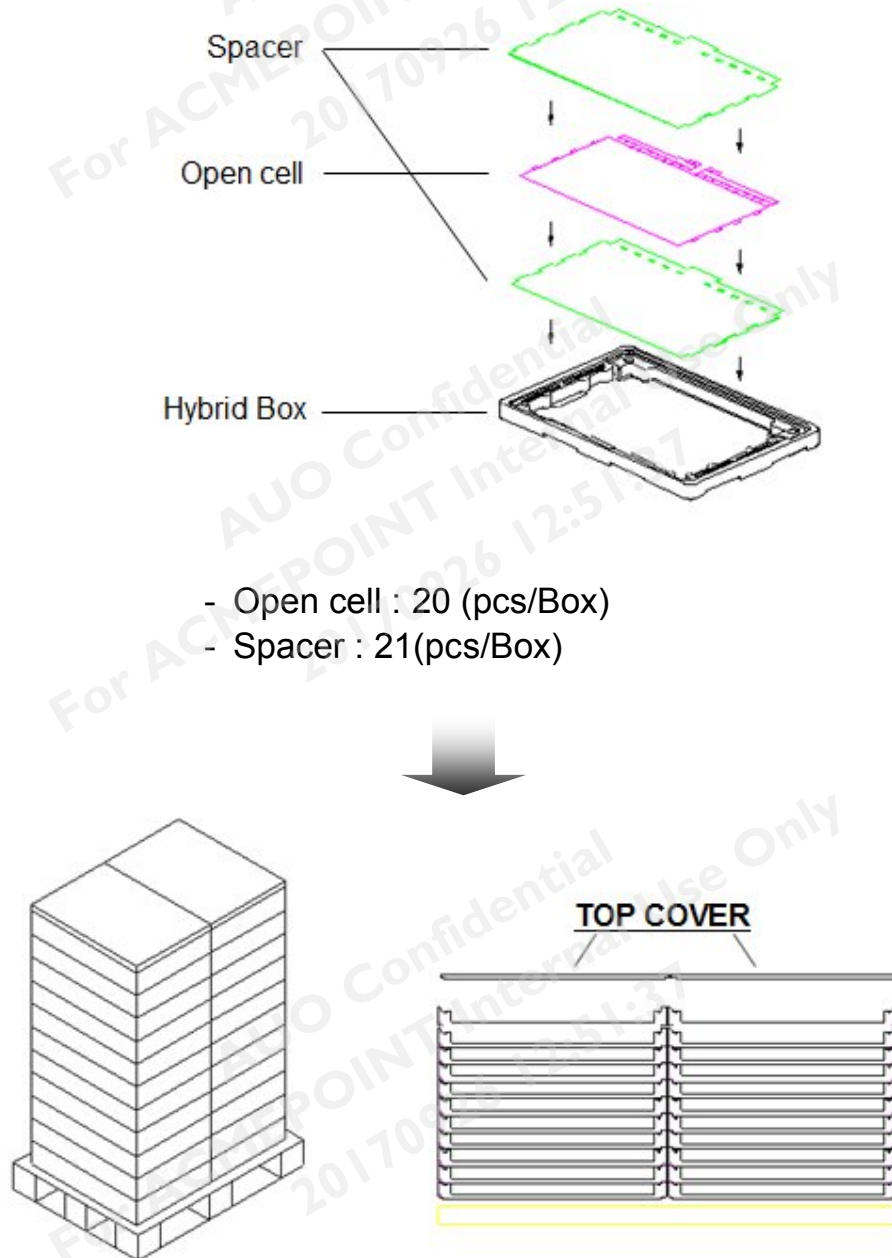
AU OPTRONICS CORPORATION

T215HVN05.1



7 Packing Specification

7.1 Packing Flow





7.2 Pallet and Shipment information

Item	Specification			Remark
	Q'ty	Dimension	Weight(kg)	
Box	1	700(L)mm x 455(W)mm x 127.5(H)mm	0.7	without cell & spacer
Packing Box	20 pcs/Box	700(L)mm x 455(W)mm x 127.5(H)mm	10.1	with cell & cushion & spacer
Pallet	1	980(L)mm x 740(W)mm x 132(H)mm	12.0	
Pallet after Packing	20 boxes/pallet	980(L)mm x 740(W)mm x 132(H)mm	214.6	