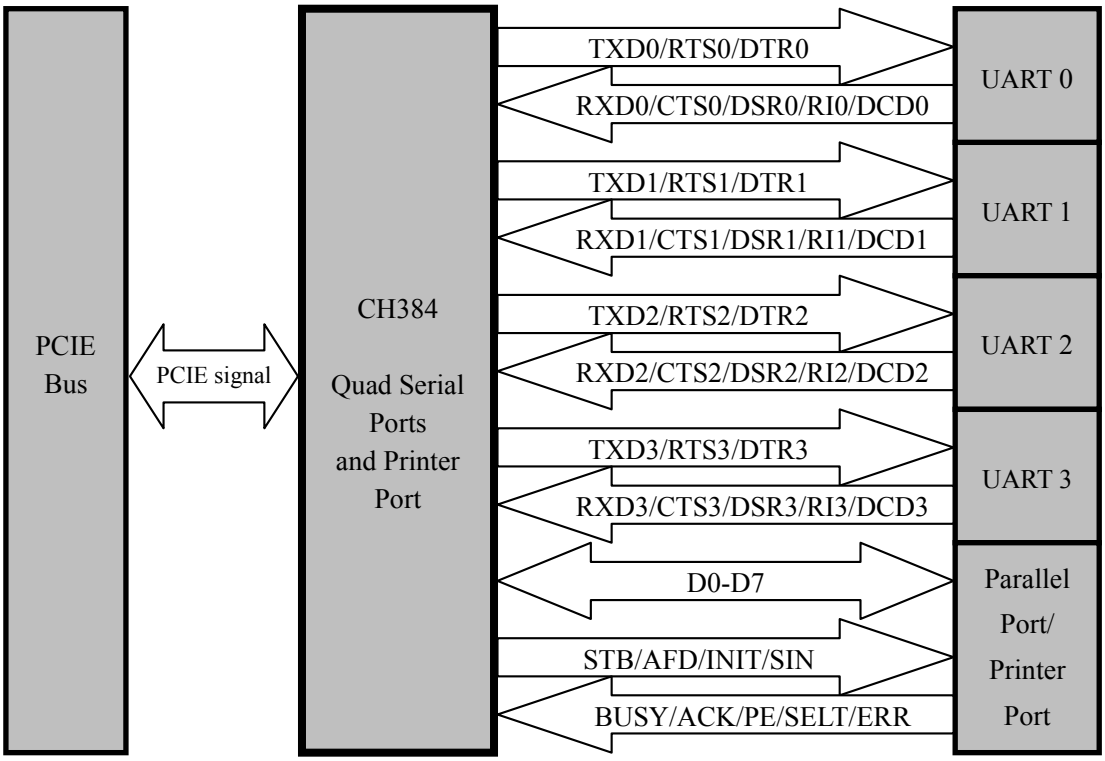
PCIE to Quad Serial Ports and Printer Port Chip CH384

Datasheet (I)
Version: 1
http://wch.cn

1. Introduction

CH384 is a PCI-Express bus converter chip, which converts PCIE bus to Quad serial ports and printer port, including four asynchronous serial ports compatible with 16C550 or 16C750, and one EPP/ECP enhanced bidirectional parallel port.CH438 chip can be added to extend 24 serial ports to the maximum. The asynchronous serial port provides a transceiver with independent 256-byte FIFO buffer, supports IrDA infrared encoding and decoding, supports communication baud rate up to 8Mbps and can be used for RS232 serial port expansion of PCIE bus, PCIE high-speed serial port with automatic hardware flow control, serial ports networking, RS485 communication, IrDA communication, parallel/printer port expansion, etc.

The figure below shows its general application block diagram.



2. Features

2.1. Overview

- The same chip can be configured as a four-channel serial ports and a parallel port/printer port or four-channel serial ports and extended multiple serial ports of PCIE Bus.
- Provides two-wire serial host interface, and EEPROM device similar to 24C0X which can be connected to store non-volatile data.
- The device identification (Vendor ID, Device ID, Class Code, etc.) of the PCIE board can be set in the EEPROM device.
- Drivers support Windows 98/ME/NT4.0/2000/XP/Vista/7/8/8.1/10/SERVER 2003/2008/2012/2016/2019and Linux.
- 3.3V power supply, I/O pins supports 5V withstand voltage, serial ports support low-power sleep

mode.

- The chip function is equivalent to CH367 with CH438, provide such application solutions as 8 serial ports, 16 serial ports and 28 serial ports.

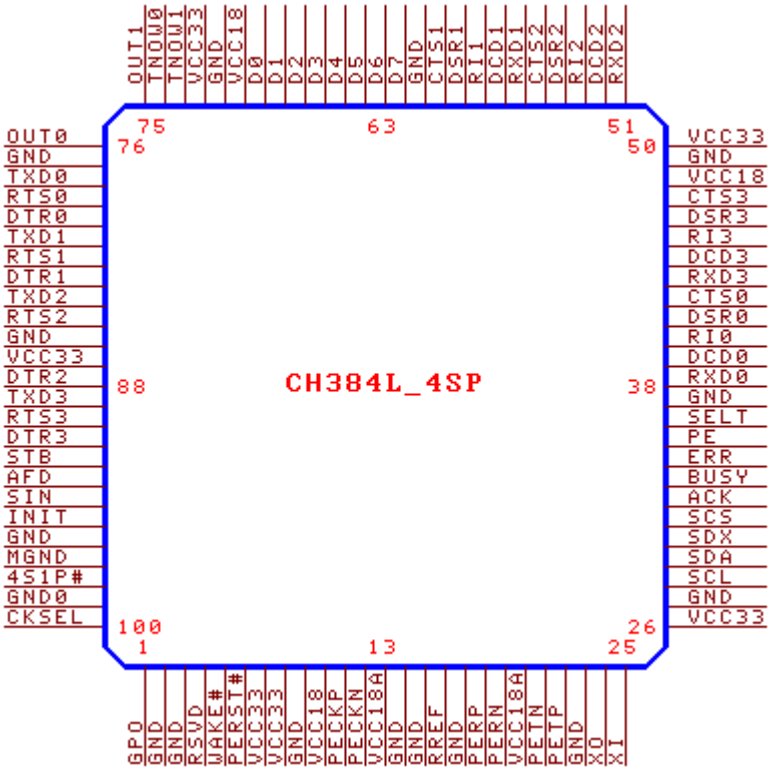
2.2. Serial Port

- 4 fully independent asynchronous serial ports, compatible with 16C550, 16C552, 16C554 and 16C750 and enhanced.
- Supports 5, 6, 7 or 8 data bits and 1 or 2 stop bits.
- Supports odd, even, mark, space and no parity. .
- Programmable communication baud rate, supports communication baud rate of 115200bps and up to 8Mbps.
- Internal 256-byte FIFO buffer, supports four FIFO trigger levels.
- Supports MODEM interface signals CTS, DSR, RI, DCD, DTR and RTS, which can be converted to RS232 signals.
- Supports automatic handshake and automatic transmission rate control of hardware flow control signals CTS and RTS, compatible with TL16C550C.
- Supports serial port frame error detection and Break line interval detection.
- Supports full-duplex and half-duplex UART communication.
- Internal SIR infrared codec of serial port 0, supports IrDA infrared communication with baud rate from 2400bps to 115200bps.
- Supports to connect to external CH438 chips to expand another 8 to 24 asynchronous serial ports to realize 8 to 28 serial ports of PCIE.

2.3. Parallel Port

- Supports SPP, Nibble, Byte, PS/2, EPP, ECP and other IEEE1284 parallel port/printer port working modes.
- Supports bidirectional-data transmission and a transmission speed of up to 1M byte/s.

3. Package



Referring to Datasheet (II) CH384DS2.PDF for the application instructions and pins diagram of quad UARTs + extended multiple serial ports.

Package	Width of Plastic	Pitch of Pin		Instruction of Package	Ordering Information
LQFP-100	14mm x 14mm	0.5mm	19.7mil	Standard LQFP 100 patch	CH384L

4. Pins

4.1. Power Line

Pin No.	Pin Name	Type	Pin Description
7, 8, 26, 50, 72, 87	VCC33	Power	3.3V I/O power
10, 48, 70	VCC18	Power	1.8V core power
13, 20	VCC18A	Power	1.8V transmission power
97, 2, 3, 9, 14, 15, 17, 23, 27, 37, 49, 61, 71, 77, 86, 96, 99	GND	Power	Ground

4.2. PCIE Bus Signal Line

Pin No.	Pin Name	Type	Pin Description
6	PERST#	Input	System reset signal lines, active low
11, 12	PECKP/PECKN	Input	Differentia input of system reference clock
18, 19	PERP/PERN	PCIE input	Differential signal input of PCIE receiver
22, 21	PETP/PETN	PCIE output	Differential signal output of PCIE transmitter
5	WAKE#	Open-drain output	Bus wake-up output, active low, not connected if not used

4.3. UART 0~3 Signal Lines

Pin No.	Pin Name	Type	Pin Description
42/60 55/47	CTS0/CTS1 CTS2/CTS3	Input	MODEM signal, clear to send, active low, built-in pull-up resistor
41/59 54/46	DSR0/DSR1 DSR2/DSR3	Input	MODEM signal, data send ready, active low, built-in pull-up resistor
40/58 53/45	RI0/RI1 RI2/RI3	Input	MODEM signal, ring indicator, active low, built-in pull-up resistor
39/57 52/44	DCD0/DCD1 DCD2/DCD3	Input	MODEM signal, data carrier detect, active low, built-in pull-up resistor
38/56 51/43	RXD0/RXD1 RXD2/RXD3	Input	Received data, built-in pull-up resistor
80/83 88/91	DTR0/DTR1 DTR2/DTR3	Output	MODEM signal, data terminal ready, active low
79/82 85/90	RTS0/RTS1 RTS2/RTS3	Output	MODEM signal, request to send, active low
78/81 84/89	TXD0/TXD1 TXD2/TXD3	Output	Transmitted data
76/75	OUT0/OUT1	Output	MODEM control output signal (OUT1 of MCR), active low

74/73	TNOW0/TNOW1	Output	Serial port sending status output (half duplex receive-transmit switching), active high

4.4. Printer Port Signal line

Pin No.	Pin Name	Type	Pin Description
62-69	D7～D0	Tri-status and bi-direction	8-bit parallel data output and input, built-in pull-up , connect to DATA7～DATA0
92	STB	Output	Read strobe output, active low, connect to STROBE
93	AFD	Output	Automatic line feed output, active low, connect to AUTO-FEED
95	INIT	Output	Initiate printer, active low, connect to INIT
94	SIN	Output	Select printer, active low, connect to SELECT-IN
34	ERR	Input	Printer error, active low, built-in pull-up, connect to ERROR or FAULT
36	SELT	Input	Printer online, active high, built-in pull-up, connect to SELECT or SELT
35	PE	Input	Printer paper empty, active high, built-in pull-up, connect to PEMPTY or PERROR
32	ACK	Input	Printer data receives response, active at the rising edge, built-in pull-up, connect to ACK
33	BUSY	Input	Printer busy, active high, built-in pull-up, connect to BUSY

4.5. Auxiliary Signal line

Pin No.	Pin Name	Type	Pin Description
16	RREF	Input	System reference current input; connect a external 12KΩ resistor to GND
25	XI	Input	Optional, input of crystal oscillator, connect to crystal and oscillation capacitor externally
24	XO	Input/ Output	Optional, inverted output of crystal oscillator, connect to crystal and oscillation capacitor externally
28	SCL	Output	General output, clock output of external configuration chip, connect to the SCL pin of the serial EEPROM configuration chip 24CXX externally
29	SDA	Open-drain output and input	General output and input, built-in pull-up resistor, connect to the SDA pin of the serial EEPROM configuration chip 24CXX externally
30	SDX	Tri-status and bi-direction	General output and input, built-in pull-up resistor
31	SCS	Input	General output
100	CKSEL	Input	Input of serial port clock frequency selection, built-in pull-up resistor
98	4S1P#	Input	Input of software identification mode selection, built-in pull-up resistor
1	GPO	Output	General output
4	RSVD	Reserved	Reserved, not connection

5. Configuration

5.1. Global Function Configuration

CH384 has two main hardware function modes: 4 serial ports and parallel port function mode, 4 serial ports and extended multiple serial ports function mode. The pin definitions are different in two function modes, and this manual only covers the former. Please refer to Datasheet (II) CH384DS2.PDF for the latter.

4S1P# pin of CH384 is used to select the software recognition mode:

4S1P# is connected to VCC33 or suspended, that is, when 4S1P#=1, it is 4 serial ports mode (parallel port/printer port is not used);

4S1P# is connected to GND, that is, when 4S1P#=0, it is 4 serial ports and printer port mode.

CKSEL pin of CH384 is used to select the clock frequency of the internal 4 serial ports:

CKSEL is connected to VCC33 or suspended, i.e. when CKSEL=1, the clock is input from XO pin, the frequency is determined by the external crystal, and the internal frequency coefficient is 1/12 frequency division by default, and frequency doubling can be selected through CK2X or CKnS;

CKSEL is connected to GND, that is, when CKSEL=0, the clock is input from XO pin. The frequency is determined by the external crystal, and the internal frequency coefficient is always forced to be frequency doubling;

CKSEL is connected to PERST# pin, that is, when CKSEL=R, the internal crystal oscillator is disabled, the internal PLL provides the clock with a frequency of 125MHz, and the internal frequency coefficient is 1/68 frequency division by default, and supported to select no frequency division through CK2X or CKnS.

5.2. External Configuration Chip

CH384 will check the data in the external 24CXX configuration chip after each power-on or PCIE Bus reset. If the configuration chip is connected and the data is valid, it will be automatically loaded into CH384 to replace the default PCIE identification information.

The configuration chip 24CXX is a 4-pin or 8-pin packaged non-volatile serial EEPROM memory. In addition to providing configuration information to CH384, it also can self-save some other parameters for application. CH384 supports the following types of 24CXX chips: 24C01 (A), 24C02, 24C04, 24C08, 24C16, etc.

The following table shows the data definition in the configuration chip 24CXX.

Byte address	Abbreviation	Description of Chip Configuration Data Area	Default
00H	CFG	The valid flag of the external configuration chip, must be 54H	54H
01H	FREQ	Bit 3 to bit 0are respectively used to select the internal frequency coefficient of serial port 3 to port 0	0FFH
03H-02H	RSVD	(Reserved)	0000H
05H-04H	VID	Vendor ID	Customize
07H-06H	DID	Device ID	Customize
08H	RID	Chip version: Revision ID	Customize
0BH-09H	CLS	Device type code: Class Code	070005H
0DH-0CH	SVID	Subsystem Vendor ID	Customize
0FH-0EH	SID	Subsystem ID	Customize
1FH-10H	RSVD	(Reserved)	00H or FFH
Other address	APP	User or application program custom unit	

5.3. Internal Clock of Serial Port

There is a clock oscillator inside CH384, the required external clock signal for the serial port can generate by connecting the external crystal and capacitor. If crystals and capacitors are not connected, connecting CKSEL pin to PERST# pins, the required clock for the serial port can generated by the internal PLL.

In CH384, the external clock signal of XI pin performs frequency division or frequency doubling to generate the internal standard clock of serial port respectively. To be compatible with the 16C550 of the existing computer serial ports, the default internal clock frequency is 1.8432MHz, and the corresponding maximum baud rate of serial port is 115200bps. CH384 supports many internal clock frequencies. When the internal clock frequency is doubled, if the software is unchanged, the actual communication baud rate will be also doubled, namely, the serial port is set to 115200bps by the software, actually, it is 230400bps.

The serial UART of CH384 selects the frequency division or frequency doubling coefficient by the SCL pin or the CFG/FREQ flag bit in the external configuration chip. The frequency of the external clock is converted to two internal clock frequencies, thereby supporting more and larger serial baud rates. The table below shows the internal clock frequency and maximum baud rate of the serial port which is generated by the CKSEL pin, CFG/FREQ flag bit and external crystal frequency. CK2X in the table is the bit 5 of IER register for each serial port; CFG in the table is the effective flag of the external configuration chip, and CKnS (namely CK0S-CK3S) are bits 0~3 of FREQ respectively.

Prerequisite Condition	CKSEL=1	CKSEL=1	CKSEL=R	CKSEL=R
Combination selection	CK2X=0 and CFG invalid or CKnS=1	CK2X=1 or CKSEL=0 or CFG valid or CKnS=0	CK2X=0 and CFG invalid or CKnS=1	CK2X=1 or CFG valid or CKnS=0
Internal frequency coefficient	1/12 frequency division	2 frequency doubling	1/68 frequency division	No frequency division
External crystal frequency 22.1184MHz	1.8432MHz 115.2Kbps	44.2368MHz 2.7648Mbps		
External crystal frequency 0.9216MHz		1.8432MHz 115.2Kbps		
External crystal frequency 11.0592MHz	0.9216MHz 57.6Kbps	22.1184MHz 1.3844Mbps		
External crystal frequency 18.432MHz		36.864MHz 2.304Mbps		
Internal PLL frequency 125MHz			1.8384MHz 114.9Kbps	125MHz 7.8125Mbps

The difference between 114.9Kbps obtained under the internal PLL mode with 1/68 frequency division and the standard 115.2Kbps is only 0.27%, which is acceptable.

6. Registers

6.1. Basic Specification

6.1.1. Abbreviation of Attribute: R=read-only, W=read and write, S=read-only but can be set in advance,…=ellipsis.
6.1.2. Numerical system of data: If it ends with H which is a hexadecimal number. Otherwise, it is a binary number.
6.1.3. Wildcard character and attribute of numeric value: r=reserved (disabled), x=any value,…=ellipsis.

6.2. PCIE Configuration Space

Address	Register Name	Register Attribute	Default Value After System Reset
01H-00H	Vendor ID	SSSS	1C00H
03H-02H	Device ID	SSSS	4 UARTs: 3470H 4 UARTs + parallel port: 3450H 4 UARTs extended to 8 UARTs: 3853H 4 UARTs extended to 28 UARTs: 4353H
05H-04H	Command	RRRRRWRRRRRRRWWW	0000000000000000
07H-06H	Status	RRRRRRRRRRRRRRR	000000000001x000
08H	Revision ID	SS	10H
0BH-09H	Class Code	SSSSSS	070005H
0FH-0CH		RRRRRRRR	00000000H
13H-10H	I/O Base Address 0	WWWWWWWWWWWWWWW WWWWWWWWRRRRRRRR	0000000000000000 0000000000000001
17H-14H		RRRRRRRR	00000008H
1BH-18H	I/O Base Address 2	WWWWWWWWWWWWWWW WWWWWWWWWWWWWRR	0000000000000000 0000000000000001
2BH-1CH		RRRR….RRRR	0000….0000H
2DH-2CH	Subsystem Vendor ID	SSSS	Same as VID
2FH-2EH	Subsystem ID	SSSS	Same as DID
33H-30H		RRRRRRRR	00000001H
34H		RR	60H
3BH-35H		RRRR….RRRR	0000….0000H
3FH-3CH	Interrupt Line & Pin	RRRRRRRRRRRRRRR RRRRRRRRWWWWWWW	0000000000000000 0000000100000000
FFFH-40H	Reserved	(Disabled)	(Disabled)

6.3. I/O Base Address 0 Register

Offset Address	Register Name	Register Attribute	Default Value After System Reset
3FH-00H	Mapped to the externally extended 8 serial registers of 0# CH438 (8*8 bytes)	WW	0FFH
7FH-40H	Mapped to the externally extended 8 serial registers of 1# CH438 (8*8 bytes)	WW	0FFH
BFH-80H	Mapped to the externally extended 8 serial registers of 2# CH438 (8*8 bytes)	WW	0FFH
C7H-C0H	8 serial registers of internal UART 0	WW	XXH
CFH-C8H	8 serial registers of internal UART 1	WW	XXH

D7H-D0H	8 serial registers of internal UART 2	WW	XXH
DFH-D8H	8 serial registers of internal UART 3	WW	XXH
E0H	Mapped to the externally extended interrupt special status register of 0# CH438	RR	00H
E3H-E1H	Reserved	(Disabled)	0FFH
E4H	Mapped to the externally extended interrupt special status register of 1# CH438	RR	00H
E5H	Reserved	(Disabled)	0FFH
E6H	Mapped to the externally extended interrupt special status register of 2# CH438	RR	00H
E7H	Reserved	(Disabled)	0FFH
E8H	General purpose output register GPOR	WWRRRWWW	00rrr111
E9H	Internal interrupt status register IINT	RRRRRRRR	0rrr0000
EAH	General purpose input register GPIR	RRRRRRRR	1xxr1rr1
EBH	External interrupt status register XINT	RRRRRRWR	111rrr0r
F7H-ECH	Reserved	(Disabled)	xxH
F8H	Control and status register CTRL	WRRRRRRR	1rrxrrrr
FFH-F9H	Reserved	(Disabled)	xxH

6.4. Register Bit

Register Name	Address	Attribute	Instruction For Use Of Bit (Default Value)	Value=0	Value=1
General purpose output register (GPOR) (I/O base address 0 + 0E8H address)	Bit 0	W	Set output value of SDA pin(1)	Low	High
	Bit 1	W	Set output value of SCL pin(1)	Low	High
	Bit 2	W	Set output value of SCL pin(1)	Low	High
	Bit 6	W	Set data direction of SDX pin(0)	Input	Output
	Bit 7	W	Set output value of SDX pin(0)	Low	High
Internal interrupt status register IINT (I/O base address 0 + 0E9H address)	Bit 0	R	Interrupt status of internal UART 0(0)	No interrupt	interrupting
	Bit 1	R	Interrupt status of internal UART 1(0)	No interrupt	interrupting
	Bit 2	R	Interrupt status of internal UART 2(0)	No interrupt	interrupting
	Bit 3	R	Interrupt status of internal UART 3(0)	No interrupt	interrupting
	Bit 7	R	Interrupt status of internal printer port(0)	No interrupt	interrupting
General purpose input register (GPIR) (I/O base address 0 + 0EAH address)	Bit 0	R	Input status of SDA pin(1)	Low	High
	Bit 3	R	Input status of INT# pin(1)	Low	High
	Bit 5	R	Input status of CKSEL pin(X)	Low	High
	Bit 6	R	Input status of MDSEL pin(X)	Low	High
	Bit 7	R	Input status of SDX pin(1)	Low	High
External interrupt status register XINT (I/O base address 0 + 0EBH address)	Bit 1	W	Set global interrupt enabling (0)	Disable interrupt	Enable interrupt
	Bit 5	R	Input status of INT0# pin(1)	Low	High
	Bit 6	R	Input status of INT1# pin(1)	Low	High
	Bit 7	R	Input status of INT2# pin(1)	Low	High

Control and status register CTRL (I/O base address 0 + 0F8H address)	Bit 4	R	Input status of XO pin(X)	Low	High
	Bit 7	W	Set output value of GPO pin(1)	Low	High

6.5. Serial UART Register

The serial UART of CH384 is compatible with the industry standard 16550 or 16C750 with enhanced. The register bit marked in gray in the table is the enhanced function, and the length of FIFO buffer is extended to 256 bytes, other registers refer to the description of the single serial port 16C550 or dual UARTs CH432 or octal UARTs CH438. The actual address of the UART 0 register is the I/O base address 0 add 0C0H adds the offset address in the table, the actual address of the UART 1 register is the I/O base address 0 adds 0C8H adds the offset address in the table, the actual address of the UART 2 register is the I/O base address 0 adds 0D0H adds the offset address in the table, and the actual address of the UART 3 register is the I/O base address 0 adds 0D8H adds the offset address in the table. The registers of all serial UART are the same. In the table, DLAB is bit 7 of the register LCR, X indicates that the value of DLAB is not concerned, RO indicates that the register is read-only, WO indicates that the register is write-only, and R/W indicates that the register is readable and writable.

Address	DLAB	R/W	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	RO	RBR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	WO	THR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	0	R/W	IER	RESET	LOWPOWER	CK2X	0	IEMODEM	IELINES	IETHRE	IERECV
2	X	RO	IIR	FIFOENS	FIFOENS	TRIG16	0	IID3	IID2	IID1	NOINT
2	X	WO	FCR	RECVTG1	RECVTG0	TRIG16	0	0	TFIFORST	RFIFORST	FIFOEN
3	X	R/W	LCR	DLAB	BREAKEN	PARMODE1	PARMODE0	PAREN	STOPBIT	WORDSZ1	WORDSZ0
4	X	R/W	MCR	HALF	0	AFE	LOOP	OUT2	OUT1	RTS	DTR
5	X	RO	LSR	RFIFOERR	TEMT	THRE	BREAKINT	FRAMEERR	PARERR	OVERR	DATARDY
6	X	RO	MSR	DCD	RI	DSR	CTS	△DCD	△RI	△DSR	△CTS
7	X	R/W	SCR	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	R/W	DLL	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	1	R/W	DLM	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8

The following table shows the default value of the serial UART register after the power-on reset or PCIE bus reset or serial port soft reset.

Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IER	0	0	0	0	0	0	0	0
IIR	0	0	0	0	0	0	0	1
FCR	0	0	0	0	0	0	0	0
LCR	0	0	0	0	0	0	0	0
MCR	0	0	0	0	0	0	0	0
LSR	0	1	1	0	0	0	0	0
MSR	DCD	RI	DSR	CTS	0	0	0	0
SCR	Keep	Keep	Keep	Keep	Keep	Keep	Keep	Keep
FIFO	Reset, including receive-transmit FIFO							
TSR	Reset; TSR is the serial port transmitter shift register							
RSR	Reset; RSR is the serial port receiver shift register							
Other	Undefined							

RBR: receiver buffer register. If the DATARDY bit of LSR is 1, the received data can be read from this

register. If FIFOEN is 1, the data received from the serial port shift register RSR is firstly stored in the receiver FIFO, and then read out through this register.

THR: transmitter holding register, including transmitter FIFO, used to write the data to be transmitted. If FIFOEN is 1, the written data is firstly stored in the transmitter FIFO, and then output one by one through the transmitter shift register TSR

IER: interrupt enable register, including enhanced function control bit and serial port interrupt enabling.

RESET: bit=1, soft reset the serial port, and this bit can be cleared to 0 automatically without software clearing.

LOWPOWER: bit=1, the internal standard clock of the serial port is turned off, so that the serial port enters a low-power status.

CK2X: bit=1, the external clock signal is forced to be 2 frequency doubling and then used as the internal standard clock of the serial port, and is not controlled by the FREQ bit CKnS.

IEMODEM: bit =1, which allows modem input status change interrupt.

IELINES: bit =1, which allows receive line status interrupt.

ETHRE: bit =1, which allows null interrupt for transmitter holding register.

ERECV: bit =1, which allows received data interrupt.

IIR: interrupt identification register, used to analyze and process the interrupt source.

IFOENS: this bit is the FIFO enabled status, and 1 means that the FIFO has been enabled.

IIR Register Bit				Priority	Interrupt Type	Interrupt Source	Clear Interrupt Method
IID3	IID2	IID1	NOINT				
0	0	0	1	none	No interrupt	No interrupt	
0	1	1	0	1	Receive line status	OVERR,PARERR, FRAMEERR,BREAKINT	Read LSR
0	1	0	0	2	Received data available	The number of bytes received reaches the trigger point of FIFO	Read RBR
1	1	0	0	2	Received data timeout	Next data is not received when the time of more than four data	Read RBR
0	0	1	0	3	THR register null	Transmitter holding register null, IETHRE changes from 0 to 1 which can re-enable the interrupt	Read IIR or write THR
0	0	0	0	4	MODEM input change	△CTS, △DSR, △RI, △DCD	Read MSR

FCR: first-in-first-out buffer FIFO control register, used to enable and reset FIFO.

TRIG16: bit=1, the trigger point interrupt of receiver FIFO and the trigger point of hardware flow control is equal to the trigger point of 16-byte FIFO. This bit is allowed to be modified only when DLAB is 1.

RECVTG1 and RECVTG0: setting the trigger point interrupt of receiver FIFO and the trigger point of hardware flow control. 00 corresponds to 1 byte, namely, available interrupt of received data is generated when 1 byte is received, and RTS pin is automatically invalid when enabling hardware flow control.

TRIG16	RECVTG1	RECVTG0	Trigger Point
0	0	0	1 byte
0	0	1	32 bytes
0	1	0	128 bytes

0	1	1	224 bytes
1	0	0	1 byte
1	0	1	4 bytes
1	1	0	8 bytes
1	1	1	14 bytes

TFIFORST: bit=1, clearing the data in the transmitter FIFO (not including TSR), this bit can be cleared to 0 automatically without software clearing.

RFIFORST: bit=1, clearing the data in the transmitter FIFO (not including RSR), this bit can be cleared to 0 automatically without software clearing.

FIFOEN: bit=1, enabling FIFO, this bit is cleared to 0, FIFO will be disabled. After FIFO is disabled, it will be 16C450 compatible mode, which is equal to only one byte in FIFO (RECVTG1=0, RECVTG0=0, FIFOEN=1). It is suggested that FIFO should enabled.

LCR: line control register, used to control the format of serial communication.

DLAB: this bit is the access enabling of the divisor latch. When it is 1, DLL and DLM can be accessed; when it is 0, RBR/THR/IER can be accessed.

BREAKEN: bit=1, it is forced to generate a BREAK line interval.

PARMODE1 and PARMODE0: when PAREN is 1, setting the format of the parity bit: 00 means odd parity, 01 means even parity, 10 means mark bit (MARK, set to 1), 11 means space bit (SPACE, cleared to 0).

PAREN: bit=1, it is allowed to generate parity bit during transmitting and to check parity bit during receiving. If it is 0, there is no parity bit.

STOPBIT: bit=1, two stop bits; bit= 0, one stop bit.

WORDSZ1 and WORDSZ0: setting the byte length; 00 means 5 data bits, 01 means 6 data bits, 10 means 7 data bits, and 11 means 8 data bits.

MCR: MODEM control register, used to control MODEM output.

HALF: bit=1, entering half-duplex reception and transmission mode, the priority is transmission, proceeding reception when not transmitting. The DTR pin always outputs sending status TNOW in half-duplex mode, which can be used to control RS485's send and receive switching. This bit is allowed to be modified only when DLAB is 1.

AFE: bit=1, the hardware automatic flow control of CTS and RTS is allowed. If AFE is 1, then the serial port will continue to send the next data only when it detects that the CTS pin input is valid (active low), otherwise, suspended. The CTS input status change will not generate the MODEM status interrupt when AFE is 1. If AFE is 1 and RTS is 1, the serial port will automatically validate the RTS pin (active low) when receiver FIFO is null, and the serial port will automatically invalidate the RTS pin until the number of received bytes reach the trigger point of FIFO , and will re-validate the RTS pin when the receiver FIFO is null. Through the hardware automatic band rate control, the CTS pin connects to the other's RTS pin, the RTS pin connects to the other's CTS pin.

LOOP: bit=1, enabling test mode of the internal loop. In the test mode, all external output pins of the serial port are at the invalid status, TXD internally returns to RXD (namely, the output of TSR internally returns to the input of RSR), RTS internally returns to CTS, DTR internally returns to DSR, OUT1 internally returns to RI and OUT2 internally returns to DCD.

OUT2: bit=1, the interrupt request output of the serial port is allowed, otherwise, the serial port will not generate the actual interrupt request.

OUT1: the bit is a user-definable MODEM control bit. In 4 serial ports + extended serial ports mode, the actual output pin is not connected; in 4 serial ports + parallel ports mode, output pin of UART 0 and UART 1 is correspond to OUT0 and OUT1.

RTS: bit=1, the RTS pin output is valid (active low), otherwise, the RTS pin output is invalid.

DTR: bit=1, the DTR pin output is valid (active low), otherwise, the DTR pin output is invalid.

LSR: line status register, used to query and analyze the status of the serial port.

RFIFOERR: bit=1, it means that there is at least one PARERR, FRAMEERR or BREAKINT error in the receiver FIFO.

TEMT: bit=1, it means that the transmitter holding register (THR) and the transmitter shift register (TSR) are empty.

THRE: bit=1, it means that the transmitter holding register (THR) is empty.

BREAKINT: bit=1, it means that the BREAK line interval is detected.

FRAMEERR: bit=1, it means the frame error of the data which being read from the receiver FIFO, and it lacks a valid stop bit.

PARERR: bit=1, it means the parity error of the data which being read from the receiver FIFO.

OVERR: bit=1, it means that the receiver FIFO buffer has overflowed.

DATARDY: bit=1, it means that there is received data in the receiver FIFO. After reading all the data in the FIFO, this bit will be automatically cleared to 0.

MSR: MODEM status register, used to query the Modem status.

DCD: this bit is bit reverse of the DCD pin, bit=1, it means that the DCD pin is valid (active low).

RI: this bit is bit reverse of the RI pin, bit=1, it means that the RI pin is valid (active low).

DSR: this bit is bit reverse of the DSR pin, bit=1, it means that the DSR pin is valid (active low).

CTS: this bit is bit reverse of the CTS pin, bit=1, it means that the CTS pin is valid (active low).

△DCD: bit=1, it means that the DCD pin input status has changed.

△RI: bit=1, it means that the input status of the RI pin has changed.

△DSR: bit=1, it means that the input status of the DSR pin has changed.

△CTS: bit=1, it means that the input status of the CTS pin has changed.

SCR: user can define register.

DLL and DLM: baud rate divisor latch. DLL is the low byte and DLM is the high byte, The 16-bit divisor formed by both which is used for the serial port baud rate generator composed by a 16-bit counter. The divisor = the internal standard clock of the serial port / 16 / the required communication baud rate. If the internal standard clock of the serial port is 1.8432MHz and the required baud rate is 9600bps, then the divisor =1843200/16/9600=12.

6.6. Parallel Port Register

The parallel port of CH384 is compatible with SPP standard printer port with enhanced. The register bits marked in gray in the table are enhanced functions. The actual address of the parallel port register is the I/O base address adds the offset address in the table. The parallel port of CH384 mainly has four operating modes: SPP (including Nibble, Byte and PS/2), EPP and ECP. ALL in the table indicates all modes, ADV indicates EPP and ECP, RO indicates that register is read-only, WO indicates that register is write-only and R/W indicates that the register is readable and writable.

Address	Mode	R/W	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	SPP	RO	PIR	D7IN	D6IN	D5IN	D4IN	D3IN	D2IN	D1IN	D0IN
0	ADV	RO	PIR	IBD7	IBD6	IBD5	IBD4	IBD3	IBD2	IBD1	IBD0
0	ALL	WO	PDR	D7OUT	D6OUT	D5OUT	D4OUT	D3OUT	D2OUT	D1OUT	D0OUT
1	SPP	RO	PSR	!BUSY	ACK	PE	SELT	ERR	!INTFLAG	1	1
1	EPP	RO	PSR						1	1	!EPPREQ
1	ECP	RO	PSR						!ECPICMD	!ECPIBF	!ECPOUT
2	ALL	R/W	PCR	1	1	DIRIN	INTEN	!SIN	INIT	!AFD	!STB
3	SPP	R/W	PXR	0	0	0	0	0	0	0	0

3	EPP	R/W	PXR	0	0	0	0	EPPADDR	MODEEPP	0	0
3	ECP	R/W	PXR	0	0	0	ECPINTF	0	0	ECPDIRIN	MODEECP

The following table shows the default of the parallel port register after the power-on reset or PCIE bus reset.

Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PIR	1	1	1	1	1	1	1	1
PDR	0	0	0	0	0	0	0	0
PSR	!BUSY	ACK	PE	SELT	ERR	1	1	1
PCR	1	1	0	0	0	0	0	0
PXR	0	0	0	0	0	0	0	0
Other	Undefined							

PIR: data input register, used to input real-time data from D7-D0 pins in SPP mode. In EPP or ECP mode, the data which has been latched input /uploaded to buffer. In EPP mode, the data is latched when the AFD pin or SIN pin outputs a low level; in ECP mode, the data is latched when the ACK pin is at the low level, and !ECPICMD is also latched at the same time.

PDR: data output register, used to write data to be outputted /downloaded. Writing into this register in SPP mode, and the data will be directly outputted to the D7-D0 pins; writing into this register in the EPP or ECP mode, and the handshake protocol of data output or data input will be automatically executed.

PSR: status register, used to query the input pin and operate the execution status.

!BUSY: this bit is the reverse value of the status of the input pin BUSY in SPP, EPP and ECP modes. When the BUSY pin inputs a high level, this bit is 0.

ACK: this bit is the status of the input pin ACK in SPP, EPP and ECP modes.

PE: this bit is the status of the input pin PE in SPP, EPP and ECP modes.

SELT: this bit is the status of the input pin SELT in SPP, EPP and ECP modes.

ERR: this bit is the status of the input pin ERR in SPP, EPP and ECP modes.

!INTFLAG: this bit is the reverse value of the interrupt flag in SPP mode. When the rising edge of the ACK pin generates an interrupt flag, this bit will be automatically cleared to 0, and will be automatically set to 1 after reading the PSR register.

!EPPREQ: this bit is the reverse value of the access operation proceeding flag in EPP mode. When writing into the PDR register, this bit will be automatically cleared to 0 and attempting the EPP access operation. This bit will be automatically set to 1 until the operation is completed.

!ECPICMD: this bit is the reverse value of the command flag during reverse transmission in ECP mode. When the reverse transmission is a command, this bit is 0.

!ECPIBF: this bit is the reverse value of the upload buffer full flag for reverse transmission in ECP mode. When the upload buffer is full, this bit will be automatically cleared to 0, and it will be automatically set to 1 after reading the PIR register.

!ECPOUT: this bit is the reverse value of the forward transmission operation proceeding in EPP mode. When writing into the PDR register, this bit will be automatically cleared to 0 and attempting the EPP forward output operation. This bit will be automatically set to 1 until the operation is completed.

PCR: control register, used to control the output pin, transmission direction and interrupt enabling.

DIRIN: this bit is the tri-status output control of the bi-directional data lines D7-D0 in SPP, EPP and ECP modes. When it is cleared to 0, it means that the D7-D0 pins allow tri-status output. When it is set to 1, it means that the D7-D0 pins disable tri-status output.

INTEN: this bit is the PCIE interrupt output enabling. When it is set to 1, the output of interrupt request is allowed; when it is cleared to 0, the output of interrupt request will be disabled.

!SIN: bit=1, the SIN pin output is valid (active low), otherwise, the SIN pin output is invalid.

INIT: bit=1, the INIT pin output is invalid, otherwise, the INIT pin output is valid (active low).
!AFD: bit=1, the AFD pin output is valid (active low), otherwise, the AFD pin output is invalid.
!STB: bit=1, the STB pin output is valid (active low), otherwise, the STB pin output is invalid.

PXR: configuration register, used to set the operating mode of parallel port.
EPPADDR: this bit is the target space selection in EPP mode. When it is 1, it corresponds to the address access operation of EPP. When it is 0, it corresponds to the data access operation of EPP.
MODEEPP: bit=1, enabling the EPP mode.
ECPINTF: this bit is an interrupt flag in ECP mode. When the falling edge of the ERR pin generates an interrupt flag, this bit will be automatically set to 1, and it will be automatically cleared to 0 after reading the PXR register.
ECPDIRIN: this bit is the transmission direction control in ECP mode. When it is 0, it corresponds to ECP forward transmission/output. When it is 1, it corresponds to ECP reverse transmission/input.
MODEECP: bit=1, enabling the EPP mode.

7. Function Descriptions

7.1. Query and Interrupt

The quad UARTs and parallel port of CH384 share a PCIE interrupt request pin, so after entering the PCIE interrupt service, firstly analyzing whether it is ch384 request interrupt and it is which UART or parallel port. After entering the interrupt service, there are two methods: specialized status analysis and sequential query.

Specialized status analysis means that reading the internal interrupt status register IINT firstly. The IINT bit 0 flag is valid indicates the UART 0 interrupted, the IINT bit 1 flag is valid indicates the UART 1 interrupted, the IINT bit 2 flag is valid indicates the UART 2 interrupted, the IINT bit 3 flag is valid indicates the UART 3 interrupted, the IINT bit flag 7 is valid indicates the parallel port interrupted. Directly process and exit it based on the analysis result, directly exit it without interrupt.

Sequential query means reading the PSR or PXR register of the parallel port firstly. If it is in ECP mode, checking the ECPINTF flag of the PXR register, otherwise, checking the !INTFLAG flag of the PSR register. If it is valid, it means there is an interrupt, exit it after processing. Read the IIR register of UART 0 without interrupt, process and exit with an interrupt; read the IIR register of UART 1 without interrupt, process and exit with an interrupt; read the IIR register of UART 3 without interrupt, process and exit with an interrupt and exit it directly without interrupt.

After ensuring that it is an interrupt of a certain UART, if it is necessary can further analyze the LSR register, analyze the reason of the interrupt and process it.

If the serial UART works in the interrupt mode, then setting the IER register to allow the corresponding interrupt request, and set OUT2 of the MCR register to allow interrupt output.

If the parallel port works in interrupt mode, then setting the INTEN of the PCR register to allow interrupt output. The SPP or EPP mode enables the interrupt request by the rising edge of the ACK pin, and the ECP mode enables the interrupt request by the falling edge of the ERR pin.

If the serial UART works in the query mode, then do not to set OUT2 of IER and MCR, and only need to query the LSR register, and analyze and process it.

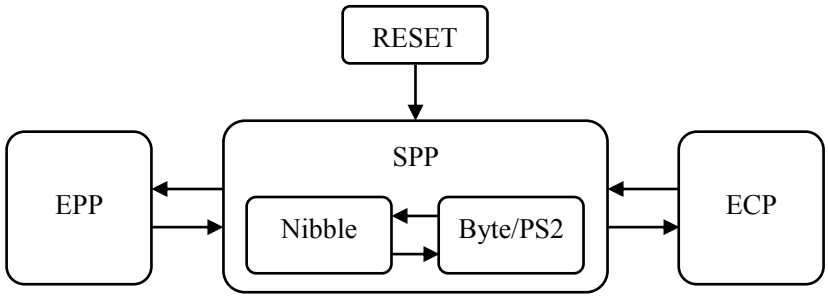
If the parallel port works in the query mode, then do not to set the INTEN of PCR, and only need to query the PSR and PXR registers, and analyze and process it.

7.2. Serial UART Operation

For specific operations, please refer to the specifications for single serial UART 16C550 or dual UARTs CH432 or octal UARTs CH438.

7.3. Parallel Port Operation

The three operating modes of CH384 parallel port are mutually exclusive, and it is SPP mode by default. In SPP mode, it can realize an additional mode such as Nibble, Byte, PS/2, etc. The PXR register can also be set to switch back and forth between SPP, EPP or ECP modes. The operating mode switching diagram of the parallel port is as shown below.



In the SPP mode, software can be used to control PCR and query PSR to realize transmission of Nibble, Byte and PS/2, etc. Refer to IEEE1284 specifications for the specific operation.

In the EPP mode, selecting the target space through the EPPADDR of the PXR, setting the transmission direction through the DIRIN of the PCR, and then writing data to the PDR (writing any data for reverse transmission) to start the EPP transmission, and query the PSR until !EPPREQ is 1; if it is a reverse transmission, data needs to be read from PIR (suggesting to read with PSR to improve efficiency).

In the ECP mode, the transmission direction should be set by the DIRIN of PCR and ECPDIRIN of PXR. For forward transmission, writing data to PDR to start ECP forward transmission, and query PSR until! ECPOUT is 1; for reverse transmission, directly query PSR until !ECPIBF is 0, and then read data from PIR (suggest to read with PSR to improve efficiency, and get !ECPICMD from PSR).

7.4. Application Specification

The serial UART's output pins of CH384 are at 3.3V LVCMOS levels, and compatible with 5V TTL. The input pins can support 5V withstand voltage and compatible with 5V CMOS, 3.3 V LVCMOS and 5V TTL and LVTTL. It can be further converted to RS232 by adding an RS232 conversion chip externally.

The pins of CH384 in serial UART mode include: data transmission pin and MODEM signal pin. The data transmission pins include: TXD and RXD, both are at high level by default. The MODEM signal pins include: CTS, DSR, RI, DCD, DTR, RTS and OUT of some serial ports in quad UARTs+ parallel port mode, all are at high level by default. All MODEM signals can be used as general-purpose IO pins, controlled and defined usage by the computer application.

CH384 has built-in independent transceiver buffer and FIFO, supporting simplex, half-duplex or full duplex serial communication. Serial data includes one low-level start bit, 5, 6, 7 or 8 data bits, 0 or 1 additional parity bit or flag bit; 1 or 2 high-level stop bits, and supports odd/even/mark/space parity. CH384 supports common communication baud rates: 1200, 2400, 4800, 9600, 19.2K, 38.4K, 57.6K, 115.2K, 230.4K, 460.8K, 921.6K, 1.8432m, 2.7648m, 7.8125M, etc. The baud rate error of the serial port transmitting signal is less than 0.2%, and the allowable baud rate error of the serial port receiving signal is not less than 2%.

In Windows and Linux OS, the drive of CH384 can be compatible with standard serial ports, so most of the original serial port applications are completely compatible and without any modification.

The parallel port's output pins of CH384 are at 3.3V LVCMOS levels, compatible with 5V TTL. The input pins can support 5V withstand voltage and are compatible with 5V CMOS, 3.3 V LVCMOS and 5V TTL and

LVTTL.

The pins of CH384 in parallel mode include: bi-directional data pins, control output pins and status input pins. Except for the INIT pin of the bidirectional data pin and control output pin are all at high level by default. In the SPP mode, all signals can be used as general-purpose IO pins, controlled and defined usage by the computer application.

In Windows and Linux OS, the drive of CH384 can be compatible with standard serial ports and standard printer ports, so most of the original serial port and parallel port applications are completely compatible and without any modification.

CH384 can be used to expand additional high-speed RS232 serial port and parallel port /printer ports for computer through PCIE bus, and support high baud rate serial port with automatic hardware speed control, RS422 or RS485 communication interface and SIR infrared communication interface, etc.

8. Parameters

8.1. Absolute Maximum Ratings

(Critical state or exceeding maximum can cause chip to not work or even be damaged)

Name	Parameter Description	Min	Max	Unit
TA	Operating ambient temperature	-40	85	℃
TS	Storage ambient temperature	-55	125	℃
VCC33	I/O supply voltage (VCC33 connects to power, GND to ground)	-0.4	4.2	V
VCC18 VCC18A	Core supply voltage (VCC18 connects to power, GND to ground) Transmission supply voltage (VCC18A connects to power, GND to ground)	-0.4	2.3	V
VIO	Voltage of PCIE signal and various auxiliary signal input or output pins	-0.4	VCC33+0.4	V
VIO5	Voltage of serial and parallel ports and extended input or output pins	-0.4	5.3V	V

8.2. Electrical Parameters

(Test Conditions: TA=25℃, VCC33=3.3V, exclude pins connected to PCIE bus)

Name	Parameter Description	Min	Type	Max	Unit
VCC33	I/O supply voltage	3.0	3.3	3.6	V
VCC18 VCC18A	Core supply voltage Transmission supply voltage	1.65	1.8	1.95	V
ICC	Operating supply current	2	90	250	mA
VIL	Input low voltage	-0.4		0.7	V
VIH	Input high voltage	2.0		VCC33+0.4	V
VOL	Output low voltage (4mA draw current)			0.4	V
VOH	Output high voltage (4mA output current)	VCC33-0.4			V
IIN	Input current of the input without pull-up			10	uA
IUP	Input current of the input with pull-up	20	40	100	uA

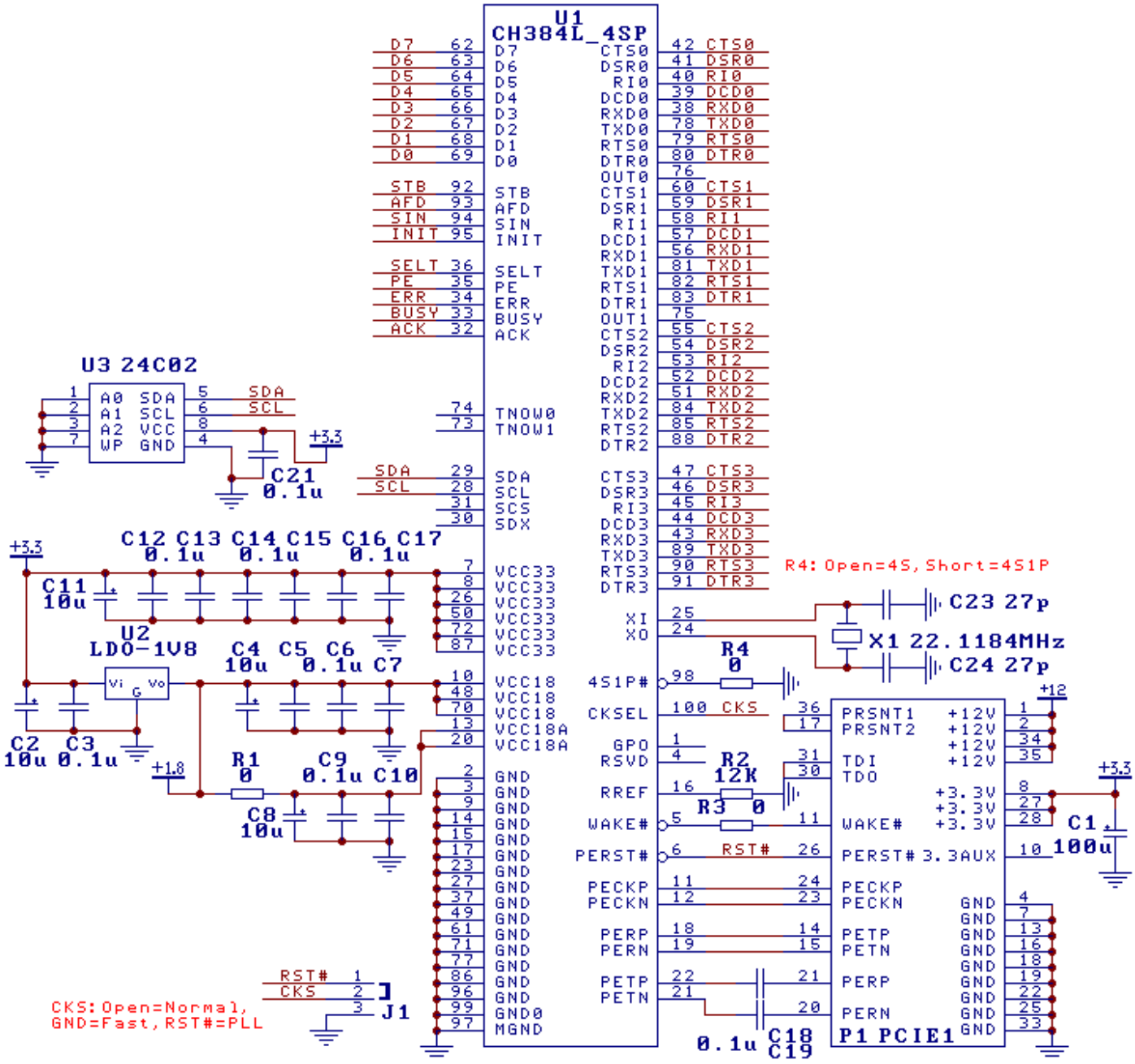
8.3. Timing Parameters

Test Conditions: TA=25℃, VCC33=3.3V, refer to the figure)

Name	Parameter Description	Min	Type	Max	Unit
FCLK	CLK input frequency (basic frequency of PCIE bus)	0	100	105	MHz
FSCL2	SCL output frequency when the automatic loading of two-wire interface		244	260	KHz
FSCL3	SCL output frequency when the automatic loading of three-wire interface		31	35	MHz
FXI	XI input frequency, crystal frequency	0.9216	22.1184	64	MHz

9. Applications

9.1. Quad Serial Ports + Parallel Port



This is the basic circuit for PCIE quad serial ports + parallel/printer port based on CH384. The figure does not include RS232 voltage conversion chip.

U3 is an optional external configuration chip, and the online configuration tool software for Windows system is available on the website.

IEEE1284 requires the printer port signals to keep impedance matching. Therefore, the parallel data singals of the printer port may be connected to resistors in series and capacitors in parallel, which can also be eliminated when the requirement is not high.

Crystal X1, capacitors C23 and C24 are used in the clock oscillation circuit. Other capacitors are used for power supply decoupling. The capacitor with a capacity of 10uF is a tantalum capacitor, and the capacitor with a capacity of 0.1uF is a monolithic or high-frequency ceramic capacitor, which are connected in parallel to the power pins of CH384 respectively.

CH384 is a high frequency circuit. Please refer to PCIE Bus specification or PCIE_PCB.PDF document when designing the PCB board.