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NL668-EAU&EU-MiniPCIe-10 Hardware User Manual

Version: V1.0.6

Date: 2019-05-06

Applicability type

No.	Product Model	Description
1	NL668-EAU-00-MiniPCIe-10	MCP is 4+2, support MAIN_ANT, DIV_ANT, GNSS_ANT, no CODEC
2	NL668-EU-01-MiniPCIe-10	Based on NL668-EAU-00-MiniPCIe-10,delete B28
3	NL668-EU-00-MiniPCIe-10	Based on NL668-EU-01-MiniPCIe-10, don't support TDD
4	NL668-EU-03-MiniPCIe-10	Based on NL668-EU-01-MiniPCIe-10, change MCP to 2+1

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Versions

Version	Author	Assessor	Approver	Update Date	Description
V1.0.0				2018-04-24	Initial version
V1.0.1				2018-05-28	Add test data, add description of sleep mode, etc.
V1.0.2				2018-06-07	Replace physical and structural images and modify GNSS data
V1.0.3	Gu Zhaoqiang	Tu Min	Tu Min	2018-08-16	Update LPG description and reference design； Update maximum working current is 3A; Update ESR< 100 m Ω
V1.0.4	Gaoying	Tumin	Tumin	2019-03-30	Add Figure and Table title change common style, Update RF parameters, add NL668-EU-MiniPCIe-10 part, update NET_MODE description
V1.0.5	Gaoying	Tumin	Tumin	2019-04-29	Update pin distribution diagram, Correct some description
V1.0.6	Gaotianhuan Heruzhi	Tumin Lixiyi	Tumin Lixiyi	2019-05-06	Add NL668-EU-03-MiniPCIe-10 product description

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1 Foreword

1.1 Introduction

This document describes the electrical characteristics, RF performance, structure size, application environment, etc. of NL668-EAU/EU-MiniPCIe-10 module. With the assistance of the document and other instructions, the developers can quickly understand the hardware functions of the NL668-EAU/EU-MiniPCIe-10 module and develop products.

1.2 Safety Instruction

By following the safety guidelines below, you can ensure your personal safety and help protect the product and work environment from potential damage. Product manufacturers need to communicate the following safety instructions to end users. In case of failure to comply with these safety rules, Fibocom will not be responsible for the consequences caused by the user's misuse.

Road safety first! When you drive, do not use the hand held devices even if it has a hand-free feature. Please stop and call!

Please turn off the mobile device before boarding. The wireless feature of the mobile device is not allowed on the aircraft to prevent interference with the aircraft communication system. Ignoring this note may result in flight safety issue or even breaking the law.

When in a hospital or health care facility, please be aware of restrictions on the use of mobile devices. Radio frequency interference may cause medical equipment to malfunction, so it may be necessary to turn off the mobile device.

The mobile device does not guarantee that an effective connection can be made under any circumstances, for example, when there is no prepayment for the mobile device or the SIM is invalid. When you encounter the above situation in an emergency, remember to use an emergency call, while keeping your device turned on and in areas where signal is strong.

Your mobile device receives and transmits RF signals when it is powered on. Radio interference occurs when it is near televisions, radios, computers, or other electronic devices.

Keep the mobile device away from flammable gases. Turn off the mobile device when near gas stations, oil depots, chemical plants or explosive workplaces. There is a safety hazard in operating electronic equipment in any potentially explosive environment.

1.3 Reference Standards

This design of the product complies with the following standards:

- 3GPP TS 51.010-1 V10.5.0: Mobile Station (MS) conformance specification; Part 1: Conformance specification
- 3GPP TS 34.121-1 V10.8.0: User Equipment (UE) conformance specification; Radio transmission and reception (FDD); Part 1: Conformance specification
- 3GPP TS 34.122 V10.1.0: Technical Specification Group Radio Access Network; Radio transmission and reception (TDD)
- 3GPP TS 36.521-1 V10.6.0: User Equipment (UE) conformance specification; Radio transmission and reception; Part 1: Conformance testing
- 3GPP TS 21.111 V10.0.0: USIM and IC card requirements
- 3GPP TS 51.011 V4.15.0: Specification of the Subscriber Identity Module -Mobile Equipment (SIM-ME) interface
- 3GPP TS 31.102 V10.11.0: Characteristics of the Universal Subscriber Identity Module (USIM) application
- 3GPP TS 31.11 V10.16.0: Universal Subscriber Identity Module (USIM) Application Toolkit (USAT)
- 3GPP TS 36.124 V10.3.0: Electro Magnetic Compatibility (EMC) requirements for mobile terminals and ancillary equipment
- 3GPP TS 27.007 V10.0.8: AT command set for User Equipment (UE)
- 3GPP TS 27.005 V10.0.1: Use of Data Terminal Equipment - Data Circuit terminating Equipment (DTE - DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS)

1.4 Related Document

- FIBOCOM_EVK-GT8230-NL User Manual
- FIBOCOM_RF Antenna Application Design Instruction
- FIBOCOM_NL668 AT Command Manual

2 Product Overview

2.1 Product Introduction

NL668-EAU/EU-MiniPCIe-10 series wireless module is a broadband wireless terminal product suitable for TDD-LTE/FDD-LTE/WCDMA/GSM.

2.2 Product Specifications

Specification		
Operating frequency	NL668-EAU	LTE FDD: Band 1,3,5,7,8,20,28
		LTE TDD: Band 38,40,41
		WCDMA/HSPA+: Band 1,5,8
		GSM/GPRS/EDGE: 850/900/1800MHz
	NL668-EU-01/03	LTE FDD: Band 1,3,5,7,8,20
		LTE TDD: Band 38,40,41
		WCDMA: Band 1,5,8
		GSM/GPRS/EDGE: 850/900/1800MHz
	NL668-EU-00	LTE FDD: Band 1,3,5,7,8,20
		WCDMA: Band 1,5,8
		GSM/GPRS/EDGE: 850/900/1800MHz
Data transmission	LTE FDD Rel.9	150Mbps DL/50Mbps UL (Cat 4); LTE Downlink MIMO 2x2, 4x2（support part of R10）
	LTE TDD Rel.9	130Mbps DL/30.5Mbps UL (Cat 4); LTE Downlink MIMO 2x2, 4x2（support part of R10）
	WCDMA Rel.8	WCDMA:384 kbps DL/384 kbps UL
		DC-HSDPA+:42Mbps (Cat 24)/HSUPA:5.76Mbps (Cat 6)
	GPRS/EDGE Rel.5	GPRS: 107kbps/85.6kbps UL (multi-slot class 33)
		EDGE(E-GPRS):296kbps DL/236.8kbps UL (multi-slot class 33)
Power	3.3V～4.3V (3.8V recommended)	
Temperature	Normal: -30°C～+75°C	
	Extended: -40°C～+85°C	

	Storage: -40°C～+85°C
Power consumption	Bottom current: <2mA
	Sleep mode: ≤3mA (USB sleep)
	Idle mode: <20mA (USB sleep); <29mA (USB wake up)
Physical characteristics	Package: PCI express Mini Card interface 52Pin
	Size: (50.8±0.15) mm×(29.85±0.15)mm×(3.4±0.2)mm
	Weight: <9.5g
Interface	
Antenna	Antenna: Main x 1, GNSS x 1, DIV x 1
Functional Interface	(U)SIM 3V/1.8V
	USB 2.0 x 1
	UART x 2, PCM, WAKEUP_IN/OUT, W_DISABLE#
	System Indicator
Software	
Protocol Stack	Embedded TCP/IP and UDP/IP protocol stack
AT Command	3GPP TS 27.007 and 27.005, and proprietary FIBOCOM AT
Firmware update	USB (UART does not support DOWNLOAD)
Voice service	SRLTE, VoLTE, HR, FR, EFR, AMR, DTMF, Caller ID, Call Transfer, Call Hold, Call Waiting and Multi-Talk, etc.
SMS	point-to-point MO, MT; cell broadcast; support Text and PDU modes
MMS service	Need AP to realize MMS protocol

Table 2-1 Product Specifications

Note:

When the temperature is beyond the normal operating temperature range (-30 °C to + 75 °C), the RF performance of the module may slightly exceed the 3GPP specifications.

2.3 Hardware Diagram

Figure 2-1 hardware diagram shows the main functions of the MiniPCIe module.

- 1-way (U)SIM card interface
- 1-way USB2.0 interface
- Sleep&wake up control
- Flight mode

- LED status indication function
- External reset function
- 3 RF antenna interfaces(optional)
- PCM digital audio interface

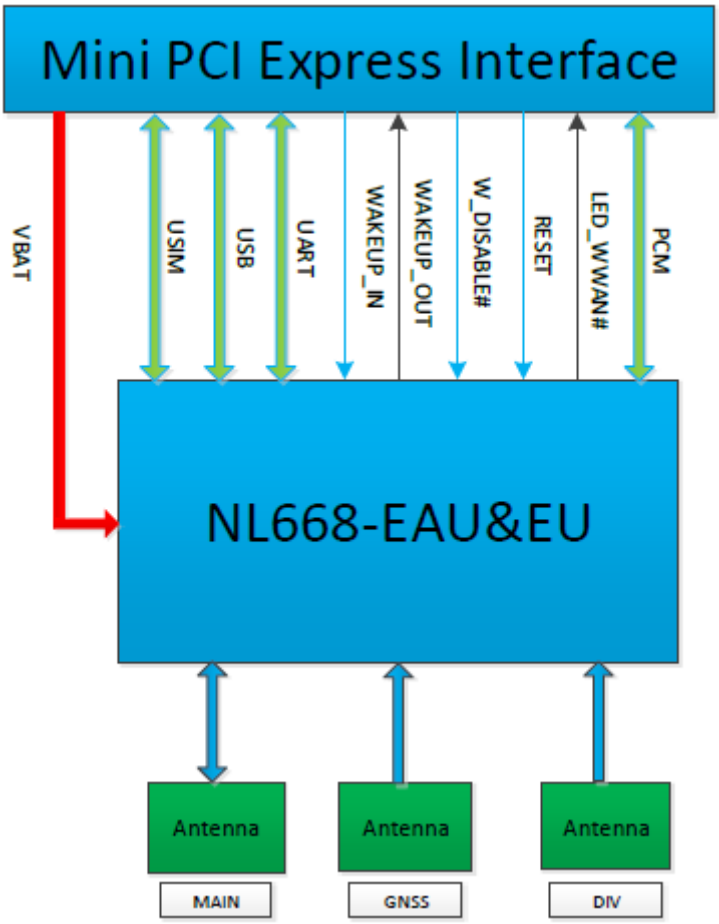


Figure 2-1 Hardware Diagram

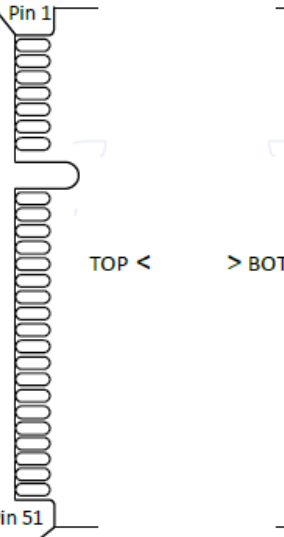
3 Application Interface

3.1 PCI express Mini Card Interface

NL668-EAU&EU-MiniPCIe-10 module adopts PCI express Mini Card interface, with a total of 52 pins.

3.1.1 Pin Distribution

Pin Name	Pin Num
MIC_P	1
MIC_N	3
SPK_P	5
SPK_N	7
GND	9
VDD_EXT	11
NC	13
GND	15
NC	17
WAKEUP_IN	19
GND	21
UART_RXD	23
UART_RTS	25
GND	27
GND	29
UART_TXD	31
NC	33
GND	35
GND	37
VBAT	39
VBAT	41
GND	43
PCM_CLK	45
PCM_OUT	47
PCM_IN	49
PCM_SYNC	51



Pin Num	Pin Name
2	VBAT
4	GND
6	NC
8	USIM_VDD
10	USIM_DATA
12	USIM_CLK
14	USIM_RST
16	NC
18	GND
20	W_DISABLE#
22	RESET_N
24	VBAT
26	GND
28	DBG_UART_RX
30	UART_CTS
32	WAKEUP_OUT
34	GND
36	USB_DM
38	USB_DP
40	GND
42	NET_MODE
44	USIM_PRESENCE
46	DBG_UART_TX
48	NC
50	GND
52	VBAT

Figure 3-1 Pin Distribution Diagram

3.1.2 Pin Definition

The pin definitions are shown in the following table.

Pin	Pin Name	I/O	Level	Description
1	MIC_P	I	Bias voltage 2.7V, bias resistor 2.2K	Reserved
2	VBAT	PI	Vmax=4.3V Vmin=3.3V Vnorm=3.8V	Module power supply
3	MIC_N	I	-	Reserved

Pin	Pin Name	I/O	Level	Description
4	GND	G		Ground
5	SPK_P	O		Reserved
6	NC	-	-	NC
7	SPK_N	O	-	Reserved
8	USIM_VDD	PO	For 1.8V USIM: Vmax=1.9V Vmin=1.7V For 3.0V USIM: Vmax=3.05V Vmin=2.7V IOmax=50mA	(U)SIM power
9	GND	G	-	Ground
10	USIM_DATA	IO	For 1.8V (U)SIM: VILmax=0.6V VIHmin=1.2V VOLmax=0.45V VOHmin=1.35V For3.0V (U)SIM: VILmax=1.0V VIHmin=1.95V VOLmax=0.45V VOHmin=2.55V	(U)SIM data signal
11	VDD_EXT	PO	1.8V	Module digital level, 1.8V output, 80mA
12	USIM_CLK	O	For 1.8V (U)SIM: VOLmax=0.45V VOHmin=1.35V For3.0V (U)SIM: VOLmax=0.45V VOHmin=2.55V	(U)SIM clock signal
13	NC	-	-	NC
14	USIM_RST	O	For 1.8V (U)SIM: VOLmax=0.45V VOHmin=1.35V For 3.0V (U)SIM: VOLmax=0.45V VOHmin=2.55V	(U)SIM reset signal
15	GND	G	-	Ground
16	NC	-	-	NC
17	NC	-	-	NC
18	GND	G	-	Ground
19	WAKEUP_IN	I	VILmin=-0.3V VILmax=0.6V VIHmin=1.2V	External device wakeup module

Pin	Pin Name	I/O	Level	Description
			VIHmax=2.0V	
20	W_DISABLE#	I	VILmin=-0.3V VILmax=0.6V VIHmin=1.2V VIHmax=2.0V	Module flight mode control
21	GND	G	-	Ground
22	RESET_N	I	VIHmax=2.0V VIHmin=1.3V VILmax=0.5V	Module reset signal
23	UART_RXD	I	VILmin=-0.3V VILmax=0.6V VIHmin=1.2V VIHmax=2.0V	Serial port receive data
24	VBAT	PI	Vmax=4.3V Vmin=3.3V Vnorm=3.8V	Module power supply
25	UART_RTS	O	V_{OL}max=0.45V V_{OH}min=1.35V	Request transmission
26	GND	G	-	Ground
27	GND	G	-	Ground
28	DBG_UART_RX	I	VILmin=-0.3V VILmax=0.6V VIHmin=1.2V VIHmax=2.0V	DEBUG serial port receive data
29	GND	G	-	Ground
30	UART_CTS	I	VILmin=-0.3V VILmax=0.6V VIHmin=1.2V VIHmax=2.0V	Clear transmission
31	UART_TXD	O	VILmin=-0.3V VILmax=0.6V VIHmin=1.2V VIHmax=2.0V	Serial port data transmission
32	WAKEUP_OUT	O	1.8V	Module wake up external device
33	NC	-	-	NC
34	GND	G		Ground
35	GND	G		Ground
36	USB_DM	IO		USB signal DM
37	GND	G		Ground
38	USB_DP	IO		USB signal -
39	VBAT	PI	Vmax=4.3V	Module power supply

Pin	Pin Name	I/O	Level	Description
			Vmin=3.3V Vnorm=3.8V	
40	GND	G	-	Ground
41	VBAT	PI	Vmax=4.3V Vmin=3.3V Vnorm=3.8V	Module power supply
42	NET_MODE	O	OC	Indicator signal
43	GND	G	-	Ground
44	USIM_PRESENCE	I	1.8V	(U)SIM hot plug detection
45	PCM_CLK	IO	VOLmax=0.45V VOHmin=1.35V VILmin=-0.3V VILmax=0.6V VIHmin=1.2V VIHmax=2.0V	PCM clock signal
46	DBG_UART_TX	O	V_{OL}max=0.45V V_{OH}min=1.35V	DEBUG serial port transmission
47	PCM_OUT	O	V_{OL}max=0.45V V_{OH}min=1.35V	PCM data transmission
48	NC	-	-	Reserved
49	PCM_IN	I	V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	PCM data reception
50	GND	G	-	Ground
51	PCM_SYNC	O	V_{OL}max=0.45V V_{OH}min=1.35V V_{IL}min=-0.3V V_{IL}max=0.6V V_{IH}min=1.2V V_{IH}max=2.0V	PCM synchronization signal
52	VBAT	PI	Vmax=4.3V Vmin=3.3V Vnorm=3.8V	Module power supply

Table 3-1 Pin Definition

Note:

Keep the unused pins floating.

3.2 Power

The power interfaces of module are shown in the following table.

Pin Name	I/O	Pin	Description
VBAT	I	2,24,39,41,52	Module power supply, 3.3V ~ 4.3V,

Pin Name	I/O	Pin	Description
			nominal value 3.8V
VDD_EXT	O	11	Voltage Output, 1.8V, 80mA
GND	-	4,9,15,18,21,26,27,29,34,35,37,40,43,50	Ground

Table 3-2 Power Interfaces

3.2.1 Power supply

module needs to be powered by the VBAT pin. The power design is shown in Figure 3-2.

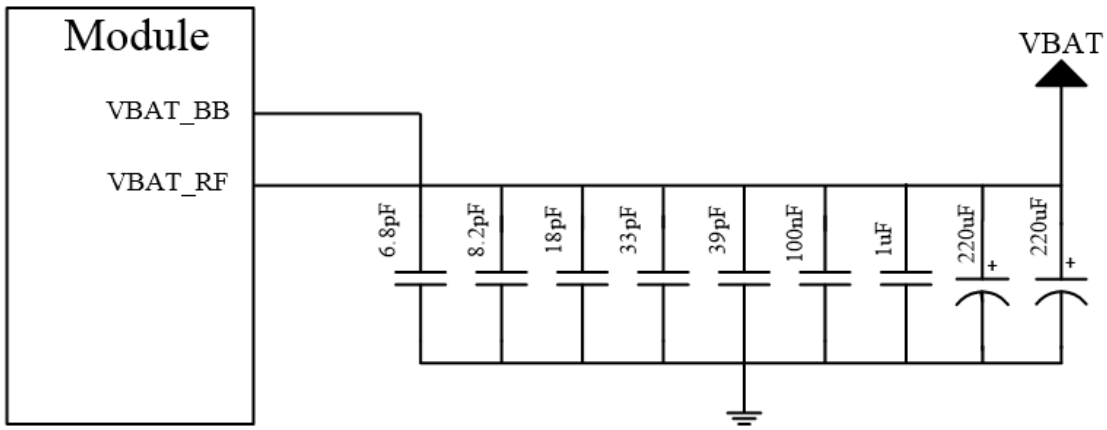


Figure 3-2 Power Design

Module power filter capacitor design is shown in the following table.

Recommended capacitor	Application	Description
220uF x 2	Regulating capacitor	Reduce power fluctuations during module operation, requiring low ESR capacitor ● LDO or DCDC power requires not less than 440uF capacitor ● Battery power can be properly reduced to 100 ~ 220uF capacitor
1uF,100nF	Digital signal noise	Filter clock and digital signal interference
39pF,33pF	700, 850/900 MHz	Filter low band radio frequency interference
18pF,8.2pF,6.8pF	1700/1800/1900,2100/2300, 2500/2600MHz	Filter middle/high band radio frequency interference

Table 3-3 Power Filter Capacitor Design

The power stability ensures the normal operation of module. The design requires special attention to the power ripple below 300mV(the circuit ESR < 100mΩ). When the module is operating in GSM mode (Burst

transmit), the maximum operating current can reach 3A, and the power voltage needs to be at least 3.3V. Otherwise, the module may power off or restart. The power limit is shown in Figure 3-3.

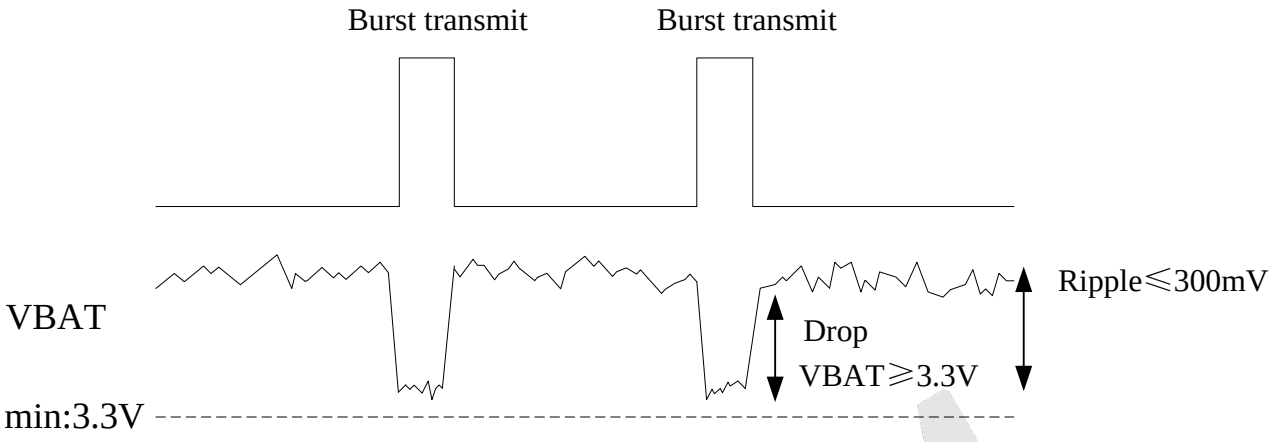


Figure 3-3 Power Limit

3.2.2 1.8V Output

Module outputs a 1.8V voltage through the VDD_EXT for use of the internal digital circuit of the module. The voltage is the logic level voltage of the module and can be used to indicate that the module is on or off, or for external low current (<80mA) circuit. If it is not in use, keep it in floating status. The logic level of VDD_EXT is defined as follows.

Parameter	Minimum	Typical	Maximum	Unit
VDD_EXT	1.71	1.8	1.89	V

Table 3-4 VDD_EXT Logic Level Definition

3.2.3 Power Consumption

The power consumption of module in the case of 3.8V power supply is shown in the following table. (Please send at+syscmd=start_pcm stop command to close codec founction)

Parameter	Mode	Condition	Average Current Typ. (mA)
I_{off}	Power off	Power supply, module power off	0.018
I_{Sleep}	GSM	MFRMS 2(USB Sleep)	≤2.6
		MFRMS 5(USB Sleep)	≤2.6
		MFRMS 9(USB Sleep)	≤2.6
	WCDMA	DRX=6(USB Sleep)	≤3
		DRX=7(USB Sleep)	≤3
		DRX=8(USB Sleep)	≤3
		DRX=9(USB Sleep)	≤3
	LTE FDD	Paging cycle #64 frames (USB Sleep)	≤3
		Paging cycle #128 frames (USB Sleep)	≤3
		Paging cycle #256 frames (USB Sleep)	≤3

Parameter	Mode	Condition	Average Current Typ. (mA)
	LTE TDD	Paging cycle #64 frames (USB Sleep)	≤3
		Paging cycle #128 frames (USB Sleep)	≤3
		Paging cycle #256 frames (USB Sleep)	≤3
I_{Idle}	GSM	MFRMS=5(USB sleep)	≤15
		MFRMS=5 USB (wake up)	≤29
	WCDMA	DRX=8 Paging cycle #256 frames (USB sleep)	≤15
		DRX=8 Paging cycle #256 frames (USB wake up)	≤29
	LTE FDD	DRX=8 Paging cycle #256 frames (USB sleep)	≤15
		DRX=8 Paging cycle #256 frames (USB wake up)	≤29
	LTE TDD	DRX=8 Paging cycle #256 frames (USB sleep)	≤15
		DRX=8 Paging cycle #256 frames(USB wake up)	≤29
Radio off	Flight mode	AT+CFUN=0 (USB sleep)	≤10
	Flight mode	AT+CFUN=0 (USB wake up)	≤25
$I_{GSM-RMS}$	GSM	EGSM900 PCL5	≤260
		DCS1800 PCL0	≤180
		GSM850 PCL5	≤260
$I_{GPRS-RMS}$ CS4	GPRS	GPRS Data transfer GSM900; PCL=5; 1Rx/4Tx	≤500
		GPRS Data transfer GSM8500; PCL=5; 1Rx/4Tx	≤565
		GPRS Data transfer DCS1800; PCL=0; 1Rx/4Tx	≤520
$I_{EGPRS-RMS}$ MCS9	EDGE	EDGE Data transfer GSM900; PCL=8; 1Rx/4Tx	≤500
		EDGE Data transfer GSM850; PCL=8; 1Rx/4Tx	≤500
		EDGE Data transfer DCS1800; PCL=2; 1Rx/4Tx	≤450
$I_{WCDMA-RMS}$	WCDMA	WCDMA Data transfer Band I @+23.5dBm	≤780
		WCDMA Data transfer Band V @+23.5dBm	≤700
		WCDMA Data transfer Band VIII @+23.5dBm	≤600
$I_{LTE-RMS}$	LTE FDD	LTE FDD Data transfer Band 1 @+23dBm	≤780
		LTE FDD Data transfer Band 3 @+23dBm	≤790
		LTE FDD Data transfer Band 5 @+23dBm	≤700
		LTE FDD Data transfer Band 7 @+23dBm	≤790
		LTE FDD Data transfer Band 8 @+23dBm	≤620
		LTE FDD Data transfer Band 20 @+23dBm	≤700
		LTE FDD Data transfer Band 28 @+23dBm	≤700
	LTE TDD	LTE TDD Data transfer Band 38 @+23dBm	≤430
		LTE TDD Data transfer Band 40 @+23dBm	≤440
		LTE TDD Data transfer Band 41 @+23dBm	≤430

Table 3-5 Power Consumption

Note:

USB sleep please use AT command：at+gtusbsleepen=2,0

3.3 Control Signal

The module provides one control signal for reset operation. The pin definition is as follows.

Pin Name	I/O	Pin num	Description
RESET_N	I	22	When the module is in operating mode, pull down RESET_N pin 700ms~1s, and then pull it high, the module is reset.

Table 3-6 Reset Control Signal

3.3.1 Module Reset

The module can reset by hardware and AT command.

Reset mode	Reset method
Hardware reset	Pull down RESET_N pin 700ms~1s, and then release it
AT command reset	AT+RESET

Table 3-7 Module Reset

3.3.1.1 Reset Circuit

The reference circuit is as follows. Customers can control the RESET_N pin using the OC/OD driver circuit or button.

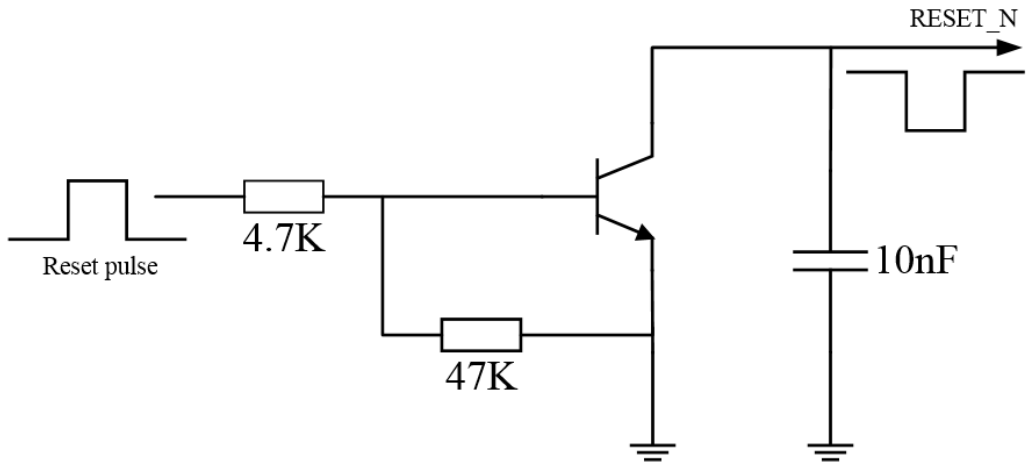


Figure 3-4 OC/OD Reset Reference Circuit

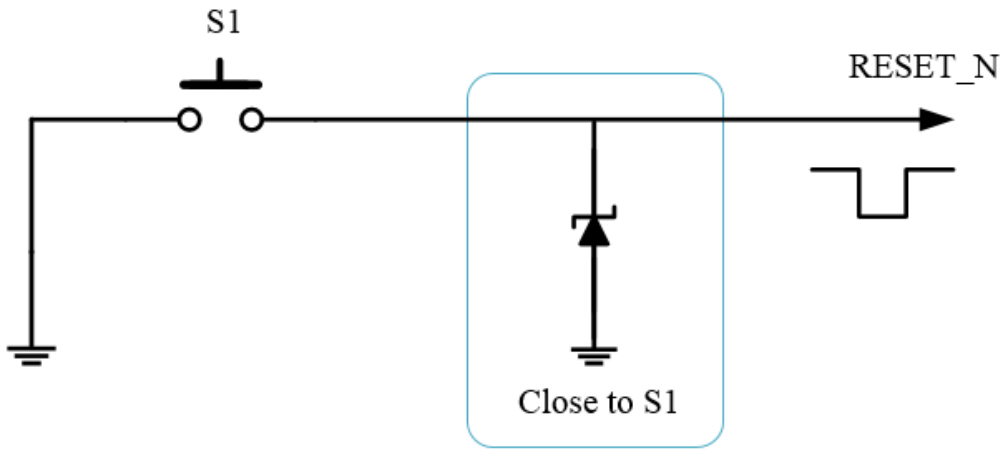


Figure 3-5 Button Reset Reference Circuit

3.3.1.2 RESET_N Control Timing

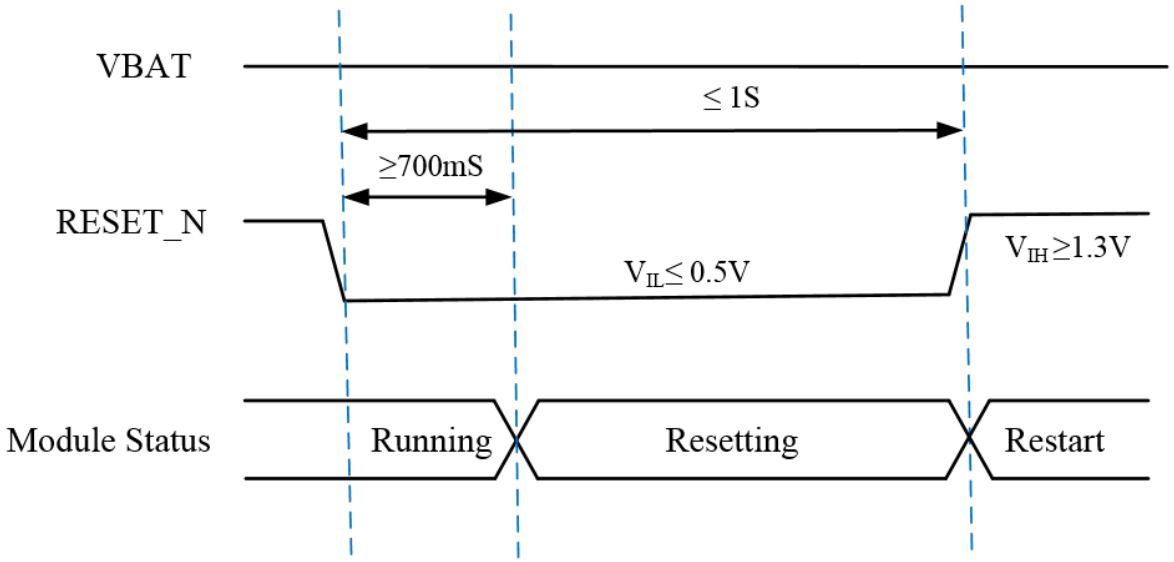


Figure 3-6 RESET_N Control Timing

Note:

RESET_N is a sensitive signal, so it is recommended to add a debouncing capacitor close to the module. The PCB layout should be kept away from the RF interference and protected by Ground. At the same time, avoid routing on PCB edge and surface (avoid module reset caused by ESD)

3.4 USB Interface

Module supports USB2.0 and is compatible with USB High-Speed (480Mbits/s) and USB Full-Speed (12Mbits/s). Refer to “Universal Serial Bus Specification 2.0” for the time slot and electrical characteristics of the module USB bus.

3.4.1 USB Interface Definition

Pin Name	I/O	Pin	Description
USB_DM	IO	36	USB differential data (-)
USB_DP	IO	38	USB differential data (+)

Table 3-8 USB Interface

For more information on the USB 2.0 specification, visit http://www.usb.org/home

Note:

Since the module supports USB 2.0 High-Speed, TVS tube equivalent capacitance on the USB_DM/DP differential signal cable is required to be less than 1pF, and a 0.5pF capacitance TVS is recommended.

Connect a 0 ohm resistor to USB_DM / DP differential cable;

USB_DM and USB_DP are high-speed differential signal cables, can achieve the maximum transmission rate of 480Mbits/s, and must follow the rules below in PCB Layout:

- USB_DM and USB_DP signal cable control differential impedance is 90 ohm;
- USB_DM and USB_DP signal cables shall be parallel and equal in length, and avoid the right-angle route;
- USB_DM and USB_DP signal cables are routed on the signal layer closest to the ground layer, and the cables shall be grounded.

3.5 (U)SIM Interface

MiniPCIe module have (U)SIM card interface, support 1.8V and 3.0V (U)SIM card.

3.5.1 (U)SIM Pin

(U)SIM pin is shown in the following table.

Pin Name	I/O	Pin Num	Description
USIM_VDD	O	8	(U)SIM Power
USIM_DATA	IO	10	(U)SIM Data
USIM_CLK	O	12	(U)SIM Clock
USIM_RST	O	14	(U)SIM Reset
USIM_PRESENCE	I	44	(U)SIM card detect for Hot-swap

Table 3-9 (U)SIM Pin

3.5.2 (U)SIM Interface Circuit

3.5.2.1 (U)SIM Card Conncetor With Detection Signal

(U)SIM design requires the use of (U)SIM card holder (Fibocom recommend: SIM016-8P-220P). We

recommend using hot plug slot with (U)SIM card detect function.

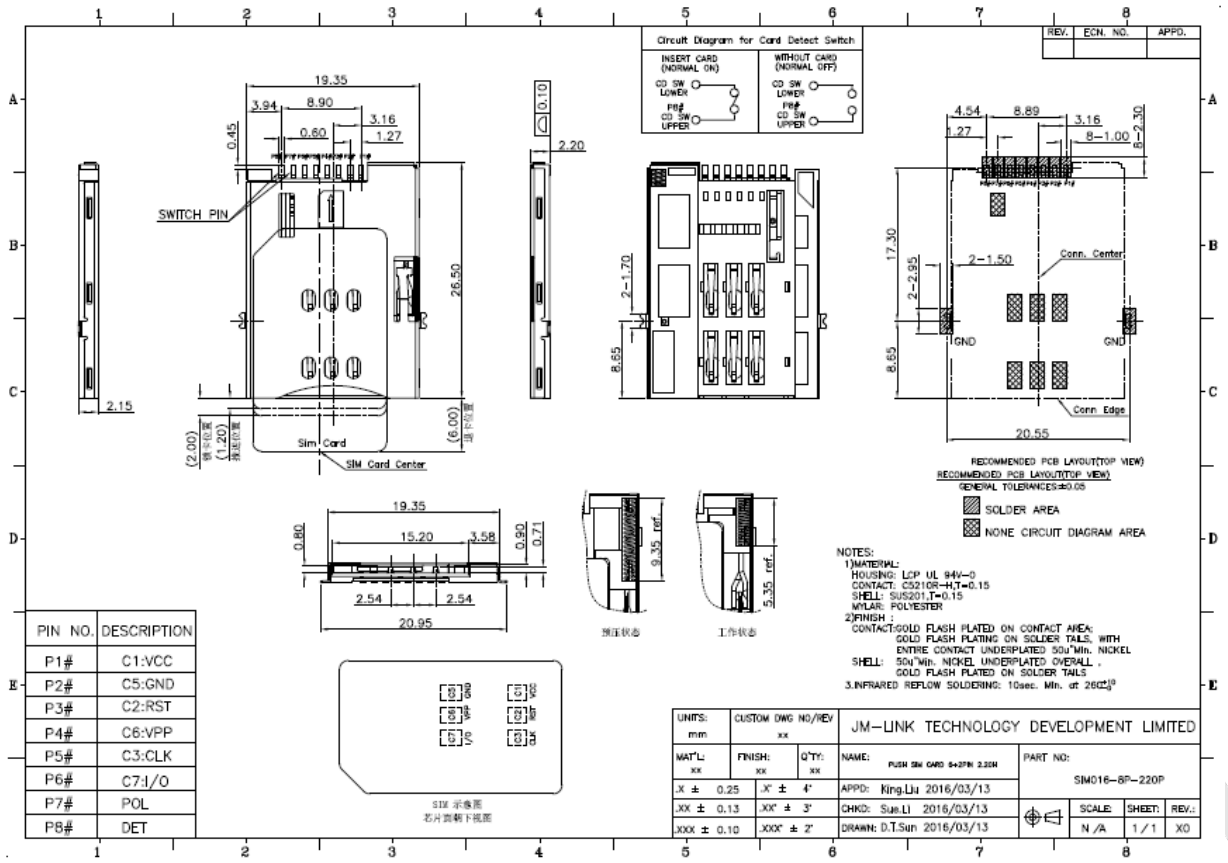


Figure 3-7 (U)SIM Card Slot Diagram SIM016-8P-220P

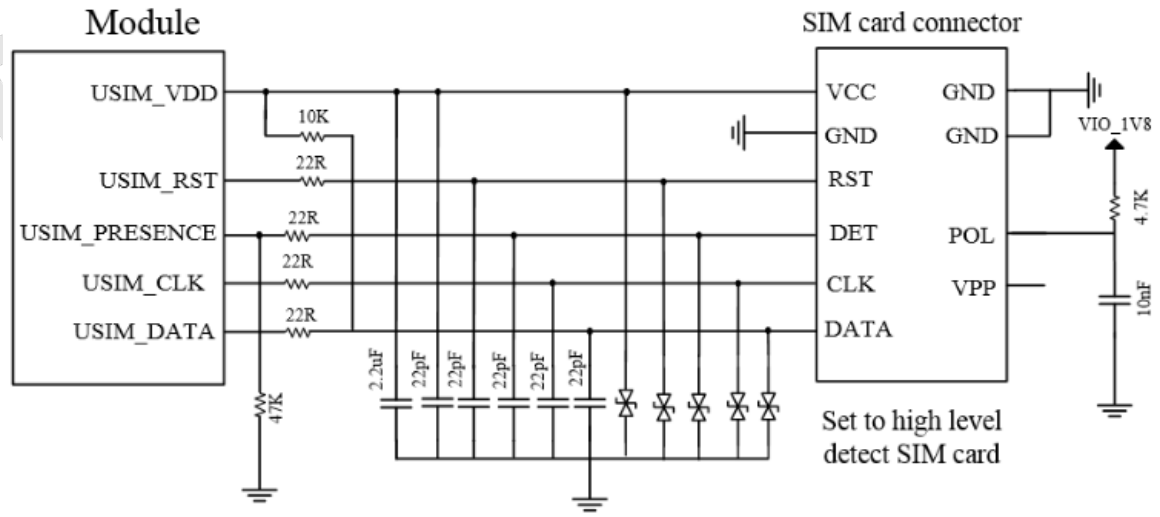


Figure 3-8 (U)SIM Interface with Card Detection Reference Design

Principles of (U)SIM card connector with card detection signal are as follows.

(U)SIM card plug in, USIM_PRESENCE is high level.
(U)SIM card plug out, USIM_PRESENCE is low level.

3.5.2.2 (U)SIM Card Connector Without Detection Signal

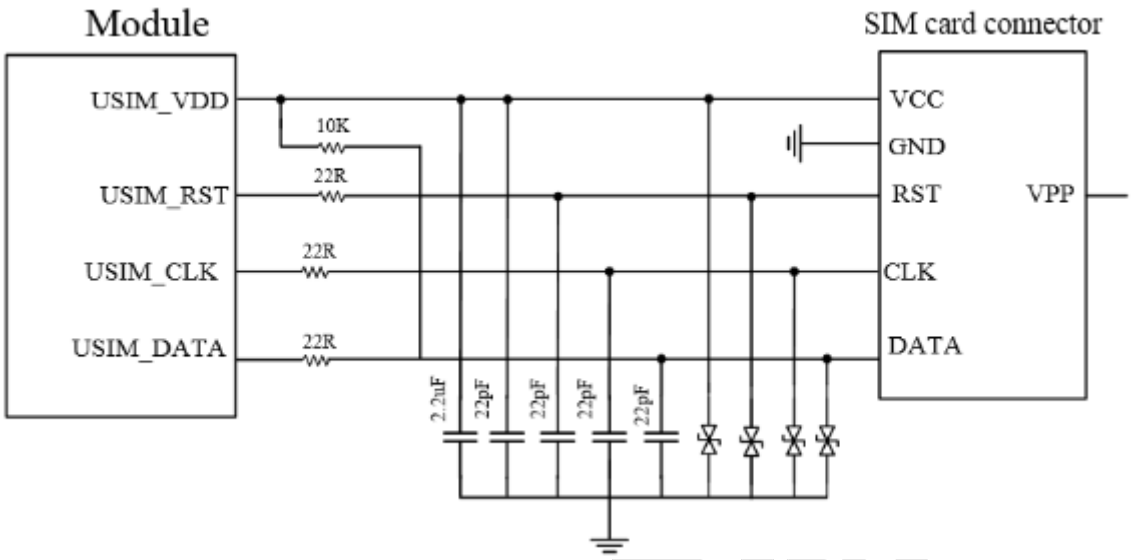


Figure 3-9 (U)SIM Interface without Card Detection Reference Design

(U)SIM card slot without card detection signal, USIM_ PRESENCE Pin remains floating.

3.5.3 (U)SIM Hot Plug

MiniPCIe supports (U)SIM card hot plug function. It determines the insertion and removal of (U)SIM card of the slot by detecting the USIM_PERSENCE pin state to support (U)SIM card hot plug function.

The (U)SIM card hot plug function can be configured by the “AT+MSMPD” command, and the AT commands are shown in the following table.

AT command	(U)SIM card hot plug detection	Function description
AT+MSMPD=1	Enable	Default, (U)SIM card hot plug detection is enabled The module detects whether the (U)SIM card is inserted through the USIM_PRESENCE pin state
AT+MSMPD=0	Close	(U)SIM card hot plug detection function is disabled The module reads the (U)SIM card when the device starts up, and does not detect the USIM_PRESENCE state

Table 3-10 (U)SIM Card Hot Plug Function

After enabling the hot plug detection function of the (U)SIM card, when USIM_PRESENCE is in high level, the module will detect the (U)SIM card insertion and then execute the initialization program of (U)SIM card. After reading the (U)SIM card information, the module will register on the network. When the USIM_PRESENCE is in low level, the module detects that (U)SIM card is removed, then it will not read the (U)SIM card.

Note:

The USIM_PRESENCE is in high level by default, and can be switched to low level by AT command.

AT command	Function description
AT+GTSET=”SIMPHASE”,1	High level detect by default
AT+ GTSET=”SIMPHASE”,0	Low level detect

Table 3-11 USIM_PRESENCE Effective Level Switch AT Command

3.5.4 (U)SIM Design Requirements

(U)SIM card circuit design shall meet EMC standards and ESD requirements, and at the same time, shall improve anti-interference ability to ensure that the SIM card can work stably. The design needs to strictly observe the following rules:

- (U)SIM card slot is placed as close to the module as possible, away from the RF antenna, DCDC power, clock signal lines and other strong interference sources;
- Adopt the (U)SIM card slot with metal shield shell to improve anti-interference ability;
- The length of cable from the module to the (U)SIM card slot shall not exceed 100mm. Longer cable reduces signal quality.
- USIM_CLK and USIM_DATA signals are isolated to avoid mutual interference. If it is difficult to do so, (U)SIM signal needs to be protected as a set;
- The filter capacitor and ESD device of SIM card signal cable are placed close to the (U)SIM card slot. Select 22 ~ 33pF capacitor for ESD device equivalent capacitor.

3.6 UART Interface

3.6.1 UART Interface Definition

Module has two serial ports: the main serial port and debug serial port. The following describes the main features of these two serial ports: the main serial port supports 4800bps, 9600bps, 19200bps, 38400bps, 57600bps, 115200bps, and 230400bps baud rate. The default baud rate is 115200bps, used for data transmission and AT command transmission.

Debug serial port supports 115200bps baud rate for FIBOCOM internal debugging.

The following table describes the main serial port pin:

Pin Name	I/O	Pin Num	Description
UART_CTS	I	30	Clear transmission
UART_RTS	O	25	Requests transmission

Pin Name	I/O	Pin Num	Description
UART_TXD	O	31	Module transmits data
UART_RXD	I	23	Module receives data

Table 3-12 Main Serial Port

The following table describes the debug serial port pin:

Pin Name	I/O	Pin Num	Description
DBG_UART_RX	I	28	Module receives data
DBG_UART_TX	O	46	Module transmits data

Table 3-13 Debug Serial Port

3.6.2 UART Interface Application

The serial interface level of MiniPCIe module is 1.8V. If the level of the client host system is 3.3V or other, a level shifter shall be added to the serial interface connection between the module and the host. The following figure shows the reference circuit design using level shifter chip.

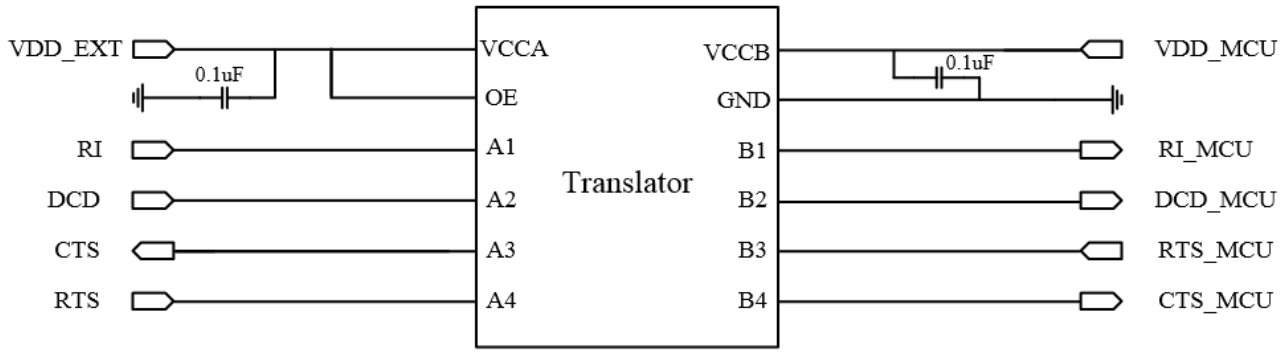


Figure 3-10 UART Signal Connection 1

Another level shift circuit is shown below. The input and output circuit design in the following dashed part can refer to that in the solid line part, but pay attention to the connection direction.

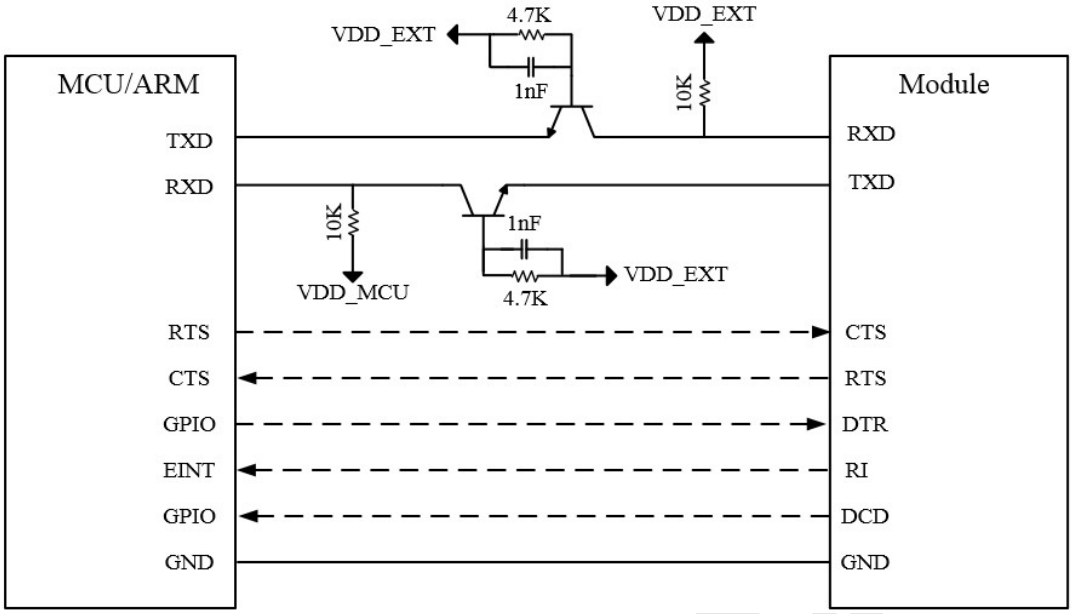


Figure 3-11 UART Signal Connection 2

Note:

This level shift circuit is not suitable for applications with baud rates above 460Kbps.

3.7 Status Indicator

The module provides one signal for displaying the operating status of the module. The status indication pin is shown in the following table.

Pin Name	I/O	Pin Num	Description
NET_MODE	O	42	Module status indication

Table 3-14 Status Indication

3.7.1 NET_MODE Signal

The module provides a network indicator NET_MODE output signal interface.

The status indicator description in the following table.

Mode	Module Network indicator pin status	Indicator light flash/off status	Description
1	600ms Low /600ms High	Flash 600ms on /600ms off	No SIM card Request SIM PIN Registering network (T<15S) Register network failed
2	3000ms Low /75ms High	Slow flash 3000ms on/75ms off	Standby

Mode	Module Network indicator pin status	Indicator light flash/off status	Description
3	75ms Low / 75ms High	Speed flash 75ms on/75ms off	Data link established
4	High	Off	Voice call

Table 3-15 Status Indicator Description

Module's NET_MODE interface reference circuit is shown as follows.

Figure 3-12 NET_MODE Reference Design

3.8 Low Power Consumption Mode

3.8.1 Flight Mode

The module provides one signal for controlling the module's interface to flight mode.

Pin Name	I/O	Pin Num	Description
W_DISABLE#	I	20	Module flight mode control

Table 3-16 Flight Mode

The MiniPCIe module supports two ways to enter the flight mode.

1	Hardware I/O interface button control	First send "AT+WDISABLEEN=1" to enable W_DISABLE# pin function. Pull high or float W_DISABLE# pin (pull high by default), module enter normal mode, pull it down, module enter airplane mode.
2	AT command control	AT+CFUN=4--module enter airplane mode AT+CFUN=1--module enter normal mode

Table 3-17 Ways to Enter the Flight Mode

3.8.2 Sleep Mode

3.8.2.1 USB application (nonsupport USB suspend, nonsupport VBUS)

If the host nonsupport USB suspend and nonsupport VBUS function, the module can enter sleep mode by disconnect USB_VBUS from the external control circuit:

Sleep:

Send AT+GTLPMMODE=1,X command to set the WAKEUP_IN pin's level of control module enter sleep mode. Reset module, command effective.

(X=0, WAKEUP_IN pin is high level, module enter sleep mode;

X=1, WAKEUP_IN pin is low level, module enter sleep mode)

AT+CSCLK=1 command to enable sleep function.

AT+GTUSBDETECTEN=1 command to enable the USB software detection function

AT+GTUSBSLEEPEN=1,0 command to set USB sleep mode

Draw out the USB cable or disable the USB HUB controller, module enter sleep mode.

Wake up:

Plug in USB cable or enable the USB HUB controller can wake up the module.

3.8.2.2 USB application (Supports USB Suspend)

If the host support USB Suspend/Resume. Setting USB sleep in Linux system.

Sleep:

Send AT+GTLPMMODE=1,X command to set the WAKEUP_IN pin's level of control module enter sleep mode. Reset module, command effective.

(X=0, WAKEUP_IN pin is high level, module enter sleep mode;

X=1, WAKEUP_IN pin is low level, module enter sleep mode)

AT+CSCLK=1 command to enable sleep function.

AT+GTUSBSLEEPEN=0,0 command to set USB sleep mode

In Linux system, set the level and control of USB device as auto to suspend the devices of module.

Standing the module and host about 2 seconds, the module can enter suspend mode automatically.

Wake up:

Any operation on USB can wake up the module from sleep mode.

3.8.2.3 UART application (WAKEUP_IN pin level control)

When host and module connected through UART, use the following steps to make the module enter sleep mode:

Sent AT+GTLPMMODE=1,X command to set et the WAKEUP_IN pin's level of control module enter sleep mode. Reset module, command effective.

(X=0, WAKEUP_IN pin is high level, module enter sleep mode;

X=1, WAKEUP_IN pin is low level, module enter sleep mode)

AT+CSCLK=1 command to enable sleep function.

AT+GTUSBSLEEPEN=2,X command to disable USB function (X can be 0 or 1)

Wake up:

The level of WAKEUP_IN pin contrary with that when the module enter sleep mode can wake up module. (X=0, WAKEUP_IN pin is low level, wake up module;

X=1, WAKEUP_IN pin is high level, wake up module)

3.8.2.4 UART application (DTR pin level control)

When host and module connected through UART, use the following steps can make the module enter

Sleep mode:

Send AT+GTLPMMODE=2,X command to set the DTR set pin's level of control module enter sleep mode. Reset module, command effective.

(X=0, DTR pin is high level, module enter sleep mode;

X=1, DTR pin is low level, module enter sleep mode)

AT+CSCLK = 1 command to enable sleep function.

AT+GTUSBSLEEPEN=2,X command to disable USB function (X can be 0 or 1)

The level of DTR pin contrary with that when the module enter sleep mode can wake up module. (X=0, DTR pin is low level, wake up module; X=1, DTR pin is high level, wake up module)

3.8.2.5 ATS24 Command

ATS24 command can also make module enter sleep mode.

Sleep:

Send AT+GTLPMMODE=0 Reset module, command effective.

ATS24=X command to into sleep after X seconds. (X is nonzero integer)

AT+GTUSBSLEEPEN=2,X command to disable USB function (X can be 0 or 1)

Wake up:

Wake up the module by send the AT command fast. If don't send AT commands between X seconds, module will try to enter sleep mode.

Note:

Since the level of UART sleep power is different, power consumption of use ATS24 command to enter sleep mode is higher than that use Pin control to enter sleep mode.

When ATS24 command enter sleep mode countdown, it isn't enter sleep mode once overtime strictly, but try to enter sleep mode. If system don't support after overtime, it will timekeeping automatically.

If you want to use the RI signal to represent the state of the module, please refer to the AT+GTWAKE command in 《FIBOCOM AT Commands User Manual_Sleep 》

For more sleep command description, please refer to 《FIBOCOM AT Commands User Manual_Sleep》

3.9 Digital Audio Interface PCM

The module provides a digital audio interface (PCM) that enables communication with digital audio devices such as external CODECs. The interface signals include the transmission clock PCM_CLK, the frame synchronization signal PCM_SYNC, and the input and output PCM_IN/PCM_OUT.

3.9.1 Support Models

S/N	Product model	Description
1	NL668-EAU-00-MiniPCIe-10	Support
2	NL668-EU-01-MiniPCIe-10	Support
3	NL668-EU-00-MiniPCIe-10	Support
4	NL668-EU-03-MiniPCIe-10	Support

Table 3-18 Support Models

3.9.2 PCM Interface Definition

PIN Name	I/O	PIN Num.	Description
PCM_CLK	IO	45	PCM clock
PCM_OUT	O	47	PCM data output
PCM_IN	I	49	PCM data input
PCM_SYNC	IO	51	PCM data synchronization signal

Table 3-19 PCM Interface Definition

3.9.3 PCM interface description

Single Name	Freq.	Duty Cycle	Coded Format	Operating Mode	Description
PCM_CLK	2.048MHz	50%	16bit Liner mono	Module serves as the master that supports PCM	PCM clock
PCM_OUT	-	-			PCM data output
PCM_IN	-	-			PCM data input
PCM_SYNC	8KHz	Short Pulse			PCM data synchronization signal (Falling edge sampling)

Table 3-20 PCM Interface Description

MiniPCIe adopts the above configuration by default, if you need to make adjustment, please contact our technical support.

3.9.4 PCM Signal Description

The MiniPCIe master chip provides PCM signals using the mainstream European E1 standard. PCM_CLK is a 2.048MHz clock, and 16bit linear format encoding. PCM_SYNC is 8kHz short pulse (488ns).

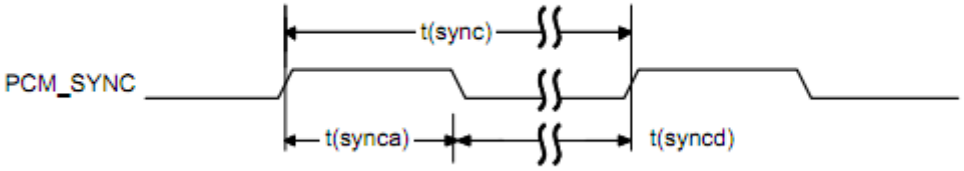


Figure 3-13 PCM_SYNC Timing

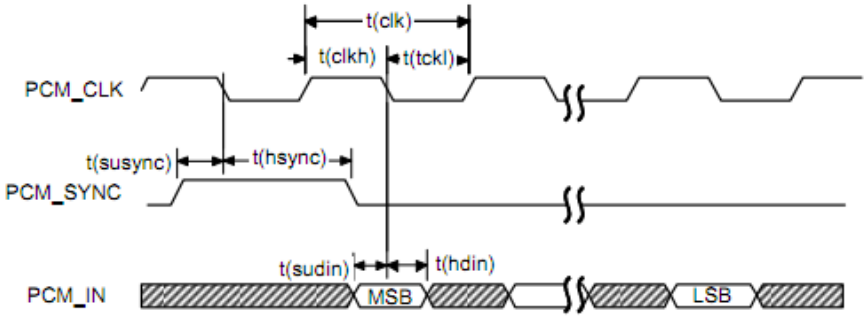


Figure 3-14 PCM_CODEC to MiniPCIe Timing

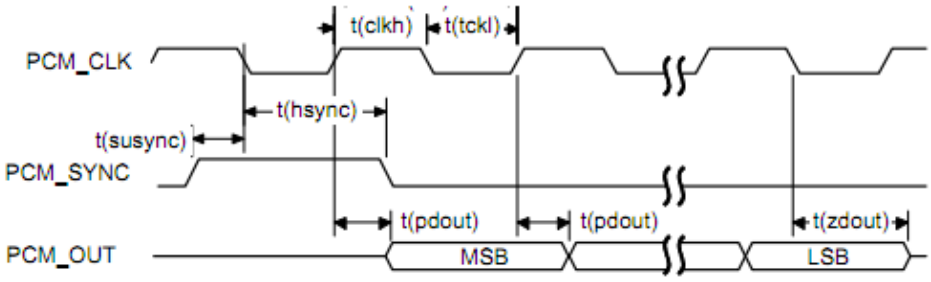


Figure 3-15 MiniPCIe to PCM_CODEC Timing

Parameter		Min	Typ	Max	Unit
t(sync)	PCM_SYNC cycle time	–	125	–	μs
t(synca)	PCM_SYNC asserted time	–	488	–	ns
t(syncd)	PCM_SYNC deasserted time	–	124.5	–	μs

Parameter		Min	Typ	Max	Unit
t(clk)	PCM_CLK cycle time	–	488	–	ns
t(clkh)	PCM_CLK high time	–	244	–	ns
t(clkl)	PCM_CLK low time	–	244	–	ns
t(susync)	PCM_SYNC offset time to PCM_CLK falling	–	122	–	ns
t(sudin)	PCM_DIN setup time to PCM_CLK falling	60	–	–	ns
t(hdin)	PCM_DIN hold time after PCM_CLK falling	10	–	–	ns
t(pdout)	Delay from PCM_CLK rising to PCM_DOUT valid	–	–	60	ns
t(zdout)	Delay from PCM_CLK falling to PCM_DOUT high impedance	–	160	–	ns

Table 3-21 CODEC Timing Parameters

4 Antenna Interface

The module provides three antenna interfaces, MAIN, DIV, and GNSS. The main set is used to receive and transmit signal, and the diversity set is only used to receive the RF signal.

4.1 Operating band

Operating Band	Description	Mode	Tx (MHz)	Rx (MHz)
Band 1	IMT 2100MHz	LTE FDD/WCDMA	1920 - 1980	2110 - 2170
Band 3	DCS 1800MHz	LTE FDD/GSM	1710 - 1785	1805 - 1880
Band 5	CLR 850MHz	LTE FDD/WCDMA/GSM	824 - 849	869 - 894
Band 7	IMT-E 2600Mhz	LTE FDD	2500 - 2570	2620 - 2690
Band 8	E-GSM 900MHz	LTE FDD/WCDMA/GSM	880 - 915	925 - 960
Band 20	EUDD 800MHz	LTE FDD	832 - 862	791 - 821
Band 28	700MHz	LTE FDD	703 - 748	758 - 803
Band 38	IMT-E 2600MHz	LTE TDD	2570 - 2620	
Band 40	IMT 2300MHz	LTE TDD	2300 - 2400	
Band 41	BRS/EBS 2500MHZ	LTE TDD	2555~2655	

Table 4-1 Antenna Operating Band

4.2 Transmission Power

The transmission power of each band of the module is shown in the following table.

Mode	Band	Tx Power(dBm)	Note
GSM	GSM 850	32.5+1/-1.5	
	GSM 900	32.5+1/-1.5	
	DCS 1800	29.5+1/-1.5	
WCDMA	Band I	23.5+1/-1.5	
	Band V	23.5+1/-1.5	
	Band VIII	23.5+1/-1.5	
LTE FDD	Band 1	23+1/-1.5	10MHz Bandwidth, 1 RB, QPSK
	Band 3	23+1/-1.5	10MHz Bandwidth, 1 RB, QPSK
	Band 5	23+1/-1.5	10MHz Bandwidth, 1 RB, QPSK

Mode	Band	Tx Power(dBm)	Note
	Band 7	23+1/-1.5	10MHz Bandwidth, 1 RB, QPSK
	Band 8	23+1/-1.5	10MHz Bandwidth, 1 RB, QPSK
	Band 20	23+1/-1.5	10MHz Bandwidth, 1 RB, QPSK
	Band 28	23+1/-1.5	10MHz Bandwidth, 1 RB, QPSK
LTE TDD	Band 38	23+1/-1.5	10MHz Bandwidth, 1 RB, QPSK
	Band 40	23+1/-1.5	10MHz Bandwidth, 1 RB, QPSK
	Band 41	23+1/-1.5	10MHz Bandwidth, 1 RB, QPSK

Table 4-2 Transmission Power

4.3 Receiving Sensitivity

The sensitivity of each band of the module is shown in the following table.

Mode	Band	Rx Sensitivity(dBm) PRX Typical	Rx Sensitivity(dBm) DRX Typical	Note
GSM	GSM 850	-109	-	BER<2.43%
	GSM 900	-109.5	-	BER<2.43%
	DCS 1800	-109	-	BER<2.43%
WCDMA	Band 1	-111	-	BER<0.1%
	Band 5	-111	-	BER<0.1%
	Band 8	-111	-	BER<0.1%
LTE FDD	Band 1	-98.5	-99	10MHz Band width
	Band 3	-99	-99	10MHz Band width
	Band 5	-98.5	-99	10MHz Band width
	Band 7	-97	-97.5	10MHz Band width
	Band 8	-98.5	-98.5	10MHz Band width
	Band 20	-98.5	-99	10MHz Band width
	Band 28	-97.5	-99	10MHz Band width
LTE TDD	Band 38	--98	-96.5	10MHz Band width
	Band 40	-98	-97	10MHz Band width
	Band 41	-97	-96.5	10MHz Band width

Table 4-3 Receiving Sensitivity

Note:

The sensitivity in the above table is the result of the main and diversity separating test. If testing prx and drx together. It can be 3dB improved

4.4 GNSS Receiver

The module supports the GPS/GLONASS/BeiDou functions using Qualcomm Gen8 technology.

Description		Condition	Typ.
Current consumption (AT+CFUN=0)		GNSS fixing	62mA
		GNSS tracking	62mA
		Standby	33mA
TTFF	GNSS	Cold start	45s
		Warm start	40s
		Hot Start	5s
Sensitivity	fixing		-145dbm
	tracking		-156dbm
	CN0	GNSS Signal@-130dBm	38.5dB-HZ
Positional Accuracy	CEP	GNSS Signal @-130dBm	<3m

Table 4-4 GNSS Receiver

4.5 Antenna Installation

4.5.1 Antenna RF Connector

The module provides three RF connectors. It is recommended that the application uses a matching RF adapter cable. MAIN is the RF main antenna interface, DIV is the diversity antenna interface, and GNSS is the GNSS antenna interface.

The RF connector of the module uses an I-PEX 20279 (MHF), with a dimension of 3.1*3.0*1.25mm, as shown in Figure 4-1.

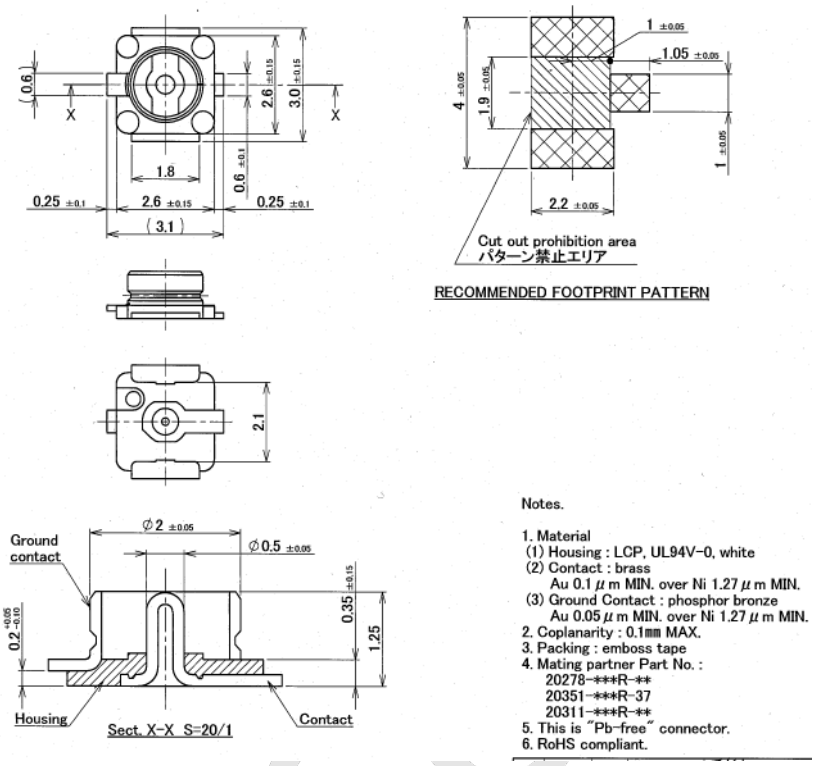


Figure 4-1 RF Connector Dimension

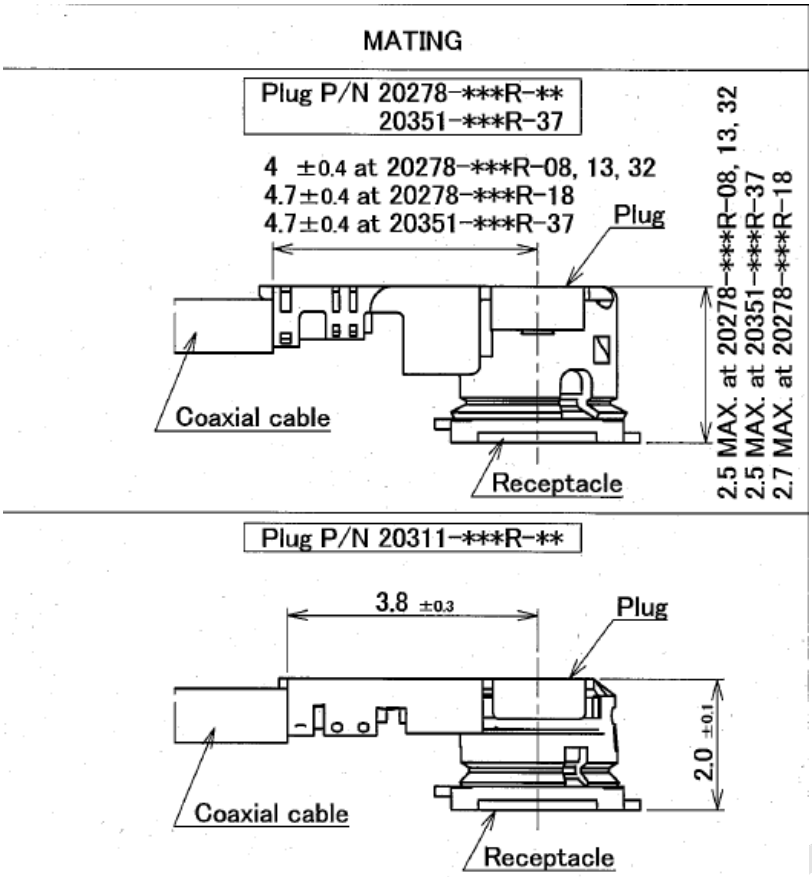


Figure 4-2 Coaxial Cable RF connector Plugs into RF Receptacle

4.6 Antenna Design

4.6.1 Antenna Design Requirement

1) Antenna efficiency

Antenna efficiency is the ratio of antenna input power to emissivity. Due to the antenna return loss, material loss, and coupling loss, the radiated power is always lower than the input power. Recommend> 40% (-4dB).

2) S11 or VSWR

S11 shows that the matching degree of the antenna's 50 ohm impedance, to a certain extent, affects the antenna efficiency. VSWR test methods can be used to measure this parameter. Recommend S11 <-10dB.

3) Polarization

Polarization is the rotation direction of the electric field in the maximum radiation direction of the antenna. It is recommended to use linear polarization.

4) Radiation pattern

Radiation pattern refers to the antenna's electromagnetic field strength in the far field in all directions. Half-wave dipole antenna is the most suitable terminal antenna. For built-in antenna, PIFA antennas or IFA antennas are recommended:

Antenna area: 6mm high*10mm wide*100mm long.

Antenna radiation direction: Omni_directional.

5) Gain and directivity

Antenna directivity refers to the electromagnetic field strength of electromagnetic wave in all directions. Gain is a collection of antenna benefits and antenna directivity.

Recommended antenna gain ≤2.5dBi.

6) Interference

In addition to the antenna performance, other interferences on the PCB also may affect the performance of the module. In order to ensure the high performance of the module, interference must be controlled.

Suggestions: For example, LCD, CPU, FPC cable, audio circuit, power supply should be as far as possible away from the antenna, and make the appropriate isolation and shielding, or filtering on the path.

7) Antenna parameter requirements

Module main antenna requirements	
Frequency range	It must use the most suitable antenna to adapt to the relevant band
Bandwidth （GSM/EDGE）	GSM900: 80 MHz GSM850: 70 MHz GSM1800(DCS): 170 MHz
Bandwidth (WCDMA)	WCDMA band I (2100): 250 MHz WCDMA band V (850): 70 MHz WCDMA band VIII (900): 80 MHz
Bandwidth (LTE)	LTE band 1(2100): 250 MHz LTE Band 3(1800): 170 MHz LTE Band 5(850): 70 MHz LTE Band 7(2600): 190 MHz LTE Band 8(900): 80 MHz LTE Band 20(800): 71 MHz LTE Band 28(700): 100 MHz LTE band 38(2600): 50 MHz LTE band 40(2300): 100 MHz LTE band 41(2500): 100 MHz

Module main antenna requirements	
Impedance	50 ohms
Input power	> 33dBm (2 W) peak power GSM > 23dBm average power WCDMA & LTE
Standing wave ratio recommended	≤ 2:1

Figure 4-3 Main Antenna Requirements

4.6.2 Antenna reference design

Antenna is a sensitive device, susceptible to the external environment. For example, the size of the module, the location of the antenna, the space it occupies, and the surrounding ground all may affect antenna performance. In addition, the RF cable connect with antenna, and the location of the fixed antenna also may affect its performance. Module's three antenna all led by welding plate. recommended clients use the U.FL-R-SMT-1 antenna connector and corresponding match adapter cable. The folllowing figure is reference design of main antenna and diversity antenna.

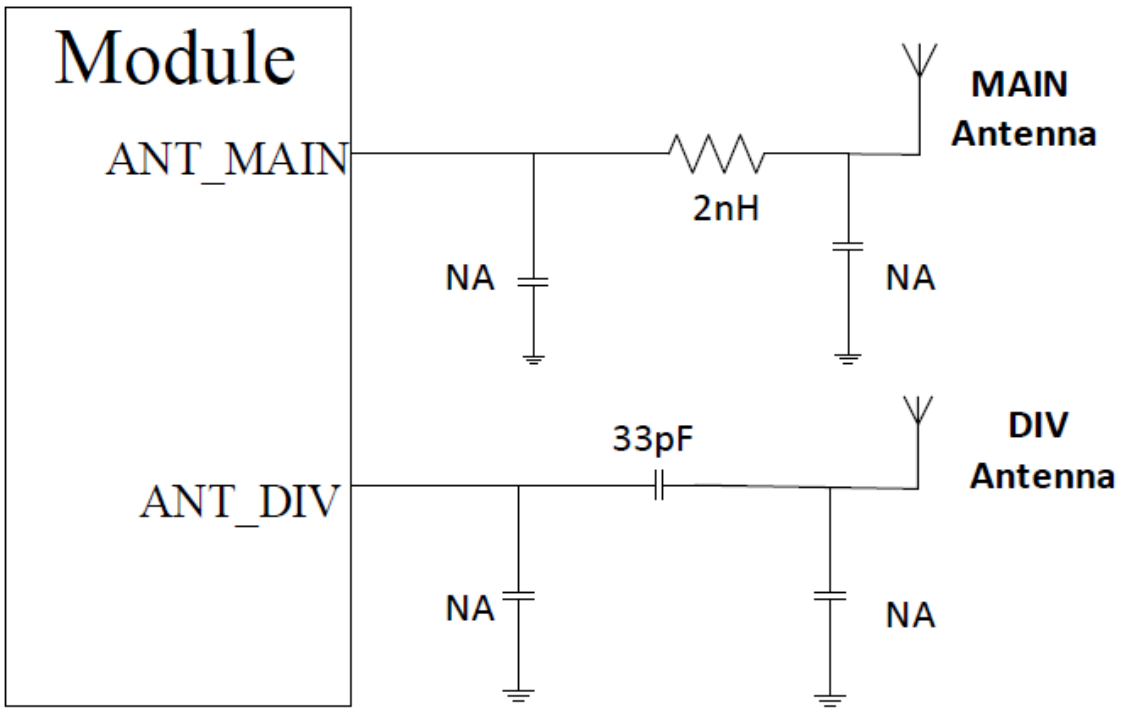


Figure 4-4 Main and diversity Antenna Reference Circuit

Reference design of GNSS antenna:

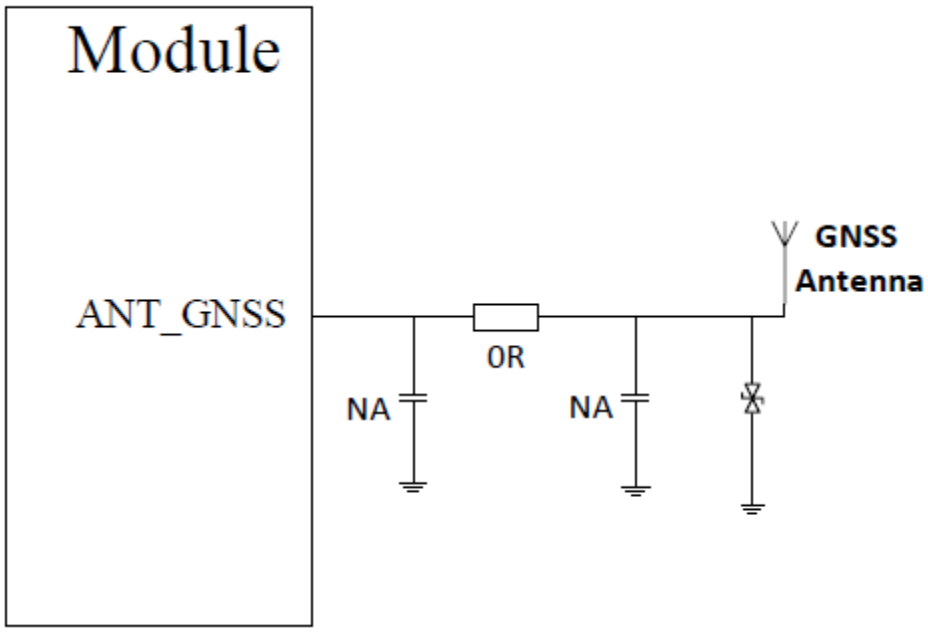


Figure 4-5 GNSS Antenna Reference Circuit

Note：

- All matches must be placed close to antenna to make sure the characteristic impedance of transmission cable is 50 ohms.
- Since the antenna loss should be less than 0.3dB, keep PCB cable as short as possible.
- Keep the PCB LAYOUT straight, and reduce holes on the route to another layer; also avoid right-angle and acute-angle wiring.
- PCB cable should have a good reference ground to avoid other signal cable near the antenna.
- Recommend a complete ground level, and use this complete ground level as a reference ground.
- Ground around antenna must be keep connect with main ground.
- For more design information please refer to《FIBOCOM RF Antenna Application Design Instruction》

5 Electrical Characteristics

5.1 Limiting Voltage Range

The limiting voltage range refers to the power voltage of the module and the maximum voltage range that the digital and analog input/output interfaces can withstand. Operating outside this range may result in damage to the product.

The voltage range of MiniPCIe is shown in the following table.

Parameter	Description	Min	Typ	Max	Unit
VBAT	Power	-0.3	-	4.7	V
GPIO	Digital IO level power voltage	-0.3	-	2.0	V

Table 5-1 Limiting Voltage Range

5.2 Environment Temperature Range

Module is recommended to operate at -30~+75℃ ambient. It is recommended that the application uses temperature control measures under harsh environmental conditions. At the same time, the limited operating temperature range of the module should be provided. Under these temperature conditions, some RF parameters may exceed the limit. It is recommended that the module application terminal be stored in certain temperature conditions. Modules outside this range may not operate or may be damaged.

Temperature	Min	Typ	Max	Unit
Operating temperature	-30	25	75	℃
Limited operating temperature	-40		85	℃
Storage temperature	-40		85	℃

Table 5-2 Environment Temperature Range

5.3 Electrical Characteristics of the Interface in Operating Status

V_L: logic low level;

V_H: logic high level;

Signal	VL		VH		Unit
	Min	Max	Min	Max	
Digital input	-0.3	0.6	1.2	2.0	V
Digital output	-	0.45	1.35	-	V

Parameter	I/O	Min	Typ	Max	Unit
VBAT	I	3.3	3.8	4.3	V
USIM_VDD	O	1.7/2.75	1.8/3	1.9/2.95	V

Table 5-3 Electrical Characteristics of the Interface in Operating Status

5.4 Environmental Reliability Requirements

Test items	Test conditions
Low temperature storage test	Temperature -40℃±3℃, 24 hours in shutdown state
High temperature storage test	Temperature +85℃±3℃, 24 hours in shutdown state
Temperature shock test	In shutdown state, 0.5 hour at -40℃ and +85℃ environment respectively, the temperature conversion time <3min, for 24 cycles
High temperature and humidity test	Temperature +85℃±3℃, humidity 90 ~ 95% RH, 24 hours in shutdown state
Low temperature operating test	Temperature -30℃±3℃, 24 hours in operating state
High temperature operating test	Temperature +75℃±3℃, 24 hours in operating state
Vibration test	Conduct vibration test according to the requirements shown in the table below: Frequency: Random vibration ASD (Acceleration Spectral Density) 5~20Hz: $0.96m^2/s^3$ 20~500Hz: $0.96m^2/s^3$(20Hz), other -3dB/octave
Connector life test	50 times of insertion/removal for connector interface; 30 times of insertion/removal for RF antenna interface cable

Table 5-4 Environmental Reliability Requirements

5.4.1 ESD Characteristics

MiniPCIe is a consumer product. Although the design of the module has considered the ESD issue and provided ESD protection, the ESD issue may occur in the transport and secondary development, so developers should consider ESD protection for the final product. In addition to considering anti-static

treatment for packaging, please refer to recommended circuit for interface design in the document for client's application.

Refer to the following table for the ESD allowable discharge range of the MiniPCIemodule.

Part	Air discharge	Contact discharge
VBAT, GND	±10KV	±5KV
Antenna port	±8KV	±4KV
Other port	±2KV	±1KV

Table 5-5 ESD Allowable Discharge Range

6 Structure Specification

6.1 Product Appearance

The product appearance of NL668-EAU-MiniPCIe-10 module is shown in Figure 6-1:

Figure 6-1 NL668-EAU-MiniPCIe-10 Module Product Appearance (Top)

The product appearance of NL668-EU-MiniPCIe-10 module is shown in Figure 6-2:

Figure 6-2 NL668-EU-MiniPCIe-10 Module Product Appearance (Top)

6.2 Structure Dimension

The structure dimension of the MiniPCIe module is shown in Figure 6-3.

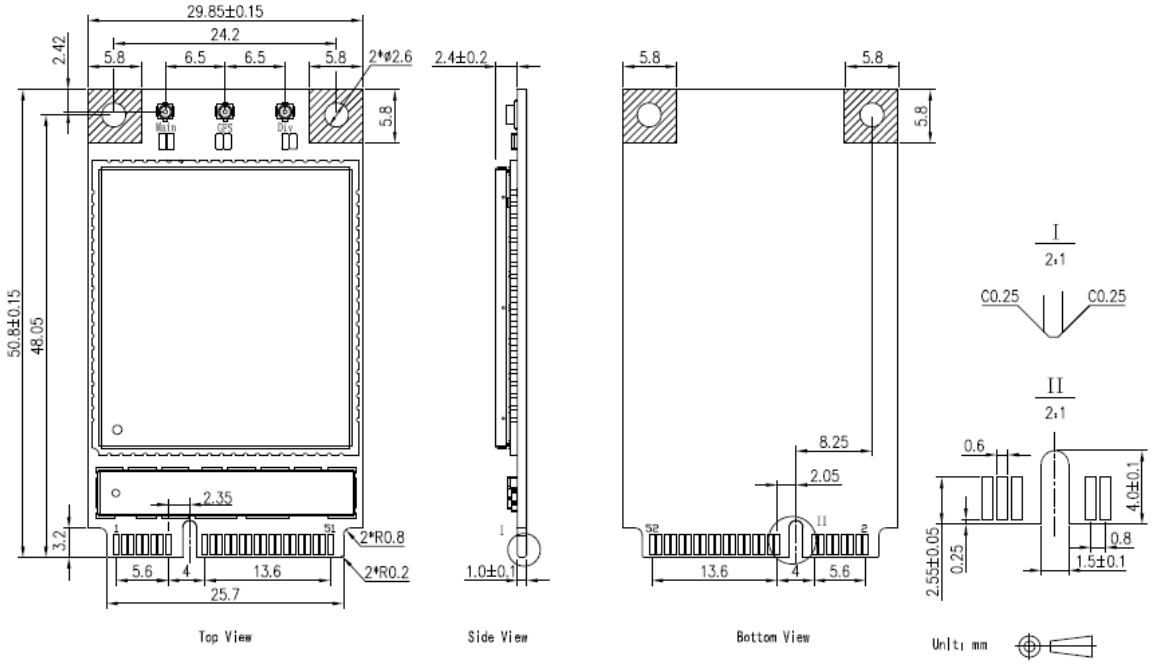


Figure 6-3 Structure Dimension (Unit: mm)

The user board can refer to the Molex's Mini PCI Express connector, model: 67910-0002, shown as follows.

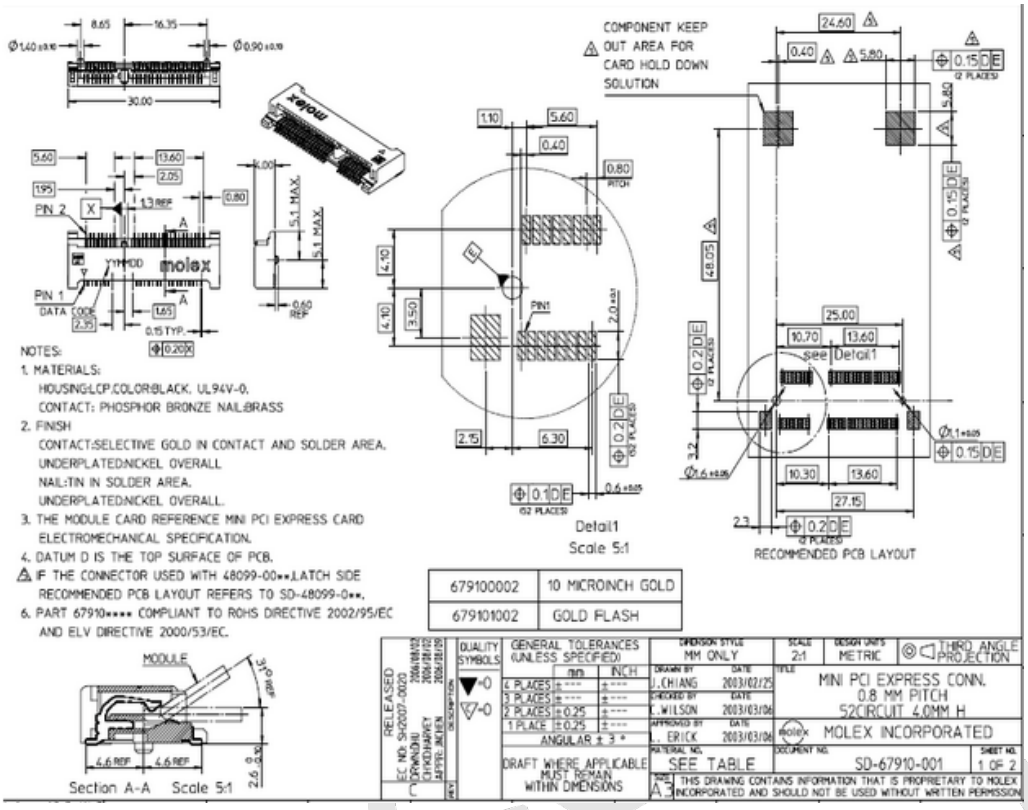


Figure 6-4 67910-0002 Connector

6.3 Packaging

MiniPCIe module adopts tray sealed vacuum packaging, combined with the outer packaging method using the hard carton box, so that the storage, transportation and the usage of modules can be protected to the greatest extent.

Note:

The vacuum bag contains desiccant. The module is a moisture-sensitive device, with moisture sensitive level 3, and it is in line with the standards of the JEDEC. Please avoid permanent damage to the product caused by moisture. The module is a precision electronic product, and may suffer permanent damage if no correct electrostatic protection measures are taken.

6.3.1 Tray Packaging Process

Tray packaging process, see Figure 6-5.

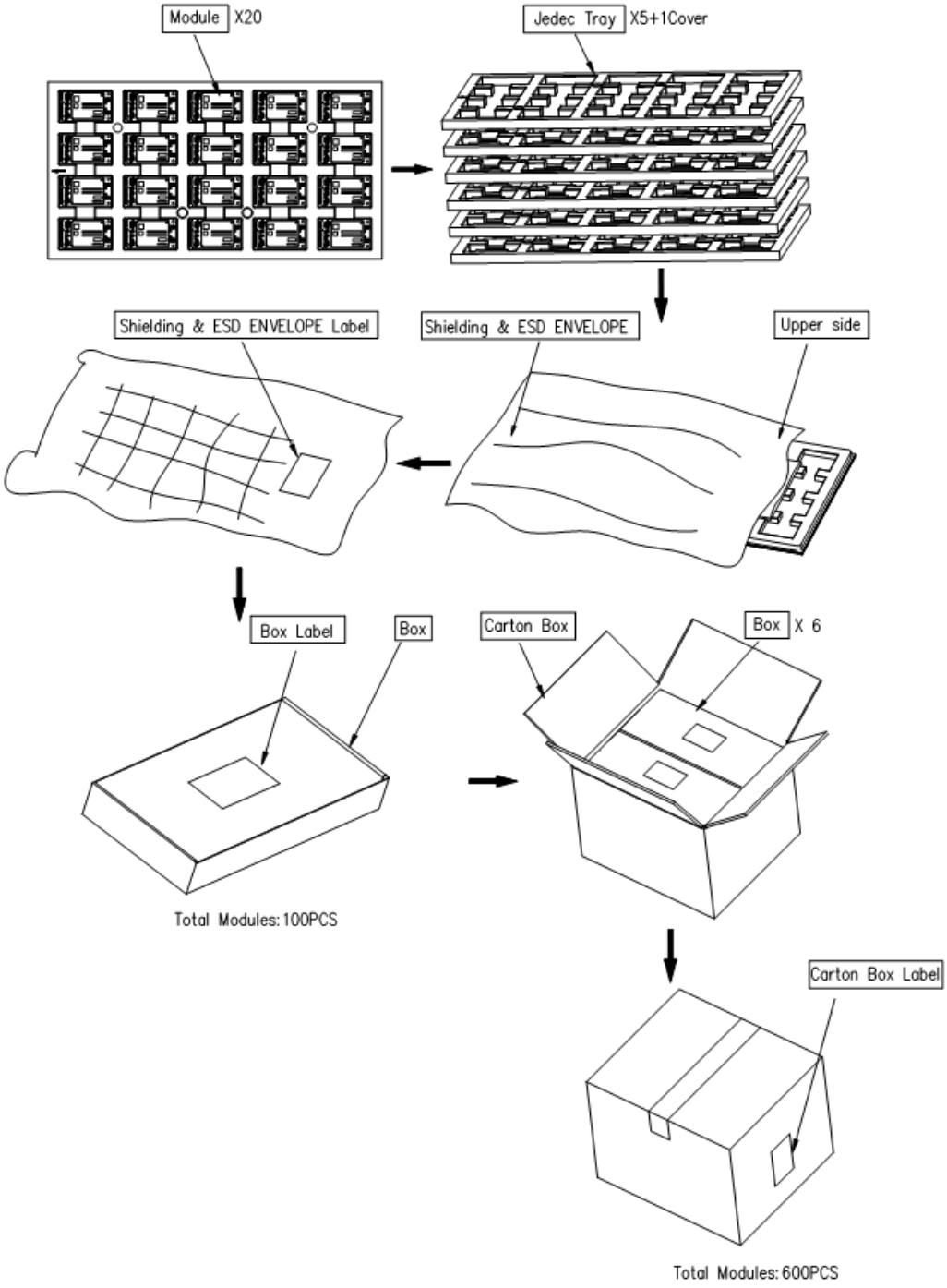


Figure 6-5 Tray Packaging Process

6.3.2 Tray Dimension

The tray dimension is shown in Figure 6-5.

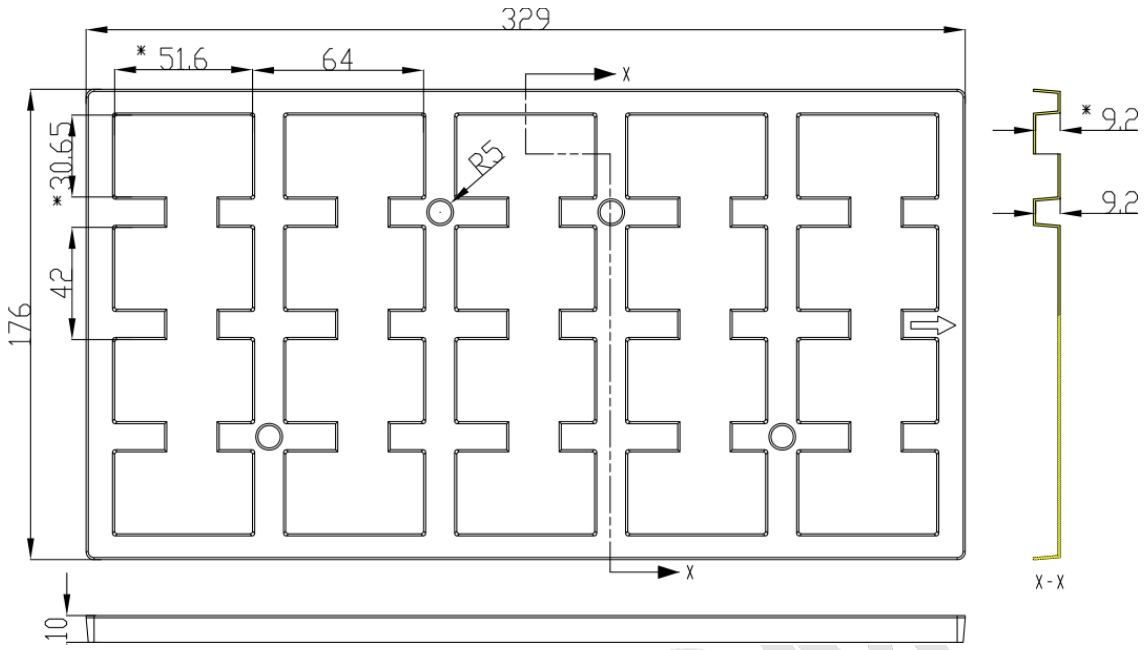


Figure 6-6 Tray Dimension (Unit: mm)

Appendix A GPRS and EGPRS Encoding Scheme

Encoding method	CS-1	CS-2	CS-3	CS-4
Rate	1/2	2/3	3/4	1
USF	3	3	3	3
Pre-coded USF	3	6	6	12
Radio Block excl.USF and BCS	181	268	312	428
BCS	40	16	16	16
Tail	4	4	4	-
Coded Bits	456	588	676	456
Punctured Bits	0	132	220	-
Data rate Kb/s	9.05	13.4	15.6	21.4

Table A- 0-1 GPRS encoding scheme

In the GPRS standard, 29 types of GPRS multislot modes are defined for use by mobile stations. The multislots class defines the maximum rate of uplink and downlink. The expression is 3+1 or 2+2, the first number indicates the number of downlink timeslots, and the second number indicates the number of uplink timeslots. Active timeslots indicates the total number of timeslots that the GPRS device can use for both uplink and downlink communications.

Multislot Class	Downlink Slots	Uplink Slots	Active Slots
1	1	1	2
2	2	1	3
3	2	2	3
4	3	1	4
5	2	2	4
6	3	2	4

Multislot Class	Downlink Slots	Uplink Slots	Active Slots
7	3	3	4
8	4	1	5
9	3	2	5
10	4	2	5
11	4	3	5
12	4	4	5
33	5	4	6

Table A-0-2 Multilevel Multislot Allocation

Coding Scheme	Modulation	Coding Family	1 Timeslot	2 Timeslot	4 Timeslot
CS-1	GMSK	/	9.05kbps	18.1kbps	36.2kbps
CS-2	GMSK	/	13.4kbps	26.8kbps	53.6kbps
CS-3	GMSK	/	15.6kbps	31.2kbps	62.4kbps
CS-4	GMSK	/	21.4kbps	42.8kbps	85.6kbps
MCS-1	GMSK	C	8.80kbps	17.6kbps	35.2kbps
MCS-2	GMSK	B	11.2kbps	22.4kbps	44.8kbps
MCS-3	GMSK	A	14.8kbps	29.6kbps	59.2kbps
MCS-4	GMSK	C	17.6kbps	35.2kbps	70.4kbps
MCS-5	8-PSK	B	22.4kbps	44.8kbps	89.6kbps
MCS-6	8-PSK	A	29.6kbps	59.2kbps	118.4kbps
MCS-7	8-PSK	B	44.8kbps	89.6kbps	179.2kbps
MCS-8	8-PSK	A	54.4kbps	108.8kbps	217.6kbps
MCS-9	8-PSK	A	59.2kbps	118.4kbps	236.8kbps

Table A-0-3 EGPRS Modulation And encoding Method

Appendix B Terms and Acronyms

Terms	Description
AMR	Adaptive Multi-rate
bps	Bits Per Second
CS	Coding Scheme
DRX	Discontinuous Reception
EGSM	Extended GSM900 Band
FDD	Frequency Division Duplexing
GMSK	Gaussian Minimum Shift Keying
GSM	Global System for Mobile Communications
HSDPA	High Speed Down Link Packet Access
IMEI	International Mobile Equipment Identity
Imax	Maximum Load Current
LED	Light Emitting Diode
LSB	Least Significant Bit
LTE	Long Term Evolution
SCell	Secondary Cell for CA
ME	Mobile Equipment
MS	Mobile Station
MT	Mobile Terminated
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PSK	Phase Shift Keying

Terms	Description
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RHCP	Right Hand Circularly Polarized RMS
RMS	Root Mean Square
RTC	Real Time Clock
Rx	Receive
SMS	Short Message Service
TDMA	Time Division Multiple Access
TE	Terminal Equipment
TX	Transmitting Direction
TDD	Time Division Duplexing
UART	Universal Asynchronous Receiver & Transmitter
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
(U)SIM	(Universal) Subscriber Identity Module
USSD	Unstructured Supplementary Service Data
Vmax	Maximum Voltage Value
Vnorm	Normal Voltage Value
Vmin	Minimum Voltage Value
VIHmax	Maximum Input High Level Voltage Value
VIHmin	Minimum Input High Level Voltage Value
VILmax	Maximum Input Low Level Voltage Value

Terms	Description
VILmin	Minimum Input Low Level Voltage Value
VImax	Absolute Maximum Input Voltage Value
VImin	Absolute Minimum Input Voltage Value
VOHmax	Maximum Output High Level Voltage Value
VOHmin	Minimum Output High Level Voltage Value
VOLmax	Maximum Output Low Level Voltage Value
VOLmin	Minimum Output Low Level Voltage Value
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access

Table B-0-1Terms and Acronyms