



**SPECIFICATION
FOR
LCM Module
KD060HDFID001**

MODULE:	KD060HDFID001
CUSTOMER:	

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STARTEK	INITIAL	DATE
PREPARED BY		
CHECKED BY		
APPROVED BY		

CUSTOMER	INITIAL	DATE
APPROVED BY		

ISO9001:2008 ISO15169:2009

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*** Description**

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorphous silicon TFT as a switching device. This module is composed of a Transmissive type TFT-LCD Panel, driver circuit, back-light unit. The resolution of a 6.0" TFT-LCD contains 720x1440 pixels, and can display up to 16.7M colors.

*** Features**

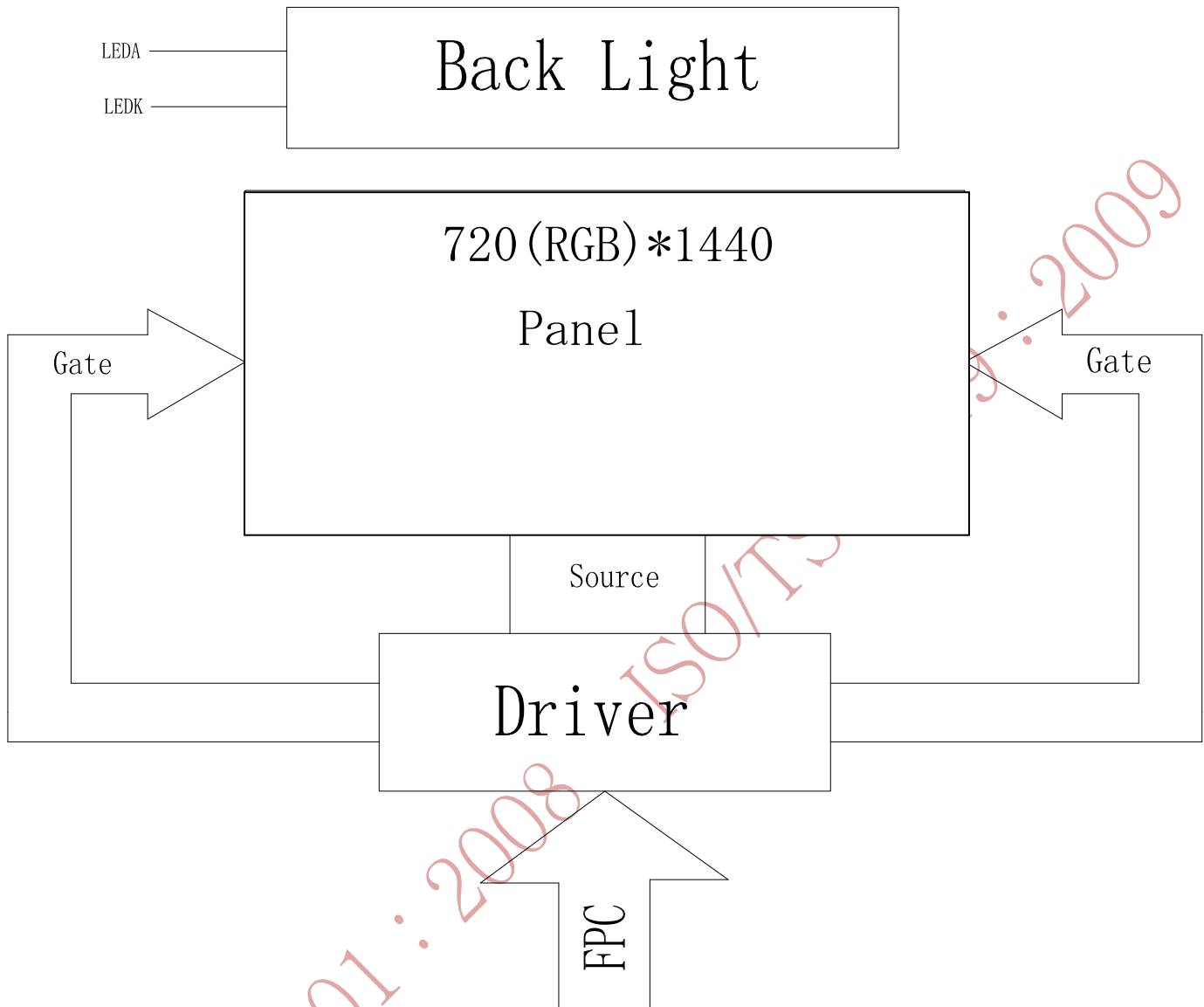
- Low Input Voltage: 3.3V(TYP)
- Display Colors of TFT LCD: 16.7M colors
- Interface: 4 Lane MIPI interface.

General Information Items	Specification	Unit	Note
	Main Panel		
Display area(AA)	68.04(H)*136.08(V) (6.0 inch)	mm	-
Driver element	TFT active matrix	-	-
Display colors	16.7M	colors	-
Number of pixels	720(RGB)*1440	dots	-
TFT Pixel arrangement	RGB vertical stripe	-	-
Pixel pitch	0.0945(H)*0.0945(V)	mm	-
Viewing angle	ALL	o'clock	-
TFT Controller IC	IL19881C	-	-
Display mode	Transmissive/Normally Black	-	-
Operating temperature	-20~+70	°C	-
Storage temperature	-30~+80	°C	-

*** Mechanical Information**

Item		Min.	Typ.	Max.	Unit	Note
Module size	Horizontal(H)		75.04		mm	-
	Vertical(V)		147.63		mm	-
	Depth(D)		2.35		mm	-
Weight			52		g	-

1. Block Diagram



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3. Input terminal Pin Assignment

NO.	SYMBOL	DISCRIPTION	I/O
1	NC	--	--
2	LEDK	Cathode pin of backlight.	P
3	NC	--	--
4	LEDA	Anode pin of backlight.	P
5	NC	--	--
6	GND	Ground	P
7	MIPI_D0N	MIPI DSI differential data pair (Data lane 0)	I/O
8	MIPI_D0P		
9	GND	Ground	P
10	MIPI_D1N	MIPI DSI differential data pair (Data lane 1)	I
11	MIPI_D1P		
12	GND	Ground	P
13	MIPI_CLN	MIPI DSI differential data pair .	I
14	MIPI_CLP		
15	GND	Ground.	P
16	MIPI_D2N	MIPI DSI differential data pair (Data lane 2)	I
17	MIPI_D2P		
18	GND	Ground	P
19	MIPI_D3N	MIPI DSI differential data pair (Data lane 3)	I
20	MIPI_D3P		
21	GND	Ground.	P
22	GND	Ground.	P
23	NC	--	--
24	GND	Ground.	P
25	TE	Tearing effect output pin. Leave the pin open when not in use.	O



26	RESET	The external reset input Initializes the chip with a low input .Be sure to execute a power-on reset after supplying power. Fix to IOVCC level when not in use.	I
27	IOVCC	Power supply for I/O pad	I
28	VCI	Power supply for analog circuits.	I
29	GND	Ground.	P
30	GND	Ground.	P

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4. LCD Optical Characteristics

4.1 Optical specification

Item	Symbol	Condition	Min.	Typ.	Max.	Unit.	Note
Contrast Ratio	CR	$\Theta=0$	800	1000	--		(1)(2)
Response time	Rising	Normal viewing angle	--	10	15	msec	(1)(3)
	Falling		--	20	25		
Color gamut	S(%)		65	68	--	%	(1)
Color Filter Chromacity	White	W_X	0.265	0.305	0.345		(1)(4)
		W_Y	0.289	0.329	0.369		
	Red	R_X	0.613	0.633	0.653		
		R_Y	0.317	0.337	0.357		
	Green	G_X	0.293	0.313	0.333		
		G_Y	0.591	0.611	0.631		
	Blue	B_X	0.125	0.145	0.165		
		B_Y	0.056	0.076	0.096		
Viewing angle	Hor.	Θ_L	--	80	--		(1)(4)
		Θ_R	--	80	--		
	Ver.	Θ_U	--	80	--		
		Θ_D	--	80	--		
Option View Direction	Free						(5)

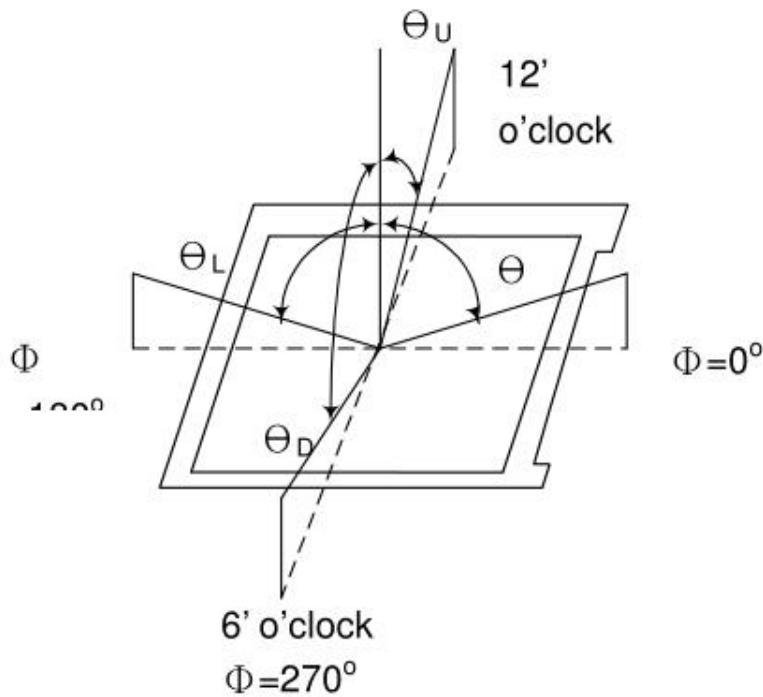
4.2 Measuring Condition

- Measuring surrounding: dark room
- Ambient temperature: $25\pm 2^\circ\text{C}$
- 15min. warm-up time.

4.3 Measuring Equipment

- FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

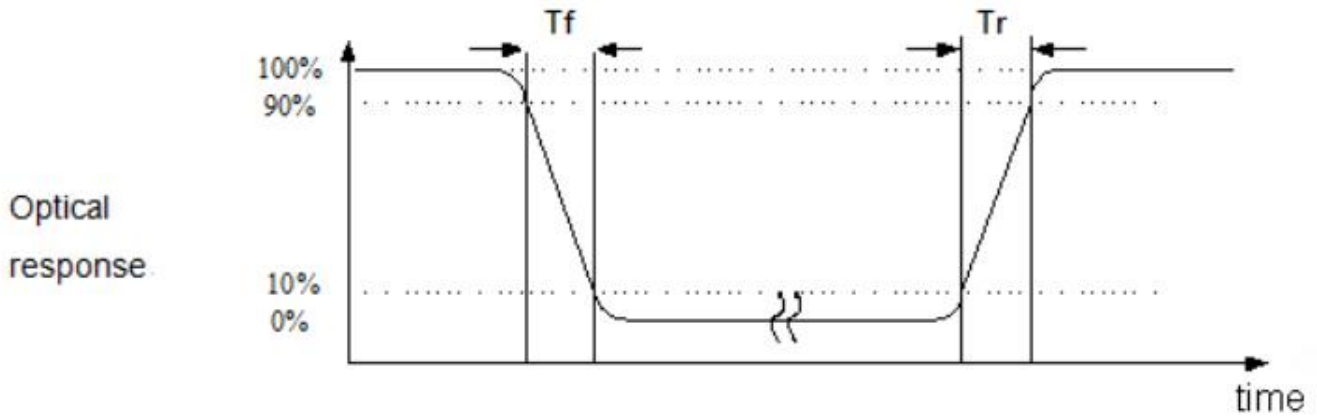
Note (1) Definition of Viewing Angle:



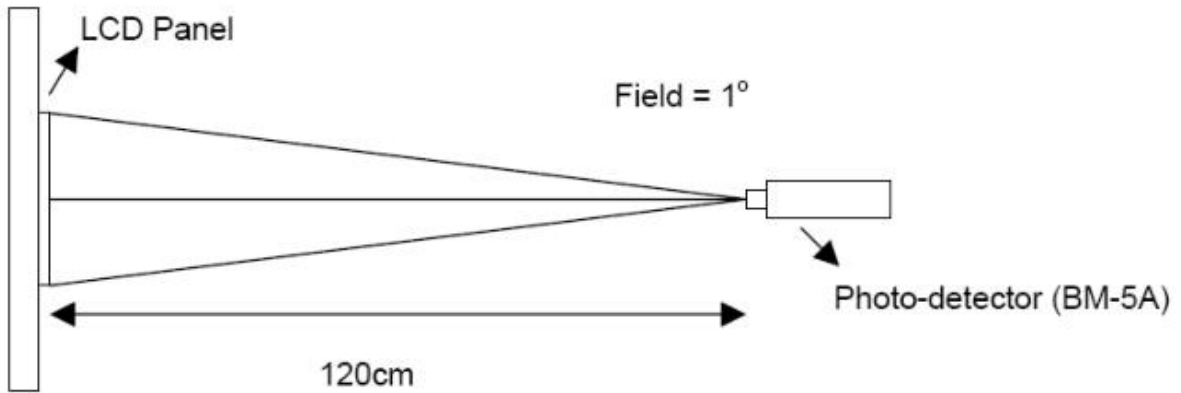
Note (2) Definition of Contrast Ratio (CR) :
measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

Note (3) Definition of Response Time : Sum of T_R and T_F



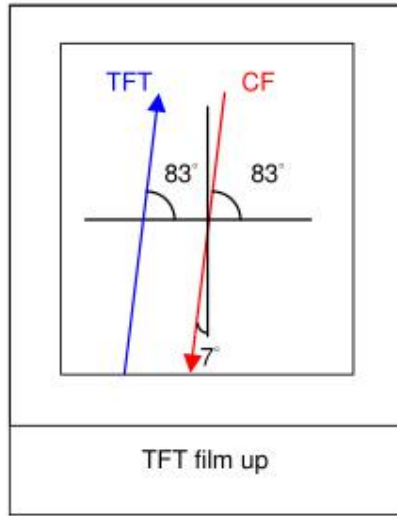
Note (4) Definition of optical measurement setup



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Note (5) Rubbing Direction (The different Rubbing Direction will cause the different optima view direction.)



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5. TFT Electrical Characteristics

5.1 Absolute Maximum Rating (Ta=25 VSS=0V)

Characteristics	Symbol	Min.	Max.	Unit
Digital Supply Voltage	VCI	-0.3	6.5	V
Supply Voltage (Logic)	IOVCC	-0.3	3.3	V
Operating temperature	T _{OP}	-20	+70	°C
Storage temperature	T _{ST}	-30	+80	°C

NOTE: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

5.2 DC Electrical Characteristics

Characteristics	Symbol	Min.	Typ.	Max.	Unit	Note
Digital Supply Voltage	VCI	2.5	3.3	6.0	V	--
Supply Voltage (Logic)	IOVCC	1.65	1.8	3.3	V	--
Normal mode Current consumption	IDD	--	40	--	mA	--
Level input voltage	V _{IH}	0.7I _{OVCC}	--	I _{OVCC}	V	--
	V _{IL}	-0.3	--	0.3 I _{OVCC}	V	--
Level output voltage	V _{OH}	0.8I _{OVCC}	--	I _{OVCC}	V	--
	V _{OL}	GND	--	0.2I _{OVCC}	V	--

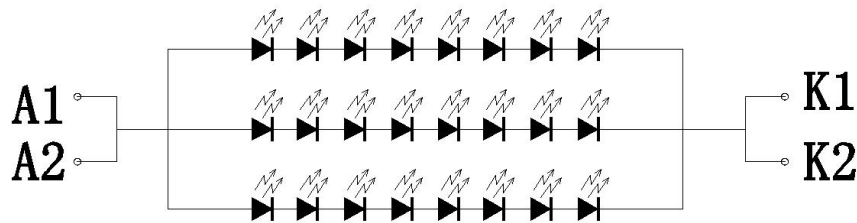
5.3 LED Backlight Characteristics

The back-light system is edge-lighting type with 24 chips White LED

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Forward Current	I_F	--	60	--	mA	--
Forward Voltage	V_F	--	24	--	V	--
LCM Luminance	L_V	540	560	--	cd/m ²	Note3
LED life time	Hr	50000			Hour	Note1,2
Uniformity	AVg	80	--	--	%	Note3

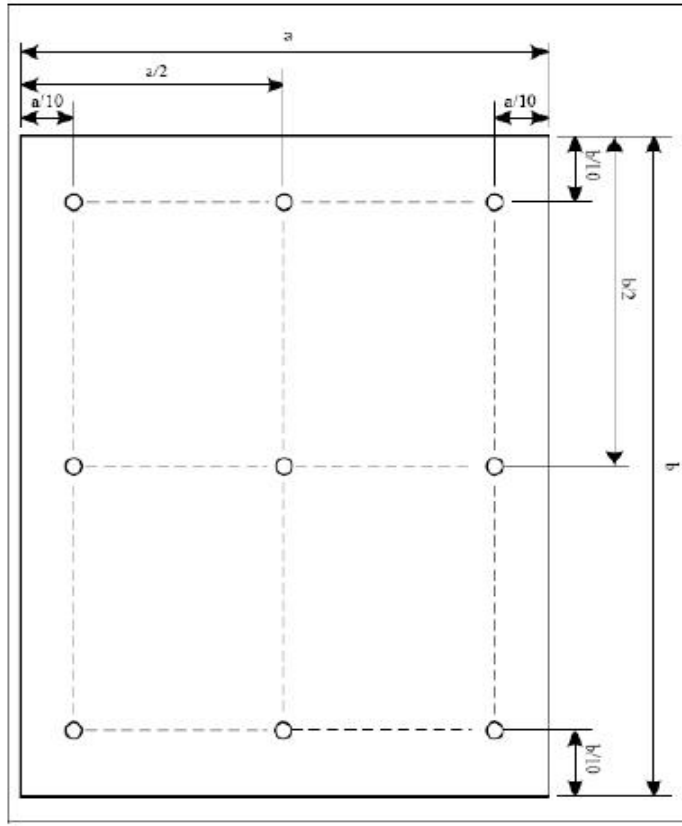
Note (1) LED life time (Hr) can be defined as the time in which it continues to operate under the condition: $T_a=25\pm3\text{ }^\circ\text{C}$, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note (2) The "LED life time" is defined as the module brightness decrease to 50% original brightness at $T_a=25^\circ\text{C}$ and $I_L=60\text{mA}$. The LED lifetime could be decreased if operating I_L is larger than 60mA. The constant current driving method is suggested.



CIRCUIT DIAGRAM

NOTE 3: Luminance Uniformity of these 9 points is defined as below:



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$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

$$\text{Luminance} = \frac{\text{Total Luminance of 9 points}}{9}$$

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6. TFT AC Characteristic

6.1 High Speed Mode – Clock Channel Timing

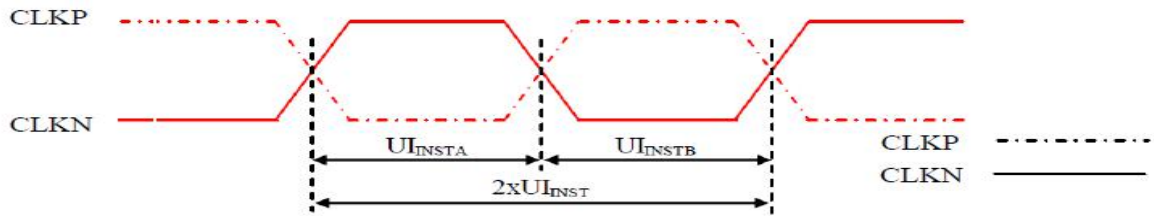


Figure 118: DSI Clock Channel Timing

Table 38: DSI Clock Channel Timing

Signal	Symbol	Parameter	Min	Max	Unit
CLKP/N	$2xUI_{INST}$	Double UI instantaneous	4	25	ns
CLKP/N	UI_{INSTA}, UI_{INSTB} (Note 1)	UI instantaneous Half	2 (Note 2)	12.5	ns

Notes:

1. $UI = UI_{INSTA} = UI_{INSTB}$
2. Define the minimum value of 24 UI per Pixel, see Table 39.

Table 39: Limited Clock Channel Speed

Data type	Two Lanes speed	Three Lanes speed	Four Lanes speed
Data Type = 00 1110 (0Eh), RGB 565, 16 UI per Pixel	566 Mbps	433 Mbps	366 Mbps
Data Type = 01 1110 (1Eh), RGB 666, 18 UI per Pixel	637 Mbps	487 Mbps	412 Mbps
Data Type = 10 1110 (2Eh), RGB 666 Loosely, 24 UI per Pixel	850 Mbps	650 Mbps	550 Mbps
Data Type = 11 1110 (3Eh), RGB 888, 24 UI per Pixel	850 Mbps	650 Mbps	550 Mbps

6.2 High Speed Mode – Data Clock Channel Timing

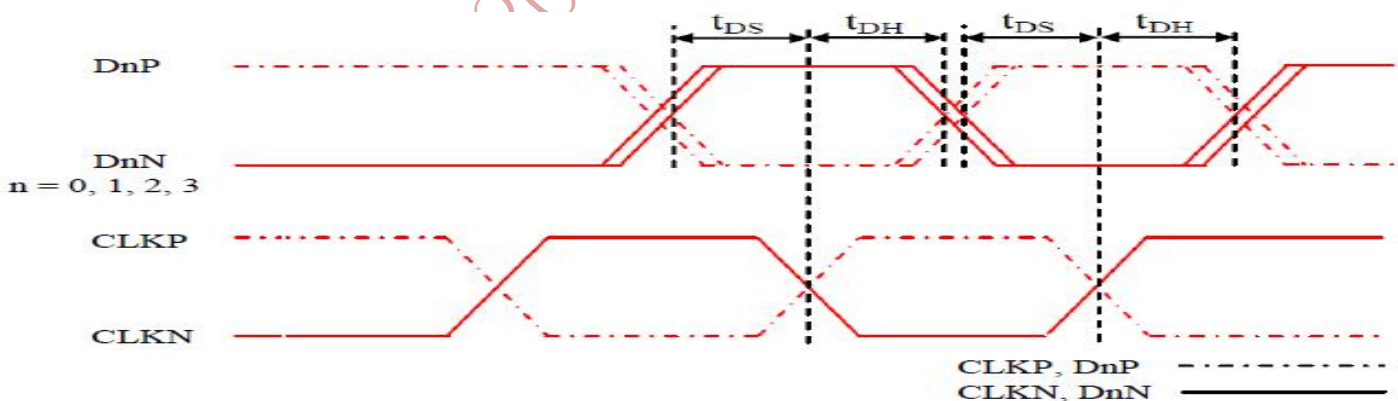


Figure 119: DSI Data to Clock Channel Timings

Table 40: DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min	Max
DnP/N , n=0 and 1	t_{DS}	Data to Clock Setup time	$0.15xUI$	-
	t_{DH}	Clock to Data Hold Time	$0.15xUI$	-

6.3 High Speed Mode – Rise and Fall Timings

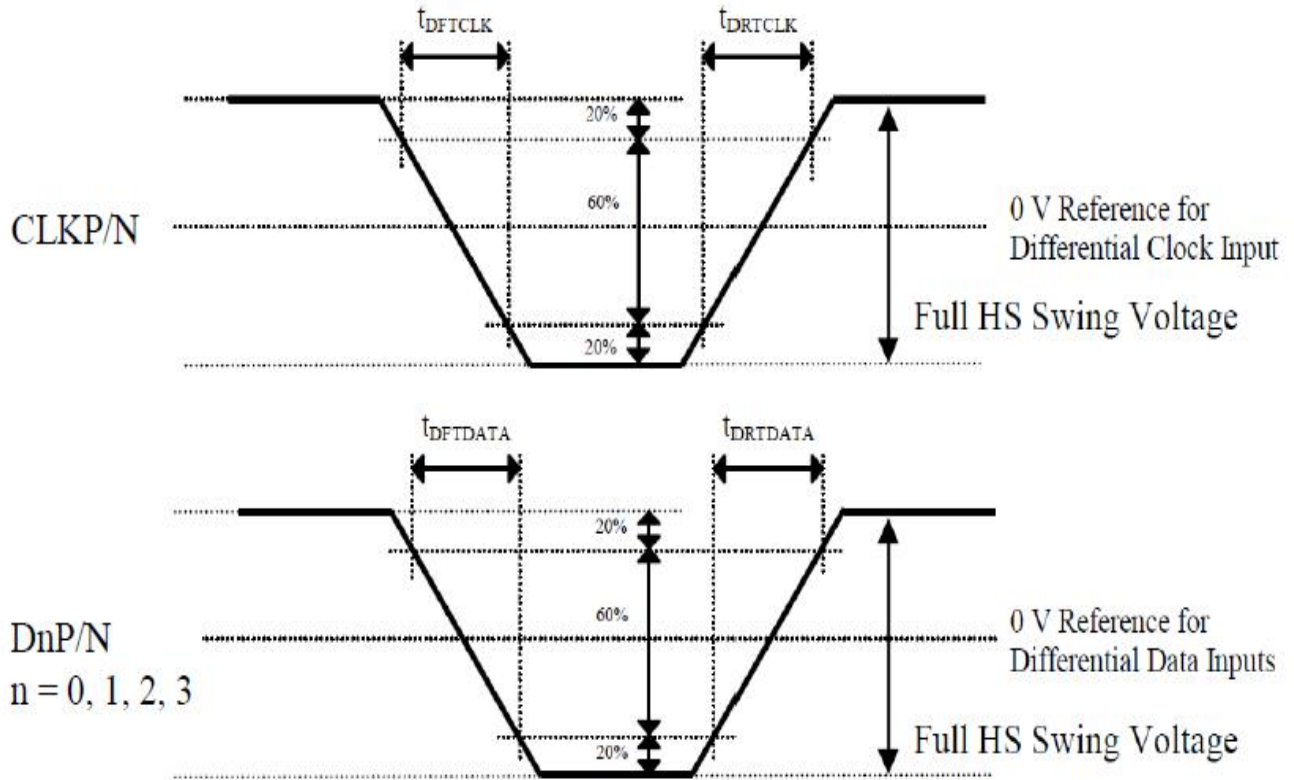


Figure 120: Rising and Falling Timings on Clock and Data Channels

Table 41: Rise and Fall Timings on Clock and Data Channels

Parameter	Symbol	Condition	Specification		
			Min	Typ	Max
Differential Rise Time for Clock	t_{DRTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Rise Time for Data	$t_{DRTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)
Differential Fall Time for Clock	t_{DFTCLK}	CLKP/N	150 ps	-	0.3UI (Note)
Differential Fall Time for Data	$t_{DFTDATA}$	DnP/N n=0 and 1	150 ps	-	0.3UI (Note)

Note: The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-Phy standard.

6.4 Low Speed Mode – Bus Turn Around

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the MCU to the Display Module (ILI9881C) are illustrated for reference purposes below.

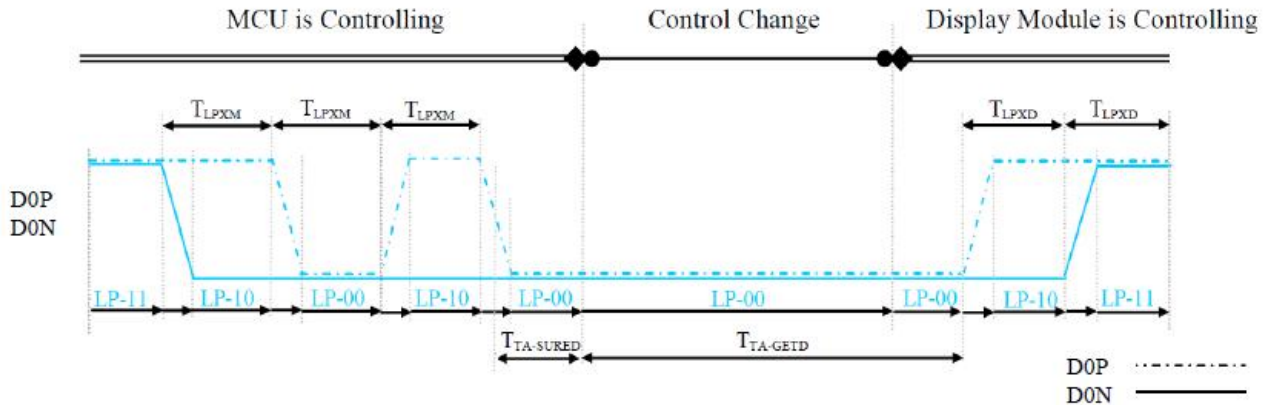
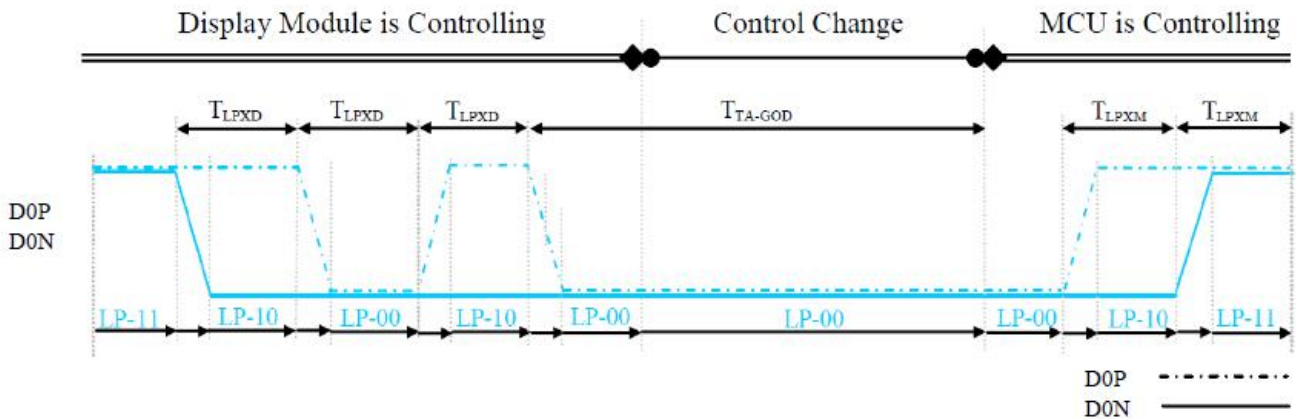


Figure 121: BTA from the MCU to the Display Module

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the Display Module (ILI9881C) to the MCU are illustrated for reference purposes below.



Signal	Symbol	Description	Min	Max	Unit
DOP/N	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MCU → Display Module (ILI9881C)	50	75	ns
DOP/N	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (ILI9881C) → MCU	50	75	ns
DOP/N	$T_{TA-SURED}$	Time-out before the Display Module (ILI9881C) starts driving	T_{LPXD}	$2 \times T_{LPXD}$	ns

Table 43: Low Power State Period Timings – B

Signal	Symbol	Description	Time	Unit
DOP/N	$T_{TA-GETD}$	Time to drive LP-00 by Display Module (ILI9881C)	$5 \times T_{LPXD}$	ns
DOP/N	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MCU	$4 \times T_{LPXD}$	ns

6.5 Data Lanes from Low Power Mode to High Speed Mode

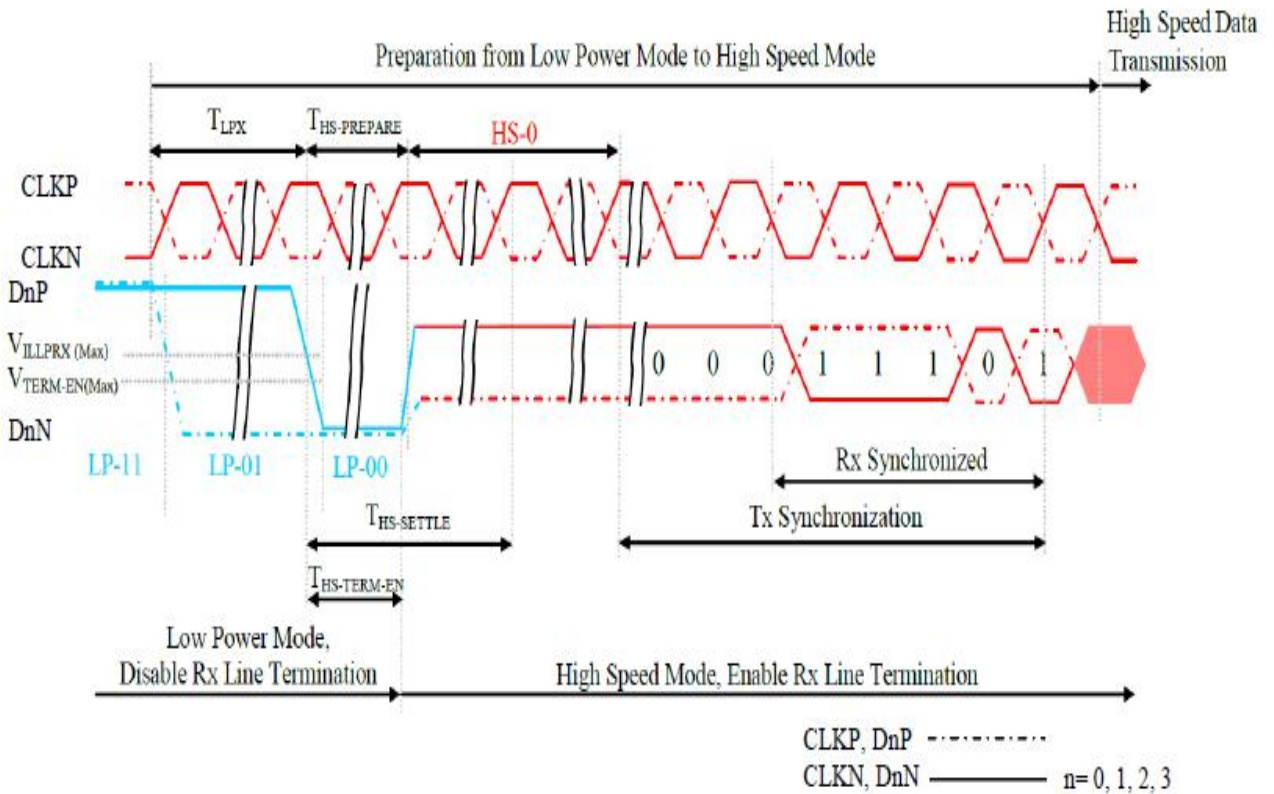


Figure 123: Data Lanes - Low Power Mode to High Speed Mode Timings

Table 44: Data Lanes - Low Power Mode to High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	T_{LPX}	Length of any Low Power State Period	50	-	ns
DnP/N, n = 0 and 1	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	$40+4xUI$	$85+6xUI$	ns
DnP/N, n = 0 and 1	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX	-	$35+4xUI$	ns

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6.6 Data Lanes from High Speed Mode to Low Power Mode

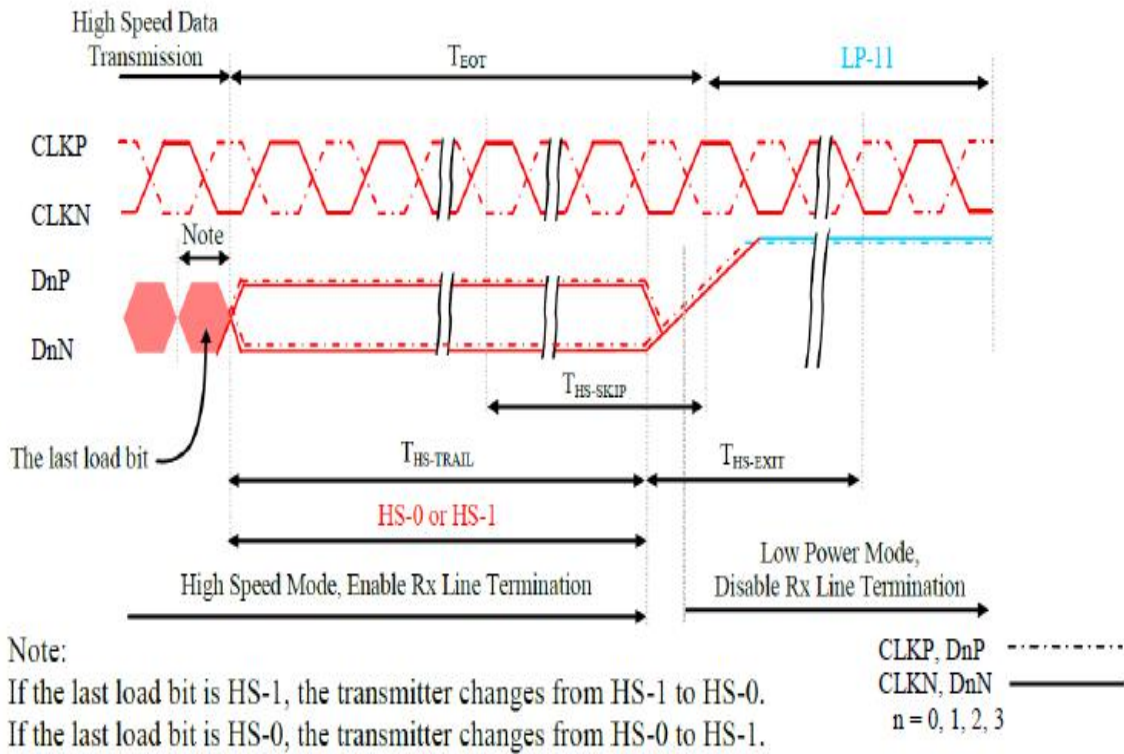


Figure 124: Data Lanes - High Speed Mode to Low Power Mode Timings

Table 45: Data Lanes - High Speed Mode to Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DnP/N, n = 0 and 1	$T_{HS-SKIP}$	Time-Out at Display Module (ILI9881C) to ignore transition period of EoT	40	55+4xUI	ns
DnP/N, n = 0 and 1	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	ns

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6.7 DSI Clock Burst – High Speed Mode to/from Low Power Mode

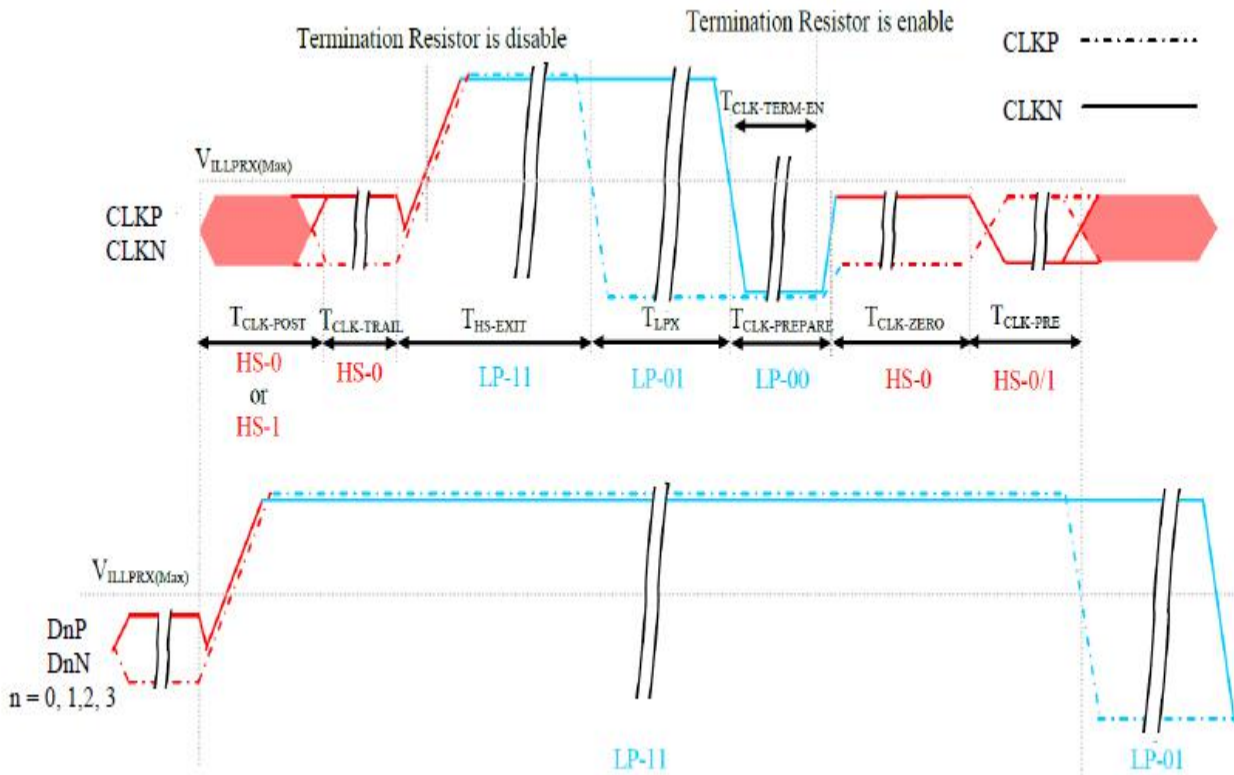
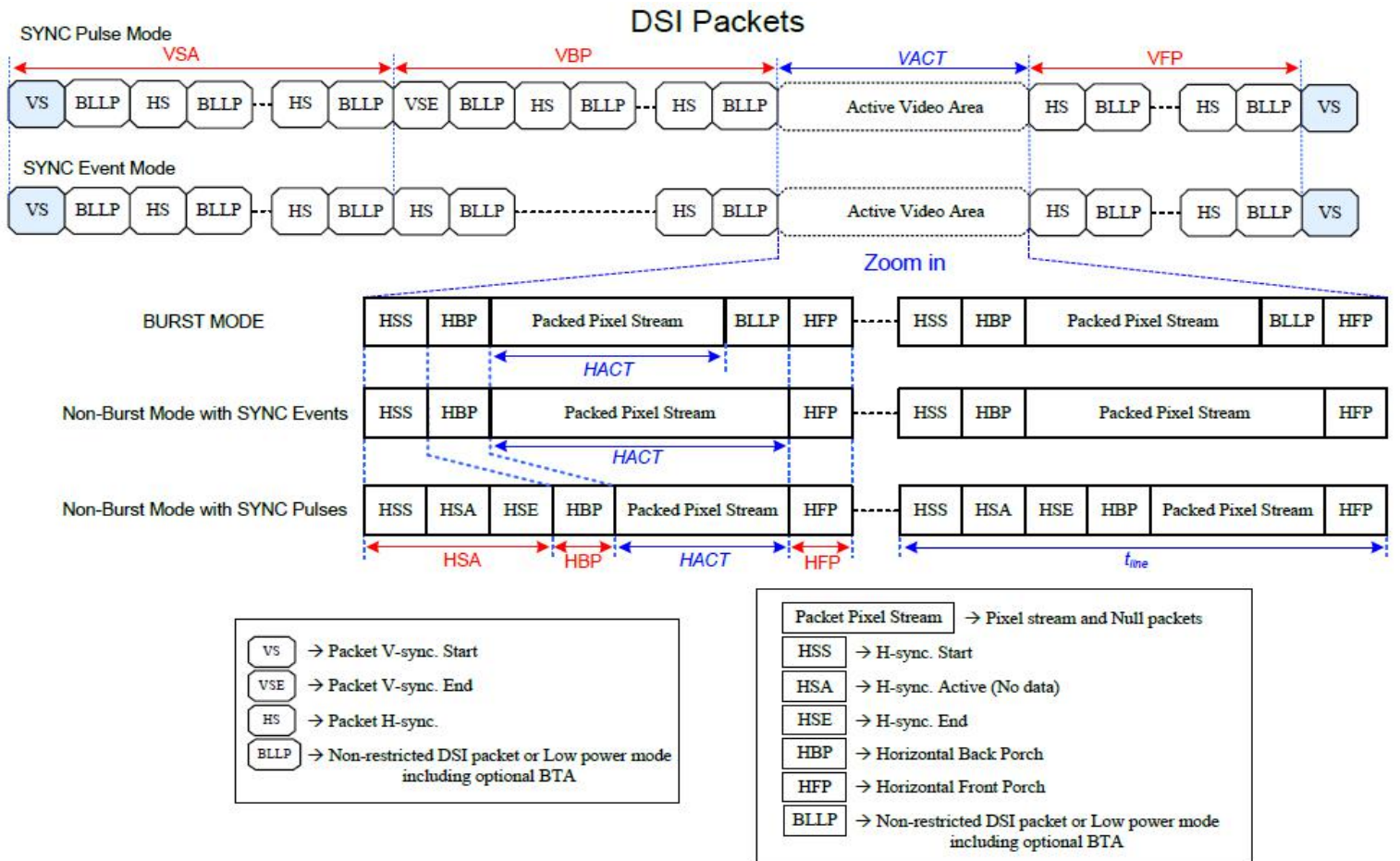


Figure 125: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Table 46: Clock Lanes - High Speed Mode to/from Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
CLKP/N	$T_{CLK-POST}$	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	$60+52xUI$	-	ns
CLKP/N	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
CLKP/N	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
CLKP/N	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
CLKP/N	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	-	38	ns
CLKP/N	$T_{CLK-PREPARE} + T_{CLK-ZERO}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
CLKP/N	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	$8xUI$	-	ns

6.8 Timing for DSI video mode



Parameters	Symbols	Min.	Typ.	Max.	Units
Vertical sync. active	VSA	TBD	TBD	-	Line
Vertical Back Porch	VBP	TBD	TBD	-	Line
Vertical Front Porch	VFP	TBD	TBD	-	Line
Active lines per frame	VACT	-	1280	-	Line
Horizontal sync. active	HSA	TBD	TBD	-	Pixel
Horizontal Back Porch	HBP	TBD	TBD	-	Pixel
Horizontal Front Porch	HFP	TBD	TBD	-	Pixel
Active pixels per line	HACT	-	800	-	Pixel
Line time	t_{line}	TBD		-	bps/lane
Bit rate	BR_{bps}	200		Note 5	Line

1 UI=1/Bit rate

$HAS(\text{pixel}) = (t_{HSA} \times \text{lane number}) / (UI \times \text{pixel format})$

$HBP(\text{pixel}) = (t_{HBP} \times \text{lane number}) / (UI \times \text{pixel format})$

$HFP(\text{pixel}) = (t_{HFP} \times \text{lane number}) / (UI \times \text{pixel format})$

$$\text{Frame Rate} = \frac{BR_{bps} \times \text{Lane}_{num}}{(VACT+VSA+VBP+VFP) \times (HACT+HSA+HBP+HFP) \times \text{Pixel Format}}$$

Note:

1. Lane_{num} : Data lane of MIPI-DSI.
2. Pixel Format: Please reference to "4.1 DSI System Interface".
3. The formula exists slightly error because of the host-transmission way.
4. The best frame rate setting : 2 data lanes : 50~60 Hz / 3 data lanes : 50~70 Hz / 4 data lanes : 50~70 Hz.
5. Please reference to "Table 39: Limited Clock Channel Speed"

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6.9 Reset input timing

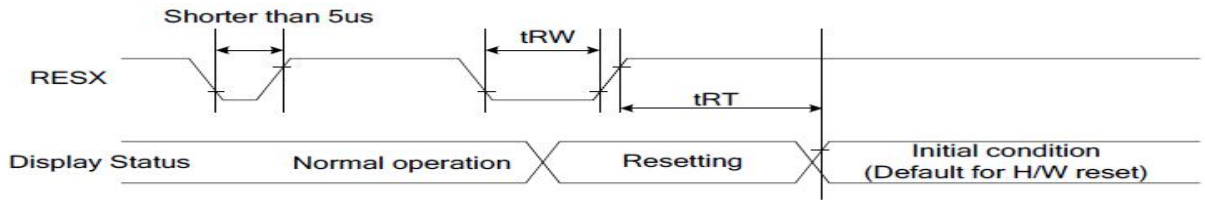


Figure 126: Reset Timing

Table 47: Reset Timing

Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		uS
	tRT	Reset cancel		5 (note 1,5) 120 (note 1,6,7)	mS

Notes:

1. The reset cancel also includes required time for loading ID bytes, VCOM setting and other settings from EEPROM to registers. This loading is done every time when there is H/W reset cancel time (tRT) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the Table 48.

Table 48: Reset Descript

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts

3. During the Resetting period, the display will be blanked (The display enters the blanking sequence, which maximum time is 120 ms, when Reset Starts in the Sleep Out mode. The display remains the blank state in the Sleep In mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection can also be applied during a valid reset pulse, as shown below:

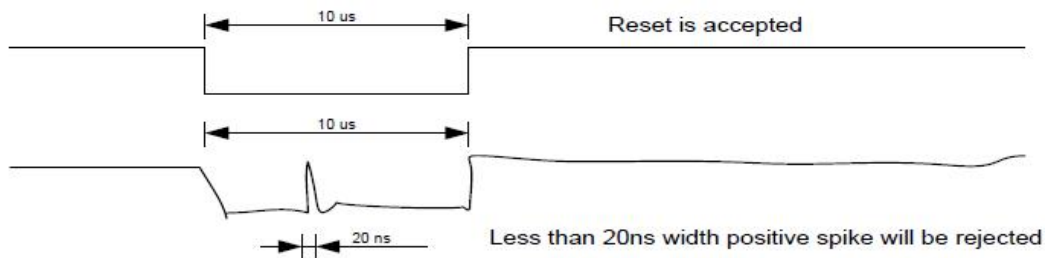


Figure 127: Positive Noise Pulse during Reset Low

5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

7. LCD Module Out-Going Quality Level

7.1 VISUAL & FUNCTION INSPECTION STANDARD

7.1.1 Inspection conditions

Inspection performed under the following conditions is recommended.

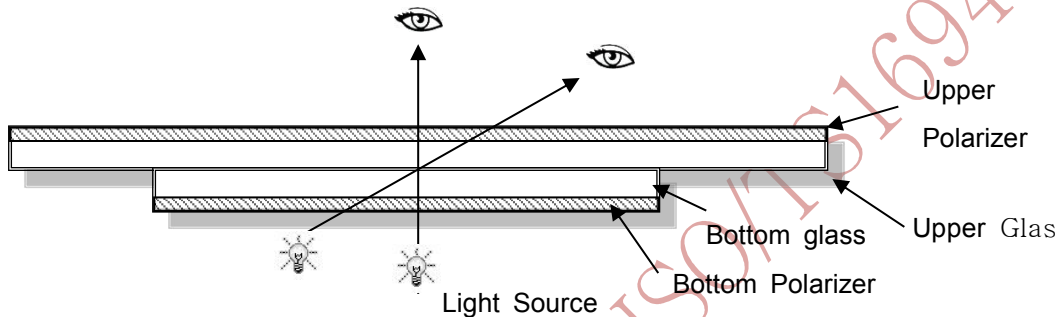
Temperature : $25 \pm 5^\circ\text{C}$

Humidity : $65\% \pm 10\% \text{RH}$

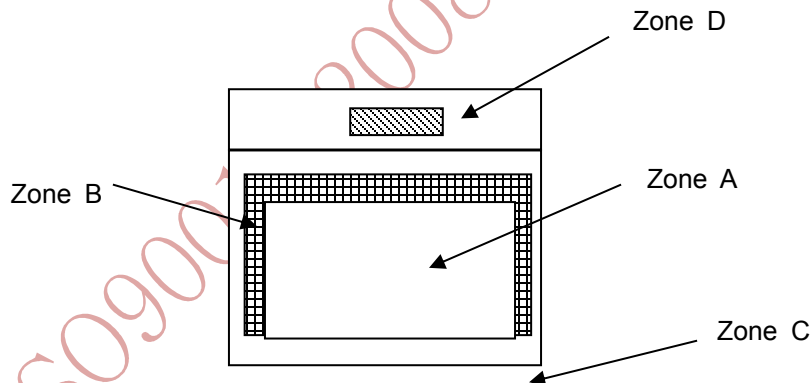
Viewing Angle : Normal viewing Angle.

Illumination: Single fluorescent lamp (300 to 700Lux)

Viewing distance: 30-50cm



7.1.2 Definition



Zone A : Effective Viewing Area(Character or Digit can be seen)

Zone B : Viewing Area except Zone A

Zone C : Outside (Zone A+Zone B) which can not be seen after assembly by customer .)

Zone D : IC Bonding Area

Note:As a general rule ,visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer

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7.1.3 Sampling Plan

According to GB/T 2828-2003 ; , normal inspection, Class II

AQL:

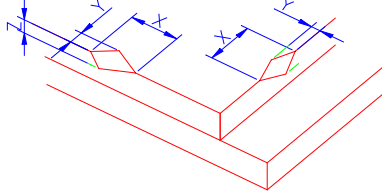
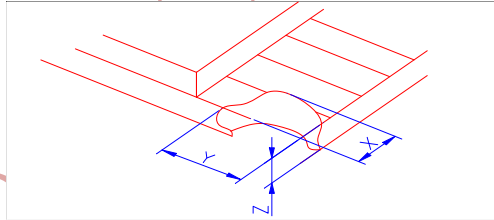
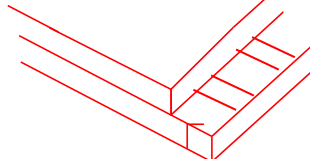
Major defect	Minor defect
0.65	1.5

LCD: Liquid Crystal Display , TP: Touch Panel , LCM: Liquid Crystal Module

No	Items to be inspected	Criteria	Classification of defects
1	Functional defects	1) No display, Open or miss line 2) Display abnormally, Short 3) Backlight no lighting, abnormal lighting. 4) TP no function	Major
2	Missing	Missing component	
3	Outline dimension	Overall outline dimension beyond the drawing is not allowed	
4	Color tone	Color unevenness, refer to limited sample	Minor
5	Spot Line defect	Light dot, Dim spot, Polarizer Bubble ; Polarizer accidented spot.	
6	Soldering appearance	Good soldering , Peeling off is not allowed.	
7	LCD/Polarizer/TP	Black/White spot/line, scratch, crack, etc.	



7.1.4 Criteria (Visual)

Number	Items	Criteria(mm)						
1.0 LCD Crack/Broken NOTE: X: Length Y: Width Z: Height L: Length of IT O, T: Height of LCD	(1) The edge of LCD broken	 <table border="1" data-bbox="758 672 1452 817"> <tr> <td>X</td> <td>Y</td> <td>Z</td> </tr> <tr> <td>≤3.0mm</td> <td><Inner border line of the seal</td> <td>≤T</td> </tr> </table>	X	Y	Z	≤3.0mm	<Inner border line of the seal	≤T
	X	Y	Z					
	≤3.0mm	<Inner border line of the seal	≤T					
(2)LCD corner broken	 <table border="1" data-bbox="837 1131 1372 1220"> <tr> <td>X</td> <td>Y</td> <td>Z</td> </tr> <tr> <td>≤3.0mm</td> <td>≤L</td> <td>≤T</td> </tr> </table>	X	Y	Z	≤3.0mm	≤L	≤T	
X	Y	Z						
≤3.0mm	≤L	≤T						
(3) LCD crack	 <p style="text-align: center;">Crack Not allowed</p>							

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2.0	Spot defect	<p style="text-align: center;">$\Phi=(X+Y)/2$</p>	① light dot (LCD/TP/Polarizer black/white spot , light dot, pinhole, dent, stain)		
	Zone		Acceptable Qty		
	Size (mm)		A	B	C
	$\Phi \leq 0.10$		Ignore		
	$0.10 < \Phi \leq 0.25$		4(distance $\geq 10\text{mm}$)		
	$0.25 < \Phi \leq 0.35$	3			
	$\Phi > 0.4$	0			
		② Dim spot (LCD/TP/Polarizer dim dot, light leakage, dark spot)			
	Zone	Acceptable Qty			
	Size (mm)	A	B	C	
	$\Phi \leq 0.1$	Ignore			
	$0.10 < \Phi \leq 0.25$	4(distance $\geq 10\text{mm}$)			
	$0.25 < \Phi \leq 0.35$	3			
	$\Phi > 0.4$	0			
		③ Polarizer accidented spot			
	Zone	Acceptable Qty			
	Size (mm)	A	B	C	
	$\Phi \leq 0.2$	Ignore			
	$0.3 < \Phi \leq 0.5$	3(distance $\geq 10\text{mm}$)			
	$\Phi > 0.5$	1			
		④ Pixel bad points (light dot, Dim dot, color dot)			
	Zone	Acceptable Qty			
	Size (mm)	A	B	C	
	$\Phi \leq 0.15$	Ignore			
	$0.2 < \Phi \leq 0.3$	2(distance $\geq 10\text{mm}$)			
	$\Phi > 0.4$	1			
		⑤ Polarizer Bubble			
	Zone	Acceptable Qty			
	Size (mm)	A	B	C	
	$\Phi \leq 0.2$	Ignore			
	$0.3 < \Phi \leq 0.4$	4(distance $\geq 10\text{mm}$)			
	$0.4 < \Phi \leq 0.5$	3			
	$\Phi > 0.5$	1			

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3.0	Line defect (LCD/TP /Polarizer backlight black/white line, scratch, stain)	Width(mm)	Length(m)	Acceptable Qty		
				A	B	C
		$\Phi \leq 0.05$	Ignore	Ignore		Ignore
		$0.05 < W \leq 0.06$	$L \leq 5.0$	$N \leq 3$		
		$0.07 < W \leq 0.08$	$L \leq 4.0$	$N \leq 2$		
$0.08 < W$	Define as spot defect					
4.0	Electronic Components SMT	Not allow missing parts, solderless connection, cold solder joint, mismatch, The positive and negative polarity opposite				
5.0	Display color & Brightness	<p>1. Color: Measuring the color coordinates, The measurement standard according to the datasheet or samples.</p> <p>2. Brightness: Measuring the brightness of White screen, The measurement standard according to the datasheet or Samples.</p>				
6.0	LCD Mura	By 5% ND filter invisible.				

7.0	RTP Related TP film bubble/accidental spot	Size Φ (mm)	Acceptable Qty		
			A	B	C
		$\Phi \leq 0.1$	Ignore		Ignore
		$0.1 < \Phi \leq 0.25$	4 (distance ≥ 10 mm)		
		$0.25 < \Phi \leq 0.35$	3		
$\Phi > 0.4$	1				

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ISO 15169:2009



		TP film scratch	<table border="1"> <thead> <tr> <th rowspan="2">Width(mm)</th> <th rowspan="2">Length (mm)</th> <th colspan="3">Acceptable Qty</th> </tr> <tr> <th>A</th> <th>B</th> <th>C</th> </tr> </thead> <tbody> <tr> <td>$\Phi \leq 0.05$</td> <td>Ignore</td> <td colspan="2">Ignore</td> <td rowspan="3">Ignore</td> </tr> <tr> <td>$0.05 < W \leq 0.06$</td> <td>$L \leq 5.0$</td> <td colspan="2">$N \leq 3$</td> </tr> <tr> <td>$0.07 < W \leq 0.08$</td> <td>$L \leq 4.0$</td> <td colspan="2">$N \leq 2$</td> </tr> <tr> <td>$0.08 < W$</td> <td colspan="4">Define as spot defect</td> </tr> </tbody> </table>	Width(mm)	Length (mm)	Acceptable Qty			A	B	C	$\Phi \leq 0.05$	Ignore	Ignore		Ignore	$0.05 < W \leq 0.06$	$L \leq 5.0$	$N \leq 3$		$0.07 < W \leq 0.08$	$L \leq 4.0$	$N \leq 2$		$0.08 < W$	Define as spot defect			
			Width(mm)			Length (mm)	Acceptable Qty																						
				A	B		C																						
$\Phi \leq 0.05$	Ignore	Ignore		Ignore																									
$0.05 < W \leq 0.06$	$L \leq 5.0$	$N \leq 3$																											
$0.07 < W \leq 0.08$	$L \leq 4.0$	$N \leq 2$																											
$0.08 < W$	Define as spot defect																												
Assembly deflection	beyond the edge of backlight $\leq 0.2\text{mm}$																												
Bulge (undulation included)	The ITO film pumped below 0.40mm, it's ok.																												
	Newton Ring	<p>Newton Ring area $> 1/3$ TP area NG</p> <p>Newton Ring area $\leq 1/3$ TP area OK</p>																											

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		TP corner broken X : length Y : width Z : height	<table border="1"> <tr> <td>X</td> <td>Y</td> <td>Z</td> </tr> <tr> <td>X≤3mm</td> <td>Y≤3mm</td> <td>Z<COVER thickness s</td> </tr> </table> <p>*Circuitry broken is not allowed.</p>	X	Y	Z	X≤3mm	Y≤3mm	Z<COVER thickness s	
		X	Y	Z						
X≤3mm	Y≤3mm	Z<COVER thickness s								
TP edge broken X : length Y : width Z : height	<table border="1"> <tr> <td>X</td> <td>Y</td> <td>Z</td> </tr> <tr> <td>X≤4mm</td> <td>Y≤2mm</td> <td>Z<COVER thickness</td> </tr> </table> <p>* Circuitry broken is not allowed.</p>	X	Y	Z	X≤4mm	Y≤2mm	Z<COVER thickness			
X	Y	Z								
X≤4mm	Y≤2mm	Z<COVER thickness								

Criteria (functional items)

Number	Items	Criteria (mm)
1	No display	Not allowed
2	Missing segment	Not allowed
3	Short	Not allowed
4	Backlight no lighting	Not allowed
5	TP no function	Not allowed

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8. Reliability Test Result

High Temperature Operating	70℃,96H	Inspection after 2~4hours storage at room temperature, the sample shall be free from defects: 1.Air bubble in the LCD;
Low Temperature Operating	-20℃, 96HR	
High Temperature Storage	80℃, 96HR	
Low Temperature Storage	-30℃, 96HR	
High Temperature & High Humidity Storage	+60℃, 90% RH ,96 hours.	
Thermal Shock (Non-operation)	-30℃,30 min ↔ 80℃,30 min, Change time:5min 20CYC.	2.Non-display; 3.Missing segments/line;
ESD test	C=150pF, R=330,5points/panel Air:±8KV, 5times; Contact:±6KV, 5 times; (Environment: 15℃~35℃, 30%~60%).	
Vibration (Non-operation)	Frequency range:10~55Hz, Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z. (6 hours for total) (Package condition).	4.Glass crack; 5.Current IDD is twice higher than initial value.
Box Drop Test	1 Corner 3 Edges 6 faces,80cm(MEDIUM BOX)	

Remark:

- 1.The test samples should be applied to only one test item.
- 2.Sample size for each test item is 5~10pcs.
- 3.For Damp Proof Test, Pure water(Resistance > 10MΩ) should be used.
- 4.In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.
- 5.Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.

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9. Cautions and Handling Precautions

9.1 Handling and Operating the Module

- (1) When the module is assembled, it should be attached to the system firmly.
Do not warp or twist the module during assembly work.
- (2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
- (3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
- (4) Do not allow drops of water or chemicals to remain on the display surface.
If you have the droplets for a long time, staining and discoloration may occur.
- (5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
- (6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.
Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
- (7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
- (8) Protect the module from static; it may cause damage to the CMOS ICs.
- (9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
- (10) Do not disassemble the module.
- (11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
- (12) Pins of I/F connector shall not be touched directly with bare hands.
- (13) Do not connect, disconnect the module in the "Power ON" condition.
- (14) Power supply should always be turned on/off by the item 6.1 Power On Sequence & 6.2 Power Off Sequence

9.2 Storage and Transportation.

- (1) Do not leave the panel in high temperature, and high humidity for a long time.
It is highly recommended to store the module with temperature from 0 to 35 °C and relative humidity of less than 70%
- (2) Do not store the TFT-LCD module in direct sunlight.
- (3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
- (4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module.
In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
- (5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.

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10. Packing

---TBD-----

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