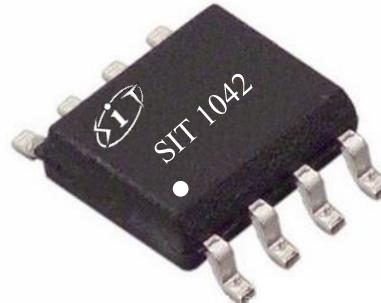


FEATURES

- Fully compatible with the ISO 11898 standard
- Thermally protected
- ±70V BUS Protection
- Driver (TXD) and standby bus (BUS) dominant overtime function
- Low-power standby mode with wake-up function
- SIT1042T/3 and SIT1042TK/3 can be interfaced directly to microcontrollers with supply voltages from 3V to 5V
- Under-voltage protection on V_{CC} and V_{IO} power supply pins
- Timing guaranteed for data rates up to 5 Mbit/s in the fast phase (CAN FD)
- Very low Electro Magnetic Emission (EME)
- Unpowered nodes do not interfere with the bus
- Provide HVSON8 / DFN3*3-8, Small Outline, Leadless Package

PRODUCT OUTLINE DIAGRAM

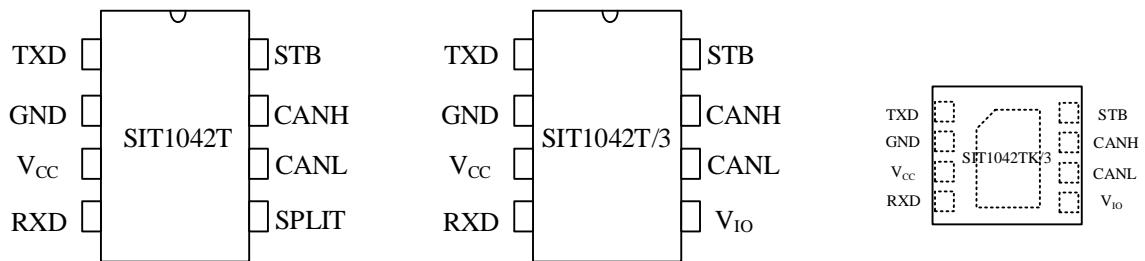
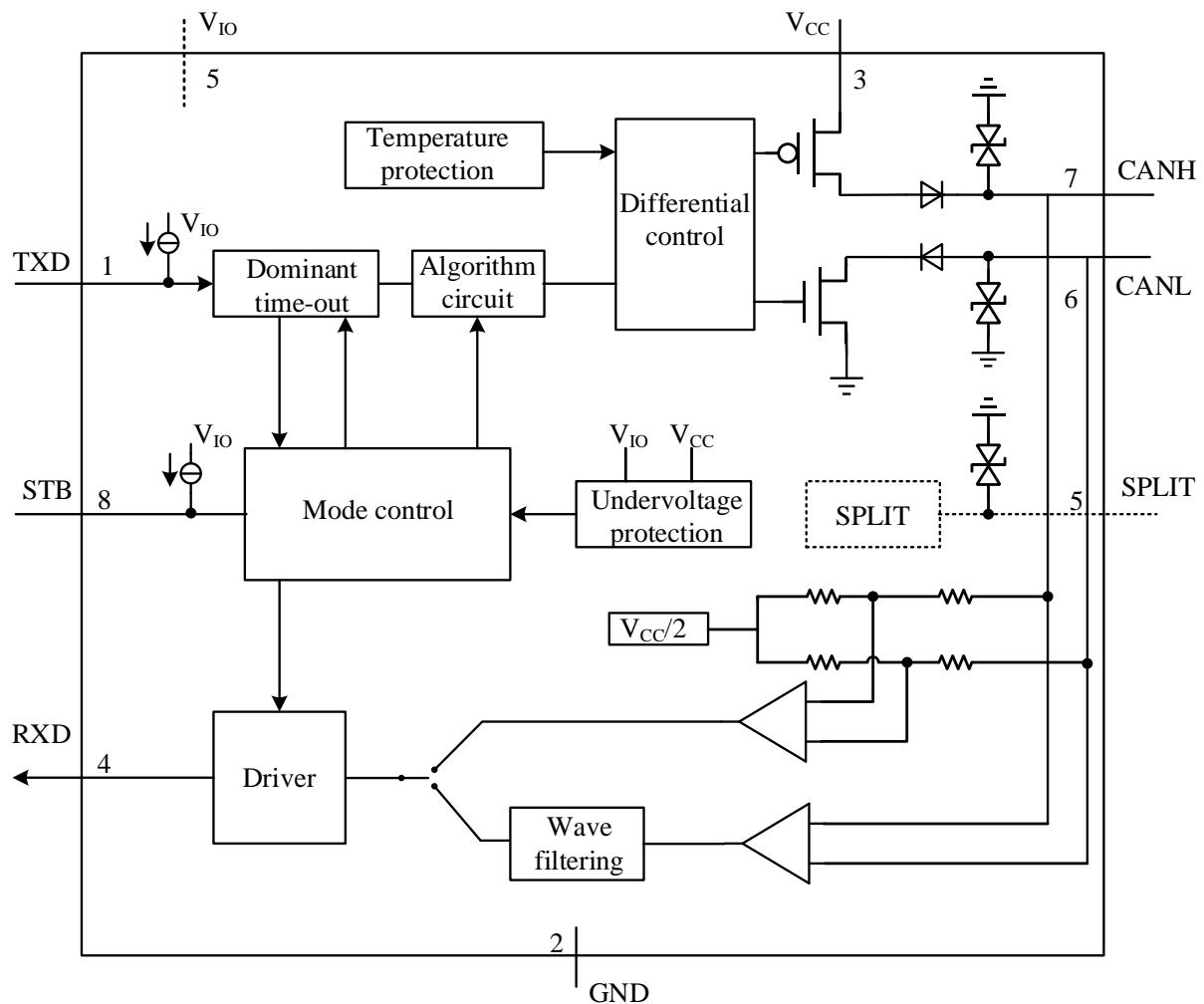


Provide Green and Environmentally
Friendly Lead-free package

DESCRIPTION

SIT1042 is an interface chip used between the CAN protocol controller and the physical bus. It can be used in trucks, buses, cars, industrial control and other fields. It supports 5Mbps (CAN FD), and has a connection between the bus and the CAN protocol controller. The ability to perform differential signal transmission between.

PARAMETER	SYMBOL	CONDITION	MIN.	MAX.	UNIT
Supply voltage	V _{CC}		4.5	5.5	V
Maximum transmission rate	1/t _{bit}	Non-return to zero code	1		Mbaud
CANH/CANL input or output voltage	V _{can}		-70	+70	V
Bus differential voltage	V _{diff}		1.5	3.0	V
Virtual junction temperature	T _j		-40	150	°C

PIN CONFIGURATION

INTERNAL CIRCUIT BLOCK DIAGRAM




LIMITING VALUES

PARAMETER	SYMBOL	VALUE	UNIT
Supply voltage	V _{CC}	-0.3~+7	V
MCU side port	TXD, RXD, STB, V _{IO}	-0.3~+7	V
Bus side input voltage	CANL, CANH	-70~70	V
Bus differential breakdown voltage	V _{CANH-CANL}	-27~27	V
Transient voltage on pins CANH, CANL and SPLIT	V _{tr}	-200~+200	V
Storage temperature		-55~150	°C
Virtual junction temperature		-40~150	°C
Welding temperature range		300	°C

The maximum limit parameters means that exceeding these values may cause irreversible damage to the device. Under these conditions, it is not conducive to the normal operation of the device. The continuous operation of the device at the maximum allowable rating may affect the reliability of the device. The reference point for all voltages is ground.

PINNING

PIN	SYMBOL	DESCRIPTION
1	TXD	transmit data input
2	GND	ground supply
3	V _{CC}	supply voltage
4	RXD	receive data output; reads out data from the bus lines
5	V _{IO}	transceiver I/O level conversion power supply voltage (SIT1042T/3 version)
5	SPLIT	common-mode stabilization output(SIT1042T version)



6	CANL	LOW-level CAN bus line
7	CANH	HIGH-level CAN bus line
8	STB	standby mode control input



DRIVER ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
CANH dominant output voltage	V _{OH(D)}	TXD=0V, STB=0V, RL=60Ω, Fig.1, Fig.2	2.9	3.4	4.5	V
CANL dominant output voltage	V _{OL(D)}		0.8		1.5	V
Bus recessive output voltage	V _{O(R)}	TXD=V _{IO} , STB=0V, RL=60Ω, Fig.1, Fig.2	2	0.5V _{CC}	3	V
Bus dominant differential output voltage	V _{OD(D)}	TXD=0V, STB=0V, RL=60Ω, Fig.1, Fig.2	1.5		3	V
Bus recessive differential output voltage	V _{OD(R)}	TXD=V _{IO} , STB=0V, Fig.1, Fig.2	-0.012		0.012	V
		TXD=V _{IO} , STB=0V, NO LOAD	-0.5		0.05	V
Transmitter dominant voltage symmetry	V _{dom(TX)sym}	V _{dom(TX)sym} =V _{CC} -V _{CANH} - V _{CANL}	-400		400	mV
Transmitter voltage symmetry	V _{TXsym}	V _{TXsym} =V _{CANH} + V _{CANL}	0.9V _{CC}		1.1V _{CC}	V
Common-mode output voltage	V _{OC}	STB=0V, Fig.8	2	0.5V _{CC}	3	V
Peak-to-peak Common-mode output voltage	△V _{OC}			30		mV
Short-circuit output current	I _{OS}	CANH=-12V, CANL=open, Fig.11	-105	-72		mA
		CANH=12V, CANL=open, Fig.11		0.36	1	mA
		CANL=-12V, CANH=open, Fig.11	-1	0.5		mA
		CANL=12V, CANH=open,		71	105	mA



		Fig.11				
Recessive output current	$I_{O(R)}$	-27V<CANH<32V 0< V_{CC} <5.25V	-2.0		2.5	mA

($V_{CC}=5V\pm10\%$ and Temp= $T_{MIN}\sim T_{MAX}$ unless specified otherwise; typical in $V_{CC}=+5V$, $V_{IO}=+5V$ and Temp= $25^\circ C$)

DRIVER SWITCHING CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation delay time, low-to-high-level output	t_{PLH}	STB=0V, Fig.4		90		ns
Propagation delay time, low-to-high-level output	t_{PHL}			65		ns
Differential output signal rise time	t_r			45		ns
Differential output signal fall time	t_f			45		ns
Enable time from standby mode to dominant	t_{EN}	Fig.7		1	45	μs
TXD dominant time-out	t_{dom_TXD}	Fig.10	0.8	2	4	ms
Bus dominant time-out time	$T_{dom\ BUS}$		0.8	2	4	ms
Bus wake-up filter time	t_{WAKE}		0.5		5	μs

($V_{CC}=5V\pm10\%$ and Temp= $T_{MIN}\sim T_{MAX}$ unless specified otherwise; typical in $V_{CC}=+5V$, $V_{IO}=+5V$ and Temp= $25^\circ C$)

RECEIVER ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Positive-going input threshold voltage	V_{IT+}	STB=0V, Fig.5			900	mV
Negative-going input threshold voltage	V_{IT-}		500			mV



Hysteresis voltage (VIT+ – VIT-)	V _{HYS}		50	120	200	mV
Standby mode positive input threshold	V _{IT+(STB)}	Standby mode			1150	mV
Standby mode negative input threshold	V _{IT-(STB)}	Standby mode	400			mV
Power-off bus input current	I _(OFF)	CANH or CANL=5V, Other pin=0V	-5		5	μA
Input capacitance to ground, (CANH or CANL)	C _I			24		pF
Differential input capacitance	C _{ID}			12		pF
Input resistance, (CANH or CANL)	R _{IN}	TXD=V _{IO} , STB=0V	9	15	28	kΩ
Differential input resistance	R _{ID}		19	30	52	kΩ
Input resistance matching	R _I _{match}	CANH=CANL	-2%		2%	
The range of common-mode voltage	V _{COM}		-30		30	V

(V_{CC}=5V±10% and Temp=T_{MIN}~T_{MAX} unless specified otherwise; typical in V_{CC}=+5V, V_{IO}=+5V and Temp=25°C)

RECEIVER SWITCHING CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Propagation delay time, low-to-high-level	t _{PLH}	STB=0V, Fig.6		65		ns



output						
Propagation delay time, low-to-high-level output	t_{PHL}			60		ns
RXD signal rise time	t_r			10		ns
RXD signal fall time	t_f			10		ns

($V_{CC}=5V\pm10\%$ and Temp= $T_{MIN}\sim T_{MAX}$ unless specified otherwise; typical in $V_{CC}=+5V$, $V_{IO}=+5V$ and Temp= $25^\circ C$)

DEVICE SWITCHING CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Loop delay1, driver input to receiver output, Recessive to Dominant	$T_{d(LOOP1)}$	STB=0V, Fig.9		90	220	ns
Loop delay 2, driver input to receiver output, Dominant to Recessive	$T_{d(LOOP2)}$			100	220	ns
Bit time of BUS output pin	$t_{bit(BUS)}$	$t_{bit(TXD)}=500ns$	435		530	ns
		$t_{bit(TXD)}=200ns$	155		210	ns
Bit time of RXD output pin	$t_{bit(RXD)}$	$t_{bit(TXD)}=500ns$	400		550	ns
		$t_{bit(TXD)}=200ns$	120		220	ns

($V_{CC}=5V\pm10\%$ and Temp= $T_{MIN}\sim T_{MAX}$ unless specified otherwise; typical in $V_{CC}=+5V$, $V_{IO}=+5V$ and Temp= $25^\circ C$)



OVER TEMPERATURE PROTECTION

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Shutdown junction temperature	$T_{j(sd)}$			190		°C

($V_{CC}=5V\pm10\%$ and Temp= $T_{MIN}\sim T_{MAX}$ unless specified otherwise; typical in $V_{CC}=+5V$, $V_{IO}=+5V$ and Temp= $25^\circ C$)

UNDER-VOLATAGE PROTECTION

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{CC} under-voltage protection	V_{uvd_VCC}		3.5		4.5	V
V_{IO} under-voltage protection	V_{uvd_VIO}		1.5		2.5	V

($V_{CC}=5V\pm10\%$ and Temp= $T_{MIN}\sim T_{MAX}$ unless specified otherwise; typical in $V_{CC}=+5V$, $V_{IO}=+5V$ and Temp= $25^\circ C$)

TXD PIN CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
HIGH-level input current	$I_{IH}(TXD)$	$TXD=V_{IO}$	-5		5	μA
LOW-level input current	$I_{IL}(TXD)$	$TXD=0V$	-260	-150	-30	μA
When $V_{CC}=0V$, current on TXD pin	$I_{O(off)}$	$V_{CC}=V_{IO}=0V$, $TXD=V_{IO}$	-1		1	μA
HIGH-level input voltage	V_{IH}		$0.7V_{IO}^{\circledR}$		$V_{IO}^{\circledR}+0.3$	V
LOW-level input voltage	V_{IL}		-0.3		$0.3V_{IO}^{\circledR}$	V
Open voltage on TXD pin	TXD_O			H		logic

($V_{CC}=5V\pm10\%$ and Temp= $T_{MIN}\sim T_{MAX}$ unless specified otherwise; typical in $V_{CC}=+5V$, $V_{IO}=+5V$ and Temp= $25^\circ C$)



STB PIN CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
HIGH-level input current	I _{IH} (STB)	STB=V _{IO}	-2		2	μA
LOW-level input current	I _{IL} (STB)	STB=0V	-20		-2	μA
When V _{CC} =0V, current on STB pin	I _O (off)	V _{CC} =V _{IO} =0V, STB=V _{IO}	-1		1	μA
HIGH-level input voltage	V _{IH}		0.7V _{IO} ^①		V _{IO} ^① +0.3	V
LOW-level input voltage	V _{IL}		-0.3		0.3V _{IO} ^①	V
Open voltage on STB pin	STB _O			H		logic

① SIT1042T model V_{IO}=V_{CC}

(V_{CC}=5V±10% and Temp=T_{MIN}~T_{MAX} unless specified otherwise; typical in V_{CC}=+5V, V_{IO}=+5V and Temp=25°C)

RXD PIN CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
HIGH-level input current	I _{OH} (RXD)	V _{IO} =V _{CC} , RXD=V _{IO} -0.4V	-8	-3	-1	mA
LOW-level input current	I _{OL} (RXD)	RXD=0.4V, bus dominant	2	5	12	mA
When V _{CC} =0V, current on STB pin	I _O (off)	V _{CC} =V _{IO} =0V, RXD=V _{IO}	-1		1	μA

(V_{CC}=5V±10% and Temp=T_{MIN}~T_{MAX} unless specified otherwise; typical in V_{CC}=+5V, V_{IO}=+5V and Temp=25°C)

COMMON-MODE STABILIZATION OUTPUT

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
SPLIT port output voltage	V _{SPLIT}	-500μA<I _{SPLIT} <500μA	0.3V _{CC}	0.5 V _{CC}	0.7V _{CC}	V

(V_{CC}=5V±10% and Temp=T_{MIN}~T_{MAX} unless specified otherwise; typical in V_{CC}=+5V, V_{IO}=+5V and Temp=25°C)



SUPPLY CURRENT

PARAMETER		SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
V _{CC} supply current	Normal dominant	I _{CC_D}	bus dominant		45	70	mA
	Normal recessive	I _{CC_R}	bus recessive		5	10	mA
	Standby	I _{CC_STB}	STB=V _{CC} , TXD=V _{IO} , (SIT1042T/3)		0.5	5	μA
			STB=V _{CC} , TXD=V _{CC} , (SIT1042T)		12	25	μA
V _{IO} supply current	Normal dominant	I _{IO_D}	RXD open, STB=0V, TXD=0V		350	1000	μA
	Normal recessive	I _{IO_R}	RXD open, STB=0V, TXD=V _{IO}		80	200	μA
	Standby	I _{IO_STB}	STB=TXD=V _{IO}		10	20	μA

(V_{CC}=5V±10% and Temp=T_{MIN}~T_{MAX} unless specified otherwise; typical in V_{CC}=+5V, V_{IO}=+5V and Temp=25°C)

ESD 性能

参数	符号	测试条件	最小	典型	最大	单位
CAN bus pin contact discharge model (IEC)	V _{ESD_IEC}	IEC 61000-4-2: Contact discharge (CANH, CANL)	-4		+4	kV
CAN bus pin human body discharge model (HBM)	V _{ESD_HBM}		-8		+8	kV
Component charging model (CDM)	V _{CDM}		-750		+750	V
Mechanical model (MM)	V _{MM}		-300		+300	V

FUNCTION TABLE
Table1.CAN TRANSCEIVER TRUTH TABLE

TXD⁽¹⁾	STB⁽¹⁾	CANH⁽¹⁾	CANL⁽¹⁾	BUS STATE	RXD⁽¹⁾
L	L	H	L	Dominate	L
H or Open	L	0.5V _{CC}	0.5V _{CC}	Recessive	H
X	H or Open	GND	GND	Recessive	H

(1) H=high level; L=low level; X=irrelevant

Table 2. RECEIVER FUNCTION TABLE

V_{ID}=CANH-CANL	RXD⁽¹⁾	BUS
V _{ID} ≥0.9V	L	Dominate
0.5<V _{ID} <0.9V	?	?
V _{ID} ≤0.5V	H	Recessive
Open	H	Recessive

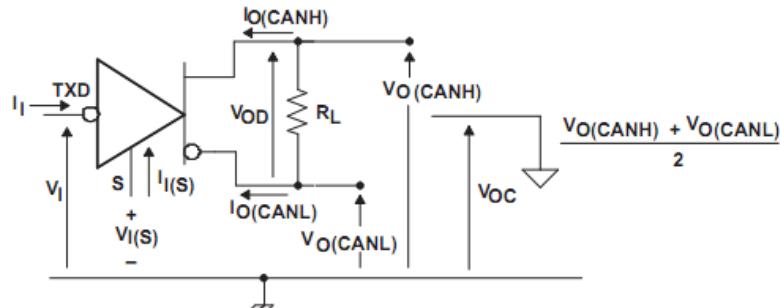
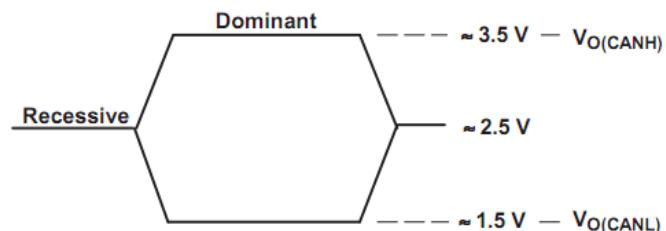
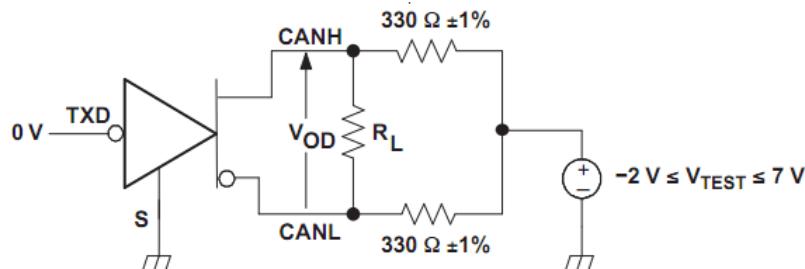
(1) H=high level; L=low level; ? =uncertain

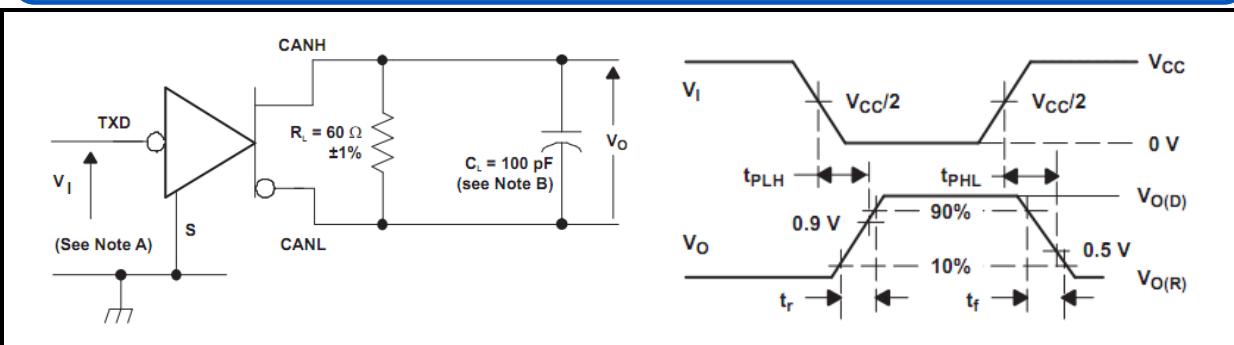
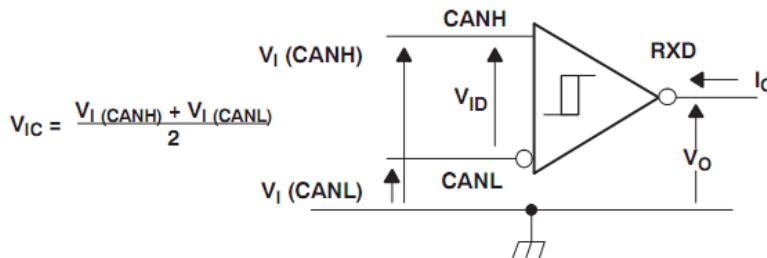
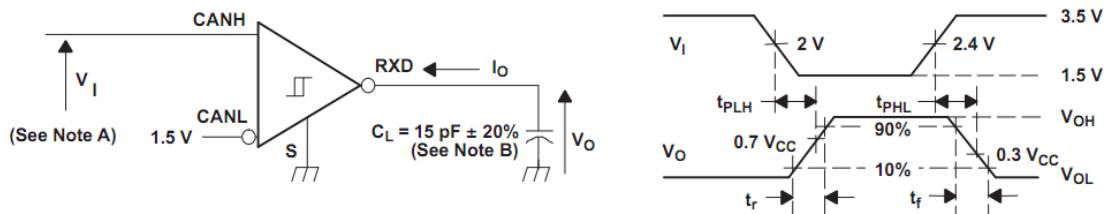
Table 3. UNDERVOLTAGE PROTECTION STATUS TABLE

V_{CC}	V_{IO}⁽¹⁾	BUS	BUS OUTPUT⁽²⁾	RXD⁽²⁾
V _{CC} >V _{uvd_VCC}	V _{IO} >V _{uvd_VIO}	normal	According to STB and TXD	Follow the bus
V _{CC} <V _{uvd_VCC}	V _{IO} >V _{uvd_VIO}	Protected status	GND	H
V _{CC} >V _{uvd_VCC}	V _{IO} <V _{uvd_VIO}	Protected status	Z	H
V _{CC} <V _{uvd_VCC}	V _{IO} <V _{uvd_VIO}	Protected status	Z	H

(1) SIT1042T/3 version only;

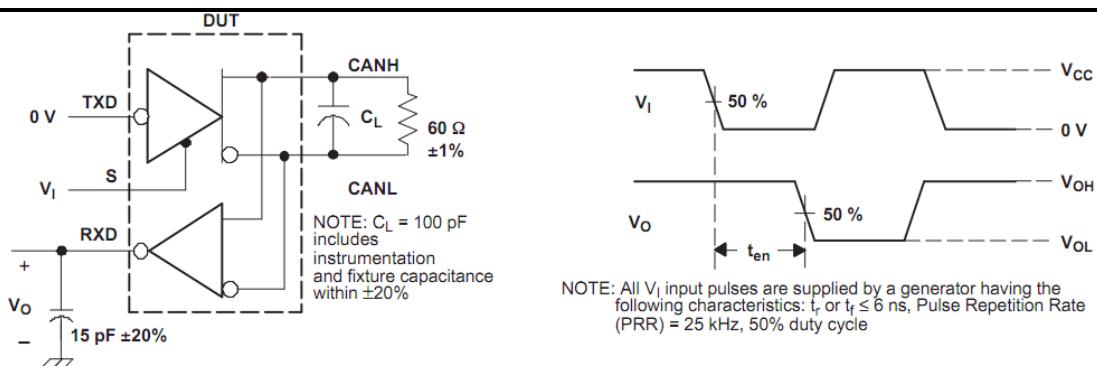
(2) H=high level; Z=high impedance;

TEST CIRCUIT

Fig.1 Driver Voltage, Current, and Test Definition

Fig.2 Bus Logic State Voltage Definition

Fig.3 Driver Vod Test Circuit


Fig.4 Driver Test Circuit and Waveform

Fig.5 Receiver Voltage and Current Definition


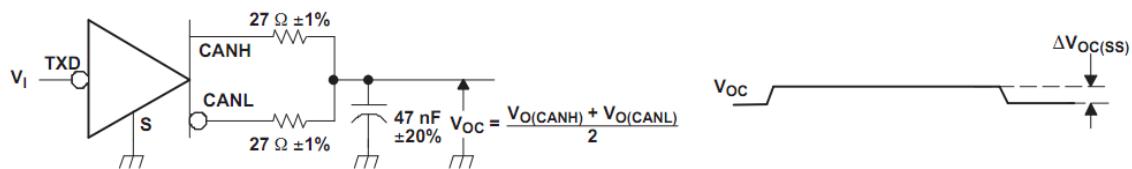
A. The input pulse is supplied by a generator having the following characteristics: PRR $\leq 125 \text{ kHz}$, 50% duty cycle, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$, $Z_0 = 50 \Omega$.

B. C_L includes instrumentation and fixture capacitance within $\pm 20\%$.

Fig.6 Receiver Test Circuit and Waveform


NOTE: All V_I input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 6 \text{ ns}$, Pulse Repetition Rate (PRR) = 25 kHz, 50% duty cycle

Fig.7 t_{en} Test Circuit and Waveform



A. All VI input pulses are from 0 V to VCC and supplied by a generator having the following characteristics: tr or tf ≤ 6 ns. Pulse Repetition Rate (PRR) = 125 kHz, 50% duty cycle.

Fig.8 Peak-to-Peak Common Mode Output Voltage Test and Waveform

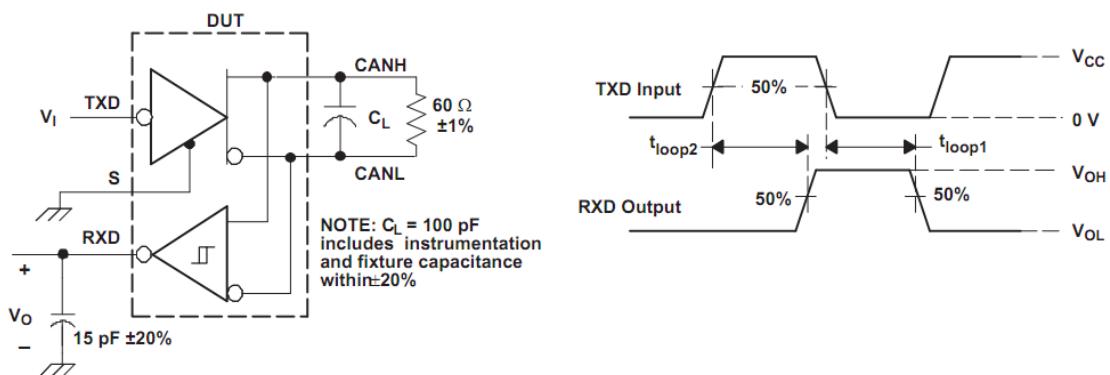


Fig.9 t_(LOOP) Test Circuit and Waveform

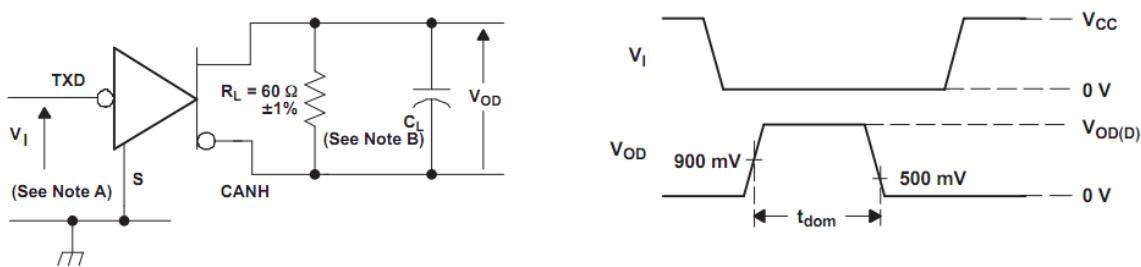


Fig.10 Dominant Time-Out Test Circuit and Waveform

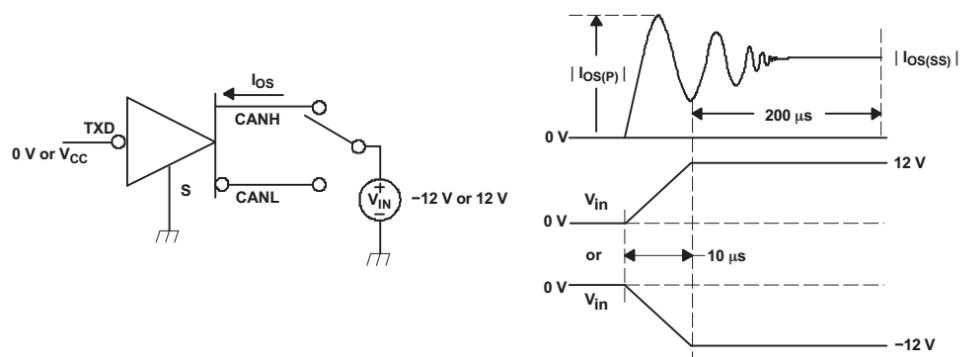


Fig.11 Driver Short-Circuit Current Test Circuit and Waveform

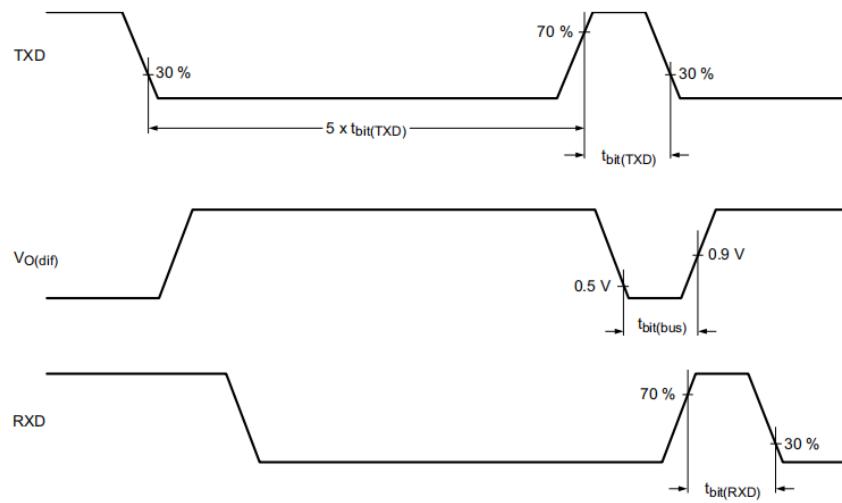


Fig.12 $t_{\text{bit}}(\text{RXD})$ test circuit and waveform

**ADDIYIONAL DESCRIPTION****1 Sketch**

The SIT1042 is the interface between the Controller Area Network (CAN) protocol controller and the physical bus, and can be applied to the fields of trucks, buses, cars, industrial control etc. Support 5Mbps CAN With Flexible Data-Rate. The device provides differential transmit capability to the bus and differential receive capability to the CAN controller, and fully compatible with the ISO 11898 standard.

2 Current protection

A current-limiting circuit protects the transmitter output stage from damage caused by accidental short-circuit to either positive or negative supply voltage, although power dissipation increases during this fault condition.

3 Over temperature protection

The output drivers are protected against over-temperature conditions. If the virtual junction temperature exceeds the shutdown junction temperature $T_j(sd)$, the output drivers will be disabled until the virtual junction temperature becomes lower than $T_j(sd)$ and TXD becomes recessive again.

By including the TXD condition, the occurrence of output driver oscillation due to temperature drifts is avoided.

4 Under-voltage protection

The SIT1042 power supply pin has an under-voltage detection function, which can put the device in a protected mode. This protects the bus when V_{CC} is lower than V_{uvd_VCC} or V_{IO} is lower than V_{uvd_VIO} .

5 Operating modes

The SIT1042 provides two modes of operation which are selectable via pin STB:

High-speed mode and standby mode.

High-speed mode is normal working mode, by connecting STB to ground to set the SIT1042 to high-speed mode. In this mode the transceiver is able to transmit and receive data via the bus lines CANH and CANL. The differential receiver converts the analog data on the bus lines into digital data which is output to pin RXD via the multiplexer (MUX).

If a logic-high or open is applied to STB, the SIT1042 enters a low-current standby mode. In this mode the transmitter and receiver are switched off, and the low-power differential receiver will monitor the bus lines. A HIGH level on pin STB activates this low-power receiver and the wake-up filter, and after tBUS the state of the CAN bus is reflected on pin RXD.

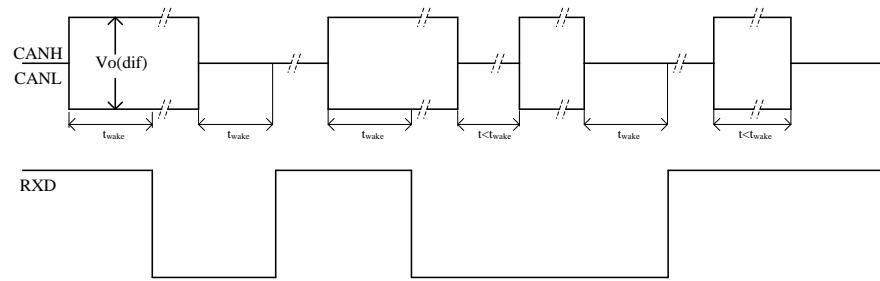


Fig 13 Wake-up timing

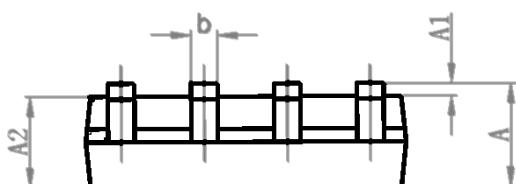
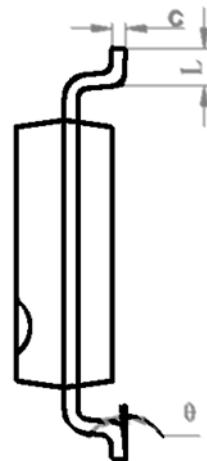
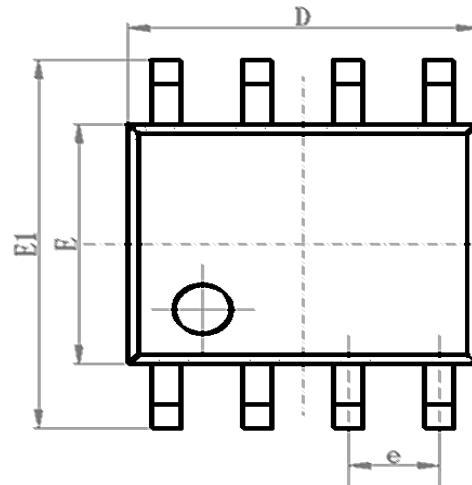
6 TXD dominant time-out function

A ‘TXD dominant time-out’ timer circuit prevents the bus lines from being driven to a permanent dominant state(blocking all network communication) if pin TXD is forced permanently LOW by a hardware and/or software application failure. The timer is triggered by a negative edge on pin TXD.

If the duration of the LOW level on pin TXD exceeds the internal timer value (t_{dom}), the transmitter is disabled, driving the bus lines into a recessive state. The timer is reset by a positive edge on pin TXD.

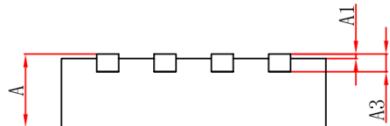
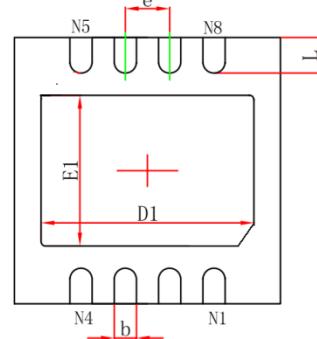
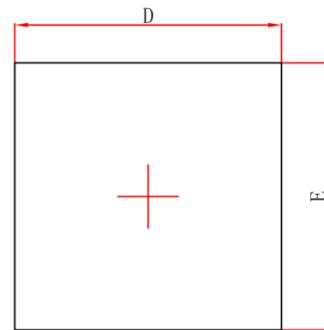
SOP8 DIMENSIONS
PACKAGE SIZE

SYMBOL	MIN./mm	TYP./mm	MAX./mm
A	1.40	-	1.80
A1	0.10	-	0.25
A2	1.30	1.40	1.50
b	0.38	-	0.51
D	4.80	4.90	5.00
E	3.80	3.90	4.00
E1	5.80	6.00	6.20
e		1.27BSC	
L	0.40	0.60	0.80
c	0.20	-	0.25
θ	0°	-	8°



DFN3*3-8 /HVSON8 DIMENSIONS
PACKAGE SIZE

SYMBOL	MIN./mm	TYP./mm	MAX./mm
A	0.70		0.80
A1	0.00	0.02	0.05
A3	0.203 REF		
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D1	2.35	2.3	2.55
E1	1.55	1.65	1.75
b	0.2	0.25	0.33
e	0.65 TYP		
L	0.35		0.45


ORDERING INFORMATION

TYPE NUMBER	TEMPERATURE	PACKAGE
SIT1042T	-40°C~150°C	SOP8
SIT1042T/3	-40°C~150°C	SOP8
SIT1042TK/3	-40°C~150°C	HVSON8 / DFN3*3-8, Small Outline, Leadless

SOP8 package is 2500 pieces/disc. HVSON8 / DFN3*3-8 package is 5000 pieces/disc.

Important statement

SIT reserves the right to change the above-mentioned information without prior notice.