LCD Module Specification

Module P/N: JH050N379A0

Version: 1.0

Description : 5.08 inch TFT 720*720 Pixels with LED backlight, ALL viewing angle

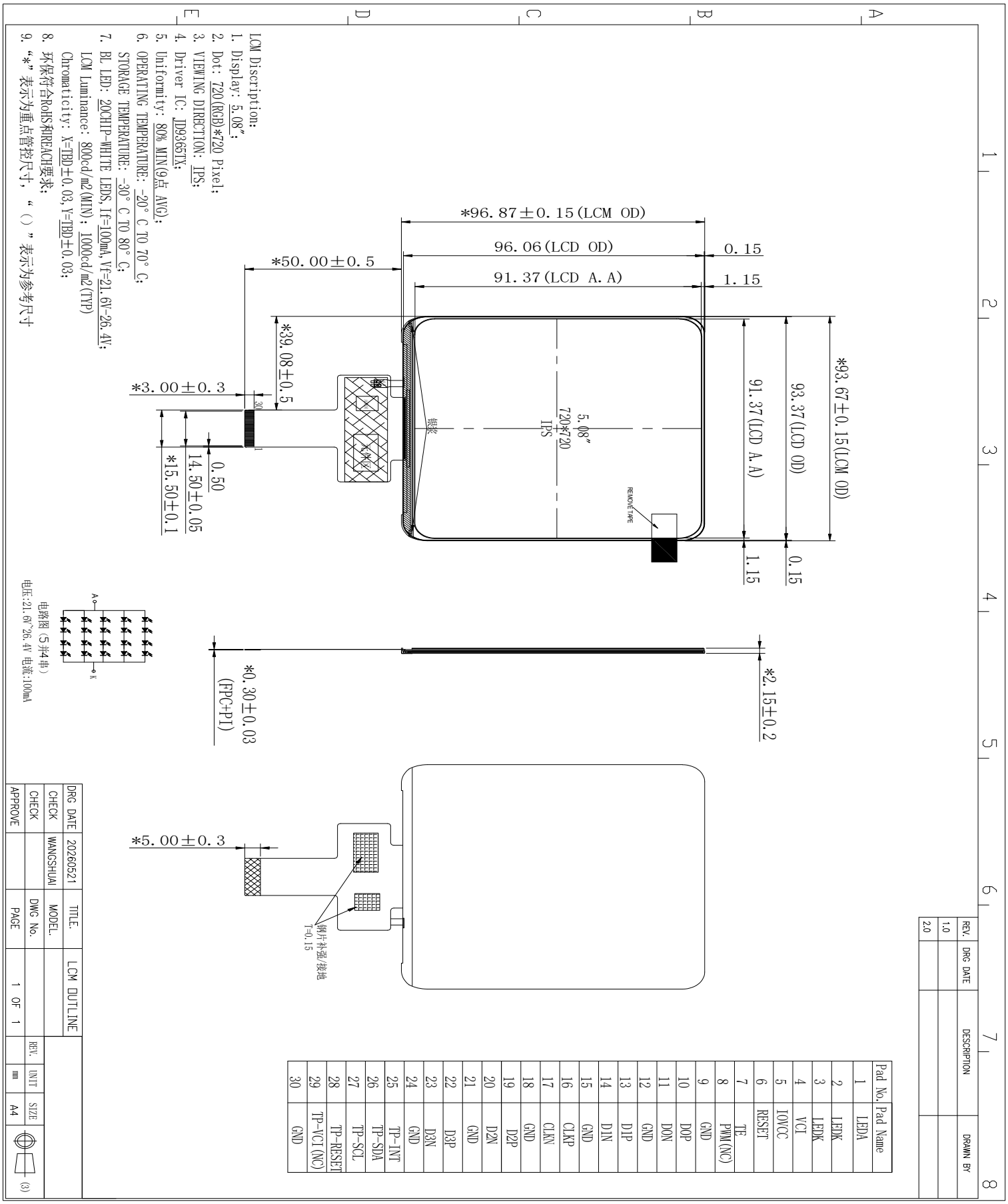
Revision History

Date	Rev.	Page	Description
2026-5-8	1.0	All	First issue

1. General Features

Item	Spec	Remark
Display Mode	Normally Black transmissive	
Gray Scale Inversion Direction	FREE	
Input Signals	MIPI	
Outside Dimensions	93.67(W)×96.87(H)×2.15(D)	Mm
Active Area	91.37(W)×91.37(H)	mm
Number of Pixels	720×RGB×720 Pixels	
Dot Pitch	0.1269(H)×0.1269(V)	mm
Pixel Arrangement	RGB Vertical Stripes	
Drive IC	JD9365TX	Incell

2.Outline Dimension



Pad No.	Pad Name
1	LEDA
2	LEDK
3	LEDK
4	VCI
5	IOVCC
6	RESET
7	TE
8	PWM(NC)
9	GND
10	D0P
11	D0N
12	GND
13	D1P
14	D1N
15	GND
16	CLKP
17	CLKN
18	GND
19	D2P
20	D2N
21	GND
22	D3P
23	D3N
24	GND
25	TP-INT
26	TP-SDA
27	TP-SCL
28	TP-RESET
29	TP-VCI(NC)
30	GND

REV.	DRG DATE	DESCRIPTION	DRAWN BY
1.0			
2.0			

DRG DATE	20260521	TITLE.	LCM OUTLINE
CHECK	WANGSHUAI	MODEL.	
CHECK		DWG No.	
APPROVE		PAGE	1 OF 1
		REV.	
		UNIT	mm
		SIZE	A4

3. Reliability and Inspection Standard

No.	Test Item		Test Conditions	INSPECTION AFTER TEST
1	High Temperature	Storage	80℃, 96Hrs	Inspection after 2-4hours storage at room temperature,the samples should be free from defects: 1,Air bubble in the LCD. 2,Seal leak. 3,Non-display. 4,Missing segments. 5,Glass crack. 6,Current IDD is twice higher than initial value. 7,The surface shall be free from damage.
		Operation	70℃, 96Hrs	
2	Low Temperature	Storage	-30℃, 96Hrs	
		Operation	-20℃, 96Hrs	
3	High Temperature and High Humidity		50℃, 90%RH, 48Hrs	
4	Temperature Cycle(storage)		-20 ~ 60℃, 30 Mins/cycle , Total 10 Cycles,	

REMARK:
1,The Test samples should be applied to only one test item.
2,Sample for each test item is 3pcs.
3,For Damp Proof Test, Pure water(Resistance＞10MΩ)should be used.
4,Failure Judgment Criterion: Basic Specification Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.

4.LCM Description

4.1 Absolute Maximum Ratings

The following are maximum values which, if exceeded may cause operation or damage to the unit.

Symbol	Parameter	Unit	Value	Note
IOVCC	Interface Supply Voltage	V	-0.3 to +2	Note(3),(4)
VCCH	High speed interface Supply Voltage	V	-0.3 to +2	Note(3) (7)
AVDD	Positive Voltage input	V	-0.3 to +6.6	Note(8)
AVEE	Negative Voltage input	V	0 to -6.6	Note(9)
VGH	Power Supply Voltage	V	-0.3 to +25	Note(10)
VGL	Power Supply Voltage	V	0 to -18	Note(11)

Note: (1) Permanent device damage may occur if absolute maximum conditions are exceeded.
(2) Functional operation should be restricted to the conditions described under DC Characteristics.
(3) VCCD/IOVCC, VSSD must be maintained.
(4) To make sure VCCD/IOVCC ≥ VSSD.
(5) To make sure VCIP≥ AVSS.
(6) To make sure VCI≥ AVSS.
(7) To make sure VCCH ≥ VSSH.
(8) To make sure AVDD ≥ AVSS.
(9) To make sure AVSS ≥ AVEE
(10) To make sure VGH ≥ AVSS.
(11) To make sure AVSS ≥ VGL
VGH +|VGL| < 32V

4.2 Electrical Specification

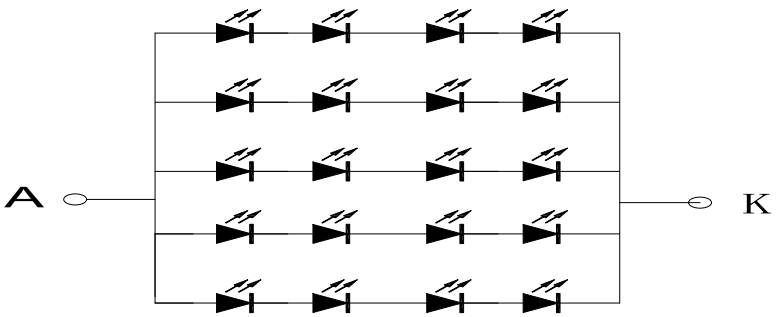
4.2.1 Driving TFT LCD Panel

Item		Sym.	Min	Typ.	Max	Unit	Note
Power for Circuit Driving		VCI	2.65	2.8	3.3	V	
Power For Circuit Logic		IOVCC	1.65	1.8	1.95	V	
Logic Input Voltage	Low Voltage	V_{IL}	0	-	0.3_{IOVDD}	V	
	High Voltage	V_{IH}	0.7_{IOVDD}	-	$_{IOVDD}$	V	
Logic Output Voltage	Low Voltage	V_{OL}	0	-	0.2_{IOVCC}	V	
	High Voltage	V_{OH}	0.8_{IOVDD}	-	$_{IOVDD}$	V	

4.2.2 Driving Backlight

Item	Sym.	Min	Typ.	Max	Unit	Note
Backlight driving voltage	V_F	21.6	-	26.4	V	
Backlight driving current	I_F	-	100	-	mA	
Backlight Power Consumption	W_{BL}	-	-	-	mW	
Life Time	-	-	20,000	-		Note 3

Note 1: (Unless specified, the ambient temperature Ta=25℃)
Note 2: The recommended operating conditions refer to a range in which operation of this product is guaranteed. Should this range is exceeded, the operation cannot be guaranteed even if the values may be without the absolute maximum ratings.
Note 3: If LED is driven by high current, high ambient temperature & humidity condition. The life time of LED will be reduced. Operating life means brightness goes down to 50% initial brightness. Typical operating life time is estimated data.



4.3 Optical Specifications

Optical characteristics are determined after the unit has been 'ON' and stable for approximately 30 minutes in a dark environment at 25 ℃. The values specified are at an approximate distance 500mm from the LCD surface at a viewing angle of Φ and θ equal to 0°.

Item	Sym.	Values			Unit	Note
		Min.	Typ.	Max.		
1)Contrast Ratio	C/R	1000	1200	-		FIG.1
2)Luminance/Without Lens	L	800	1000	-	cd/m^2	FIG.1
3)Response time	Tr+Tf	-	-	35	ms	FIG.2
4)Viewing Angle	Θ_L	-	80	-	Degree	FIG.3
	Θ_R	-	80	-		
	Θ_U	-	80	-		
	Θ_D	-	80	-		
5)Chromaticity	Wx	-0.03	TBD	+0.03		
	Wy		TBD			
	Rx		-			
	Ry		-			
	Gx		-			
	Gy		-			
	Bx		-			
	By		-			

◆ Measurement System

Notes:

1. Contrast Ratio(CR) is defined mathematically as :

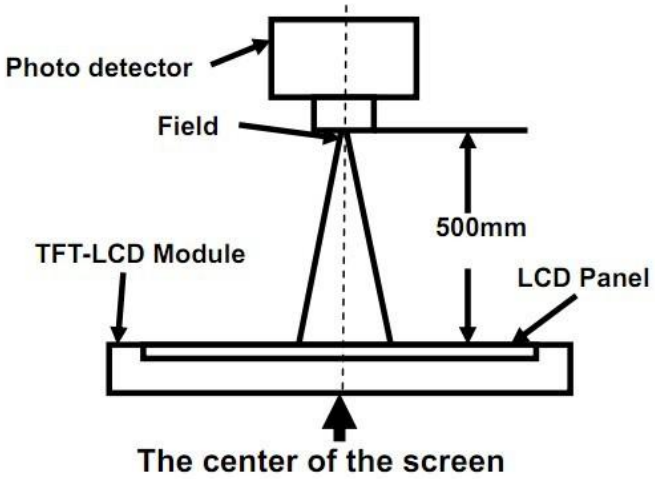
$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

2. Surface luminance is the center point across the LCD surface 500mm from the surface with all pixels displaying white. For more information see FIG 1.

3. Response time is the time required for the display to transition from white to black (Rising Time, Tr) and from black to white (Falling Time, Tf). For additional information see FIG 2.

4. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see FIG 3.

FIG. 1 Optical Characteristic Measurement Equipment and Method



Item	Photo detector	Field
Contrast Ratio	SR-3A	1°
Luminance		
Chromaticity		
Lum Uniformity		
Response Time	BM-7A	2°

FIG. 2 The definition of Response Time

The response time is defined as the following figure and shall be measured by switching the input signal for “black” and “white”.

Response Time = Rising Time(Tr) + Falling Time(Tf)

- Rising Time(Tr) : Full White 90% → Full White 10% Transmittance.
- Falling Time(Tf) : Full White 10% → Full White 90% Transmittance.

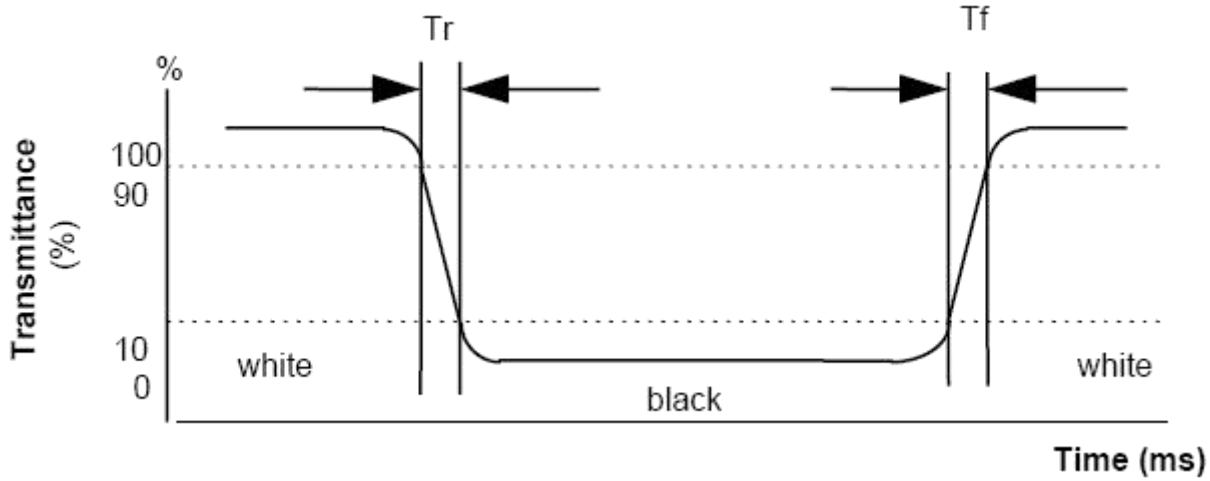
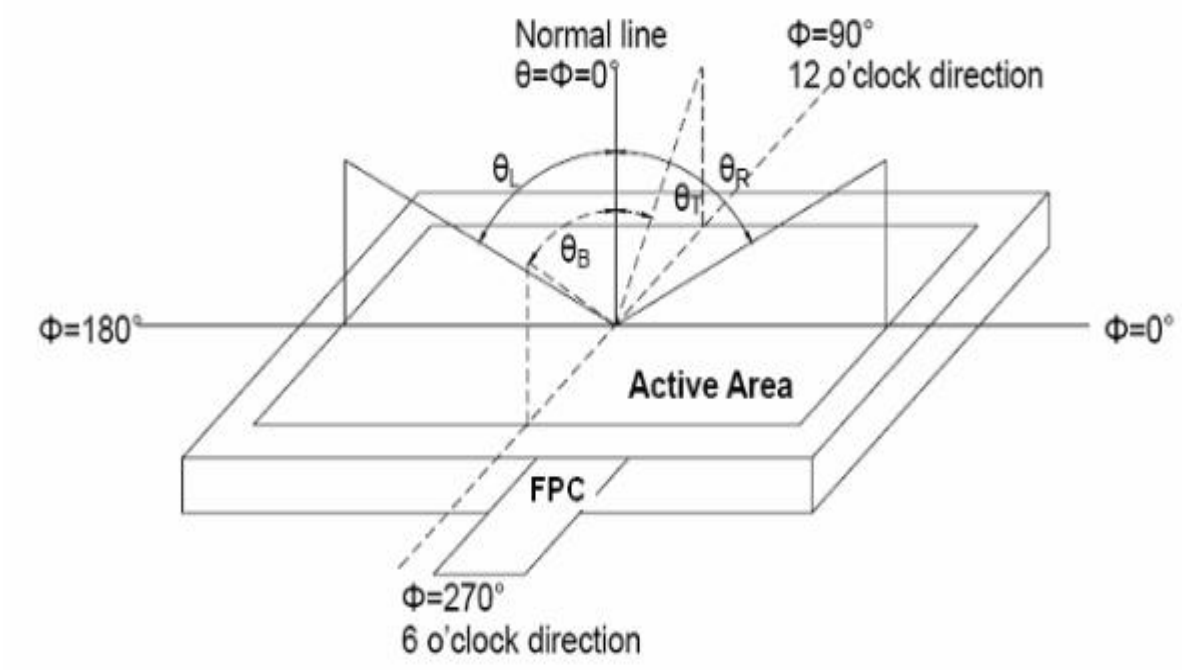
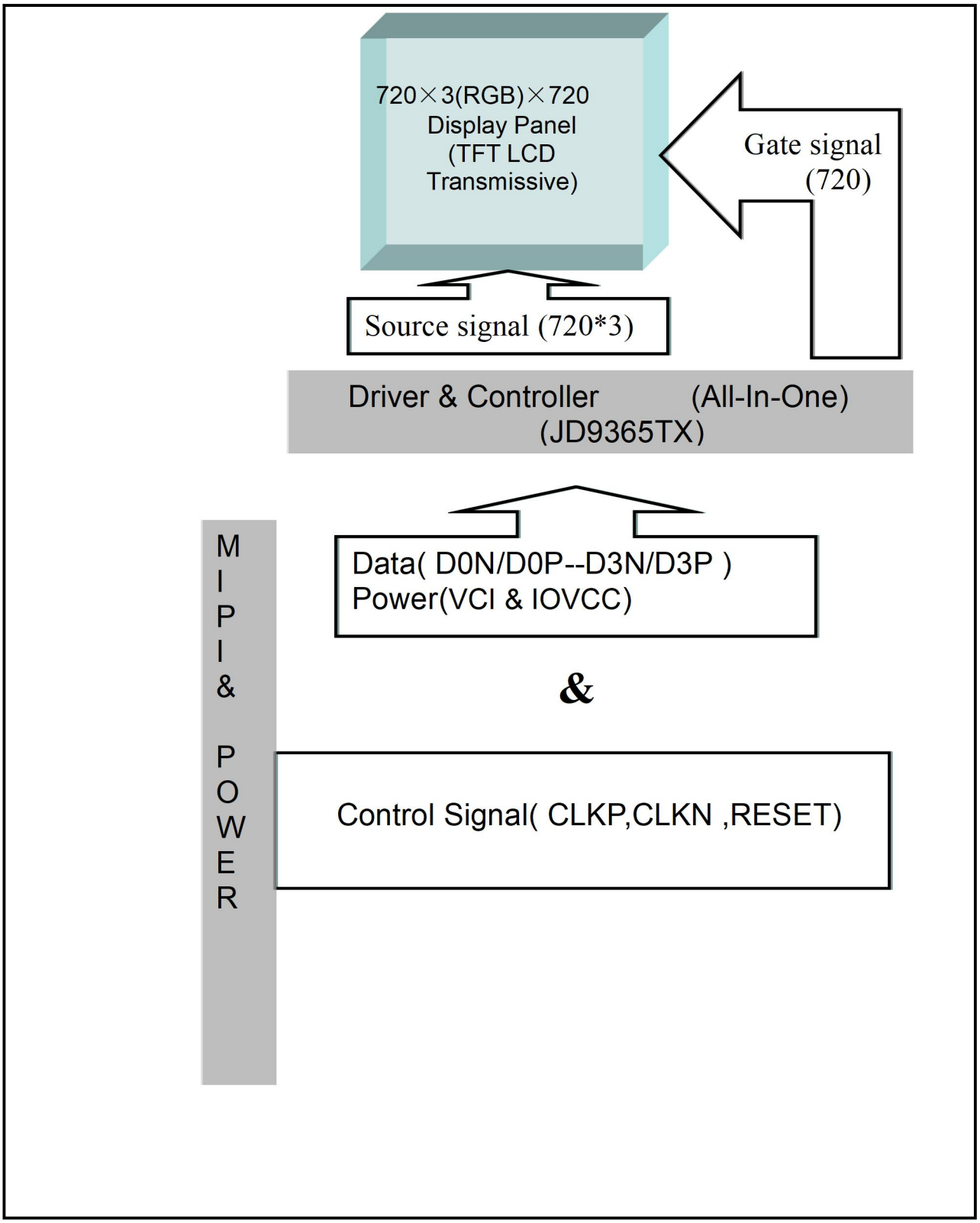


FIG. 3 The definition of Viewing Angle

Use Fig. 1(Test Procedure) under Measurement System to measure the contrast from the measuring direction specified by the conditions as the following figure.



4.4 Block Diagram



4.5 Pin Description

Item	Terminal	Functions
1	LEDA	Backlight A Aothod input pin.
2	LEDK1	Backlight K Cathode input pin.
3	LEDK2	Backlight K Cathode input pin.
4	VCI	Power supply 2.8V-3.3V
5	IOVCC	Power supply +1.8V-3.3V
6	RESET	LCD reset signal pin
7	TE	Tearing effect output pin to synchronies MCU to frame writing, activated by S/W command.
8	PWM	Backlight on/off control. This pin can be connected to external LED driver IC.
9	GND	Power ground
10	MIPI_D0P	Positive polarity of low voltage differential data0 signal
11	MIPI_D0N	Negative polarity of low voltage differential data0 signal
12	GND	Power ground
13	MIPI_D1P	Positive polarity of low voltage differential data1 signal
14	MIPI_D1N	Negative polarity of low voltage differential data1 signal
15	GND	Power ground
16	MIPI_CLKP	positive polarity of low voltage differential clock signal
17	MIPI_CLKN	Negative polarity of low voltage differential clock signal
18	GND	Power ground
19	MIPI_D2P	Positive polarity of low voltage differential data2 signal
20	MIPI_D2N	Negative polarity of low voltage differential data2 signal
21	GND	Power ground
22	MIPI_D3P	Positive polarity of low voltage differential data3 signal
23	MIPI_D3N	Negative polarity of low voltage differential data3 signal
24	GND	Power ground
25	TP-INT	I2C Interrupt signal
26	TP-SDA	I2C Serial Data Input/Output
27	TP-SCL	I2C Serial Clock Input
28	TP-RESET	TP reset signal pin
29	TP-VDD	NC
30	GND	Power ground

4.6 Timing Characteristics

4.6.1 High Speed Mode-Clock / Data Timings

This section specifies the required timings on the high-speed signaling interface independent of the electrical characteristics of the signal. The PHY is a source synchronous interface in the Forward direction. In either the Forward or Reverse signaling modes there shall be only one clock source. In the Reverse direction, Clock is sent in the Forward direction and one of four possible edges is used to launch the data.

The Master side of the Link shall send a differential clock signal to the Slave side to be used for data sampling. This signal shall be a DDR (half-rate) clock and shall have one transition per data bit time. All timing relationships required for correct data sampling are defined relative to the clock transitions. Therefore, implementations may use frequency spreading modulation on the clock to reduce EMI.

The DDR clock signal shall maintain a quadrature phase relationship to the data signal. Data shall be sampled on both the rising and falling edges of the Clock signal. The term "rising edge" means "rising edge of the differential signal, i.e. CLKP – CLKN, and similarly for "falling edge". Therefore, the period of the Clock signal shall be the sum of two successive instantaneous data bit times. This relationship is shown in Figure 13.5.

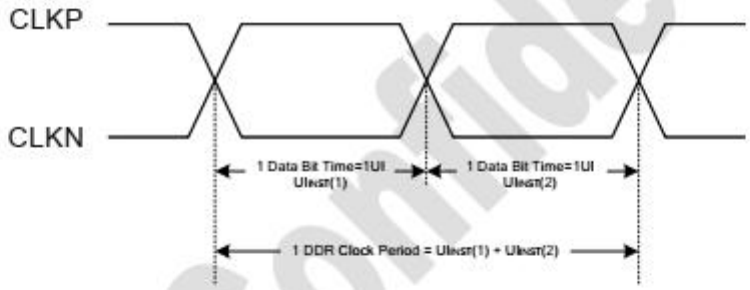


Figure 11.6: DDR Clock Definition

The same clock source is used to generate the DDR Clock and launch the serial data. Since the Clock and Data signals propagate together over a channel of specified skew, the Clock may be used directly to sample the Data lines in the receiver. Such a system can accommodate large instantaneous variations in UI.

The allowed instantaneous UI variation can cause large, instantaneous data rate variations. Therefore, devices shall either accommodate these instantaneous variations with appropriate FIFO logic outside of the PHY or provide an accurate clock source to the Lane Module to eliminate these instantaneous variations.

The UIINST specifications for the Clock signal are summarized in following Table.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
UI instantaneous	UI_{INST}	-	-	12.5	ns	(1), (2), (3), (4), (5), (6)

Note: (1) This value corresponds to a minimum 80 Mbps data rate.
(2) The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.
(3) Maximum total bit rate is 1.7Gbps of 2 data lanes 24-bit data format/ 1.27Gbps of 2 data lane 18-bit data format/ 1.13Gbps of 2 data lane 16-bit data format.
(4) Maximum total bit rate is 2Gbps of 3 data lanes 24-bit data format/ 1.5Gbps of 3 data lane 18-bit data format/ 1.33Gbps of 3 data lane 16-bit data format.
(5) Maximum total bit rate is 2Gbps of 4 data lanes 24-bit data format/ 1.5Gbps of 4 data lane 18-bit data format/ 1.33Gbps of 4 data lane 16-bit data format.

Table 11.11: Reverse HS Data Transmission Timing Parameters

The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in Figure 8.13. Data is launched in a quadrature relationship to the clock such that the Clock signal edge may be used directly by the receiver to sample the received data.
The transmitter shall ensure that a rising edge of the DDR clock is sent during the first payload bit of a transmission burst such that the first payload bit can be sampled by the receiver on the rising clock edge, the second bit can be sampled on the falling edge, and all following bits can be sampled on alternating rising and falling edges.
All timing values are measured with respect to the actual observed crossing of the Clock differential signal. The effects due to variations in this level are included in the clock to data timing budget.
Receiver input offset and threshold effects shall be accounted as part of the receiver setup and hold parameters.

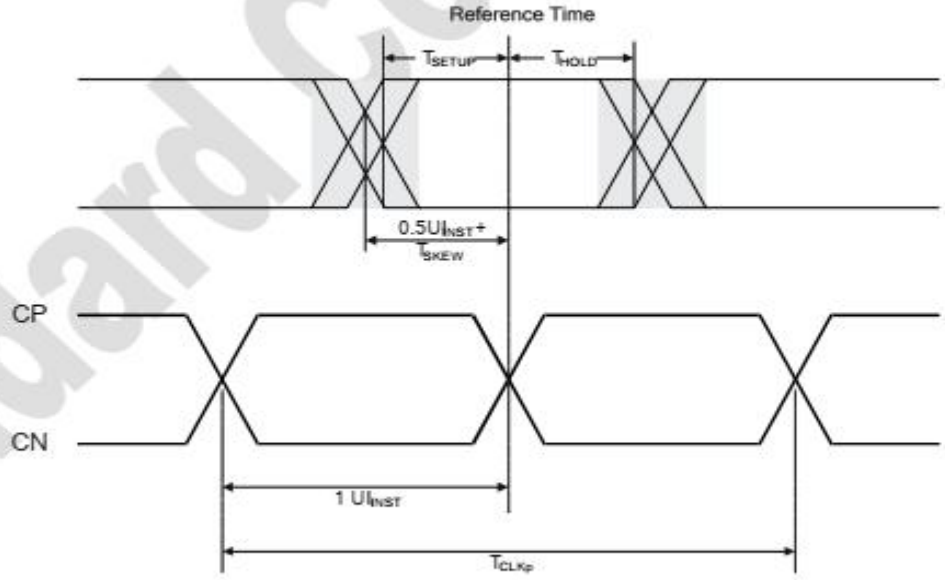


Figure 11.7: Data to Clock Timing Definitions

4.6.3 Reset Timing

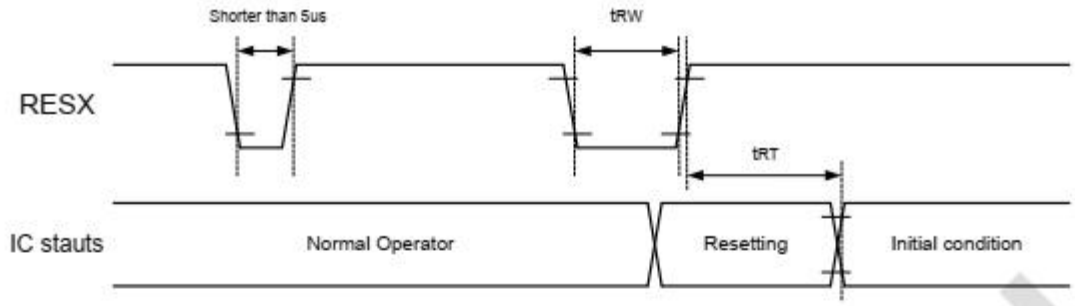


Figure 11.1: Reset input timings

Symbol	Parameter	Related pins	Min.	Max.	Unit
t_{RW}	Reset pulse width(2)	RESX	10	-	µs
t_{RT}	Reset complete time(3)	-	-	5 (Note 5)	ms
		-	-	120 (Note 6, 7)	ms

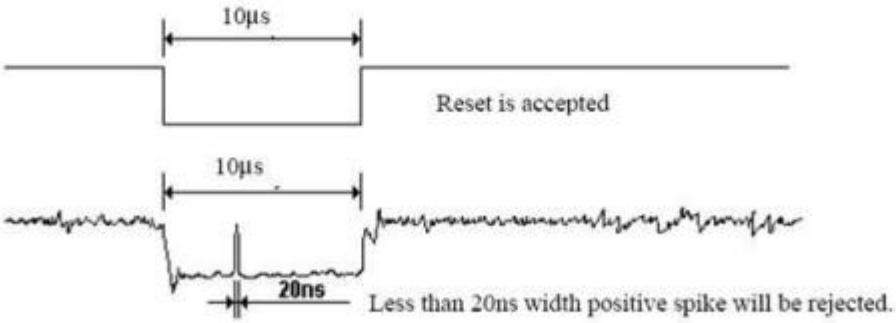
Note: (1) The reset complete time also required time for loading ID bytes from OTP to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

(2) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5 µs	Reset Rejected
Longer than 10 µs	Reset
Between 5 µs and 10 µs	Reset Start

(3) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then returns to Default condition for H/W reset.

(4) Spike Rejection also applies during a valid reset pulse as shown below:



(5) When Reset is applied during Sleep In Mode.

(6) When Reset is applied during Sleep Out Mode.

(7) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

(8) After Sleep Out Command, it is necessary to wait 120msec then send RESX.

Table 11.3: Reset timings