

MOSFET – N-Channel, Shielded Gate, POWERTRENCH®

150 V, 9.4 A, 134 mΩ

FDMC86244, FDMC86244-L701

General Description

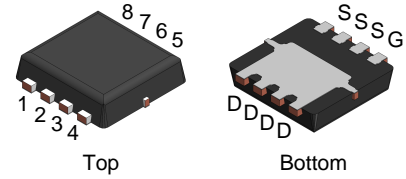
This N-Channel MOSFET is produced using onsemi's advanced POWERTRENCH process that incorporates Shielded Gate technology. This process has been optimized for the on-state resistance and yet maintain superior switching performance.

Features

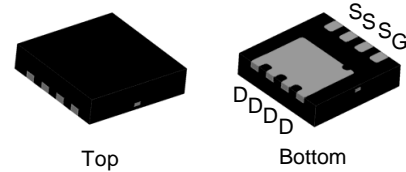
- Max $r_{DS(on)}$ = 134 mΩ at $V_{GS} = 10\text{ V}$, $I_D = 2.8\text{ A}$
- Max $r_{DS(on)}$ = 186 mΩ at $V_{GS} = 6\text{ V}$, $I_D = 2.4\text{ A}$
- Low Profile – 1 mm Max in Power 33
- 100% UIL Tested
- These Devices are Pb-Free and are RoHS Compliant

Applications

- DC – DC Conversion

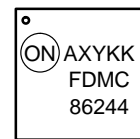


WDFN8 3.3x3.3, 0.65P
CASE 511DR
FDMC86244

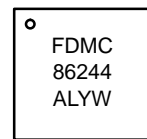


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MARKING DIAGRAM



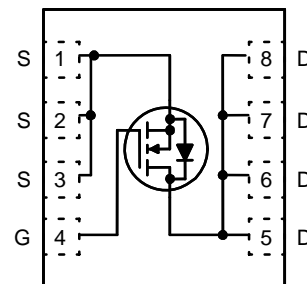
FDMC86244



FDMC86244-L701

FDMC86244 = Specific Device Code
A = Assembly Site
XY = 2-Digit Date Code
KK = 2-Digit Lot Run Traceability Code
L = Wafer Lot Number
YW = Assembly Start Week

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 6.

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MOSFET MAXIMUM RATINGS ($T_A = 25\text{ }^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DS}	Drain to Source Voltage	150	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current	Continuous $T_C = 25\text{ }^\circ\text{C}$	9.4
		Continuous (Note 2a) $T_A = 25\text{ }^\circ\text{C}$	2.8
		Pulsed	12
E_{AS}	Single Pulse Avalanche Energy (Note 1)	12	mJ
P_D	Power Dissipation $T_C = 25\text{ }^\circ\text{C}$	26	W
	Power Dissipation (Note 2a) $T_A = 25\text{ }^\circ\text{C}$	2.3	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

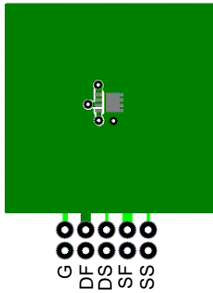
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Starting $T_J = 25\text{ }^\circ\text{C}$; N-ch: $L = 1.0\text{ mH}$, $I_{AS} = 5.0\text{ A}$, $V_{DD} = 135\text{ V}$, $V_{GS} = 10\text{ V}$.

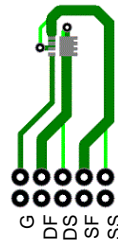
THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	4.7	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 2a)	125	

2. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a $1.5 \times 1.5\text{ in.}$ board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a $53\text{ }^\circ\text{C/W}$ when mounted on a 1 in^2 pad of 2 oz copper



b $125\text{ }^\circ\text{C/W}$ when mounted on a minimum pad of 2 oz copper

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ELECTRICAL CHARACTERISTICS ($T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0\ \text{V}$	150	–	–	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$	–	106	–	mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 120\ \text{V}$, $V_{GS} = 0\ \text{V}$	–	–	1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\ \text{V}$, $V_{DS} = 0\ \text{V}$	–	–	± 100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\ \mu\text{A}$	2	2.6	4	V
$\Delta V_{GS(th)} / \Delta T_J$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$	–	–9	–	mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\ \text{V}$, $I_D = 2.8\ \text{A}$	–	105	134	m Ω
		$V_{GS} = 6\ \text{V}$, $I_D = 2.4\ \text{A}$	–	120	186	
		$V_{GS} = 10\ \text{V}$, $I_D = 2.8\ \text{A}$, $T_J = 125\text{ }^\circ\text{C}$	–	199	254	
g_{FS}	Forward Transconductance	$V_{DS} = 10\ \text{V}$, $I_D = 2.8\ \text{A}$	–	8	–	S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 75\ \text{V}$, $V_{GS} = 0\ \text{V}$, $f = 1\ \text{MHz}$	–	257	345	pF
C_{oss}	Output Capacitance		–	32	45	pF
C_{rss}	Reverse Transfer Capacitance		–	1.8	5	pF

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 75\ \text{V}$, $I_D = 2.8\ \text{A}$, $V_{GS} = 10\ \text{V}$, $R_{GEN} = 6\ \Omega$	–	5.3	11	ns
t_r	Rise Time		–	1.5	10	ns
$t_{d(off)}$	Turn-Off Delay Time		–	9.9	20	ns
t_f	Fall Time		–	2.3	10	ns
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\ \text{V}$ to $10\ \text{V}$, $V_{DD} = 75\ \text{V}$, $I_D = 2.8\ \text{A}$	–	4.2	5.9	nC
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\ \text{V}$ to $5\ \text{V}$, $V_{DD} = 75\ \text{V}$, $I_D = 2.8\ \text{A}$	–	2.4	3.4	nC
Q_{gs}	Total Gate Charge	$V_{DD} = 75\ \text{V}$, $I_D = 2.8\ \text{A}$	–	1.1	–	nC
Q_{gd}	Gate to Drain "Miller" Charge		–	1.0	–	nC

DRAIN-SOURCE DIODE CHARACTERISTICS

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\ \text{V}$, $I_S = 2.8\ \text{A}$ (Note 3)	–	0.81	1.3	V
		$V_{GS} = 0\ \text{V}$, $I_S = 2\ \text{A}$ (Note 3)	–	0.79	1.2	
t_{rr}	Reverse Recovery Time	$I_F = 2.8\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$	–	48	76	ns
Q_{rr}	Reverse Recovery Charge		–	38	61	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.

TYPICAL CHARACTERISTICS ($T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted)

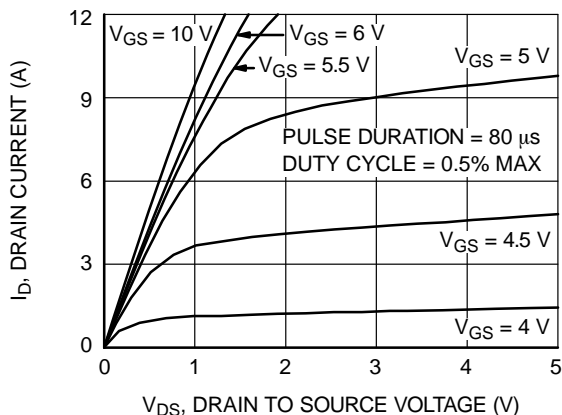


Figure 1. On Region Characteristics

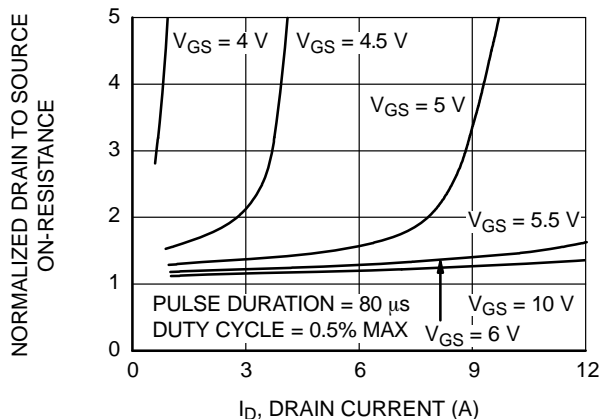


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

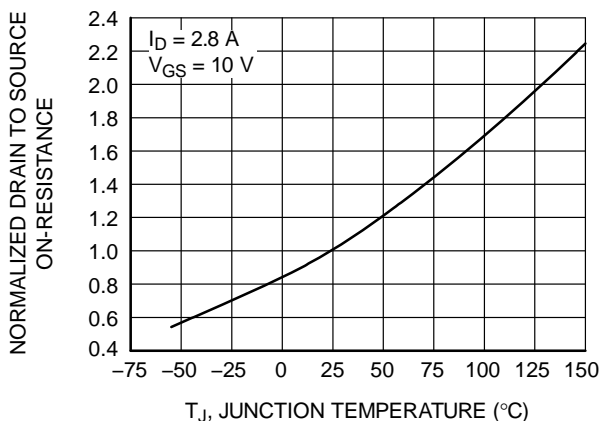


Figure 3. Normalized On Resistance vs. Junction Temperature

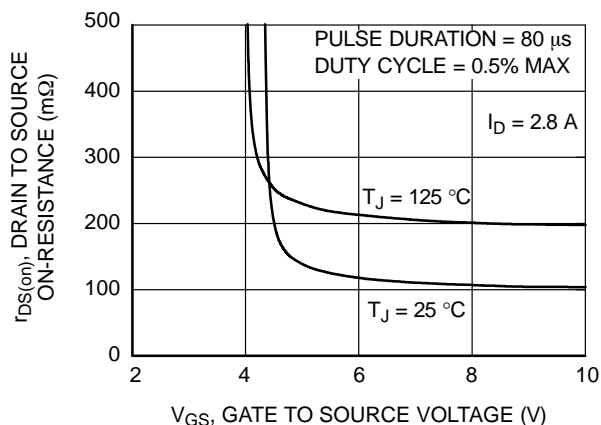


Figure 4. On-Resistance vs. Gate to Source Voltage

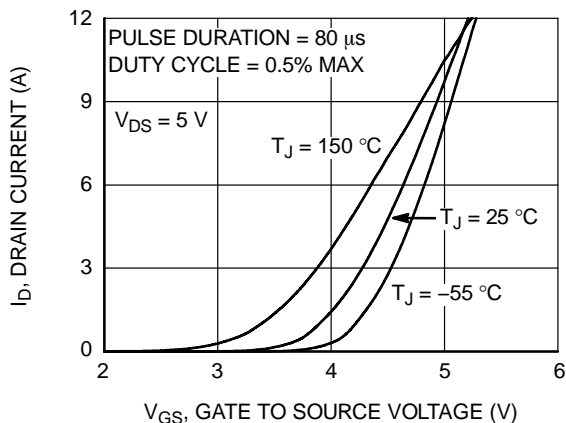


Figure 5. Transfer Characteristics

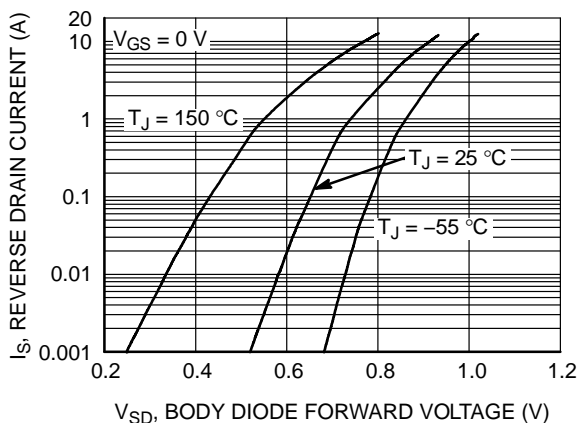


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS ($T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted) (continued)

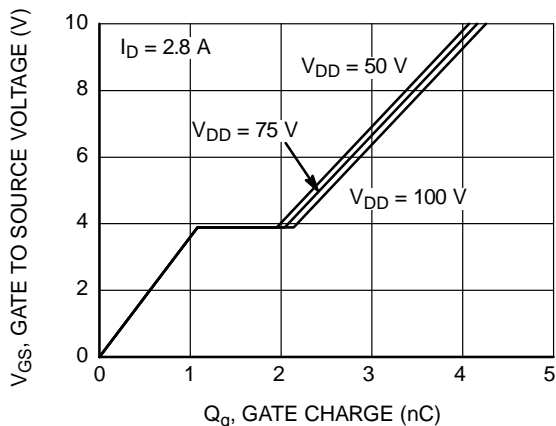


Figure 7. Gate Charge Characteristics

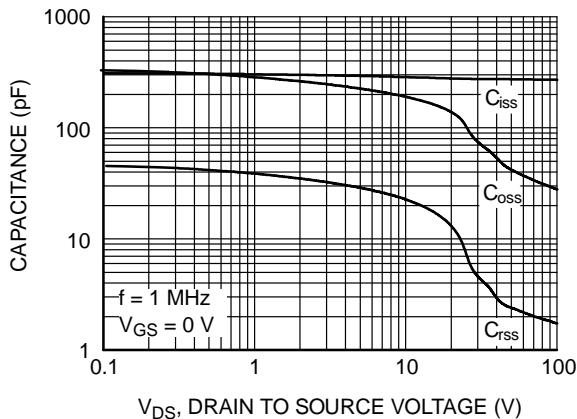


Figure 8. Capacitance vs. Drain to Source Voltage

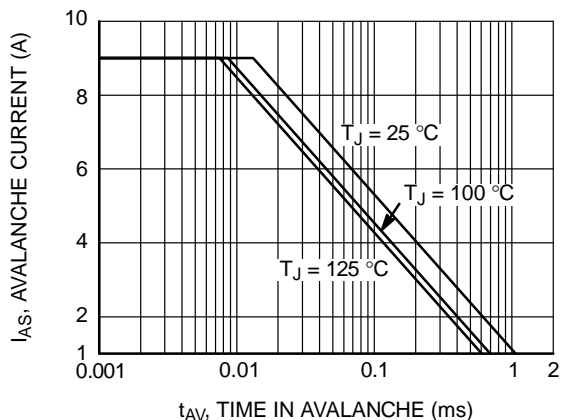


Figure 9. Unclamped Inductive Switching Capability

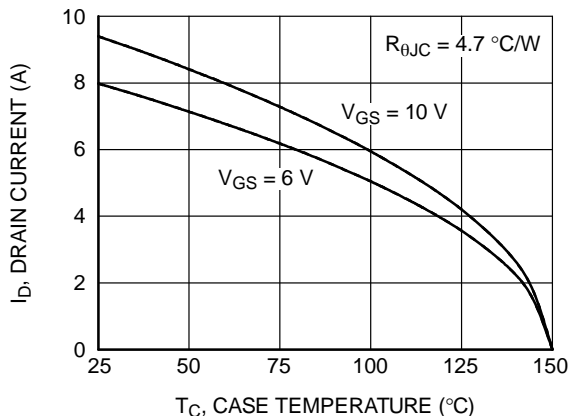


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

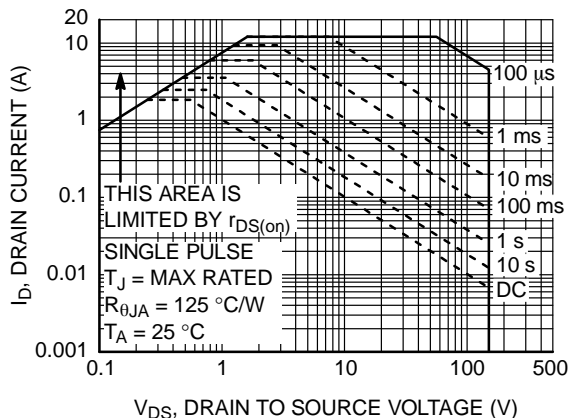


Figure 11. Forward Bias Safe Operating Area

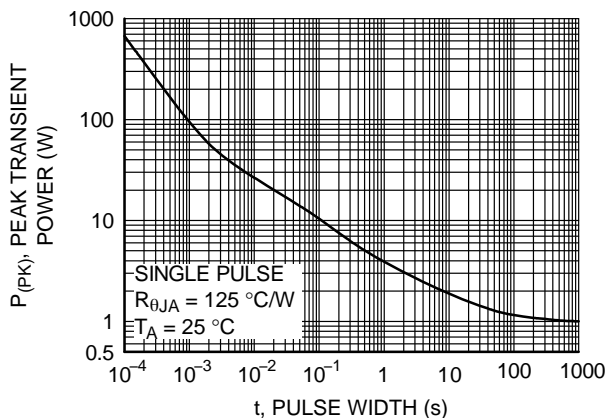


Figure 12. Single Pulse Maximum Power Dissipation

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TYPICAL CHARACTERISTICS ($T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted) (continued)

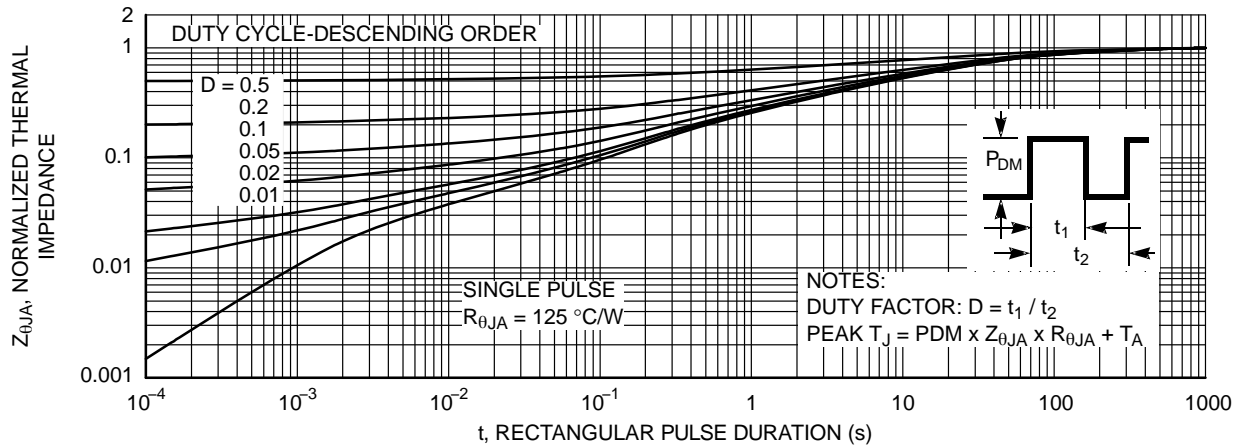


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

ORDERING INFORMATION

Device	Device Marking	Package Type	Reel Size	Tape Width	Shipping [†]
FDMC86244	FDMC86244	WDFN8 3.3x3.3, 0.65P Power 33 (Pb-Free)	13"	12 mm	3000 / Tape & Reel

DISCONTINUED (Note 4)

FDMC86244-L701	FDMC86244	WDFN8 3.3x3.3, 0.65P Power 33 (Pb-Free)	13"	12 mm	3000 / Tape & Reel
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[†] For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

4. **DISCONTINUED:** This device is not available. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.

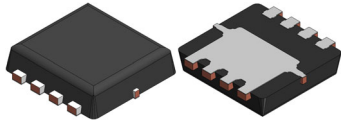
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REVISION HISTORY

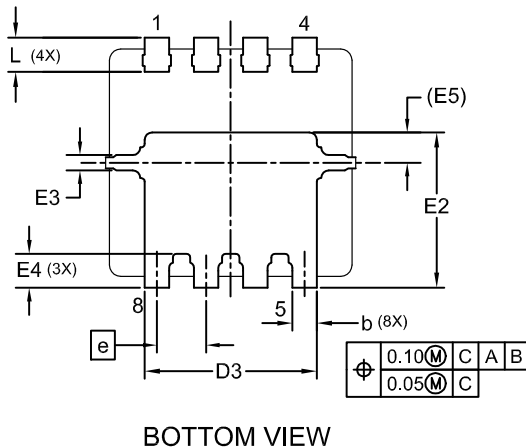
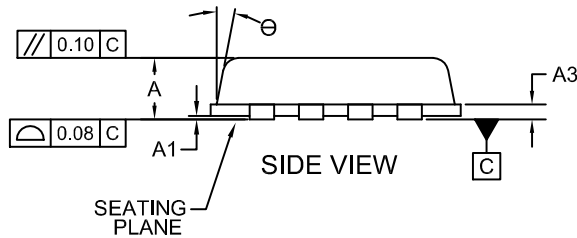
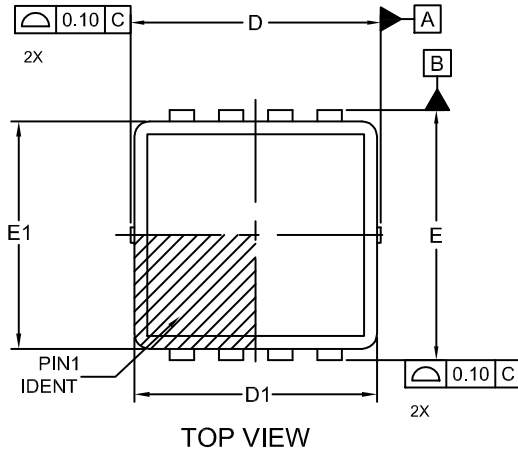
Revision	Description of Changes	Date
4	Rebranded the document to onsemi format. FDMC86244-L701 OPN marked as Discontinued.	2/16/2026

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.



WDFN8 3.3x3.3, 0.65P
CASE 511DR
ISSUE B

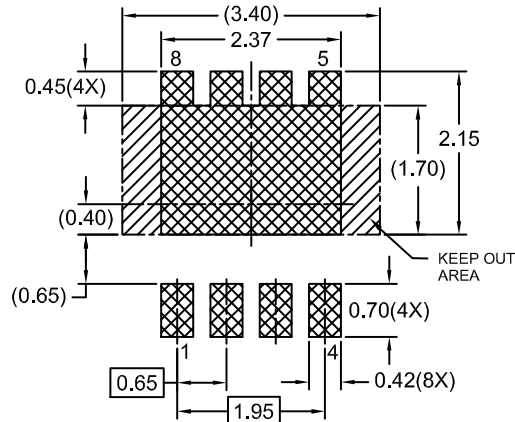
DATE 02 FEB 2022



NOTES:

- A. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- B. SEATING PLANE IS DEFINED BY TERMINAL TIPS ONLY
- C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH PROTRUSIONS NOR GATE BURRS. MOLD FLASH PROTRUSION OR GATE BURR DOES NOT EXCEED 0.150MM.

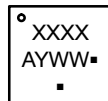
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	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3	0.15	0.20	0.25
b	0.27	0.32	0.37
D	3.20	3.30	3.40
D1	3.10	3.20	3.30
D3	2.17	2.27	2.37
E	3.20	3.30	3.40
E1	2.90	3.00	3.10
E2	1.95	2.05	2.15
E3	0.15	0.20	0.25
E4	0.30	0.40	0.50
E5	0.40 REF		
e	0.65 BSC		
L	0.30	0.40	0.50
Θ	0°	-	12°



RECOMMENDED LAND PATTERN

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



- XXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

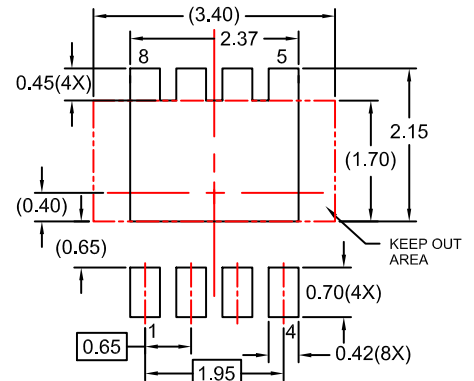
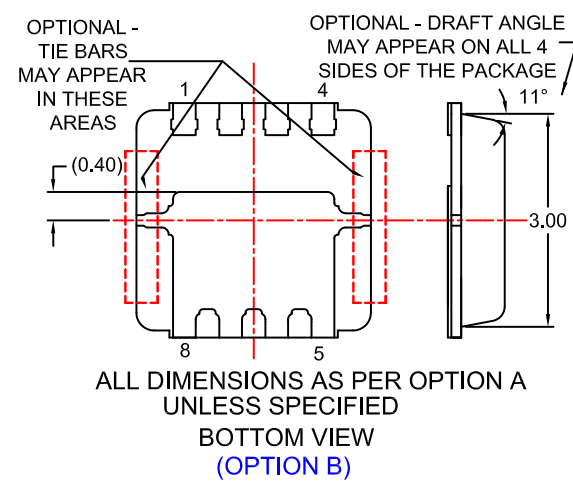
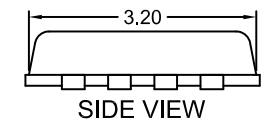
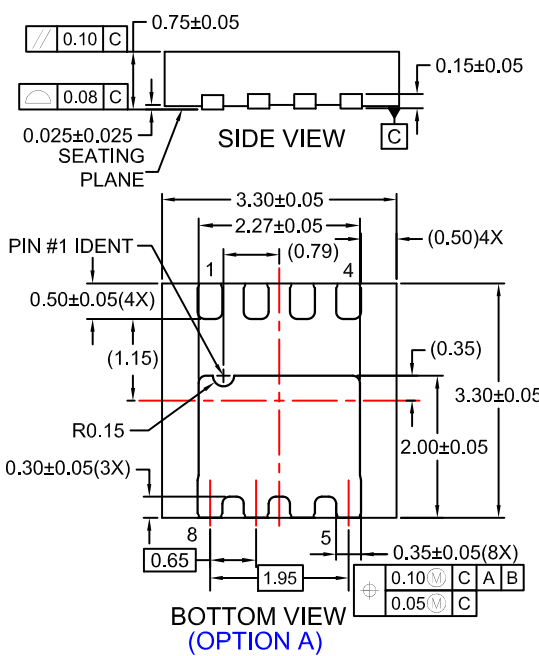
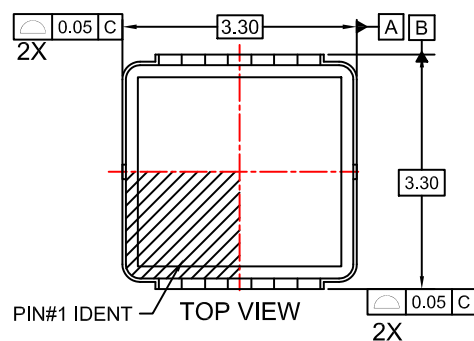
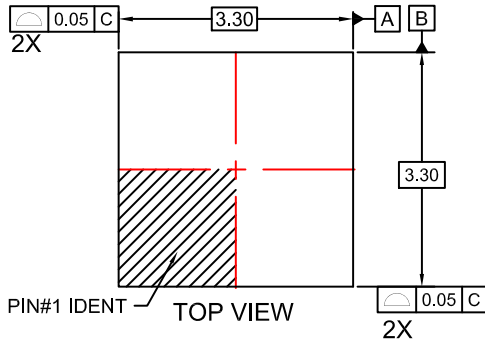
(Note: Microdot may be in either location)

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CASE 511DQ
ISSUE O

DATE 31 OCT 2016



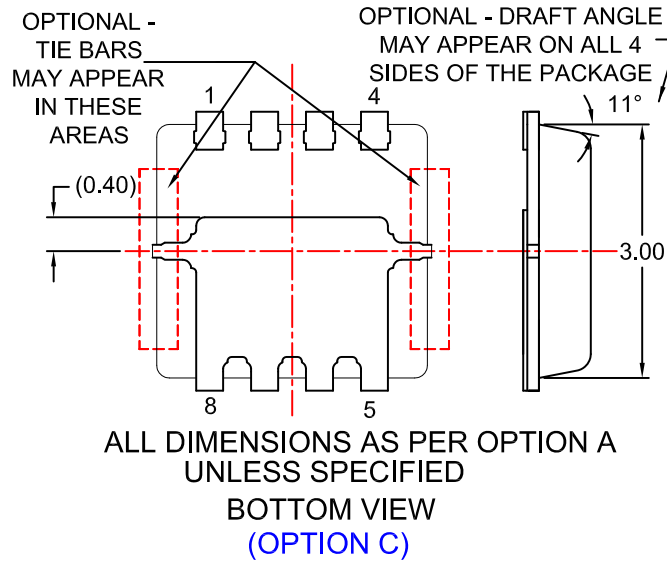
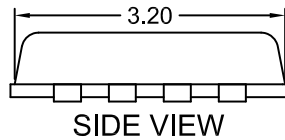
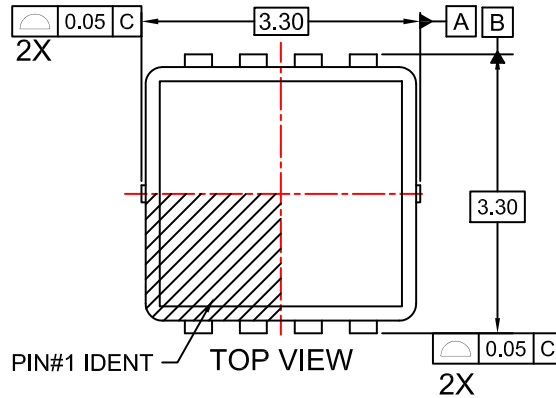
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WDFN8 3.3x3.3, 0.65P
CASE 511DQ
ISSUE O

DATE 31 OCT 2016



NOTES:

- A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC REGISTRATION MO-240.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN
- E. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. BURRS OR MOLD FLASH SHALL NOT EXCEED 0.10MM.

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