PERFECT WIRELESS EXPERIENCE

FIBOCOM SC138 Series Hardware Guide

Version: V1.0.1

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Applicability Type

No.	Product Model	Description
1	SC138-EAU-00	2+32 eMCP, Version 4G
2	SC138-EAU-20	4+64 uMCP, Version 4G
3	SC138-W-00	2+32 eMCP, Version WiFi
4	SC138-W-20	4+64 uMCP, Version WiFi

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Note

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Trademark

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Revision History

Version	Author	Reviewer	Approver	Date	Description
V1.0.0	Tan Qiuye	Tu Min	Chen Guojiang	2020-12-29	Initial version
V1.0.1	Ye Xincai Huang Feng	Tu Min Li Xiyi	Chen Guojiang	2021-04-18	First revision, Adding W-20 version; Updating some RF parameters.

Contents

1 About This Document

1.1 Description

The document describes information on electrical characteristics, RF performance, structural dimension, application environment, etc. of SC138 series modules. With the help of this document and other related documents, the application developer can quickly understand the hardware functions of SC138-EAU series modules and develop the hardware of the product.

1.2 References

This product is designed with reference to the following standards:

- 3GPP TS 51.010-1 V10.5.0: Mobile Station (MS) conformance specification; Part 1: Conformance specification
- 3GPP TS 34.121-1 V10.8.0: User Equipment (UE) conformance specification; Radio transmission and reception (FDD); Part 1: Conformance specification
- 3GPP TS 36.521-1 V12.9.0: User Equipment (UE) conformance specification; Radio transmission and reception; Part 1: Conformance testing
- 3GPP TS 21.111 V10.0.0: U(U)SIM and IC card requirements
- 3GPP TS 51.011 V4.15.0: Specification of the Subscriber Identity Module -Mobile Equipment ((U)SIM-ME) interface
- 3GPP TS 31.102 V10.11.0: Characteristics of the Universal Subscriber Identity Module (U(U)SIM) application
- 3GPP TS 31.11 V10.16.0: Universal Subscriber Identity Module (U(U)SIM) Application Toolkit (USAT)
- 3GPP TS 36.124V10.3.0: Electro Magnetic Compatibility (EMC) requirements for mobile terminals and ancillary equipment
- 3GPP TS 27.007 V10.0.8: AT command set for User Equipment (UE)
- 3GPPTS27.005 V10.0.1: Use of Data Terminal Equipment - Data Circuit terminating Equipment
- IEEE 802.11n WLAN MAC and PHY, October 2009 + IEEE 802.11-2007 WLAN MAC and PHY, June

2007

- IEEE Std 802.11b, IEEE Std 802.11n, IEEE Std 802.11a, IEEE Std 802.11g, IEEE Std 802.11ac
- IEEE 802.11-2007 WLAN MAC and PHY, June 2007
- Bluetooth Radio Frequency TSS and TP Specification 1.2/2.0/2.0 + EDR/2.1/2.1+ EDR/3.0/3.0+
- HS, August 6, 2009
- Bluetooth Low Energy RF PHY Test Specification, RF-PHY.TS/4.0.0, December 15, 2009
- Bluetooth Low Energy RF PHY Test Specification, RF-PHY.TS/5.0.2, December 07,2017

1.3 Related Documents

FIBOCOM SC138 Series SMT Design Guide

2 Product Overview

2.1 Product Introduction

SC138 series intelligent modules integrate core devices such as Baseband, eMCP, PMU, Transceiver and PA, and support remote communication modes of FDD/TDD-LTE, WCDMA, GSM and multiple types, WIFI/BT short-range wireless transmission technology and GNSS wireless positioning technology(SC138-W support WiFi/BT only). SC138-EAU series modules are embedded in the open Android operating system and support multiple interfaces such as MIPI/USB/UART/SPI/I2C, so they are the preferred schemes for the core system of wireless intelligent products. The corresponding network type and the band of SC138 modules are shown in the following table:

Table 2-1 Available band of SC138-EAU

Mode	Band
GSM/GPRS/EDGE	GSM850/EGSM900/PCS1900/DCS1800
WCDMA	Band 1/2/5/8
FDD-LTE	Band 1/3/5/7/8/20/28
TDD-LTE	Band 38/40/41(2496-2690MHz)
WIFI 802.11a/b/g/n/ac	2402-2482 MHz，5170-5835MHz
BT5.0	2402-2480 MHz
GNSS	GPS +GLONASS +BeiDou

2.2 Performance

SC138 modules are packaged with LCC+LGA and have a total of 276 pins, including 148 LCC pins and 128 LGA pins, with the dimensions of 41 mm × 41 mm × 2.8 mm. They can be embedded in various M2M product applications, and are applicable to the development of intelligent POS, cash register, robot, unmanned aerial vehicle, home automation, security monitoring, multimedia terminal and other intelligent devices. The following table describes the detailed performance parameters of SC138 series modules.

Table 2-2 Performance and specification

Performance	Description
Power supply	DC 3.5 V–4.2 V Typical voltage: 3.8 V
Application processor	Kyro™260 8 core architecture 64-bit processor; the main frequency is up to 2 GHz
Storage	16 Gb LPDDR4X+32 GB eMMC Flash (optional)
Power level	Class 4 (33dBm±2dB) for GSM850/900 Class 1 (30dBm±2dB) for DCS1800/1900 Class E2 (27dBm±3dB) for GSM850/900 8-PSK Class E2 (26dBm+3/-4dB) for DCS1800/1900 8-PSK Class 3 (24dBm+1/-3dB) for WCDMA bands Class 3 (23dBm±2dB) for LTE FDD bands Class 3 (23dBm±2dB) for LTE TDD bands
GSM/GPRS/EDGE characteristics	R99: CSD transmission rate: 9.6 kbps and 14.4 kbps GPRS: Support GPRS multi-slot class 33. Coding format: CS-1/CS-2/CS-3 and CS-4 Maximum 5 Rx slots per frame EDGE: Support EDGE multi-slot class 33. Support GMSK and 8-PSK. Uplink coding format: CS 1-4 and MCS 1-9 Downlink coding format: CS 1-4 and MCS 1-9

Performance	Description
WCDMA characteristics	Support 3GPP R9 DC-HSPA+ Support 16-QAM, 64-QAM and QPSK modulation CAT8 HSUPA: maximum uplink rate: 11.4 Mbps CAT24 DC-HSPA+: maximum downlink rate: 42 Mbps
LTE characteristics	Support FDD/TDD R12 CAT4 (UL CAT5 DL CAT4) Support 1.4 M-20 M RF bandwidth Downlink supports multi-user MIMO Maximum uplink rate: 75 Mbps; maximum downlink rate: 150 Mbps
VLAN characteristics	Support 2.4 G and 5 G WLAN wireless communication, and 802.11 a, 802.11 b, 802.11 g, 802.11 n, 802.11 ac and other types, with the maximum rate up to 433 Mbps
Bluetooth characteristics	BT5.0
Satellite positioning	GPS +GLONASS +BeiDou
SMS	Text and PDU mode Point-to-point MO and MT SMS cell broadcast SMS storage: It is stored in the module by default.
LCD interface	1 set of 4-Lane MIPI_DSI interfaces, with the maximum support of 2,520 × 1,080 1 set of DP over type-C interface with developing functions
Camera interface	3 sets of 4-Lane MIPI_CSI interfaces, with the maximum rate up to 2.5 Gbps per Lane, which supports the maximum 25 MP pixel.
Audio interface	Audio input: 3 sets of analog MIC inputs Internal integration bias Audio output: Class AB stereo earphone output Class AB differential handset output

Performance	Description
	Class D differential speaker power amplifier output
USB interface	USB 2.0 high speed (HS) interface, with the maximum data transmission rate of 480 Mbps USB 3.1 super speed (SS) interface, with the maximum data transmission rate of 5 Gbps Support USB OTG.
(U)SIM interface	2 sets of (U)SIM interfaces, supporting (U)SIM: 1.8 V/3 V self-adaption Support dual-SIM dual standby and hot plug functions (off by default).
UART interface	3 sets of UART serial ports, with the maximum rate up to 4 Mbps, wherein: 1 set of four-wire serial port supporting RTS and CTS hardware flow control 1 set of two-wire serial port 1 set of two-wire debugging serial port
SDIO interface	Support SD 3.0 and 4 bits SDIO; SD supports hot plug.
I2C interface	6 sets of I2C interfaces, which can be used for TP, Camera, Sensor and other peripherals
ADC interface	Universal 15-bit precise ADC
RTC	Supported
Antenna interface	TRX antenna, DRX antenna, GNSS antenna and WIFI/BT antenna interfaces
Physical characteristics	Dimensions: 41mm × 41mm × 2.8mm Package: 148 LCC + 128 LGA Weight: 9.6±1g
Temperature range	Operating temperature: –30°C to 75°C[1)] Expansion temperature: –40°C~85°C [2)]

Performance	Description
	Storage temperature: –40°C to 85°C
Software upgrade	USB/OTA/SD
RoHS	Conform to RoHS standard.

Note:

1) When the modules work in this temperature range, their functions are normal, and relevant performance meets the requirements of 3GPP standard.
2) When the modules work in this temperature range, their functions are normal, but relevant performance may not meet the requirements of 3GPP standard. And the temperature return to Operating temperature, the performance meets the requirements of 3GPP standard.

2.3 Function Diagram

The function diagram shows the main hardware functions of SC138 series modules, including the following items:

- Baseband
- Wireless transceiver
- Power management
- Storage
- Peripheral interface
  - -- Communication extension interface (USB/UART/I2C/SDC)
  - -- (U)SIM interface
  - -- MIPI DSI interface
  - -- MIPI CSI interface
  - -- Analog audio interface

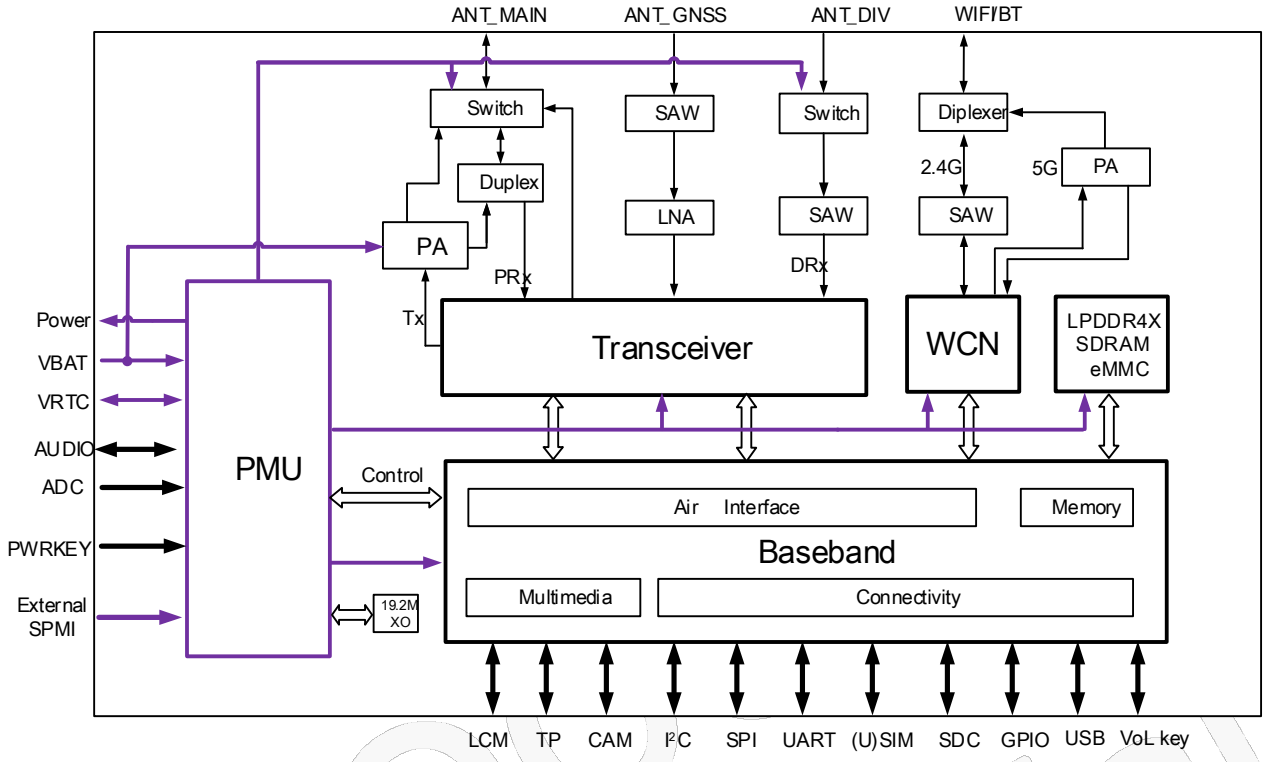
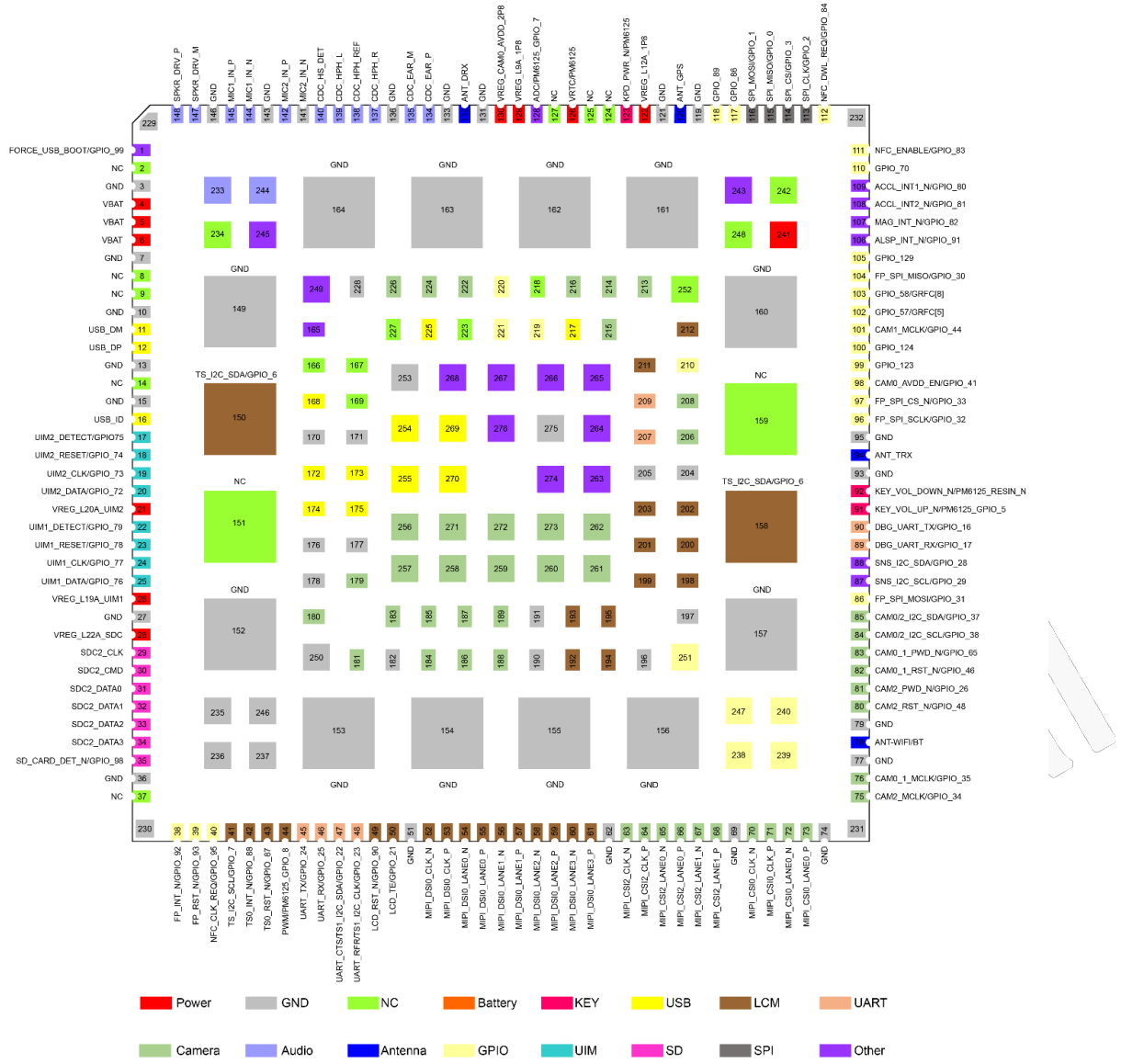


Figure 2-1 Function diagram

2.4 Pin Definition

2.4.1 Pin Distribution



Note:

"NC" stands for No Connect. The pin at this position is reserved, and no connection is required.

2.4.2 Pin Description

Table 2-3 Description of I/O parameters

Type	Description
IO	Input/output
DI	Digital input
DO	Digital output

Type	Description
PI	Power input
PO	Power output
AI	Analog input
AO	Analog output
OD	Open drain

The pins of SC138 modules are described in the following table:

Pin Name	Pin No.	I/O	Pin Description	Remarks
Power				
VBAT	4,5,6	PI	Main power supply input	-
VRTC	126	PI/PO	RTC power supply pin	-
VREG_CAM0_DVDD_1P104	226	PO	1.1 V voltage output	-
VREG_L9A_1P8	129	PO	1.8 V voltage output	-
VREG_L12A_1P8	122	PO	1.8 V voltage output	-
VREG_CAM_AF_2P8	224	PO	2.8 V voltage output	-
VREG_L22A_2P96	28	PO	SD power supply	-
VREG_L19A_1P8	26	PO	(U)SIM 1 power supply	1.8 V/3 V self-adaption
VREG_L20A_1P8	21	PO	(U)SIM 2 power supply	1.8 V/3 V self-adaption
VREG_CAM0_AVDD_2P8	130	PO	2.8 V voltage output	-

Pin Name	Pin No.	I/O	Pin Description	Remarks
VREG_CAM1_2_AVDD_2P8	222	PO	2.8 V voltage output	-
VREG_CAM1_2_DVDD_1P2	264	PO	1.2 V voltage output, camera power supply	-
VREG_ALS_VLED_3P0	265	PO	3.0 V voltage output, light sensor power supply	-
VREG_3P0	266	PO	3.0 V voltage output	-
VREG_L15A_3P128	241	PO	3.1 V voltage output	-
GND	3,7,10,13,15,27,36,51,62,69,74,77,79,93,95,119,121,131,133,136, 143,146,149,152,153,154,155,156,157,160,161,162,163,164,170,171, 176,177,178,182,190,191,196,197,204,205,228,229,230,231,232,235, 236,237,246,250,253,275		Ground	58 pcs
Special Function Interface				
CBL_PWR_N	165	DI	Trigger startup signal	-
Key				
KPD_PWR_N	123	DI	Startup and shutdown key	Active low; do not pull up externally.
KEY_VOL_UP_N	91	DI	Volume up key	Active low
KEY_VOL_DOWN_N	92	DI	Volume down key	Active low; volume down key by default, which can be configured for low level

Pin Name	Pin No.	I/O	Pin Description	Remarks
				shutdown and restart; do not pull up externally.
(U)SIM Interface				
UIM1_DATA	25	I/O	(U)SIM 1 data signal	-
UIM1_CLK	24	DO	(U)SIM 1 clock signal	-
UIM1_RESET	23	DO	(U)SIM 1 reset signal	-
UIM1_DETECT	22	DI	(U)SIM 1 plug detection	Off by default
UIM2_DATA	20	I/O	(U)SIM 2 data signal	-
UIM2_CLK	19	DO	(U)SIM 2 clock signal	-
UIM2_RESET	18	DO	(U)SIM 2 reset signal	-
UIM2_DETECT	17	DI	(U)SIM 2 plug detection	Off by default
VREG_L19A_1P8	26	PO	(U)SIM 1 power supply	1.8 V/3 V self-adaption
VREG_L20A_1P8	21	PO	(U)SIM 2 power supply	1.8 V/3 V self-adaption
SD Interface				
SDC2_DATA3	34	I/O	SD data interface	-
SDC2_DATA2	33	I/O	SD data interface	-
SDC2_DATA1	32	I/O	SD data interface	-
SDC2_DATA0	31	I/O	SD data interface	-
SDC2_CLK	29	DO	SD clock	-
SDC2_CMD	30	I/O	SD command interface	-
SD_CARD_DET_N	35	DI	SD detection	Active low by default
VREG_L22A_2P96	28	PO	SD power supply	-

Pin Name	Pin No.	I/O	Pin Description	Remarks
I2C Interface				
SNS_I2C_SCL	87	OD	I2C clock	Being used for sensor by default
SNS_I2C_SDA	88	OD	I2C data line	Being used for sensor by default
TS_I2C_SCL	41	OD	I2C clock	Being used for TP by default
TS_I2C_SDA	150,158	OD	I2C data line	Being used for TP by default
CAM0_I2C_SCL	84	OD	I2C clock	Being used for camera by default
CAM0_I2C_SDA	85	OD	I2C data line	Being used for camera by default
CAM2_SCL	206	OD	I2C clock	Being used for camera by default
CAM2_SDA	208	OD	I2C data line	Being used for camera by default
APPS_I2C_SCL	268	OD	I2C clock	Need be Pulled-up too, when unused
APPS_I2C_SDA	267	OD	I2C data line	
USB Interface				

Pin Name	Pin No.	I/O	Pin Description	Remarks
USB_IN_DET	168	PI	VBUS input Detection	-
USB_DP	12	I/O	USB 2.0 differential data signal+	-
USB_ DM	11	I/O	USB 2.0 differential data signal-	-
USB_ID	16	DI	USB ID pin	
USB_SS_RX1_P	269	DI	USB 3.1 differential data reception+	-
USB_SS_RX1_M	254	DI	USB 3.1 differential data reception-	-
USB_SS_TX1_P	270	DO	USB 3.1 differential data sending+	-
USB_SS_TX1_M	255	DO	USB 3.1 differential data sending-	-
USB_SS_RX0_P	173	DI	USB 3.1 differential data reception+	-
USB_SS_RX0_M	175	DI	USB 3.1 differential data reception-	-
USB_SS_TX0_P	172	DO	USB 3.1 differential data sending+	-
USB_SS_TX0_M	174	DO	USB 3.1 differential data sending-	-
DP_AUX_N	263	I/O	DisplayPort auxiliary transmission channel-	-
DP_AUX_P	274	I/O	DisplayPort auxiliary transmission channel+	-
USB_PHY_PS	276	DI	USB front and back plug logo	-
UART Interface				
DBG_UART_TX	90	DO	UART data sending (QUP0 SE4)	Debug serial port by default

Pin Name	Pin No.	I/O	Pin Description	Remarks
DBG_UART_RX	89	DI	UART data reception (QUP0 SE4)	
UART_TX	45	DO	UART data sending (QUP1 SE0)	-
UART_RX	46	DI	UART data reception (QUP1 SE0)	-
UART_CTS/TS1_I2C_SDA	47	DI	UART clear to send (QUP1 SE0)	Can be configured to I3C
UART_RFR/IS1_I2C_CLK	48	DO	UART request to send (QUP1 SE0)	Can be configured to I3C
UART_TX/GPIO_8	209	DO	UART data sending (QUP0 SE2)	-
UART_RX/GPIO_9	207	DI	UART data reception (QUP0 SE2)	-
SPI Interface				
SPI_CLK	113	DO	SPI clock	-
SPI_CS	114	DO	SPI chip selection	-
SPI_MISO	115	DI	SPI MISO	-
SPI_MOSI	116	DO	SPI MOSI	-
I2S Interface				
GPIO_125/I2S1_SCK	247	DO	I2S serial clock	-
GPIO_126/I2S1_WS	238	DO	I2S frame clock	-
GPIO_127/I2S1_DATA0	239	DO	I2S data 0	-
GPIO_128/I2S1	240	DO	I2S data 1	-

Pin Name	Pin No.	I/O	Pin Description	Remarks
_DATA1				
GPIO_118/MCLK2	251	DO	I2S system clock	Boot Config, Flash Memory type configure
Display Screen Interface				
MIPI_DSI0_CLK_P	53	AO	Main TP MIPI clock+	-
MIPI_DSI0_CLK_N	52	AO	Main TP MIPI clock-	-
MIPI_DSI0_LANE0_P	55	AI/AO	Main TP MIPI Lane0+	-
MIPI_DSI0_LANE0_N	54	AI/AO	Main TP MIPI Lane0-	-
MIPI_DSI0_LANE1_P	57	AI/AO	Main TP MIPI Lane1+	-
MIPI_DSI0_LANE1_N	56	AI/AO	Main TP MIPI Lane1-	-
MIPI_DSI0_LANE2_P	59	AI/AO	Main TP MIPI Lane2+	-
MIPI_DSI0_LANE2_N	58	AI/AO	Main TP MIPI Lane2-	-
MIPI_DSI0_LANE3_P	61	AI/AO	Main TP MIPI Lane3+	-
MIPI_DSI0_LANE3_N	60	AI/AO	Main TP MIPI Lane3-	-
LCD0_RST_N	49	DO	Main TP reset signal	-
PWM	44	DO	LCD backlight PWM control	-
LCD_BL_EN	211	DO	LCD backlight enabling control	-

Pin Name	Pin No.	I/O	Pin Description	Remarks
LCD_TE	50	DI	LCD refreshing synchronization signal	NC when it is not in use.
TP interface				
TS0_INT_N	42	DI	Main TP interrupt signal	-
TS0_RST_N	43	DO	Main TP reset signal	-
Camera Interface				
MIPI_CSI2_CLK_P	64	AO	Camera 2 MIPI clock+	-
MIPI_CSI2_CLK_N	63	AO	Camera 2 MIPI clock-	-
MIPI_CSI2_LANE0_P	66	AI/AO	Camera 2 MIPI Lane 0+	-
MIPI_CSI2_LANE0_N	65	AI/AO	Camera 2 MIPI Lane 0-	-
MIPI_CSI2_LANE1_P	68	AI/AO	Camera 2 MIPI Lane 1+	-
MIPI_CSI2_LANE1_N	67	AI/AO	Camera 2 MIPI Lane 1-	-
MIPI_CSI2_LANE2_P	181	AI/AO	Camera 2 MIPI Lane 2+	-
MIPI_CSI2_LANE2_N	183	AI/AO	Camera 2 MIPI Lane 2-	-
MIPI_CSI2_LANE3_P	180	AI/AO	Camera 2 MIPI Lane 3+	-
MIPI_CSI2_LANE3_N	179	AI/AO	Camera 2 MIPI Lane 3-	-
CAM0_MCLK	75	DO	Camera 0 MCLK signal	-
CAM0_RST_N	80	DO	Camera 0 reset signal	-

Pin Name	Pin No.	I/O	Pin Description	Remarks
CAM0_PWD_N	81	DO	Camera 0 PWD signal	-
MIPI_CSI0_CLK_P	71	AO	Camera 3 MIPI clock+	-
MIPI_CSI0_CLK_N	70	AO	Camera 3 MIPI clock-	-
MIPI_CSI0_LANE0_P	73	AI/AO	Camera 3 MIPI Lane 0+	-
MIPI_CSI0_LANE0_N	72	AI/AO	Camera 3 MIPI Lane 0-	-
MIPI_CSI0_LANE1_P	184	AI/AO	Camera 3 MIPI Lane 1+	-
MIPI_CSI0_LANE1_N	185	AI/AO	Camera 3 MIPI Lane 1-	-
MIPI_CSI0_LANE2_P	186	AI/AO	Camera 4 MIPI Lane 2+	-
MIPI_CSI0_LANE2_N	187	AI/AO	Camera 4 MIPI Lane 2-	-
MIPI_CSI0_LANE3_P	188	AI/AO	Camera 4 MIPI Lane 3+	-
MIPI_CSI0_LANE3_N	189	AI/AO	Camera 4 MIPI Lane 3-	-
CAM1_MCLK	76	DO	Camera 1 MCLK signal	-
CAM1_RST_N	82	DO	Camera 1 reset signal	-
CAM1_PWD_N	83	DO	Camera 1 PWD signal	-
MIPI_CSI1_CLK_P	257	AO	Camera 1 MIPI clock+	
MIPI_CSI1_CLK_N	256	AO	Camera 1 MIPI clock-	

Pin Name	Pin No.	I/O	Pin Description	Remarks
MIPI_CSI1_LANE0_P	271	AI/AO	Camera 1 MIPI Lane 0+	
MIPI_CSI1_LANE0_N	258	AI/AO	Camera 1 MIPI Lane 0-	
MIPI_CSI1_LANE1_P	272	AI/AO	Camera 1 MIPI Lane 1+	
MIPI_CSI1_LANE1_N	259	AI/AO	Camera 1 MIPI Lane 1-	
MIPI_CSI1_LANE2_P	273	AI/AO	Camera 1 MIPI Lane 2+	
MIPI_CSI1_LANE2_N	260	AI/AO	Camera 1 MIPI Lane 2-	
MIPI_CSI1_LANE3_P	262	AI/AO	Camera 1 MIPI Lane 3+	
MIPI_CSI1_LANE3_N	261	AI/AO	Camera 1 MIPI Lane 3-	
CAM2_MCLK	213	DO	Camera 2 MCLK signal	-
CAM2_RST_N	214	DO	Camera 2 reset signal	-
CAM2_PWD_N	215	DO	Camera 2 PWD signal	-
IOVDD_1.8V_EN	210	DO	IOVDD power enabling signal	-
GPIO_44	101	DO	Camera 3 MCLK signal	
Audio Interface				
SPKR_DRV_P	148	AO	Loudspeaker drive output+	-
SPKR_DRV_N	147	AO	Loudspeaker drive output-	-
CDC_EAR_P	134	AO	Handset output+	-
CDC_EAR_N	135	AO	Handset output-	-
CDC_HPH_L	139	AO	Earphone left channel output	-

Pin Name	Pin No.	I/O	Pin Description	Remarks
CDC_HPH_REF	138	/	Earphone reference ground	-
CDC_HPH_R	137	AO	Earphone right channel output	-
CDC_HS_DET	140	AI	Earphone plug detection	-
MIC2_IN_P	142	AI	Earphone MIC input+	-
MIC2_IN_N	141	AI	Earphone MIC input-	-
MIC1_N	144	AI	Main MIC differential input-	-
MIC1_P	145	AI	Main MIC differential input+	-
MIC3_IN_N	233	AI	Auxiliary MIC differential input-	
MIC3_IN_P	244	AI	Auxiliary MIC differential input+	
Antenna Interface				
ANT_TRX	94	I/O	2G/3G/4G main antenna	-
ANT_DRX	132	AI	Diversity receiving antenna	-
ANT-WIFI/BT	78	I/O	WIFI/BT antenna	-
ANT_GPS	120	AI	GNSS antenna	-
Interrupt Interface				
ALSP_INT_N	106	DI	Ambient light sensor interrupt	-
MAG_INT_N	107	DI	Interruption of geomagnetic sensor	-
ACCL_INT2_N	108	DI	Interruption 2 of acceleration sensor	-
ACCL_INT1_N	109	DI	Interruption 1 of acceleration sensor	-
ADC Interface				
ADC	128	AI	ADC detection	It can be configured as 0.3 V-VBAT.
Forced Downloading Script				

Pin Name	Pin No.	I/O	Pin Description	Remarks
FORCE_USB_BOOT	1	DI	Forced downloading	The high level (1.8 V) is effective, and the module cannot be pulled up before starting.
GPIO Interface				
GPIO_32	96	I/O	General GPIO, 1.8 V power domain	B-PD:nppukp Boot Config
GPIO_95	40	I/O		B-PD:nppukp
GPIO_5	16	I/O		B-PD:nppukp
GPIO_21	50	I/O		B-PD:nppukp
GPIO_98	35	I/O		B-PD:nppukp
GPIO_30	104	I/O		B-PD:nppukp
GPIO_89	118	I/O		B-PD:nppukp
GPIO_90	49	I/O		B-PD:nppukp
GPIO_129	105	I/O		B-PD:nppukp Boot Config
GPIO_70	110	I/O		B-PD:nppukp
GPIO_86	117	I/O		B-PD:nppukp Boot Config
GPIO_87	43	I/O		B-PD:nppukp Boot Config
GPIO_88	42	I/O		B-PD:nppukp
GPIO_84	112	I/O		B-PD:nppukp
GPIO_33	97	I/O		B-PD:nppukp
GPIO_83	111	I/O		B-PD:nppukp

Pin Name	Pin No.	I/O	Pin Description	Remarks
GPIO_124	100	I/O		B-PD:nppukp
GPIO_58	103	I/O		B-PD:nppukp
GPIO_57	102	I/O		B-PD:nppukp
GPIO_130	220	I/O		B-PD:nppukp
GPIO_132	221	I/O		B-PD:nppukp
GPIO_92	38	I/O		B-PD:nppukp
GPIO_93	39	I/O		B-PD:nppukp
GPIO_95	40	I/O		B-PD:nppukp
GPIO_123	99	I/O		B-PD:nppukp
GPIO_31	86	I/O		B-PD:nppukp
GPIO_41	98	I/O		B-PD:nppukp
GPIO_116	217	I/O		B-PD:nppukp
GPIO_115	216	I/O		B-PD:nppukp
GPIO_113	212	I/O		B-PD:nppukp
GPIO_117	218	I/O		B-PD:nppukp
GPIO_119	219	I/O		B-PD:nppukp
PM6125_GPIO_1	249	I/O	PMIC GPIO	B-PD:nppukp unused first
PM6125_GPIO_2	245	I/O	PMIC GPIO	B-PD:nppukp unused first
PM6125_GPIO_4	243	I/O	PMIC GPIO	B-PD:nppukp unused first
NC Pin				
NC	2,8,9,14,37,124,125,127,151,159,166,167,169,192,193,194,195,198,199,200,201,202,203,223,225,227,234,242,248,252	NC		Hanging in the air

Note:

Pins marked with "Boot configuration" do not allow hardware pull-up.

Use CPU GPIO first, not PM6125_GPIO until there is no CPU GPIO.

The configuration of SC138 module QUP interface is described in the following table:

Pin Number	GPIO	QUP Configuration		Function 1	Function 2	Function 3	Function 4
115	GPIO_0	QUP0 SE0	L0	UART_CTS	SPI_MISO	I2C_SDA	-
116	GPIO_1		L1	UART_RFR	SPI_MOSI	I2C_SCL	-
113	GPIO_2		L2	UART_TX	SPI_SCLK	-	-
114	GPIO_3		L3	UART_RX	SPI_CS_N	-	-
267	GPIO_4	QUP0 SE1	L0	-	-	I2C_SDA	-
268	GPIO_5		L1	-	-	I2C_SCL	-
150/158	GPIO_6	QUP0 SE2	L0	UART_CTS	SPI_MISO	I2C_SDA	-
41	GPIO_7		L1	UART_RFR	SPI_MOSI	I2C_SCL	-
209	GPIO_8		L2	UART_TX	SPI_SCLK	-	-
207	GPIO_9		L3	UART_RX	SPI_CS_N	-	-
90	GPIO_16	QUP0 SE4	L0/2	UART_TX	I2C_SDA	-	-
89	GPIO_17		L1/3	UART_RX	I2C_SCL	-	-
47	GPIO_22	QUP1 SE0	L0	UART_CTS	SPI_MISO	I2C_SDA	I3C_SDA
48	GPIO_23		L1	UART_RFR	SPI_MOSI	I2C_SCL	I3C_SCL
45	GPIO_24		L2	UART_TX	SPI_SCLK	-	-
46	GPIO_25		L3	UART_RX	SPI_CS_N	-	-
81	GPIO_26		L4	-	SPI_CS1	-	-
210	GPIO_27		L5	-	SPI_CS2	-	-
88	GPIO_28	QUP1 SE2	L0	-	I2C_SDA	-	-
87	GPIO_29		L1	-	I2C_SCL	-	-
104	GPIO_30	QUP1 SE1	L0	UART_CTS	SPI_MISO	I2C_SDA	-
86	GPIO_31		L1	UART_RFR	SPI_MOSI	I2C_SCL	-
96	GPIO_32		L2	UART_TX	SPI_SCLK	-	-

97	GPIO_33		L3	UART_RX	SPI_CS_N	-	-

Note:

Only one protocol can be selected in one QUP engine at a time. For example, simultaneous UART and I2C functionality are no longer supported.

3 Application Interface

3.1 Power

SC138 provides 3 VBAT pins for connecting external power supply to the module. The range of power input voltage is 3.5 V-4.2 V, and the recommended value is 3.8 V. The performance of module power supply, such as load capacity and ripple size, will directly affect the performance and stability of the module during normal operation. The peak current of the module can reach 3 A under limiting cases. If the power supply capacity is insufficient and the power supply voltage falls to below 3 V, the module may power off or restart. The power supply voltage drop is shown in the following figure:

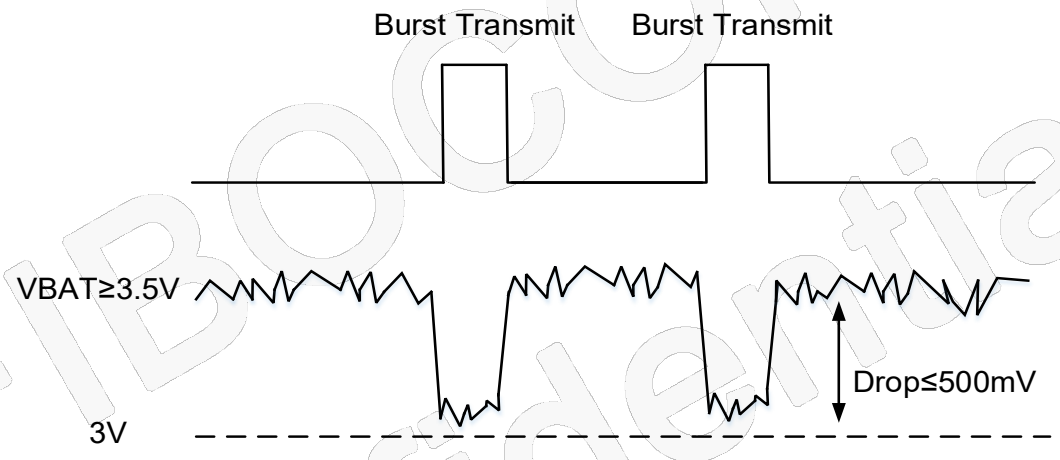


Figure 3-1 Voltage drop

3.1.1 Power Input

The external power supply supplies power to SC138 series modules through VBAT pins. In order to ensure that the power supply voltage is no less than 3 V, it is recommended to parallel two 220 uF tantalum capacitors with low ESR and filter capacitors of 1 uF, 100 nF, 39 pF 33 pF, etc. near the VBAT input terminal, and the PCB routing of VBAT be as short and wide as possible (no less than 3 mm). The ground plane of the power supply part should be as complete as possible to reduce the equivalent impedance of VBAT routing, and ensure that there will not be too large falling of voltage under high-current at the maximum transmitting power.

Table 3-1 Power supply

Parameters	Minimum Value	Recommended Value	Maximum Value	Unit
VBAT (DC)	3.5	3.8	4.2	V

Note:

The supply voltage of VBAT must be in the range of 3.5 V-4.2 V. If the supply voltage is lower than 3.5V, the system may be unstable. If the supply voltage is higher than 4.2 V, the hardware may be damaged or even destroyed.

The reference design of power supply circuit is shown in the following figure:

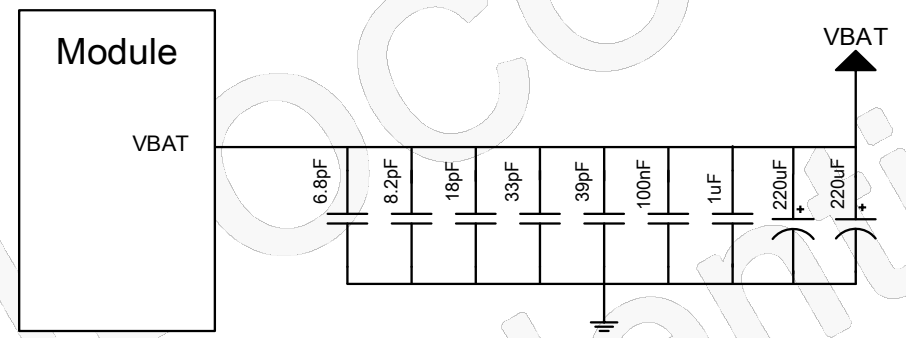


Figure 3-2 Reference design of power supply circuit

The filter capacitor design of power supply is shown in the following table:

Table 3-2 Filter capacitor design of power supply

Recommended Capacitance	Application	Description
220uF x 2	Stabilized capacitance	Low ESR capacitance is required to reduce the power fluctuation of the module during operation. LDO or DCDC power supply requirements are not less than 440 uF capacitance. Battery power supply can be reduced to 100 uF-220 uF capacitance.

Recommended Capacitance	Application	Description
1uF, 100nF	Filter capacitance	Filter out the interference caused by clock and digital signal.
39pF, 33pF, 18pF, 8.2pF, 6.8pF	Decoupling capacitance	Filter out high-frequency interference.

3.1.2 VRTC

VRTC supplies power for the RTC clock inside the module. When the VBAT power supply of the module is powered on, VRTC will output voltage; otherwise, it is powered by external power supply (for example, button battery) if the real-time clock needs to be maintained. VRTC parameters are shown in the following table:

Table 3-3 VRTC parameters

Parameters	Minimum Value	Typical Value	Maximum Value	Unit
VRTC output voltage	2.5	3.1	3.2	V
VRTC input voltage (normal clock)	2.0	3.0	3.25	V
VRTC input current (normal clock)	-	8	-	uA

If VRTC power supply is powered by external battery, the reference circuit is shown in the following figure:

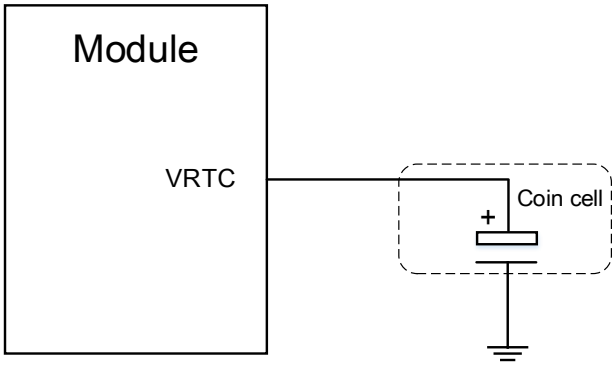


Figure 3-3 Reference circuit of VRTC power

3.1.3 Power Output

SC138 module has multiple power output channels, for peripheral circuit power supply. During application, capacitors of 33 pF and 10 pF can be paralleled to eliminate high-frequency interference.

Table 3-4 Output power

Pin Name	Programmable Range (V)	Default Voltage (V)	Drive Current (mA)
VREG_CAM0_DVDD_1P104	0.312–1.304	1.1	600
VREG_L9A_1P8	1.504–2.000	1.8	600
VREG_L12A_1P8	1.504–2.000	1.8	300
VREG_CAM_AF_2P8	1.5–3.4	2.8	400
VREG_L22A_2P96	1.504–3.544	2.96	600
VREG_L20A_1P8	1.504–3.544	1.8	150
VREG_L19A_1P8	1.504–3.544	1.8	150
VREG_CAM0_AVDD_2P8	1.5–3.4	2.8	400
VREG_CAM1_2_AVDD_2P8	1.5–3.4	2.8	400
VREG_CAM1_2_DVDD_1P2	0.528–1.504	1.2	1000
VREG_ALS_VLED_3P0	1.5–3.4	3.0	400
VREG_3P0	1.5–3.4	3.1	400
VREG_L15A_3P104	1.504–3.544	3.104	150

3.2 Control Signal

3.2.1 Startup and Shutdown

SC138 module has 1-channel on/off control signal to operate the startup/shutdown, restart, sleep/wakeup for the module.

Table 3-5 On/off control signals

Pin Name	Pin No.	I/O	Description	Remarks
KEY_PWR_N	123	DI	Active low, can be used as on/off, restart, sleep/wakeup control.	-

3.2.1.1 Startup

After the VBAT is powered on, the trigger module starts up through pulling down the KEY_PWR_N pin for 2s to 8s. The design of key startup circuit and OC drive startup reference circuit is shown in the following figure:

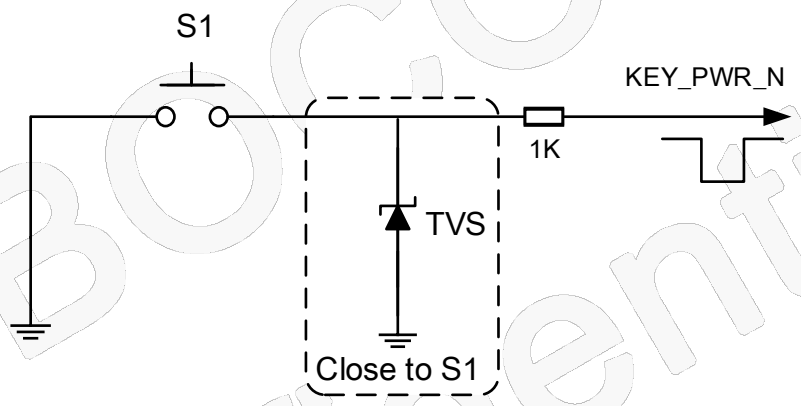


Figure 3-4 Key startup circuit

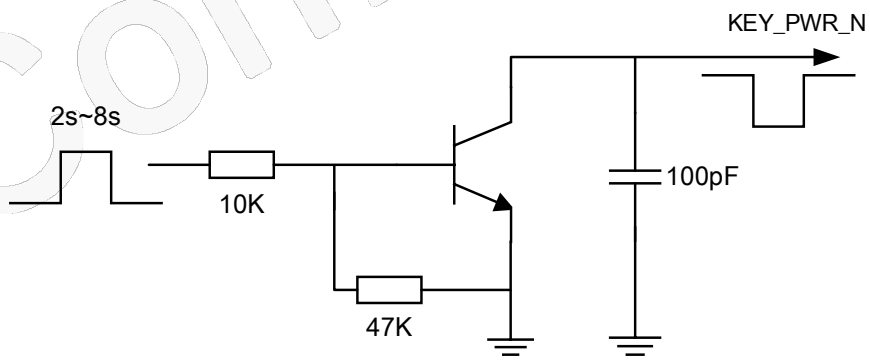


Figure 3-5 OC drive startup circuit

The startup timing sequence is shown in the following figure:

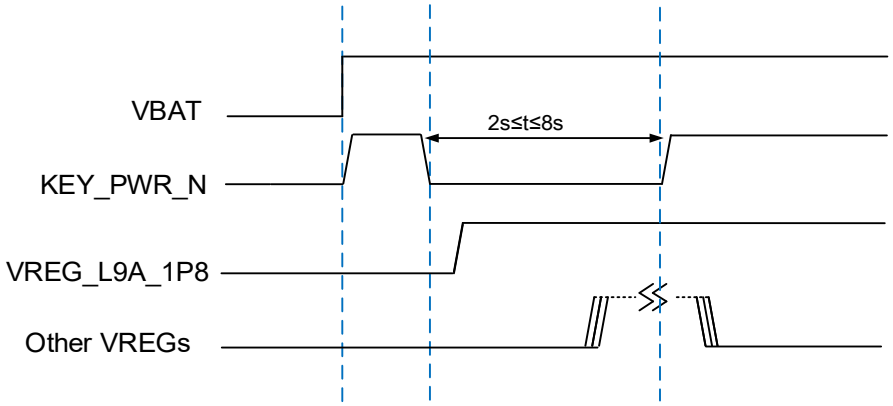


Figure 3-6 Startup timing sequence

3.2.1.2 Startup

Normal shutdown: When the machine is turned on, pull down KEY_PWR_N pin for more than 0.5s, and then a checkbox will pop up in the display interface (choose shutdown or restart).

Forced shutdown: Pull down KEY_PWR_N for 9s-15s, and then the system will be forced to shut down.

The forced shutdown timing sequence is shown in the following figure:

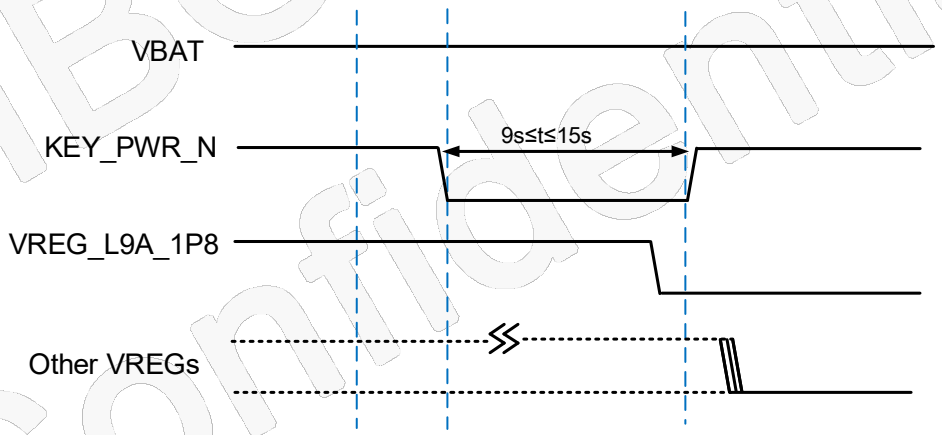


Figure 3-7 Shutdown timing sequence

Note:

In case of system abnormality or crash, the modules can be forced to shut down. Generally, use the normal shutdown mode; otherwise, data loss and other abnormalities may occur.

3.2.1.3 Sleep/Wakeup

Modules are in the standby mode, pull down KEY_PWR_N pin for 0.1s, and then the modules will enter the sleeping status. The system supports automatic sleeping, and the time from the standby status to the

sleeping status can be configured by software.

When the modules are in the sleeping status, pull down KEY_PWR_N pins for 0.1s, and then the modules can be waked up.

3.2.2 Volume Control

KEY_VOL_UP_N/KEY_VOL_DOWN_N pin is the volume increase/decrease key; for the circuit design of volume key, refer to the startup circuit design.

Note:

The parallel capacitance of volume key should not exceed 100 pF.

3.3 SPMI Interface

None

3.4 USB Interface

SC138 series modules support 1-channel USB 3.0 interfaces, being downward compatible with USB 2.0 interfaces; USB 2.0 interfaces support HS (480 Mbps) mode, being downward compatible with USB 1.1 FS (12 Mbps), USB 3.0 ports support SS (5G bps) mode, USB interfaces support OTG functions and HUB expansion interfaces. USB 2.0 interfaces support software downloading, but USB 3.0 interfaces do not support software downloading. The following table defines pins of USB interfaces:

Table 3-6 Definition of pins of USB 2.0 interfaces

Pin name	Pin No.	I/O	Description	Remarks
USB_IN_DET	168	PI	VBUS input Detection	-
USB_DP	12	I/O	USB differential signal +	-
USB_ DM	11	I/O	USB differential signal -	-
USB_ID	16	DI	USB ID pin	-

Table 3-7 Definition of pins of USB 3.0 interfaces

Pin Name	Pin No.	I/O	Description	Remarks
USB_SS_RX1_P	269	DI	USB 3.1 differential data reception+	-
USB_SS_RX1_M	254	DI	USB 3.1 differential data reception-	-
USB_SS_TX1_P	270	DO	USB 3.1 differential data sending+	-
USB_SS_TX1_M	255	DO	USB 3.1 differential data sending-	-
USB_SS_RX0_P	173	DI	USB 3.1 differential data reception+	-
USB_SS_RX0_M	175	DI	USB 3.1 differential data reception-	-
USB_SS_TX0_P	172	DO	USB 3.1 differential data sending+	-
USB_SS_TX0_M	174	DO	USB 3.1 differential data sending-	-
DP_AUX_N	263	I/O	DisplayPort auxiliary transmission channel-	-
DP_AUX_P	274	I/O	DisplayPort auxiliary transmission channel+	-
USB_PHY_PS	276	DI	USB front and back plug logo	-

The reference design of USB 2.0 interface circuit is shown in the following figure:

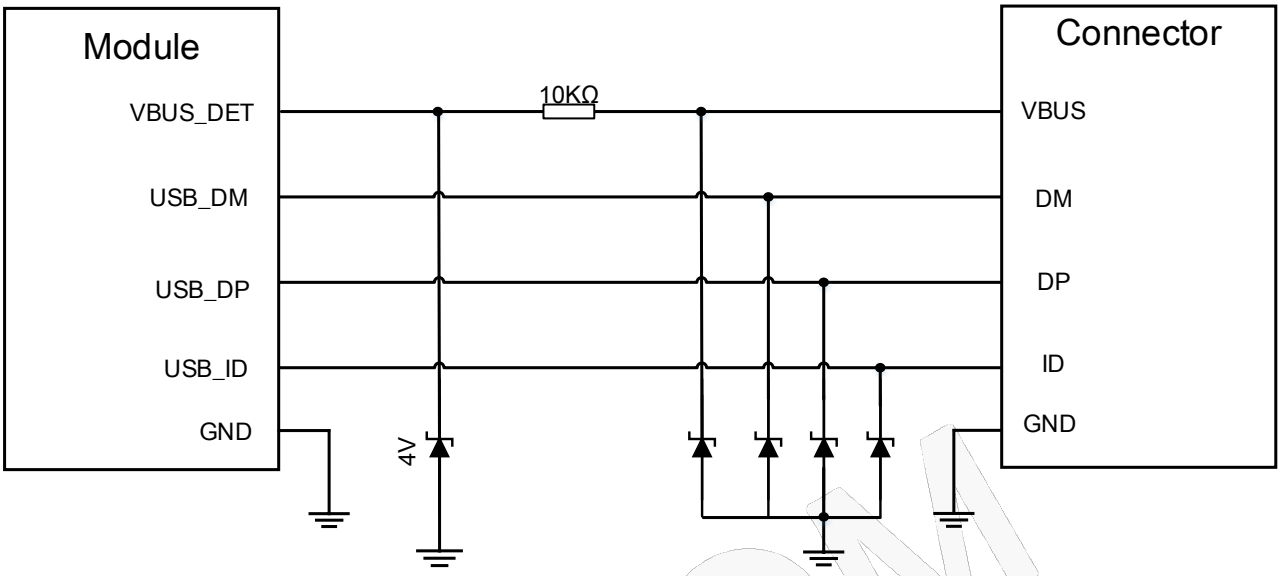


Figure 3-8 USB 2.0 interface reference circuit design

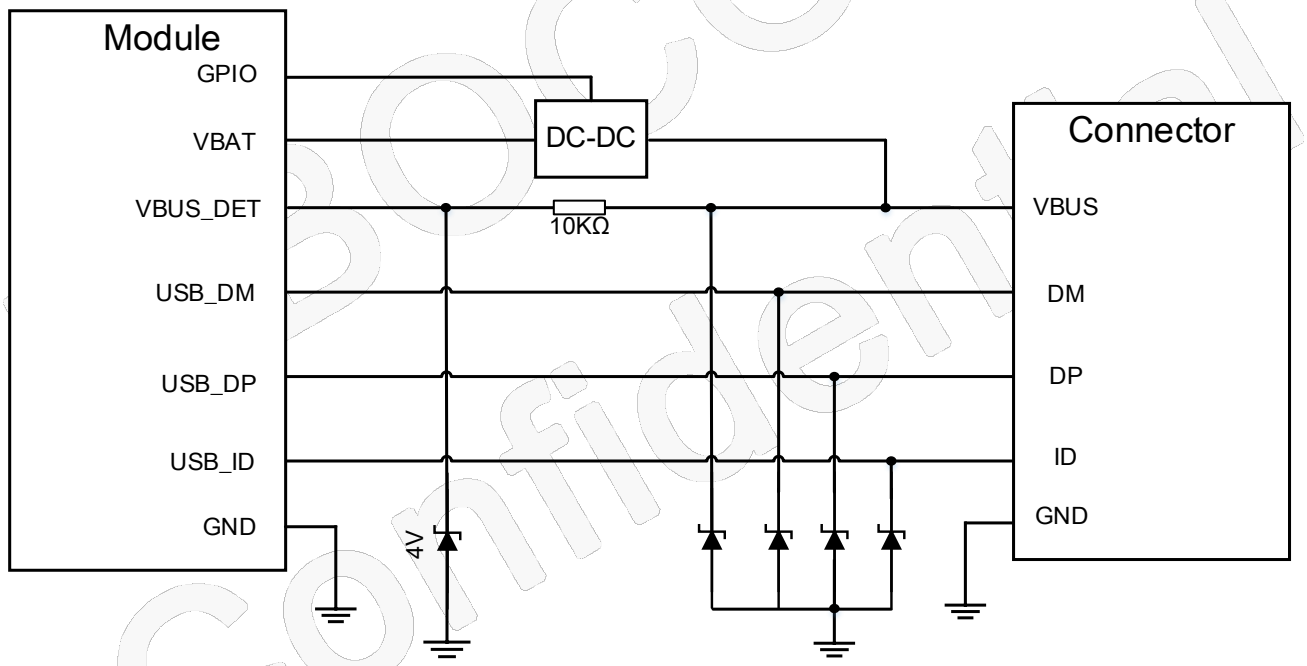


Figure 3-9 USB 2.0 interface reference circuit design (with OTG functions)

The reference circuit design of USB 3.0 (Type-C) interfaces is shown in the following figure:

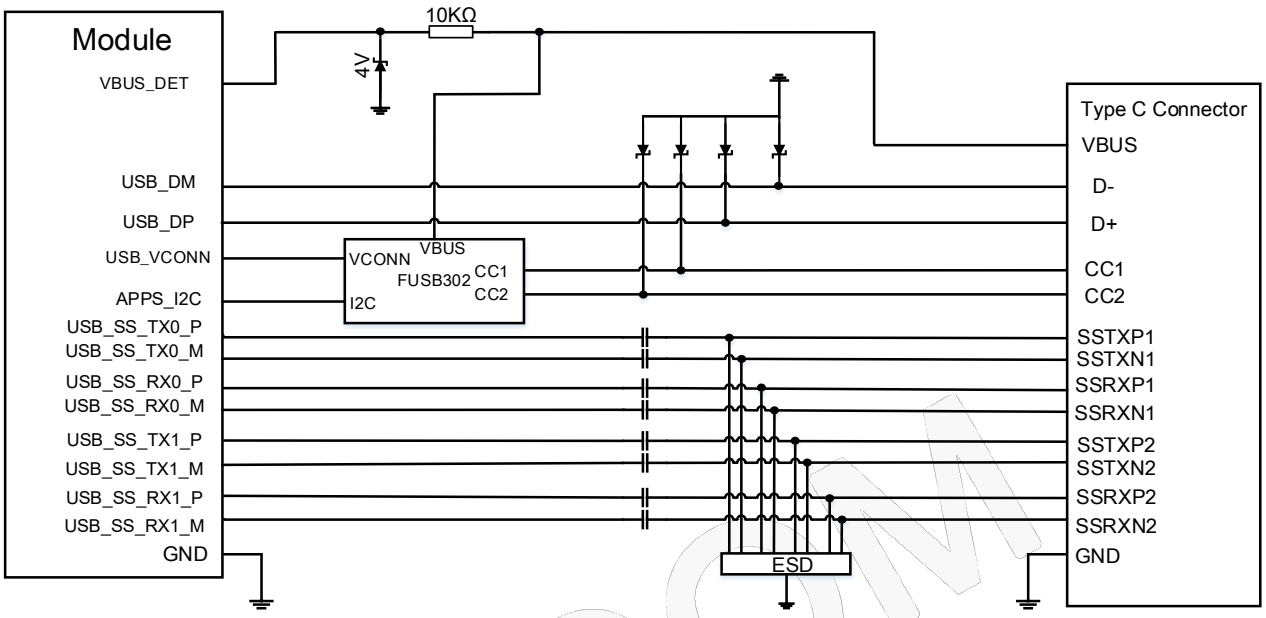


Figure 3-10 USB 3.0 interface reference circuit design

Note:

1) The ESD protection device of USB_DP/DM requires the junction capacitance to be less than 2 pF.
2) USB_DP and USB_DM are high-speed differential signal lines with a maximum transmission rate of 480 Mbps. PCB Layout must observe the following requirements:
   - USB_DP and USB_DM signal lines are required to be of equal length, and the length difference of the differential lines is within 2 mm and parallel. The right-angle routing is avoided and the differential 90 Ω impedance control is made properly.
   - USB 2.0 interface differential signal lines are laid in the signal layer nearest to the ground, and grounding lines are made properly.
3) For the reference circuit design DC-DC supporting OTG functions, select the specification output 5 V.
4) The Module is NO-PMI version default, so VBUS needs to be connected to VBUS_ Det pin, and with a 1KΩ Series Resistance.

USB 3.1 interface design considerations:

1) USB 3.1 interface is a high-speed signal line, which needs to be shielded properly (differential lines are surrounded by grounding lines in a three-dimensional manner), and follow the principle of high-

speed differential routing.

2) The differential impedance control is made properly, 90 Ω + - 10%, and the length difference of differential line is controlled within 0.7 mm.

3) The stray capacitance of ESD device must be less than 0.5 pF.

3.5 UART

SC138 module has three UART interfaces, which are all in voltage domain of 1.8 V. The pin definition is as follows:

Table 3-8 Definition of pins of UART interfaces

Pin Name	Pin No.	I/O	Description	Remarks
DBG_UART_TX	90	DO	UART data transmission	Debug interface
DBG_UART_RX	89	DI	UART data receiving	
UART_TX	45	DO	UART data transmission	-
UART_RX	46	DI	UART data receiving	-
UART_CTS/TS1_I2C_SDA	47	DI	UART clear-to-send	Can be configured to I3C
UART_RFR/IS1_I2C_CLK	48	DO	UART request-to-send	Can be configured to I3C
UART_TX/GPIO_8	209	DO	UART data transmission	-
UART_RX/GPIO_9	207	DI	UART data receiving	-

The voltage domain of each serial port is 1.8 V; when communicating with other voltage domain serial ports, it is necessary to add level conversion chips. The reference circuit design is shown in the following figure:

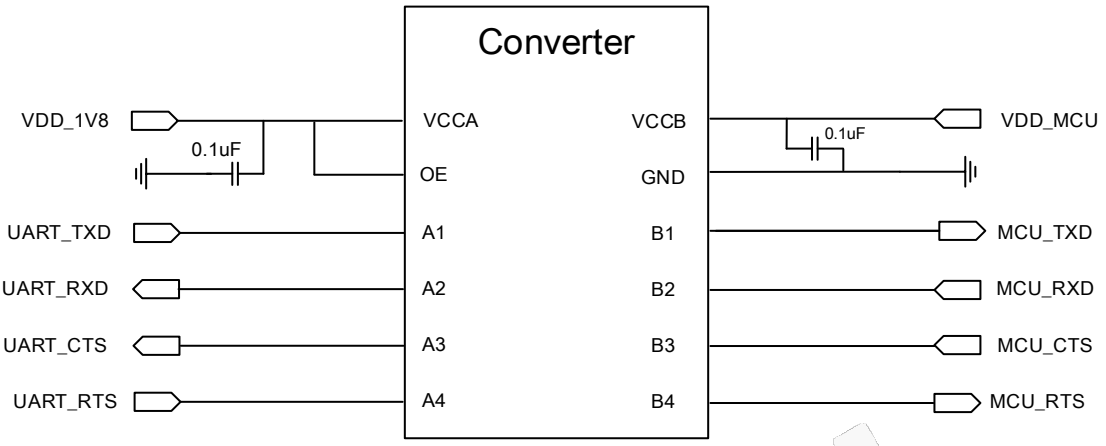


Figure 3-11 Reference circuit of level conversion

3.6 SPI

SC138 series modules provide a set of SPI interfaces and only support the main device mode. The pin definition is shown in the following figure:

Table 3-9 Definition of pins of SPI interfaces

Pin Name	Pin No.	I/O	Description	Remarks
SPI_CLK	113	DO	SPI clock	-
SPI_CS	114	DO	SPI device selection	-
SPI_MISO	115	DI	SPI MISO	-
SPI_MOSI	116	DO	SPI MOSI	-

3.7 (U) SIM

SC138 series modules support 2-channel (U)SIMs, dual-SIM dual standby and single-pass functions, as well as hot plug (off by default).

Table 3-10 (U)SIM pin definition

Pin Name	Pin No.	I/O	Description	Remarks
UIM1_DATA	25	I/O	(U)SIM 1 data	-
UIM1_CLK	24	DO	(U)SIM 1 clock	-

Pin Name	Pin No.	I/O	Description	Remarks
UIM1_RESET	23	DO	(U)SIM 1 reset	-
UIM1_DETECT	22	DI	(U)SIM 1 plug detection	Off by default
UIM2_DATA	20	I/O	(U)SIM 2 data	-
UIM2_CLK	19	DO	(U)SIM 2 clock	-
UIM2_RESET	18	DO	(U)SIM 2 reset	-
UIM2_DETECT	17	DI	(U)SIM 2 plug detection	Off by default
VREG_L19A_1P8	26	PO	(U)SIM 1 power supply	-
VREG_L20A_1P8	21	PO	(U)SIM 2 power supply	-

The reference circuit of (U)SIM interface is shown in the following figure:

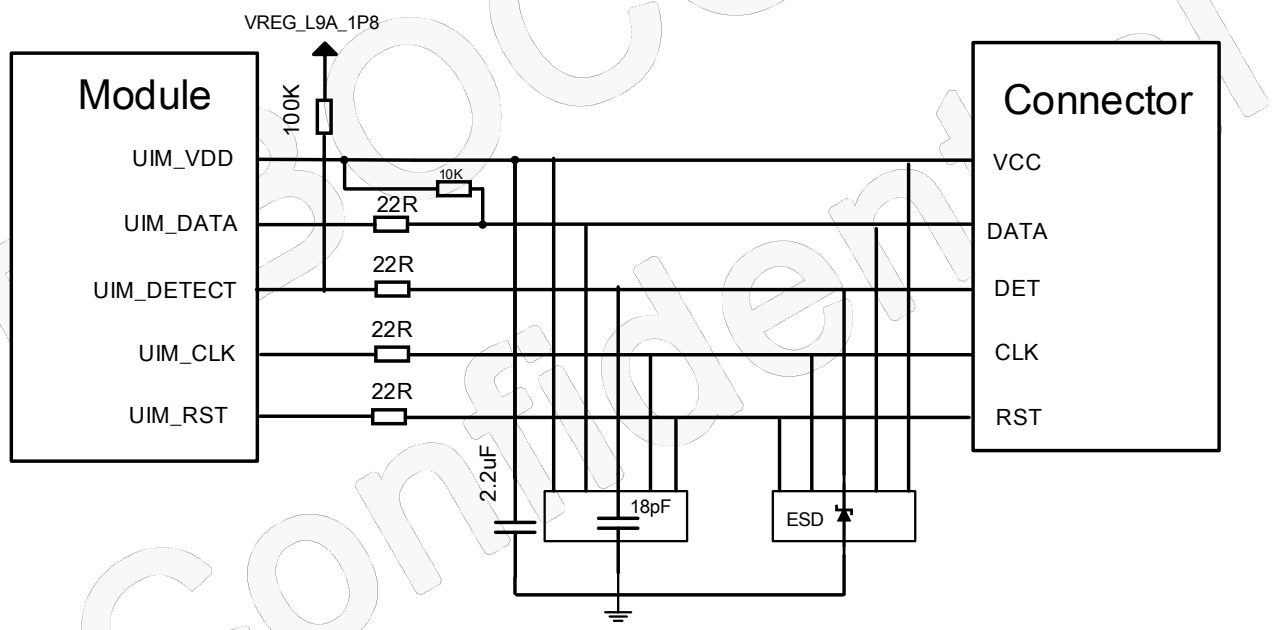


Figure 3-12 (U)SIM reference circuit

(U)SIM design considerations:

1) The length of route from the (U)SIM card slot to the module should be less than 100 mm.
2) The layout and routing of (U)SIM must be away from EMI interference sources, such as RF antenna and digital switching power supply.
3) The filter capacitor and ESD device of (U)SIM signal should be placed close to the card slot.

3.8 SDIO Interface

SC138 supports 1-channel SDIO interfaces, and the pin definition is shown in the following table:

Table 3-11 Definition of pins of SDIO interfaces

Pin No.	Pin Name	I/O	Description	Remarks
SDC2_DATA3	34	I/O	SD data interface	-
SDC2_DATA2	33	I/O	SD data interface	-
SDC2_DATA1	32	I/O	SD data interface	-
SDC2_DATA0	31	I/O	SD data interface	-
SDC2_CLK	29	DO	SD clock	-
SDC2_CMD	30	I/O	SD command interface	-
SD_CARD_DET_N	35	DI	SD detection	-
VREG_L22A_2P96	28	PO	SD power supply	-

The reference circuit design of SDIO interfaces is shown in the following figure:

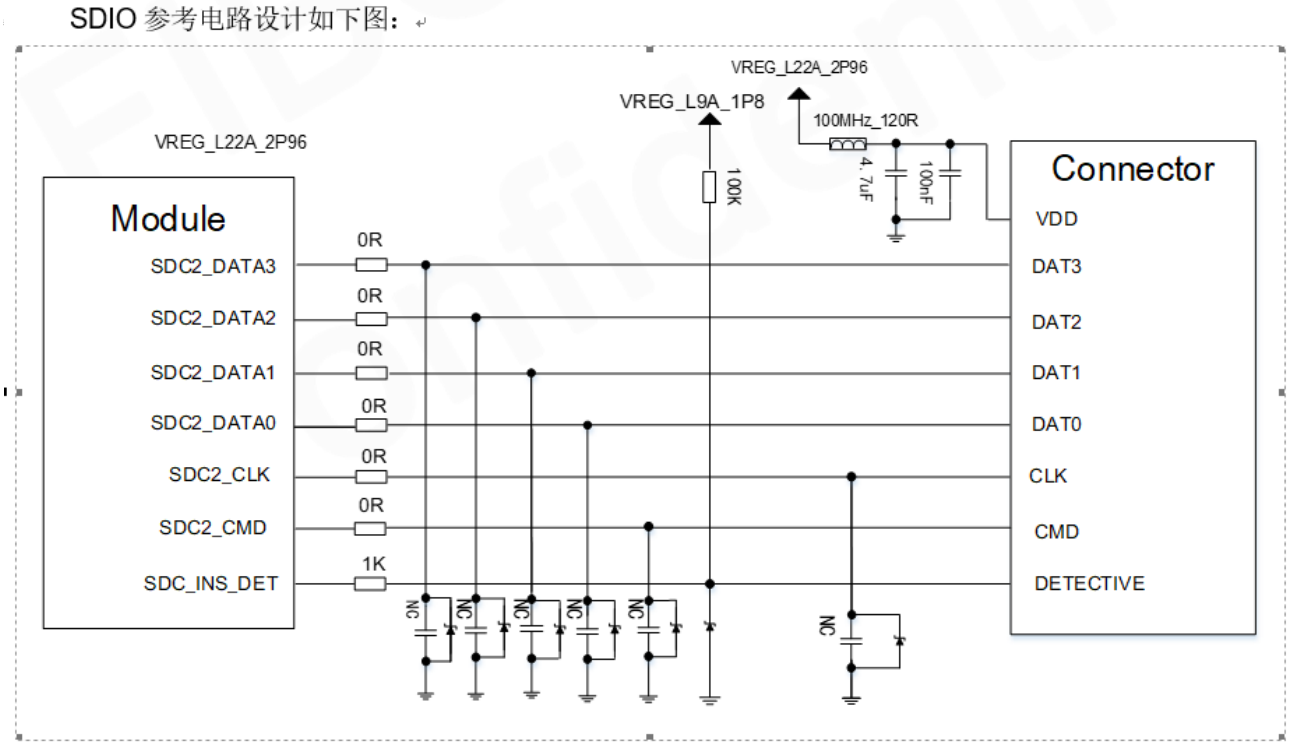


Figure 3-13 Reference circuits of SDIO interfaces

SDIO interface design considerations:

1) VREG_L22A_2P96 is an external drive power supply for SD card, which can provide about 600 mA current with the line width of 1 mm.
2) The SD_CARD_DET_N pull-up resistor is connected to VREG_L9A_1P8 power supply.
3) SDIO is a high-speed digital signal line and needs to be shielded.
4) SDIO data lines are processed to be of equal length.

3.9 GPIO

SC138 series modules have abundant GPIO resources, the interface level is 1.8 V, and the pin definition is shown in the following table:

Table 3-12 GPIO list

Pin Name	Pin No.	Reset State	Interrupt Function
GPIO_129	105	B-PD:nppukp	NO
GPIO_70	110	B-PD:nppukp	NO
GPIO_86	117	B-PD:nppukp	NO
GPIO_84	112	B-PD:nppukp	NO
GPIO_33	97	B-PD:nppukp	YES
GPIO_83	111	B-PD:nppukp	NO
GPIO_124	100	B-PD:nppukp	YES
GPIO_58	103	B-PD:nppukp	YES
GPIO_57	102	B-PD:nppukp	YES
GPIO_130	220	B-PD:nppukp	YES
GPIO_132	221	B-PD:nppukp	YES
GPIO_93	39	B-PD:nppukp	NO
GPIO_123	99	B-PD:nppukp	YES
GPIO_31	86	B-PD:nppukp	NO
GPIO_41	98	B-PD:nppukp	NO
GPIO_116	217	B-PD:nppukp	NO
GPIO_115	216	B-PD:nppukp	NO

Pin Name	Pin No.	Reset State	Interrupt Function
GPIO_113	212	B-PD:nppukp	NO
GPIO_117	218	B-PD:nppukp	YES
GPIO_119	219	B-PD:nppukp	NO
PM6125_GPIO_1	249	B-PD:nppukp	YES
PM6125_GPIO_2	245	B-PD:nppukp	YES
PM6125_GPIO_4	243	B-PD:nppukp	YES

Note:

B: Bidirectional digits with CMOS input.

H: High voltage resistance.

NP: pdpukp = no pull by default, with programmable options after the colon (:).

PD: nppukp = pull-down by default, with programmable options after the colon (:).

PU: nppdkp = pull-up by default, with programmable options after the colon (:).

KP: nppdpu = floating by default, with programmable options after the colon (:).

3.10 I²C

SC138 series modules have 5 sets of I2C interfaces, which can be used for TP, camera, sensor and others respectively. The 5 sets of I2C interfaces are all open-drain outputs, and a pull-up resistor must be added to the 1.8V power domain when in use. The I2C interface pin definition is shown in the following table:

Table 3-13 I²C interface pin definition

Pin Name	Pin No.	I/O	Description	Remarks
SNS_I2C_SCL	87	OD	Sensor I2C clock	-
SNS_I2C_SDA	88	OD	Sensor I2C data	-
TS_I2C_SCL	41	OD	Touch screen I2C clock	-
TS_I2C_SDA	150,158	OD	Touch screen I2C data	-

Pin Name	Pin No.	I/O	Description	Remarks
CAM0_I2C_SCL	84	OD	Camera I2C clock	They are special for the camera and cannot be used on other devices.
CAM0_I2C_SDA	85	OD	Camera I2C data	
CAM2_SCL	206	OD	Camera I2C clock	
CAM2_SDA	208	OD	Camera I2C data	
APPS_I2C_SCL	268	OD	I2C clock	Need be Pulled-up too, when unused
APPS_I2C_SDA	267	OD	I2C data line	

Note:

When mounting multiple peripherals on the I2C channel, please ensure the uniqueness of each peripheral address. When mounting peripherals with high real-time performance requirements, do not share I2C with other peripherals.

APPS_I2C must be configured Pull-up outside the module, even if the I2C unused.

3.11 ADC

The SC138 series modules have an ADC interface with a precision of 15 bits. The pin definition is shown in the following table:

Table 3-14 ADC pin definition

Pin Name	Pin No.	I/O	Description	Remarks
ADC	128	AI	ADC detection	Configurable voltage is 0.3 V-VBAT

3.12 I2S Interface

The SC138 series modules have special audio I2S interfaces. Details are as follows:

Table 3-15 I2S interface definition

I2S Interface				
GPIO_125/I2S1_SCK	247	DO	I2S serial clock	-
GPIO_126/I2S1_WS	238	DO	I2S frame clock	-
GPIO_127/I2S1_DATA0	239	DO	I2S data 0	-
GPIO_128/I2S1_DATA1	240	DO	I2S data 1	-
GPIO_118/MCLK2	251	DO	I2S system clock	Boot Config, Flash Memory type configure

3.13 Battery Power Supply Interface

None

3.14 Motor Drive Interface

None

3.15 LCM

SC138 series module screen interfaces are based on MIPI_DSI standard, supporting transmission of 4 sets of high-speed differential data; each set has a maximum speed of 2.5 Gbps, and supports the maximum display of 1080*2520.

Table 3-16 LCM pin definition

Pin Name	Pin No.	I/O	Description	Remarks
MIPI_DSI0_CLK_P	53	AO	Main TP MIPI clock+	-
MIPI_DSI0_CLK_N	52	AO	Main TP MIPI clock-	-
MIPI_DSI0_LANE0_P	55	AI/AO	Main TP MIPI Lane0+	-
MIPI_DSI0_LANE0_N	54	AI/AO	Main TP MIPI Lane0-	-

Pin Name	Pin No.	I/O	Description	Remarks
MIPI_DSI0_LANE1_P	57	AI/AO	Main TP MIPI Lane1+	-
MIPI_DSI0_LANE1_N	56	AI/AO	Main TP MIPI Lane1-	-
MIPI_DSI0_LANE2_P	59	AI/AO	Main TP MIPI Lane2+	-
MIPI_DSI0_LANE2_N	58	AI/AO	Main TP MIPI Lane2-	-
MIPI_DSI0_LANE3_P	61	AI/AO	Main TP MIPI Lane3+	-
MIPI_DSI0_LANE3_N	60	AI/AO	Main TP MIPI Lane3-	-
LCD0_RST_N	49	DO	Main TP reset signal	-
PWM	44	DO	LCD backlight PWM control	-
LCD1_BL_EN	211	DO	LCD backlight enabling control	-
LCD_TE	50	DI	LCD refreshing synchronization signal	NC when it is not in use.

The reference circuit of LCM interface is shown in the following figure:

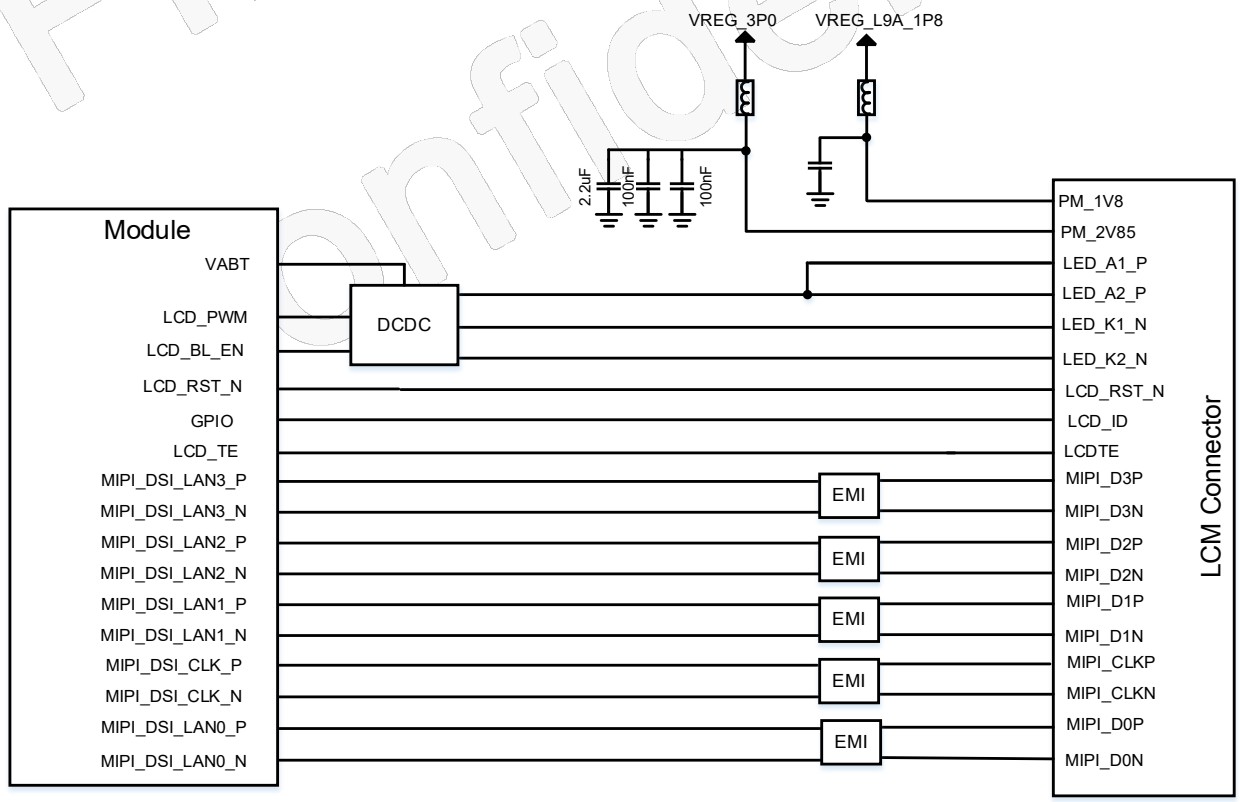


Figure 3-14 LCM reference circuit

LCM design considerations:

1) MIPI is a high-speed signal line. It is recommended to connect a common mode choke in series near the LCD connector to improve the electromagnetic radiation interference of the circuit.
2) MIPI route is recommended to be placed on the inner layer, and be surrounded by grounding lines in a three-dimensional manner.
3) The MIPI signal line needs to be controlled by a differential impedance of 100 Ω, with an error of ±10%.
4) The total length of the route does not exceed 300 mm.
5) The length difference of the differential lines in the set is controlled within 0.7 mm.
6) The length difference between sets is controlled within 1.4 mm.
7) It is recommended that the spacing between differential lines in the group should be 1.5 times the line width, and the spacing between differential lines and other routes should be 3 times the line width.
8) The total stray capacitance of devices on MIPI differential signal line should not exceed 1pF.

3.16 TP

SC138 series modules provide a set of I2C interfaces that can be used to connect to the touch screen. They also provide the power, interrupt and reset pins required by the TP. The pin definition is shown in the following table:

Table 3-17 TP pin definition

Pin Name	Pin No.	I/O	Description	Remarks
TS0_INT_N	42	DI	TP interrupt signal	-
TS0_RST_N	43	DO	TP reset signal	-
VREG_L9A_1P8	129	PO	TP IO power supply	-
VREG_3P0	266	PO	TP VDD power supply	-
TS_I2C_SCL	41	OD	Main TP I2C clock	-
TS_I2C_SDA	150, 158	OD	Main TP I2C data	-

The TP reference circuit is shown in the following figure:

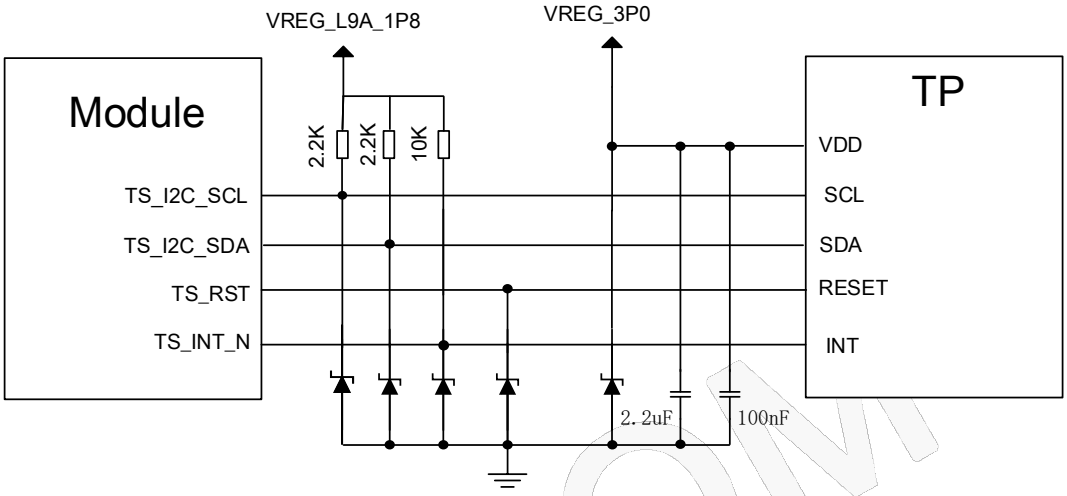


Figure 3-15 TP reference circuit

3.17 Camera

The video input interface of the SC138 series module is based on the MIPI_CSI standard, and can support 3 (4+4+4-Lane) or 4 (4+4+2+1-Lane) cameras. It is equipped with 3 cameras by default. Support 21 MP pixel camera at maximum. The camera interface pin definition is shown in the following table:

Table 3-18 Camera interface pin definition

Pin Name	Pin No.	I/O	4-Lane+4-Lane+4-Lane (Default Configuration) (Configurable)	
MIPI_CSI2_CLK_P	64	AO	Camera 2 MIPI clock+	-
MIPI_CSI2_CLK_N	63	AO	Camera 2 MIPI clock-	-
MIPI_CSI2_LANE0_P	66	AI/AO	Camera 2 MIPI Lane 0+	-
MIPI_CSI2_LANE0_N	65	AI/AO	Camera 2 MIPI Lane 0-	-
MIPI_CSI2_LANE1_P	68	AI/AO	Camera 2 MIPI Lane 1+	-
MIPI_CSI2_LANE1_N	67	AI/AO	Camera 2 MIPI Lane 1-	-
MIPI_CSI2_LANE2_P	181	AI/AO	Camera 2 MIPI Lane 2+	-
MIPI_CSI2_LANE2_N	183	AI/AO	Camera 2 MIPI Lane 2-	-

Pin Name	Pin No.	I/O	4-Lane+4-Lane+4-Lane (Default Configuration) (Configurable)	
MIPI_CSI2_LANE3_P	180	AI/AO	Camera 2 MIPI Lane 3+	-
MIPI_CSI2_LANE3_N	179	AI/AO	Camera 2 MIPI Lane 3-	-
CAM0_MCLK	75	DO	Camera 0 MCLK signal	-
CAM0_RST_N	80	DO	Camera 0 reset signal	-
CAM0_PWD_N	81	DO	Camera 0 PWD signal	-
MIPI_CSI0_CLK_P	71	AO	Camera 3 MIPI clock+	-
MIPI_CSI0_CLK_N	70	AO	Camera 3 MIPI clock-	-
MIPI_CSI0_LANE0_P	73	AI/AO	Camera 3 MIPI Lane0+	-
MIPI_CSI0_LANE0_N	72	AI/AO	Camera 3 MIPI Lane0-	-
MIPI_CSI0_LANE1_P	184	AI/AO	Camera 3 MIPI Lane1+	-
MIPI_CSI0_LANE1_N	185	AI/AO	Camera 3 MIPI Lane1-	-
MIPI_CSI0_LANE2_P	186	AI/AO	Camera 4 MIPI Lane2+	-
MIPI_CSI0_LANE2_N	187	AI/AO	Camera 4 MIPI Lane2-	-
MIPI_CSI0_LANE3_P	188	AI/AO	Camera 4 MIPI Lane3+	-
MIPI_CSI0_LANE3_N	189	AI/AO	Camera 4 MIPI Lane3-	-
CAM1_MCLK	76	DO	Camera 1 MCLK signal	-
CAM1_RST_N	82	DO	Camera 1 reset signal	-
CAM1_PWD_N	83	DO	Camera 1 PWD signal	-
MIPI_CSI1_CLK_P	257	AO	Camera 1 MIPI clock+	
MIPI_CSI1_CLK_N	256	AO	Camera 1 MIPI clock-	
MIPI_CSI1_LANE0_P	271	AI/AO	Camera 1 MIPI Lane0+	
MIPI_CSI1_LANE0_N	258	AI/AO	Camera 1 MIPI Lane0-	
MIPI_CSI1_LANE1_P	272	AI/AO	Camera 1 MIPI Lane1+	
MIPI_CSI1_LANE1_N	259	AI/AO	Camera 1 MIPI Lane1-	
MIPI_CSI1_LANE2_P	273	AI/AO	Camera 1 MIPI Lane2+	
MIPI_CSI1_LANE2_N	260	AI/AO	Camera 1 MIPI Lane2-	
MIPI_CSI1_LANE3_P	262	AI/AO	Camera 1 MIPI Lane3+	

Pin Name	Pin No.	I/O	4-Lane+4-Lane+4-Lane (Default Configuration) (Configurable)	
MIPI_CSI1_LANE3_N	261	AI/AO	Camera 1 MIPI Lane3-	
CAM2_MCLK	213	DO	Camera 2 MCLK signal	-
CAM2_RST_N	214	DO	Camera 2 reset signal	-
CAM2_PWD_N	215	DO	Camera 2 PWD signal	-
IOVDD_1.8V_EN	210	DO	IOVDD power enabling signal	-
CAM1_MCLK/GPIO_44	101	DO	Camera 3 MCLK signal	

3.17.1 Camera 1

The reference circuit design of camera 1 is shown in the following figure:

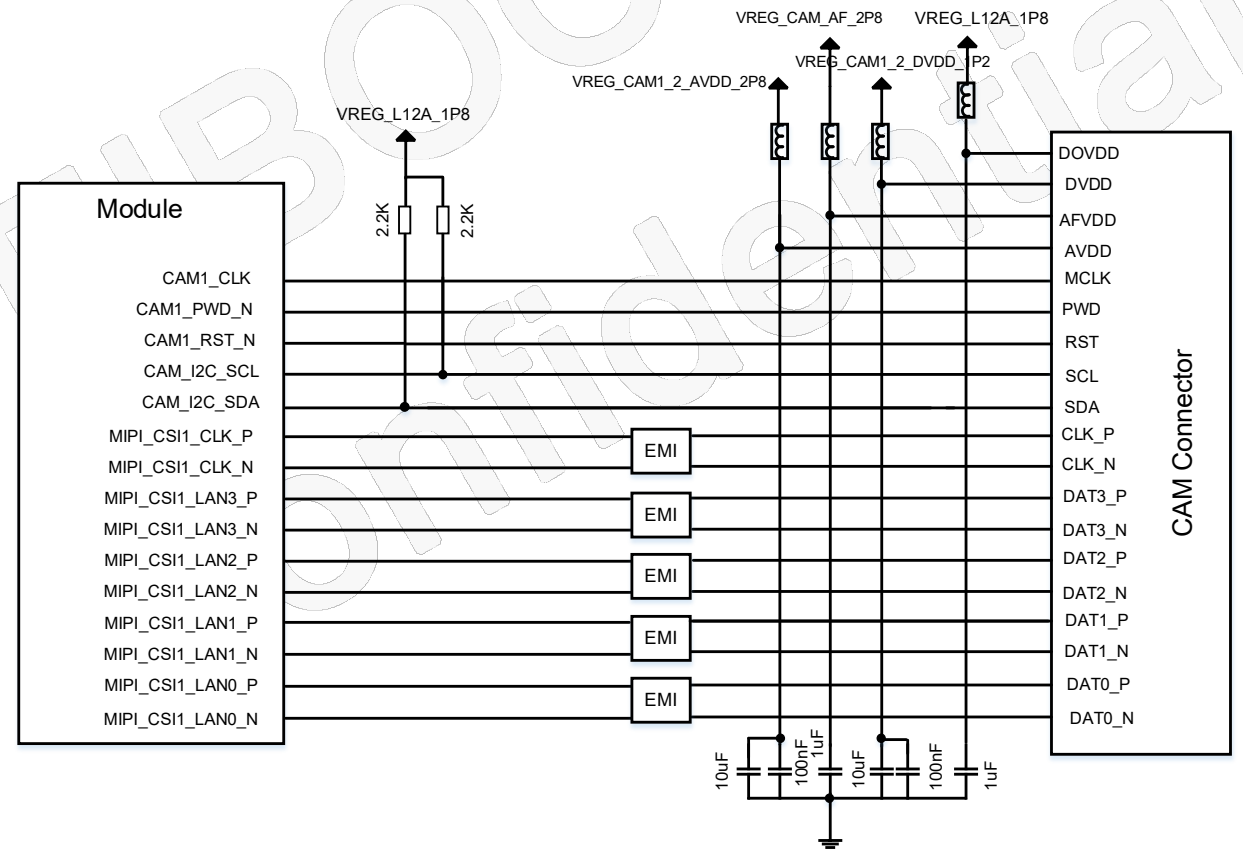


Figure 3-16 Reference circuit for camera 1

3.17.2 Camera 2

The reference circuit design of 4-Lane front camera is shown in the following figure:

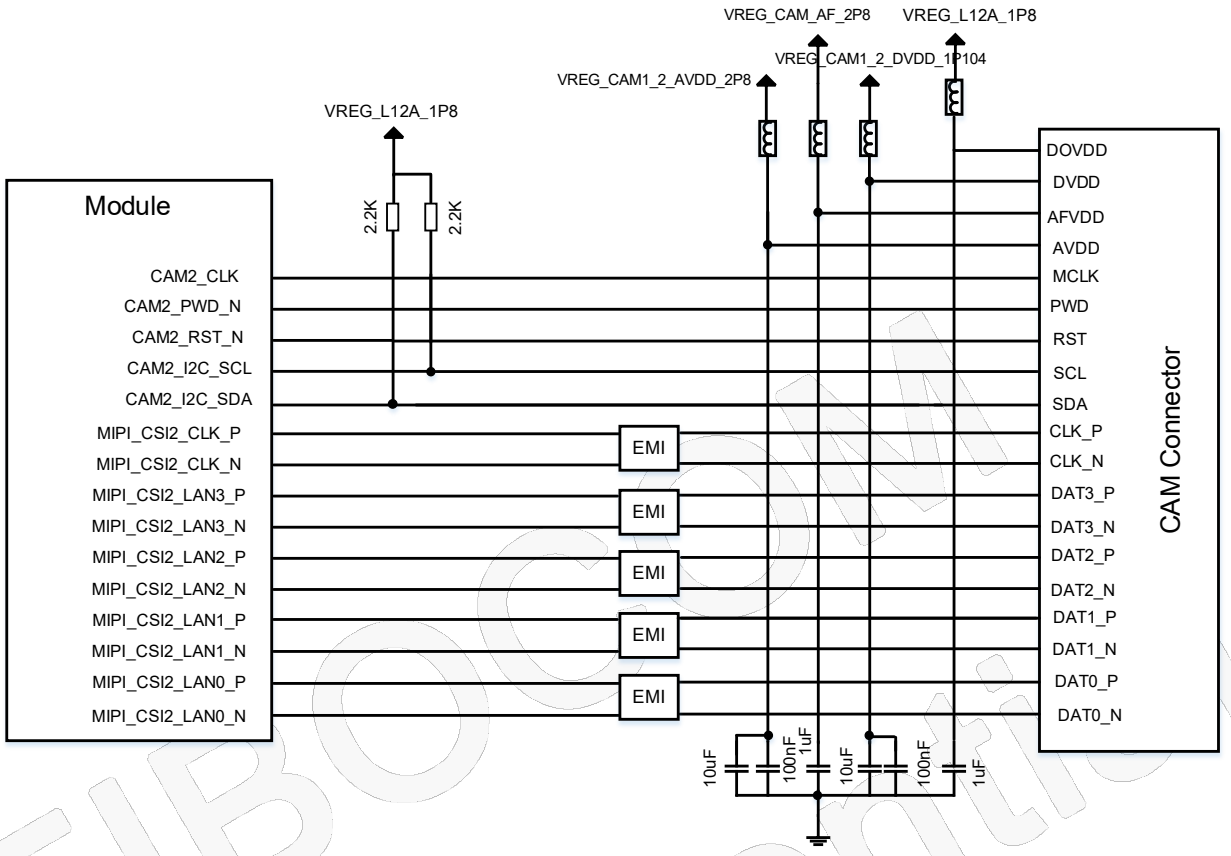


Figure 3-17 Reference circuit for camera 2

3.17.3 Camera 3

The reference circuit of camera 3 is shown in the following figure:

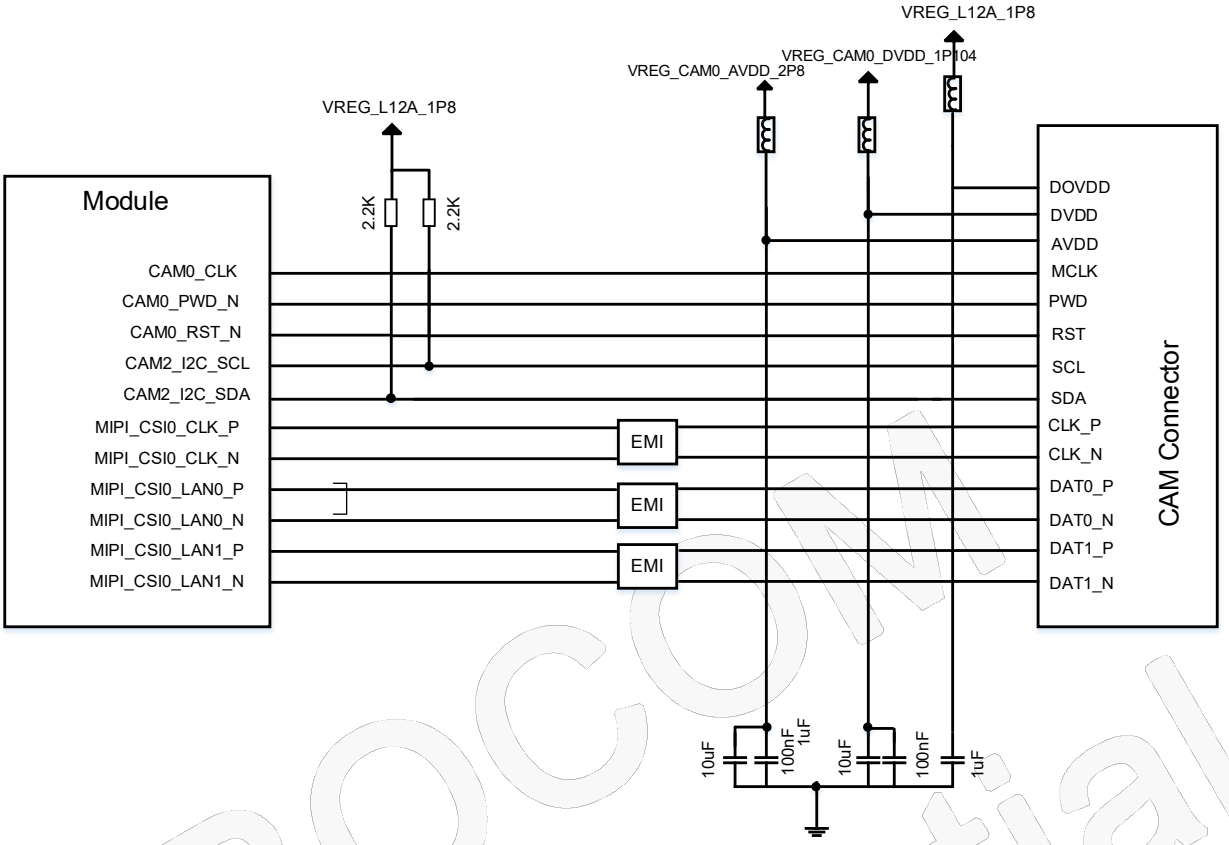


Figure 3-18 Reference circuit for camera 3

3.17.4 Camera 4

The reference circuit of camera 4 is shown in the following figure:

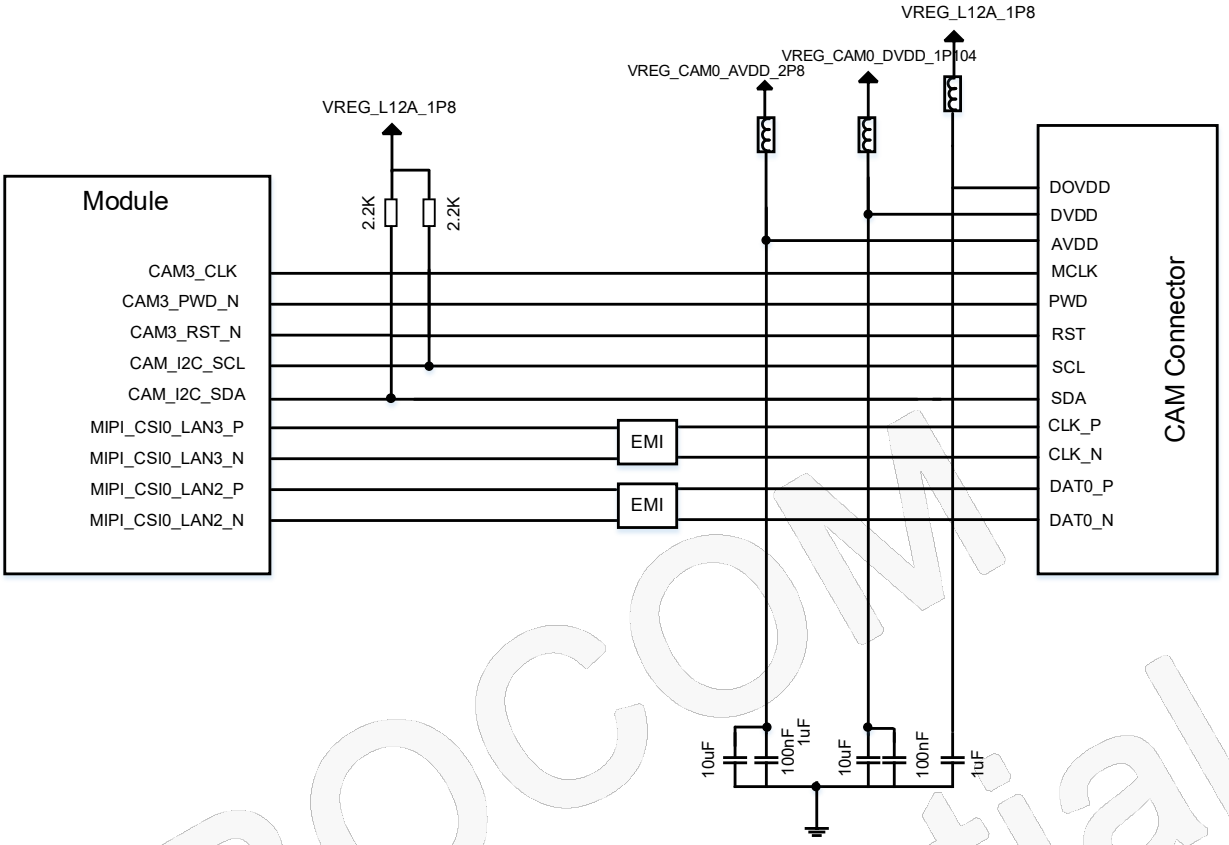


Figure 3-19 Reference circuit for camera 4

3.17.5 Design Considerations

MIPI_CSI is a high-speed data line. PCB layout must observe the following requirements:

1) MIPI is a high-speed signal line. It is recommended to connect a common mode choke in series near the camera connector to reduce EMI.
2) MIPI route is recommended to be placed on the inner layer, and be surrounded by grounding lines in a three-dimensional manner.
3) The MIPI signal line needs to be controlled by a differential impedance of 100 Ω, with an error of ±10%.
4) The total length of the route does not exceed 300 mm.
5) The length difference of the differential lines in the set is controlled within 0.7 mm.
6) The length difference between sets is controlled within 1.4 m.
7) It is recommended that the spacing between differential lines in the group should be 1.5 times the line width, and the spacing between differential lines and other routes should be 3 times the line

width.

8) The total stray capacitance of devices on MIPI differential signal line should not exceed 1pF.

Other signal line design considerations:

1) CAM_CLK is a high-speed clock signal and needs to be surrounded by grounding lines in a three-dimensional manner.
2) If the front and rear cameras share I2C, the I2C addresses of the two cameras should be confirmed that there is no conflict.
3) The analog voltage AVDD route should be away from the interference source to avoid the power noise.
4) It is recommended to place an LDO with high power supply rejection ratio close to the camera AVDD.

3.18 Sensor

SC138 supports I2C communication with various sensors, including accelerometers, distance and ambient light sensors, geomagnetic sensors, gyroscopes, etc.

Table 3-19 Sensor interface pin definition

Pin Name	Pin No.	I/O	Description	Remarks
SNS_I2C_SCL	87	OD	I2C clock	-
SNS_I2C_SDA	88	OD	I2C data line	-
ALSP_INT_N	106	DI	Interrupt signal of ambient light sensor	-
MAG_INT_N	107	DI	Interrupt signal of geomagnetic sensor	-
ACCL_INT2_N	108	DI	G-Sensor interrupt signal 2	-
ACCL_INT1_N	109	DI	G-Sensor interrupt signal 1	-

3.19 Audio

3.19.1 Audio Interface Definition

SC138 series modules support analog audio interfaces with 3 inputs and 3 outputs, and the pin definition is shown in the following table:

Table 3-20 Audio interface definition

Pin Name	Pin No.	I/O	Description	Remarks
SPKR_DRV_P	148	AO	Loudspeaker drive output+	Load of 8 Ω and power of 800 mW
SPKR_DRV_N	147	AO	Loudspeaker drive output-	
CDC_EAR_P	134	AO	Handset output+	Load of 32 Ω and power of 123 mW
CDC_EAR_N	135	AO	Handset output-	
CDC_HPH_L	139	AO	Earphone left channel output	-
CDC_HPH_REF	138	-	Earphone reference ground	-
CDC_HPH_R	137	AO	Earphone right channel output	-
CDC_HS_DET	140	AI	Earphone plug detection	-
MIC2_IN_P	142	AI	Earphone MIC input+	-
MIC2_IN_N	141	AI	Earphone MIC input-	-
MIC1_N	144	AI	Main MIC differential input-	-
MIC1_P	145	AI	Main MIC differential input+	-
MIC3_IN_N	233	AI	Auxiliary MIC differential input-	-
MIC3_IN_P	244	AI	Auxiliary MIC differential input+	-
MIC4_IN_N	252	AI	Auxiliary MIC differential input-	Unavailable function by default, and grounding
MIC4_IN_P	248	AI	Auxiliary MIC differential	Unavailable function by

Pin Name	Pin No.	I/O	Description	Remarks
			input+	default, and grounding

Audio interface design considerations:

1) There is a MIC bias circuit in the SC138 module, so no external addition is required.
2) SPK is equipped with Class-D power amplifier, so no external power amplifier is allowed. It is recommended to connect an 8 Ω loudspeaker. The route width should meet the requirements of rated power. If an external audio power amplifier is required, select the earphone output as the input source of the external power amplifier. For double-ended input, use two channels. For single-ended input, the channel can be configured by software.
3) The earphone reference ground has already been grounded in the module. It is recommended that the external circuit does not need to be grounded, and a resistor can be reserved.
4) It is recommended to use a 32 Ω impedance device for the handset.
5) To reduce noise and improve audio quality, the suggestions are shown in the following:
   - The audio PCB route should be as far away as possible from antennas and high-frequency digital signals.
   - The LC filter circuit is reserved in the audio circuit to reduce EMI.
   - Audio route needs to be shielded.

3.19.2 Microphone Circuit Design

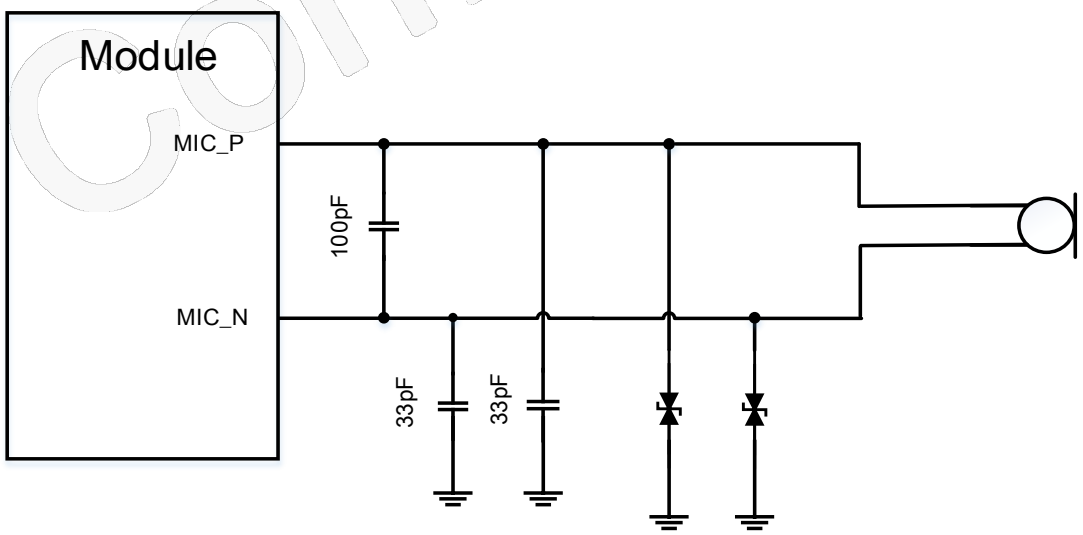


Figure 3-20 Microphone circuit design

3.19.3 Handset Circuit Design

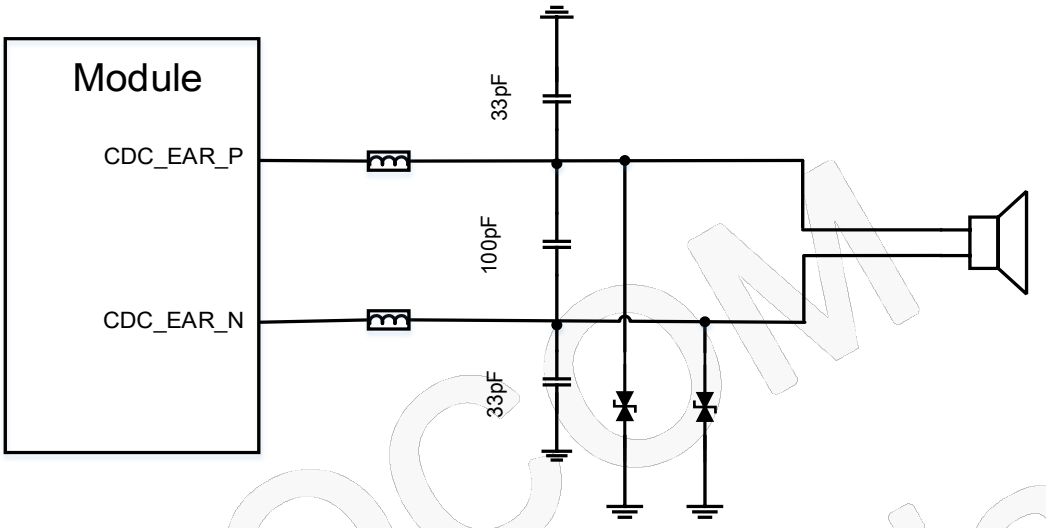


Figure 3-21 Handset circuit design

3.19.4 Earphone Interface Circuit Design

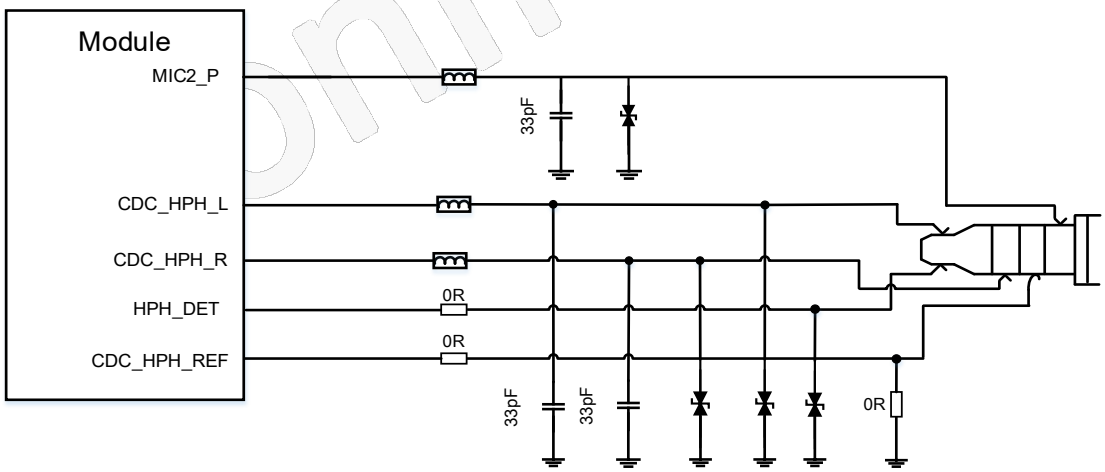


Figure 3-22 Earphone interface circuit design

Note:

For the ESD protection device of the earphone interface, use the bidirectional TVS tubes.

3.19.5 Speaker Circuit Design

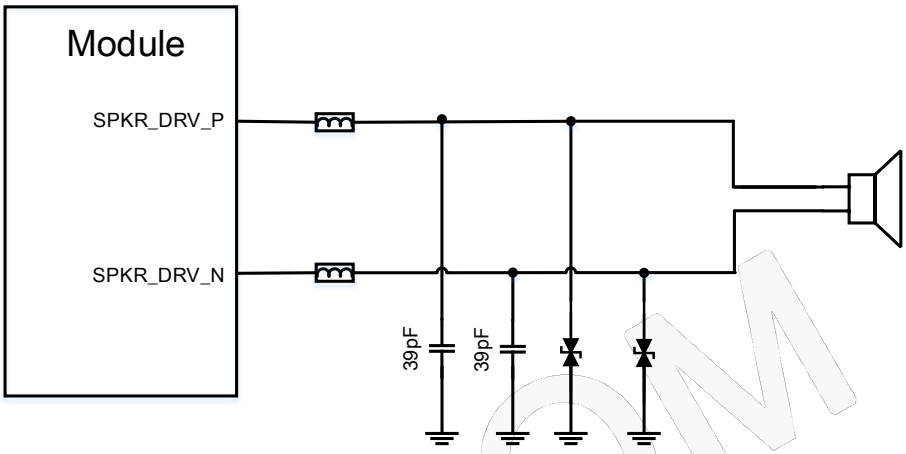


Figure 3-23 Speaker circuit design

3.20 Forced Downloading Interface Design

SC138 series modules provide FORCE_USB_BOOT pins as emergency downloading interfaces. Short-circuit the USB_FORCE_BOOT and VREG_L9_1P8 pins when starting up, and the module can enter the emergency downloading mode. It is the final processing method when the product cannot start up or run normally due to faults. Reserve this pin to facilitate the subsequent software upgrade and commissioning of the product. The reference circuit is shown in the following figure:

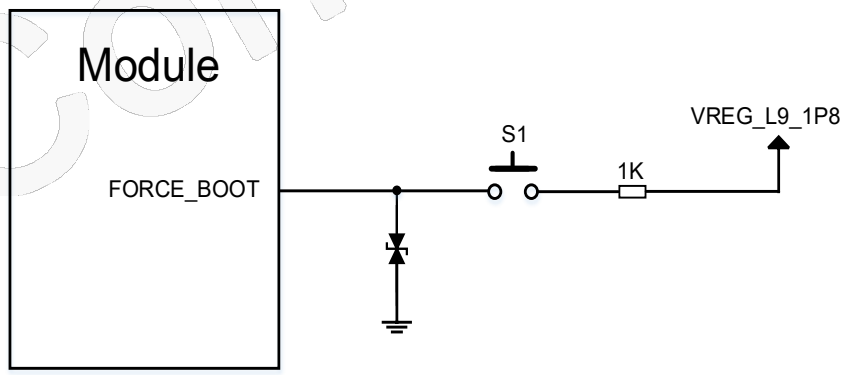


Figure 3-24 Forced downloading interface design

4 Antenna Interface

SC138 series modules support 2G/3G/4G main antenna/diversity receiving antenna, WIFI/BT antenna and GNSS antenna.

4.1 TRX/DRX Antenna

SC138 series modules provide 2 2G/3G/4G antenna interfaces, and ANT_TRX is used for receiving and sending RF signals, and ANT_DRX is used for diversity reception.

Table 4-1 TRX/DRX antenna interface definition

Pin Name	Pin No.	I/O	Description	Remarks
ANT_TRX	94	AI/AO	2G/3G/4G antenna interface	-
ANT_DRX	132	AI	Diversity receiving antenna	-

4.1.1 Band

Table 4-2 SC138-EAU band

Mode	Band	Tx (MHz)	Rx (MHz)
GSM	850	824–849	869–894
	900	880–915	925–960
	1800	1710–1785	1805–1880
	1900	1850–1910	1930–1990
WCDMA	Band 1	1920–1980	2110–2170
	Band 2	1850–1910	1930–1990
	Band 5	824–849	869–894
	Band 8	880–915	925–960
LTE FDD	Band 1	1920–1980	2110–2170
	Band 3	1710–1785	1805–1880

Mode	Band	Tx (MHz)	Rx (MHz)
	Band 5	824–849	869–894
	Band 7	2500–2570	2620–2690
	Band 8	880–915	925–960
	Band 20	832–862	791–821
	Band 28	703–748	758–803
LTE TDD	Band 38	2570–2620	2570–2620
	Band 40	2300–2400	2300–2400
	Band 41	2496–2690	2496–2690

4.1.2 Circuit Reference Design

When using SC138 series modules, it is necessary to connect the antenna pins and the RF connector or antenna feedpoint on the main board through the RF route. Microstrip line is recommended for the RF route, the insertion loss is controlled within 0.2 dB, and the impedance is controlled within 50 Ω. A π-type circuit is reserved between the module and the antenna connector (or feedpoint) for antenna commissioning. Two parallel devices are directly jumped and connected to the RF route without branch. The reference circuit is shown in the following figure:

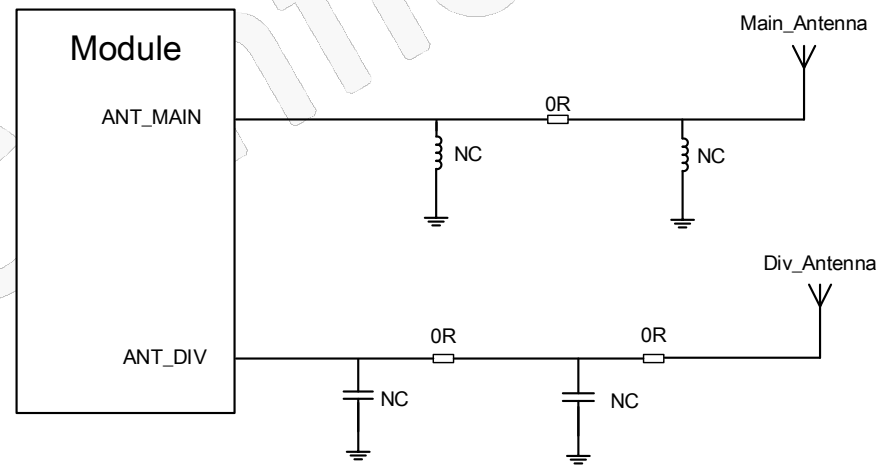


Figure 4-1 TRX/DRX antenna reference circuit

4.2 WIFI/BT Antenna

Microstrip line is recommended for the RF routing of WIFI/BT antenna, the insertion loss is controlled within 0.2 dB, and the impedance is controlled within 50 Ω.

Table 4-3 Definition of WIFI/BT antenna interface

Pin Name	Pin No.	I/O	Description	Remarks
ANT-WIFI/BT	78	I/O	WIFI/BT antenna interface	-

4.2.1 WIFI/BT Band

Table 4-4 WIFI/BT band

Mode	Frequency	Unit
WIFI	2402–2482	MHz
	5170–5835	MHz
BT5.0	2402–2480	MHz

4.2.2 Circuit Reference Design

WIFI/BT antenna connection reference circuit is shown in the following figure.

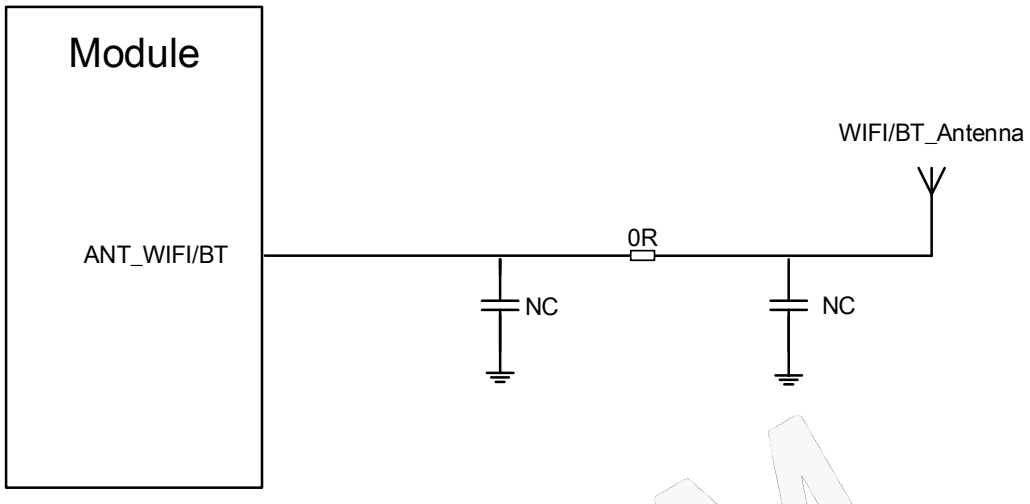


Figure 4-2 WIFI/BT reference circuit

4.3 GNSS Antenna

GNSS supports GPS, GLONASS and Beidou.

Table 4-5 Definition of GNSS antenna interface

Pin Name	Pin No.	I/O	Description	Remarks
ANT_GPS	120	AI	GNSS antenna interface	-

4.3.1 GNSS Band

Table 4-6 GNSS band

Mode	Frequency Band	Unit
GPS	1575.42±1.023	MHz
GLONASS	1597.42-1605.8	MHz
BeiDou	1561.098±2.046	MHz

4.3.2 Circuit Reference Design

The LNA is built into the SC138 series module, and the passive antenna is selected in the whole machine design. Microstrip line is recommended for the GNSS RF routing, the insertion loss is controlled within 0.2 dB, and the impedance is controlled within 50 Ω. The connection reference circuit is shown in the following figure:

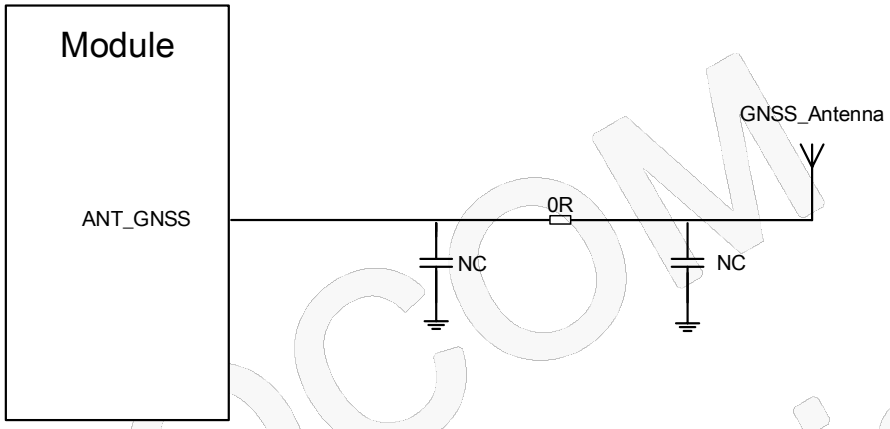


Figure 4-3-1 Reference circuit of GNSS passive antenna

The reference circuit of active antenna is shown in the following figure:

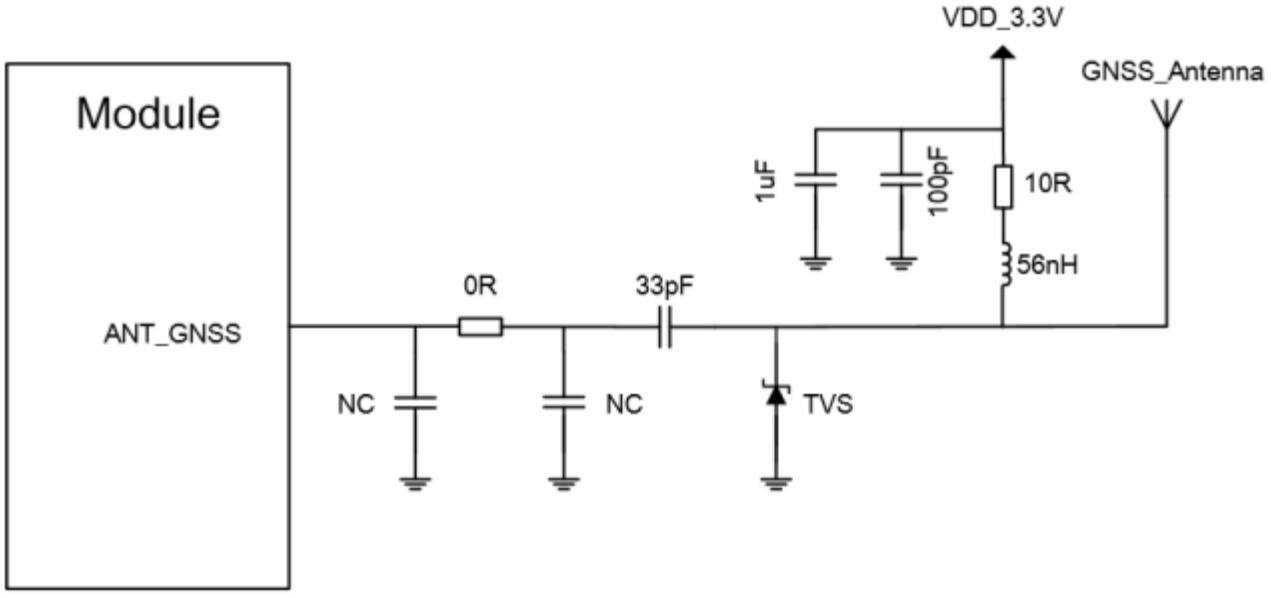


Figure 4-4-2 Reference circuit of GNSS active antenna

The power supply of the active antenna is fed by 56 nH inductance from the signal line of the antenna. The common active antenna supplies power for 3.3 V–5.0 V.

The power consumption of active antenna is very small, but the power supply is required to be stable and clean. It is recommended to use LDO with high performance to power the antenna. The gain of active antenna is required to be < 17 dB. If the gain is > 17 dB, it is necessary to use the reserved π type matching to increase the attenuation network.

4.4 Antenna Requirements

SC138 series modules provide four antenna interfaces: master set, diversity, WIFI/BT and GNSS. The antenna requirements are shown in the following table:

Table 4-7 Antenna requirements

SC138SC138 Series Modules Antenna Requirements	
System	**Antenna Requirements**
GSM/WCDMA/LTE	Standing wave ratio: ≤ 2 Gain (dBi): 1 Maximum input power (W): 5 Input impedance (Ω): 50 Polarization type: vertical direction Insertion loss: < 1 dB (0.7-1GHz) Insertion loss: < 1.5 dB (1.4-2.2GHz) Insertion loss: < 2 dB (2.3-2.7GHz)
WIFI/BT	Standing wave ratio: ≤ 2 Gain (dBi): 1 Maximum input power (W): 5 Input impedance (Ω): 50 Polarization type: vertical direction Insertion loss: < 1dB

SC138SC138 Series Modules Antenna Requirements	
GNSS	Frequency range: 1559 MHz–1607 MHz Polarization type: right hand circularly polarized (RHCP) or linearly polarized Standing-wave ratio: < 2 (typical value) Passive antenna gain: > 0 dBi Active antenna noise coefficient: < 1.5 dB (typical value) Active antenna gain: > –2 dBi LNA gain in active antenna: < 17 dB (typical value)
GPS- MAIN Antenna Isolation	>20dB
WiFi-cellular Antenna Isolation	>20dB

5 RF PCB Layout Design Guide

For user PCB, the characteristic impedance of all RF signal lines shall be controlled at 50 Ω. In general, the impedance of the RF signal line is determined by the dielectric constant of the material, the routing width (W), the ground clearance (S), and the height of the reference ground plane (H). The characteristic impedance of PCB is usually controlled by microstrip line and coplanar waveguide. In order to reflect the design principle, the following figure displays the structure design of microstrip line and coplanar waveguide when the impedance line is controlled at 50 Ω.

- Complete structure of microstrip line

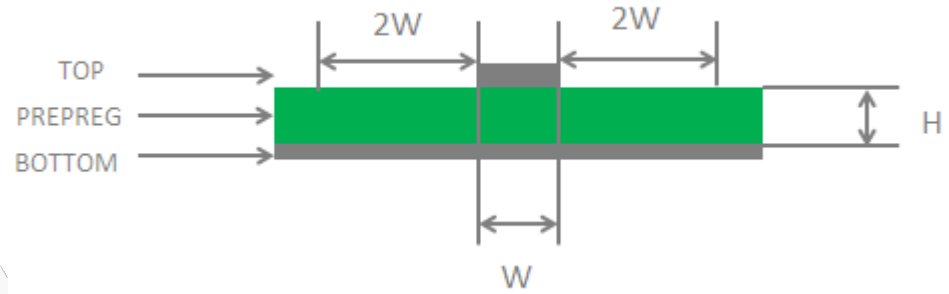


Figure 5-1 Microstrip line structure of two-layer of PCB

- Complete structure of coplanar waveguide

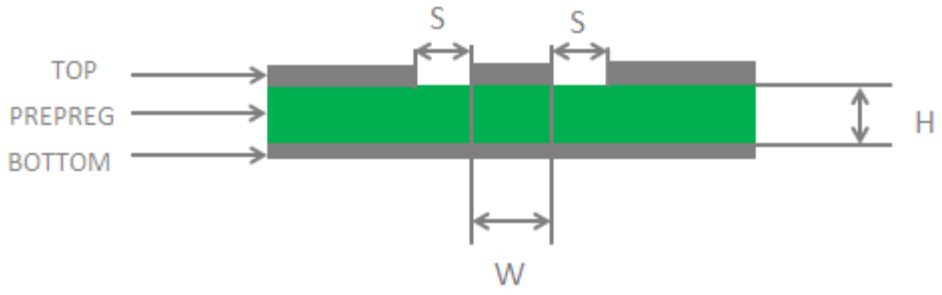


Figure 5-2 Coplanar waveguide structure of two-layer PCB

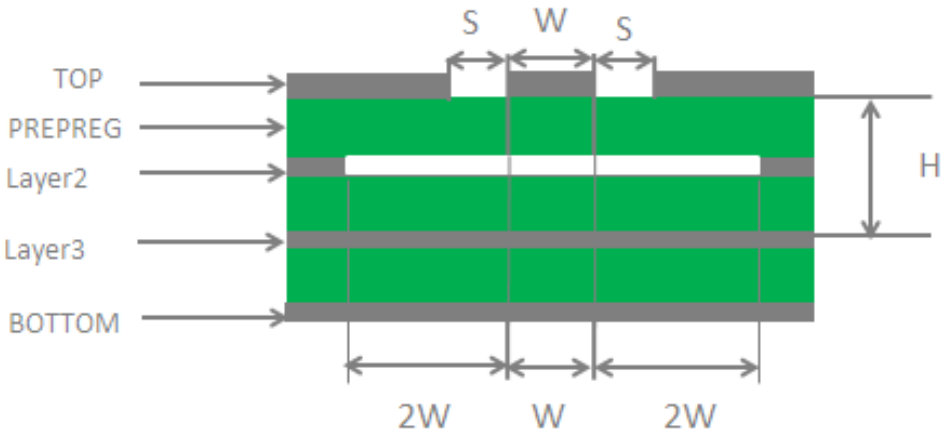


Figure 5-3 Coplanar waveguide structure of four-layer PCB (reference ground layer 3)

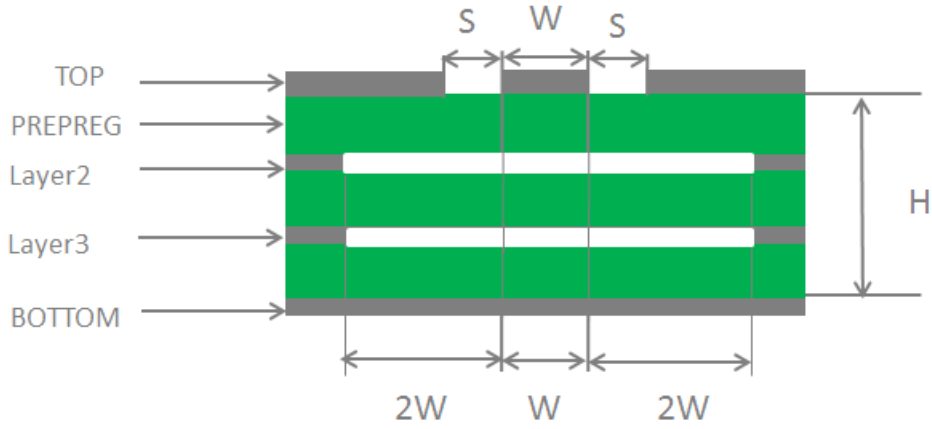


Figure 5-4 Coplanar waveguide structure of four-layer PCB (reference ground layer 4)

In the circuit design of RF antenna interface, in order to ensure the good performance and ALT of RF signal, the following design principles are recommended in the circuit design:

- The impedance simulation calculation tools shall be used to accurately control the 50 Ω impedance of the RF signal line.
- GND pins adjacent to RF pins shall not be hot bonding pads and shall be fully contacted with the ground.
- The distance between RF pin and RF connector shall be as short as possible; in order to avoid right-angle routing, the recommended routing angle is 135°.
- When connecting the device package, it shall be noted that the signal pin shall be kept at a certain distance from the ground.

- The reference ground plane of RF signal line shall be complete; adding a certain amount of ground holes around the signal line and the reference ground can help improve the RF performance; the distance between the ground hole and the signal line shall be at least twice the line width (2 * W).

6 WIFI and Bluetooth

6.1 WIFI Overview

SC138SC138 series modules support 2.4G and 5G WLAN wireless communication, and support the types of 802.11a, 802.11b, 802.11g, 802.11n and 802.11ac, with the highest rate of 433 Mbps.

Characteristics are described as follows:

- Support Wake-on-WLAN (WoWLAN)
- Support ad hoc mode
- Support WAPI
- Support AP mode
- Support Wi-Fi Direct
- Support MCS 0-7 for HT20 and HT40 (if the 2.4G WIFI 40M needs to be opened, the ini file shall be configured, but it is not recommended)
- Support MCS 0-8 for VHT20
- Support MCS 0-9 for VHT40 and VHT80

6.2 WIFI Performance Indicators

Test conditions: supply voltage 3.8 V, ambient temperature 25ºC.

Table 6-1 WIFI transmission power

Frequency	Mode	Date Rate	Bandwidth (MHz)	TX Power (dBm)
2.4G	802.11b	1Mbps	20	17.0±3
		11Mbps	20	17.0±3
	802.11g	6Mbps	20	16.0±3
		54Mbps	20	13.0±3
	802.11n	MCS0	20	15.0±3
		MCS7	20	12.0±3
		MCS0	40	15.0±3

Frequency	Mode	Date Rate	Bandwidth (MHz)	TX Power (dBm)
		MCS7	40	12.0±3
5G	802.11a	6Mbs	20	19.0±3
		54Mbps	20	16.0±3
	802.11n	MCS0	20	18.0±3
		MCS7	20	15.0±3
		MCS0	40	17.0±3
		MCS7	40	14.0±3
	802.11ac	MCS0	20	17.0±3
		MCS8	20	14.0±3
		MCS0	40	16.0±3
		MCS9	40	13.0±3
		MCS0	80	15.0±3
		MCS9	80	12.0±3

Table 6-2 WIFI receiving sensitivity

Frequency	Mode	Date Rate	Bandwidth (MHz)	Sensitivity(dBm) [2]
2.4G	802.11b	1Mbps	20	-94.0
		11Mbps	20	-88.0
	802.11g	6Mbps	20	-89.0
		54Mbps	20	-73.0
	802.11n	MCS0	20	-88.0
		MCS7	20	-69.0
		MCS0	40	-84.0
		MCS7	40	-66.0
5G	802.11a	6Mbps	20	-90.0
		54Mbps	20	-76.0

Frequency	Mode	Date Rate	Bandwidth (MHz)	Sensitivity(dBm) 2)
	802.11n	MCS0	20	-90.0
		MCS7	20	-71.0
	802.11n	MCS0	40	-88.0
		MCS7	40	-68.0
	802.11ac	MCS0	20	-90.0
		MCS8	20	-69.0
		MCS0	40	-88.0
		MCS9	40	-65.0
		MCS0	80	-85.0
		MCS9	80	-62.0

Note:

2) The sensitivity here is typical.

6.3 Bluetooth Overview

SC138SC138 series modules support BT5.0 (BR/EDR+BLE) specifications, and the modulation mode supports GFSK; the channel bandwidth of 8-DPSK and π/4-DQPSK.BR/EDR is 1 MHz, which can accommodate 79 channels; BLE channel bandwidth is 2 MHz, which can accommodate 40 channels. Its main characteristics are as follows:

- BT 5.0+BR/EDR+BLE
- Support for ANT protocol
- Support for BT-WLAN coexistence operation, including optional concurrent receive
- Up to 3.5 piconets (master, slave, and page scanning)

Table 6-3 BT rate and version information

Version	Date Rate	Throughput	Note
BT1.2	1Mbit/s	> 80Kbit/s	-
BT2.0+EDR	3Mbit/s	> 80Kbit/s	-
BT3.0+HS	24Mbit/s	For details, see 3.0+HS	-
BT5.0 LE	24Mbit/s	For details, see 5.0 LE	-

6.4 Bluetooth Performance Indicators

Test conditions: supply voltage 3.8 V, ambient temperature 25ºC.

Table 6-4 BT performance indicators

Type	DH-5	2-DH5	3-DH5	BLE	Unit
Transmitter	11±2.5	9±2.5	8±2.5	6±2.5	dBm
Sensitivity	-86	-85	-83	-93	dBm

7 GNSS

7.1 Overview

SC138SC138 series intelligent modules support GPS, GLONASS and Beidou and other positioning systems. LNA is embedded in the module, which can effectively improve the sensitivity of GNSS.

7.2 Performance Index

Test conditions: supply voltage 3.8 V, ambient temperature 25ºC.

Table 7-1 GNSS positioning performance

Parameter	Description	Type Result	Unit
Sensitivity	Acquisition	-145	dBm
	Tracking	-158	dBm
C/N	-130dBm	39	dB-Hz
TTFF	Cold Start	45	s
	Warm Start	42	s
	Hot Start	2	s
CEP	Static accuracy（95% @-130dbm）	4	m

8 Electrical, ALT and RF Performance

8.1 Recommended Parameters

Table 8-1 recommended parameters

Parameter	Min	Normal	Max	Unit
VBAT	3.5	3.8	4.2	V
USB_IN_DET	4.75	5	5.25	V
VRTC	2.0	3.0	3.25	V
Operating Temperature	-30	25	75	ºC
Storage Temperature	-40	25	85	ºC

8.2 Operating Current

Test conditions: supply voltage 3.8 V, ambient temperature 25ºC.

Table 8-2 SC138 operating current

Parameter	Description	Condition	Type	Unit
I_{off}	Power Off	Power Off	50	uA
I_{sleep}	GSM	MFRMS=5	4.5	mA
	WCDMA	DRX=8	4.5	
	TDD LTE	DPC (Default Paging Cycle) =#256	4.5	
	FDD LTE	DPC (Default Paging Cycle) =#256	4.5	
	Radio Off	AT+CFUN=4 Flight Mode	4	
$I_{GSM-RMS}$	GSM voice RMS Current	GSM850@ PCL=5	280	mA
		GSM850@ PCL=19	120	
		EGSM900@ PCL=5	280	
		EGSM900@ PCL=19	120	
		DCS1800@ PCL=0	210	

Parameter	Description	Condition	Type	Unit
		DCS1800@ PCL=15	110	
		PCS1900@ PCL=0	210	
		PCS1900@ PCL=15	110	
$I_{GSM-MAX}$	GSM voice Peak current	EGSM900@ PCL=5	2200	mA
		DCS1800@ PCL=0	1400	
$I_{GPRS-RMS}$	GPRS data RMS Current	GSM850@Gamma=3（1UL/1DL）	270	mA
		GSM850@Gamma=3（4UL/1DL）	620	
		EGSM900@Gamma=3（1UL/1DL）	270	
		EGSM900@Gamma=3（4UL/1DL）	620	
		DCS1800@Gamma=3（1UL/1DL）	200	
		DCS1800@Gamma=3（4UL/1DL）	480	
		PCS1900@Gamma=3（1UL/1DL）	200	
		PCS1900@Gamma=3（4UL/1DL）	480	
$I_{EGPRS-RMS}$	EGPRS data RMS Current	GSM850@Gamma=6（1UL/1DL）	220	mA
		GSM850@Gamma=6（4UL/1DL）	660	
		EGSM900@Gamma=6（1UL/1DL）	220	
		EGSM900@Gamma=6（4UL/1DL）	660	
		DCS1800@Gamma=5（1UL/1DL）	180	
		DCS1800@Gamma=5（4UL/1DL）	450	
		PCS1900@Gamma=5（1UL/1DL）	180	
		PCS1900@Gamma=5（4UL/1DL）	450	
$I_{WCDMA-RMS}$	WCDMA RMS Current	Band1@ max power	580	mA
		Band2@ max power	580	
		Band5@ max power	620	
		Band8@ max power	680	
$I_{LTE-RMS}$	FDD data RMS Current	Band1@max power(10MHz,1RB)	580	mA
		Band3@max power(10MHz,1RB)	680	
		Band5@max power(10MHz,1RB)	610	
		Band7@max power(10MHz,1RB)	720	
		Band8@max power(10MHz,1RB)	650	
		Band20@max power(10MHz,1RB)	560	

Parameter	Description	Condition	Type	Unit
		Band28A@max power(10MHz,1RB)	680	
		Band28B@max power(10MHz,1RB)	680	
	TDD data RMS Current	Band38@max power(10MHz,1RB)	430	
		Band40@max power(10MHz,1RB)	340	
		Band41@max power(10MHz,1RB)	450	

8.3 RF Transmitting Power

The transmission power of SC138 series modules in bands is shown in the following table:

Test conditions: supply voltage 3.8 V, ambient temperature 25ºC, the bandwidths of LTE maximum power test are 10M and 12 RB.

Table 8-3 SC138-EAU RF transmitting power

Mode	Band	Max Power (dBm)	Min Power (dBm)
GSM	850 (GMSK)	33±2	5±5
	900 (GMSK)	33±2	5±5
	1800 (GMSK)	30±2	0±5
	1900 (GMSK)	30±2	0±5
GSM	850 (8PSK)	27±3	5±5
	900 (8PSK)	27±3	5±5
	1800 (8PSK)	26+3/-4	0±5
	1900 (8PSK)	26+3/-4	0±5
WCDMA	Band 1	24+1/-3	< -49
	Band 2	24+1/-3	< -49
	Band 5	24+1/-3	< -49
	Band 8	24+1/-3	< -49
LTE FDD	Band 1	23±2	< -39
	Band 3	23±2	< -39

Mode	Band	Max Power (dBm)	Min Power (dBm)
	Band 5	23±2	<-39
	Band 7	23±2	< -39
	Band 8	23±2	< -39
	Band 20	23±2	< -39
	Band 28	23±2	< -39
	Band 38	23±2	< -39
	Band 40	23±2	< -39
	Band 41	23±2	< -39

8.4 RF Receiving Sensitivity[3)]

The sensitivity of SC138-EAU series modules in bands is shown in the following table:

Test conditions: power supply voltage 3.8 V, ambient temperature 25ºC, LTE sensitivity test bandwidth is 10M, see 3 gpp for details of RB configuration.

Table 8-4 SC138-EAU RF receiving sensitivity

Mode	Band	Primary	Diversity	PRX+Div	3GPP Requirement	Unit
GSM	850	-108.5	N/A	N/A	-102.0	dBm
	900	-108.5	N/A	N/A	-102.0	dBm
	1800	-108	N/A	N/A	-102.0	dBm
	1900	-108	N/A	N/A	-102.0	dBm
WCDMA	Band 1	-109	N/A	N/A	-106.7	dBm
	Band 2	-109	N/A	N/A	-104.7	dBm
	Band 5	-109.5	N/A	N/A	-104.7	dBm
	Band 8	-109.5	N/A	N/A	-103.7	dBm
LTE-FDD (10M)	Band 1	-98	-98	-100.5	-97	dBm
	Band 3	-98	-98	-100.5	-94	dBm
	Band 5	-98.5	-99	-101	-95	dBm

	Band 7	-97.5	-98.5	-100	-94	dBm
	Band 8	-98.5	-99	-101	-97	dBm
	Band 20	-98.5	-98.5	-100.5	-94	dBm
	Band 28A	-98.5	-98.5	-100	-95.5	dBm
	Band 28B	-98.5	-98	-100	-95.5	dBm
LTE-TDD (10M)	Band 38	-96.5	-98.5	-99.5	-97	dBm
	Band 40	-96	-98	-99	-97	dBm
	Band 41	-96	-98	-99	-95	dBm

Note:

3) The sensitivity here is typical.

8.5 Electrostatic Protection

In the application of modules, due to the static electricity generated by human body static electricity and charged friction between microelectronics, it may cause damage to the module through various ways, so ESD protection shall be paid attention to. ESD protection measures shall be taken in the process of R&D, production assembly and testing, especially in product design. For example, at the interface of circuit design and the points easily damaged or affected by electrostatic discharge, anti-static protection shall be added; anti-static gloves shall be worn in production.

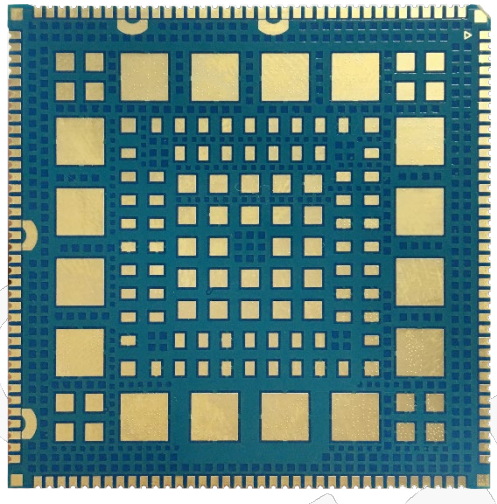
List of ESD Performance Parameters 1-6 (temperature: 25ºC, humidity: 45%–60%).

Table 8-5 ESD performance

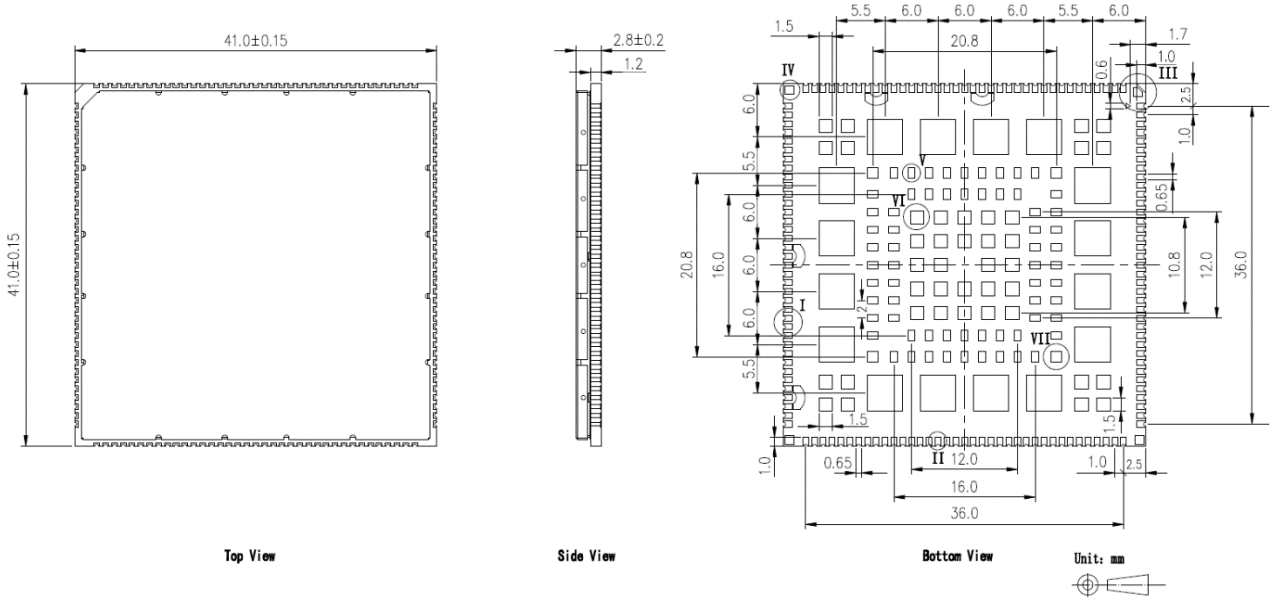
Test Point	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	KV
Antenna interface	±4	±8	KV
Other interfaces	±0.5	±1	KV

9 Structural Specification

9.1 Product Appearance



9.2 Structure Size



9.3 Reference PCB Bonding Pad Design

For details of recommended design of PCB bonding pad and corresponding steel mesh, see *FIBOCOM SC138 Series SMT Design Guide*.

10 Production and Storage

10.1 SMT Patch

For details of SMT production process parameters and related requirements, see *FIBOCOM SC138 Series SMT Design Guide*.

10.2 Packaging and Storage

For details of packing and storage, see *FIBOCOM SC138 Series SMT Design Guide*.

Appendix A Abbreviations

Table A-1 Abbreviations

Abbreviation	Meaning
AMR	Adaptive Multi-rate
bps	Bits Per Second
CS	Coding Scheme
DRX	Discontinuous Reception
FDD	Frequency Division Duplexing
GMSK	Gaussian Minimum Shift Keying
HSDPA	High Speed Down Link Packet Access
IMEI	International Mobile Equipment Identity
Imax	Maximum Load Current
LED	Light Emitting Diode
LSB	Least Significant Bit
LTE	Long Term Evolution
CA	Carrier Aggregation
DLCA	Downlink Carrier Aggregation
SCell	Secondary Cell for CA
ME	Mobile Equipment
MS	Mobile Station
MT	Mobile Terminated
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency

Abbreviation	Meaning
RHCP	Right Hand Circularly PolarizedRMS
RMS	Root Mean Square
RTC	Real Time Clock
Rx	Receive
SMS	Short Message Service
TDMA	Time Division Multiple Access
TE	Terminal Equipment
TX	Transmitting Direction
TDD	Time Division Duplexing
UART	Universal Asynchronous Receiver & Transmitter
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
(U)SIM	(Universal) Subscriber Identity Module
USSD	Unstructured Supplementary Service Data
Vmax	Maximum Voltage Value
Vnorm	Normal Voltage Value
Vmin	Minimum Voltage Value
VIHmax	Maximum Input High Level Voltage Value
VIHmin	Minimum Input High Level Voltage Value
VILmax	Maximum Input Low Level Voltage Value
VILmin	Minimum Input Low Level Voltage Value
VImax	Absolute Maximum Input Voltage Value
VImin	Absolute Minimum Input Voltage Value
VOHmax	Maximum Output High Level Voltage Value
VOHmin	Minimum Output High Level Voltage Value
VOLmax	Maximum Output Low Level Voltage Value
VOLmin	Minimum Output Low Level Voltage Value
VSWR	Voltage Standing Wave Ratio

Abbreviation	Meaning
WCDMA	Wideband Code Division Multiple Access

Appendix B GPRS Coding Scheme

Table B-1 GPRS coding scheme

Coding Mode	CS-1	CS-2	CS-3	CS-4
Code Rate	1/2	2/3	3/4	1
USF	3	3	3	3
Pre-coded USF	3	6	6	12
Radio Block excl.USF and BCS	181	268	312	428
BCS	40	16	16	16
Tail	4	4	4	-
Coded Bits	456	588	676	456
Punctured Bits	0	132	220	-
Data Rate Kb/s	9.05	13.4	15.6	21.4

Appendix C GPRS Multi-slot

In the GPRS specification, 29 kinds of GPRS multi-slot modes are defined for mobile stations. The multi-slot class defines the maximum rate of uplink and downlink. Expressed as 3 + 1 or 2 + 2, the first number represents the number of downlink slots, and the second number represents the number of uplink slots. Active slot represents the total number of slots that can be used simultaneously for uplink and downlink communication of GPRS devices

Table C-1 Multi-slot allocation with different levels

Multi-slot Class	Downlink Slots	Uplink Slots	Active Slots
1	1	1	2
2	2	1	3
3	2	2	3
4	3	1	4
5	2	2	4
6	3	2	4
7	3	3	4
8	4	1	5
9	3	2	5
10	4	2	5
11	4	3	5
12	4	4	5

Appendix D EDGE Modulation and Coding Mode

Table D-1 EDGE modulation and coding mode

Coding Scheme	Modulation	Coding Family	1 Timeslot	2 Timeslot	4 Timeslot
CS-1	GMSK	/	9.05kbps	18.1kbps	36.2kbps
CS-2	GMSK	/	13.4kbps	26.8kbps	53.6kbps
CS-3	GMSK	/	15.6kbps	31.2kbps	62.4kbps
CS-4	GMSK	/	21.4kbps	42.8kbps	85.6kbps
MCS-1	GMSK	C	8.80kbps	17.6kbps	35.2kbps
MCS-2	GMSK	B	11.2kbps	22.4kbps	44.8kbps
MCS-3	GMSK	A	14.8kbps	29.6kbps	59.2kbps
MCS-4	GMSK	C	17.6kbps	35.2kbps	70.4kbps
MCS-5	8-PSK	B	22.4kbps	44.8kbps	89.6kbps
MCS-6	8-PSK	A	29.6kbps	59.2kbps	118.4kbps
MCS-7	8-PSK	B	44.8kbps	89.6kbps	179.2kbps
MCS-8	8-PSK	A	54.4kbps	108.8kbps	217.6kbps
MCS-9	8-PSK	A	59.2kbps	118.4kbps	236.8kbps