

NCE N-Channel Super Trench Power MOSFET



The NCEP1580D uses **Super Trench** technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of R_{DS(ON)} and Q_g. This device is ideal for high-frequency switching and synchronous rectification. **General Features**

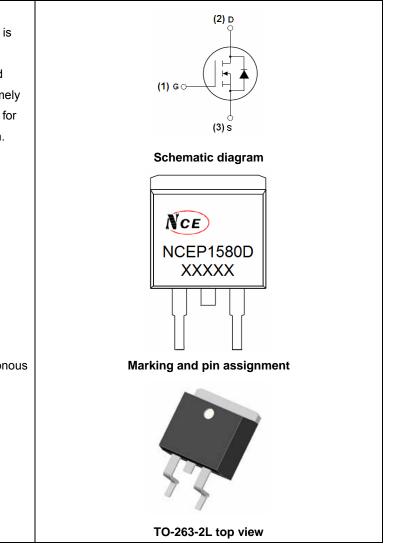
- V_{DS} =150V,I_D =80A
 - $R_{DS(ON)}$ <12.5m Ω @ V_{GS}=10V
- Excellent gate charge x R_{DS(on)} product(FOM)
- Very low on-resistance R_{DS(on)}
- 175 °C operating temperature
- Pb-free lead plating
- 100% UIS tested

Application

- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification

100% UIS TESTED!

100% ΔVds TESTED!



Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
NCEP1580D	NCEP1580D	TO-263-2L	-	-	-

Absolute Maximum Ratings (T_c=25[°]C unless otherwise noted)

Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	Vds	150	V	
Gate-Source Voltage	Vgs	±20	V	
Drain Current-Continuous	Ι _D	80	А	
Drain Current-Continuous(T _C =100 ℃)	I _D (100℃)	56.6	А	
Pulsed Drain Current	I _{DM}	320	А	
Maximum Power Dissipation	PD	210	W	
Derating factor		1.4	W/℃	
Single pulse avalanche energy (Note 5)	E _{AS}	672	mJ	
Operating Junction and Storage Temperature Range	T _J ,T _{STG}	-55 To 175	°C	



Thermal Characteristic

Electrical Characteristics (T_C=25[°]C unless otherwise noted)

Parameter	Symbol	Condition	Min	Тур	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =250µA	150		-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =150V,V _{GS} =0V	-	-	1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V,V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	V _{GS(th)}	$V_{DS}=V_{GS}$, I _D =250µA	2.5	-	4.5	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =40A	-	10.4	12.5	mΩ
Forward Transconductance	g fs	V _{DS} =10V,I _D =40A	-	38	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C _{lss}		-	3200	-	PF
Output Capacitance	C _{oss}	V _{DS} =75V,V _{GS} =0V, F=1.0MHz	-	382	-	PF
Reverse Transfer Capacitance	C _{rss}	F=1.0MHZ	-	17.9	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =75V,I _D =40A V _{GS} =10V,R _G =4.7Ω	-	17	-	nS
Turn-on Rise Time	tr		-	35	-	nS
Turn-Off Delay Time	t _{d(off)}		-	32	-	nS
Turn-Off Fall Time	t _f		-	9	-	nS
Total Gate Charge	Qg		-	44.1		nC
Gate-Source Charge	Q _{gs}	$V_{DS} = 75V, I_D = 40A,$	-	19.6		nC
Gate-Drain Charge	Q _{gd}	V _{GS} =10V	-	7.1		nC
Drain-Source Diode Characteristics	· ·					
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V,I _S =80A	-		1.2	V
Diode Forward Current (Note 2)	I _S		-	-	80	Α
Reverse Recovery Time	t _{rr}	T_J = 25°C, I_F = I_S	-	58		nS
Reverse Recovery Charge	Qrr	di/dt = 100A/µs ^(Note3)	-	138		nC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.

2. Surface Mounted on FR4 Board, t \leq 10 sec.

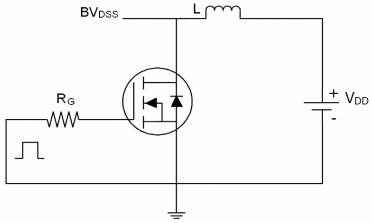
3. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2%.

4. Guaranteed by design, not subject to production

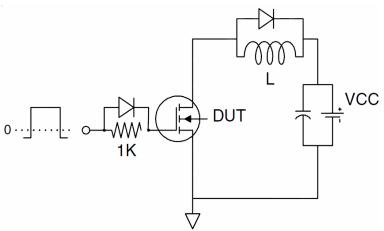
5. EAS condition : Tj=25 $^\circ\!\mathrm{C}$,V_DD=50V,V_G=10V,L=0.5mH,Rg=25 Ω



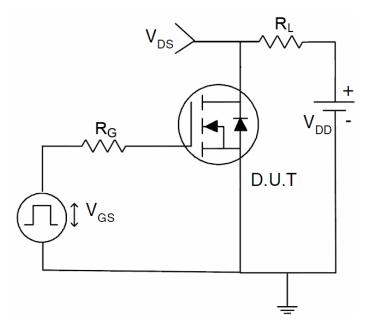
Test Circuit 1) E_{AS} test Circuit



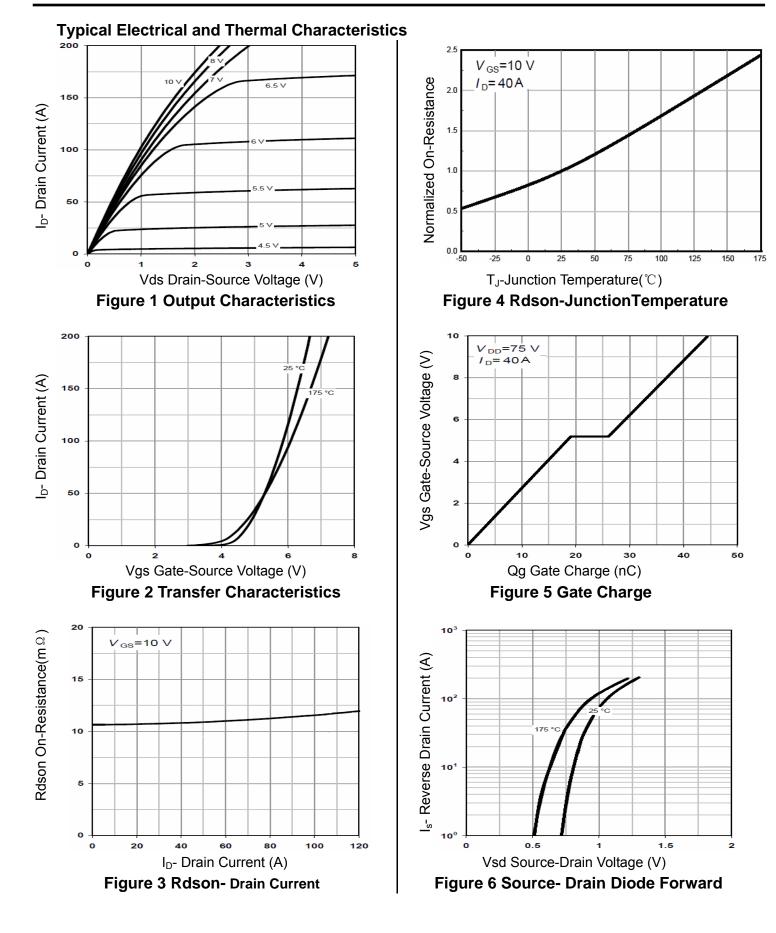
2) Gate charge test Circuit



3) Switch Time Test Circuit



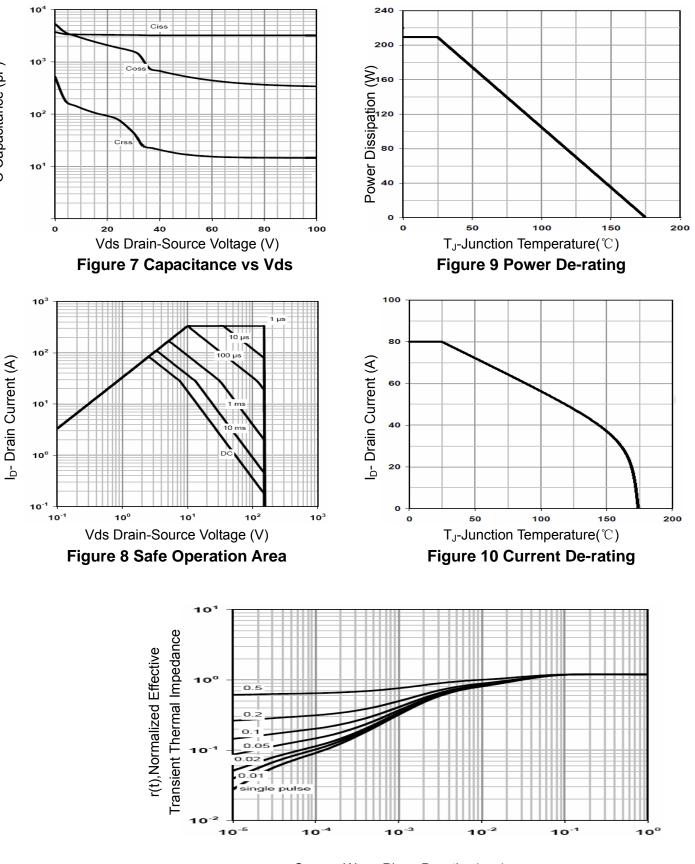






C Capacitance (pF)

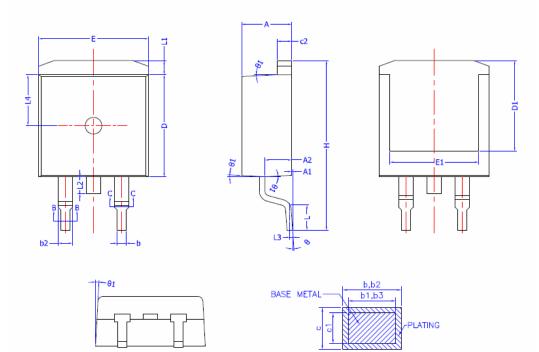
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Square Wave Pluse Duration(sec) Figure 11 Normalized Maximum Transient Thermal Impedance



TO-263-2L Package Information



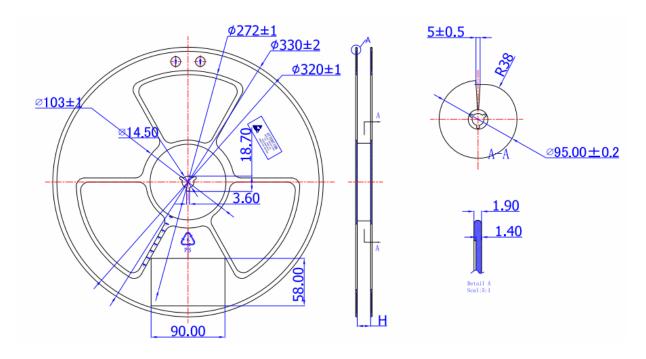
COMMON DIMENSIONS (UNITS OF MEASURE =MILLIMETER)

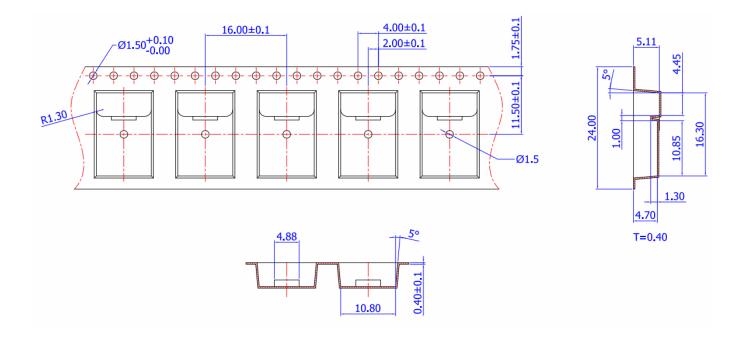
SECTION B-B&C-C

(ONTIO OF THE ADDIRE - PRECEDENCIER)				
SYMBOL	MIN	NOM	MAX	
А	4.40	4.50	4.60	
A1	0	0.10	0.25	
A2	2,20	2,40	2,60	
b	0,76		0,89	
b1	0,75	0,80	0,85	
b2	1,23		1,37	
b3	1,22	1,27	1,32	
с	0,47		0.60	
c1	0,46	0,51	0.56	
c2	1,25	1,30	1.35	
D	9,10	9,20	9.30	
D1	8,00			
E	9,80	9,90	10.00	
E1	7.80		—	
е	2.54 BSC			
Н	14,90	15,30	15.70	
L	2.00	2,30	2.60	
L1	1.17	1.27	1.40	
L2		- 1,75		
L3	0.25BSC			
L4	4.60 REF			
θ	0°	— 8°		
θ1	1°	3° 5°		

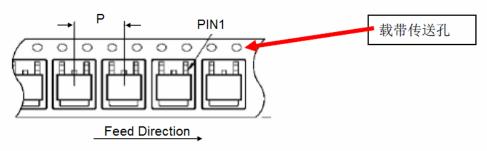


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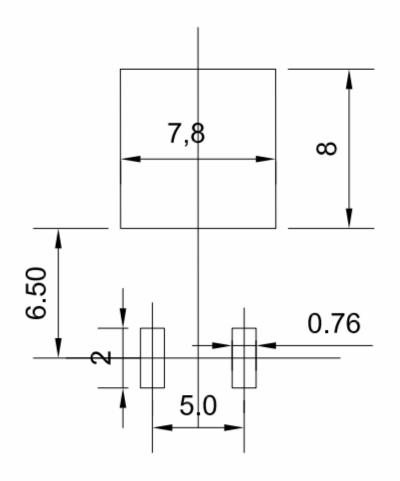
注:产品编入卷盘中时,产品第一支脚(PIN 1)方向朝向载带传送孔。如下图所示。





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