BOE

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TITLE : DV320FHB-N02

Product Specification

Rev.O

BEIJING BOE Display TECHNOLOGY Co., LTD

REVISION HISTORY

( )preliminary specification
(√)Final specification

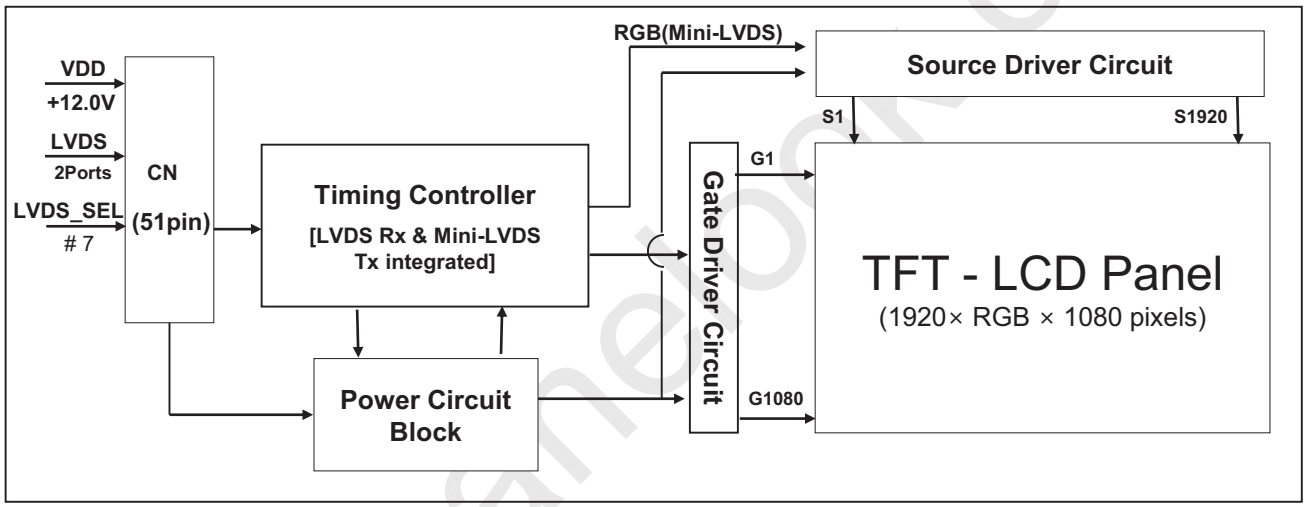
Revision No.	Page	Description of changes	Date	Prepared
P0	-		2022.05.09	Zhang Di
O	-		2022.09.08	Zhang Di

Contents

1.0 GENERAL DESCRIPTION

1.1 Introduction

DV320FHB-N02 is a color active matrix TFT LCD open cell using amorphous silicon TFT's (Thin Film Transistors) as an active switching devices. This module has a 31.51 inch diagonally measured active area with FHD resolutions (1920 horizontal by 1080 vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical stripe and this module can display 16.7M colors. The TFT-LCD panel used for this module is adapted for a low reflection and higher color type.



1.2 Features

- LVDS interface with 2 port pixel / clock
- High-speed response
- Low color shift image quality
- 8-bit color depth, display 16.7M colors
- High luminance and contrast ratio, low reflection and wide viewing angle
- DE (Data Enable) only mode
- ADS technology is applied for high display quality
- RoHS compliant

1.3 Application

- Display Terminals for Control System
- Landscape and Portrait Display

1.4 General Specification

< Table 1. General Specifications >

Parameter	Specification	Unit	Remark
Active area	698.4(H) × 392.85 (V)	mm	
Number of pixels	1920(H) ×1080(V)	pixels	
Pixel pitch	121.25(H) ×RGB×363.75(V)	μm	
Pixel arrangement	Pixels RGB Vertical stripe		
Display colors	16.7M (8bits-true)	colors	8bit driver IC
Display mode	Transmission mode, Normally Black		
Open Cell Transmittance	5.0 (typ.)	%	At center point with BOE BLU
Weight	850	gram	
Power Consumption	4.0	Watt	With TCON board
Surface Treatment	Haze 1% ，2H(Min)，Anti-Glare Layer (for Front) ，Clear(for Rear)		

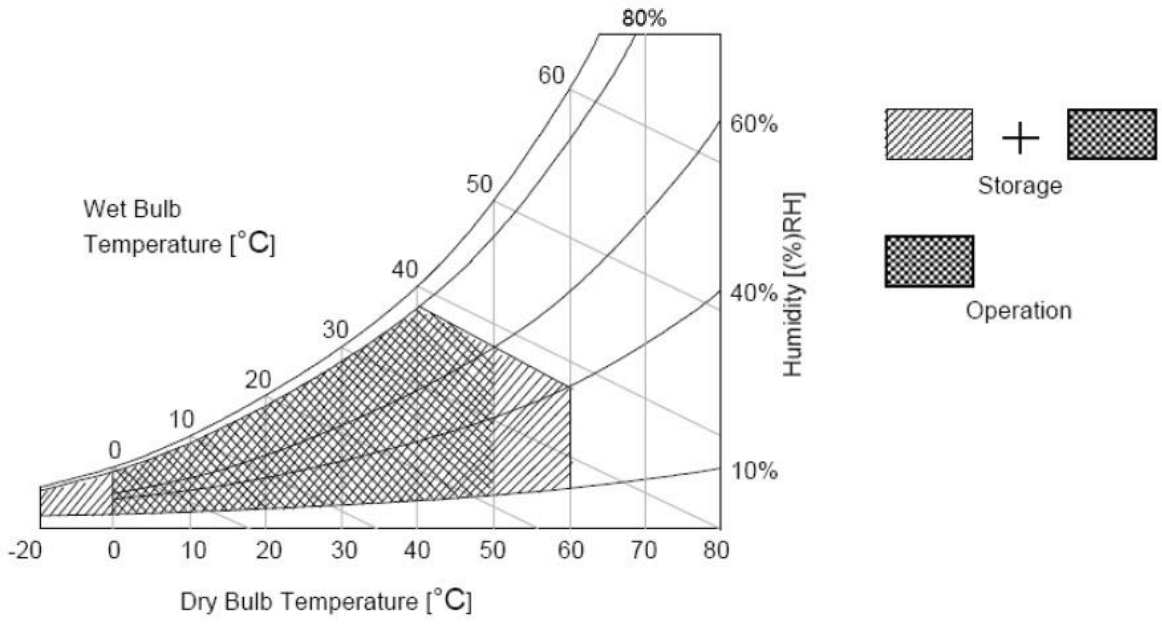
2.0 ABSOLUTE MAXIMUM RATINGS

The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit. The operational and non-operational maximum voltage and current values are listed in Table 2.

< Table 2. Open Cell Absolute Maximum Ratings > [VSS=GND=0V]

Parameter	Symbol	Min.	Max.	Unit	Remark
Operating Temperature	T_{OP}	0	+50	℃	Note 1
Storage Temperature	T_{SUR}	-20	+60	℃	
	T_{ST}	-20	+60	℃	
Operating Ambient Humidity	Hop	10	80	%RH	
Storage Humidity	Hst	10	80	%RH	

Note 1 : Temperature and relative humidity range are shown in the figure below.
Wet bulb temperature should be 39 ℃ max. and no condensation of water.



3.0 ELECTRICAL SPECIFICATIONS

3.1 TFT LCD Open Cell

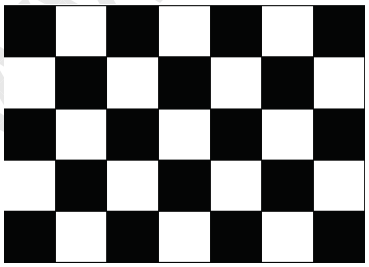
< Table 3. Open Cell Electrical Specifications >

[Ta =25±2 ℃]

Parameter		Symbol	Values			Unit	Remark
			Min	Typ	Max		
Power Supply Input Voltage		VDD	10.8	12	13.2	Vdc	
Power Supply Ripple Voltage		VRP	-	-	300	mV	
Power Supply Current		IDD	-	333	630	mA	Note 1
Power Consumption		PDD	-	4.0	7.6	Watt	
Rush current		IRUSH	-	-	4	A	Note 2
LVDS Interface	Differential Input High Threshold Voltage	VLVTH	-	-	100	mV	VLVC=1.2V
	Differential Input Low Threshold Voltage	VLVTL	-100	-	-	mV	
	Common Input Voltage	VLVC	1.0	1.2	1.4	V	
CMOS Interface	Input High Threshold Voltage	VIH	2.7	-	3.3	V	
	Input Low Threshold Voltage	VIL	0	-	0.6	V	

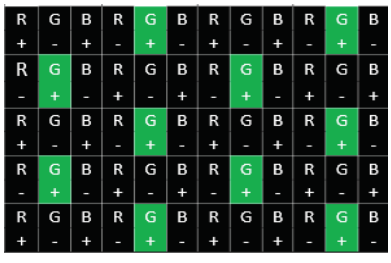
Note 1 : The supply voltage is measured and specified at the interface connector of LCM.
The current draw and power consumption specified is for VDD=12.0V,
Frame rate f_V=60Hz and Clock frequency = 74.25MHz.
Test Pattern of power supply current

a) Typ : Mosaic 7X5 (L0/L255)



b) Max : Horizontal 1 Line (L0/L255)

c) Flicker Test Pattern



3.2 TCON Characteristics

< Table 4. TCON Characteristics >

Parameter	Symbol	Values			Unit	Remark
		Min	Typ	Max		
TCON Surface Temperature	T_{TS}	-	-	110	℃	Note

Note 1 : Any point on the TCON surface must be less than 110 ℃ under any conditions.

Note 2 : This test condition is based on BOE module.

3.3 Driver Characteristics

< Table 5. Driver Characteristics >

Parameter	Symbol	Values			Unit	Remark
		Min	Typ	Max		
Driver Surface Temperature	T_{DS}	-	-	125	℃	Note

Note 3 : Any point on the driver surface must be less than 125 ℃ under any conditions.

Note 4: This test condition is based on BOE module.

3.4 PMIC Characteristics

< Table 6. PMIC Characteristics >

Parameter	Symbol	Values			Unit	Remark
		Min	Typ	Max		
PMIC Surface Temperature	T_{PS}	-	-	100	℃	Note

Note 5 : Any point on the PMIC surface must be less than 100 ℃ under any conditions.

Note 6: This test condition is based on BOE module.

3.5 VCOM I2C Bus Format

Step1 Reset

*Device Address is 0x74 or 0x75(7Bits)

S	Slave Address	W	A	Index Address 0	A	Control Byte	A	P
	1 1 1 0 1 0 0 0 0xE8 Device Address + W			0 0 0 0 0 0 0 0 0x00 Control Address		0 0 0 1 0 0 1 0 0x12 Reset + OUT_EN		

Step2 Read VCOM

*Data = 7Bits

S	Slave Address	W	A	Index Address 1	SR	Slave Address	R	A	DATA 0/1	NA	P
	1 1 1 0 1 0 0 0 0XE8 Device address + W			0 0 0 0 0 0 0 1 0X01 VCOM Address		1 1 1 0 1 0 0 1 0XE9 Device address + R			X X X X X X X X Data		

Step3 Adjust VCOM

*DVCOM= 8Bits

S	Slave Address	W	A	Index Address 1	A	DVCOM	A	P
	1 1 1 0 1 0 0 0 0XE8 Device address + W			0 0 0 0 0 0 0 1 0X01 VCOM Address		0000000X~1111111X 0x00~0xFF VCOM value		

Step4 Write VCOM

S	Slave Address	W	A	Index Address 1	A	Control Byte | (0x02)	A	P
	1 1 1 0 1 0 0 0 0xE8 Device Address + W			0 0 0 0 0 0 0 0 0x00 Control Address		0 0 0 0 1 0 1 0 0X0A Write DAC to NVM + OUT_EN		

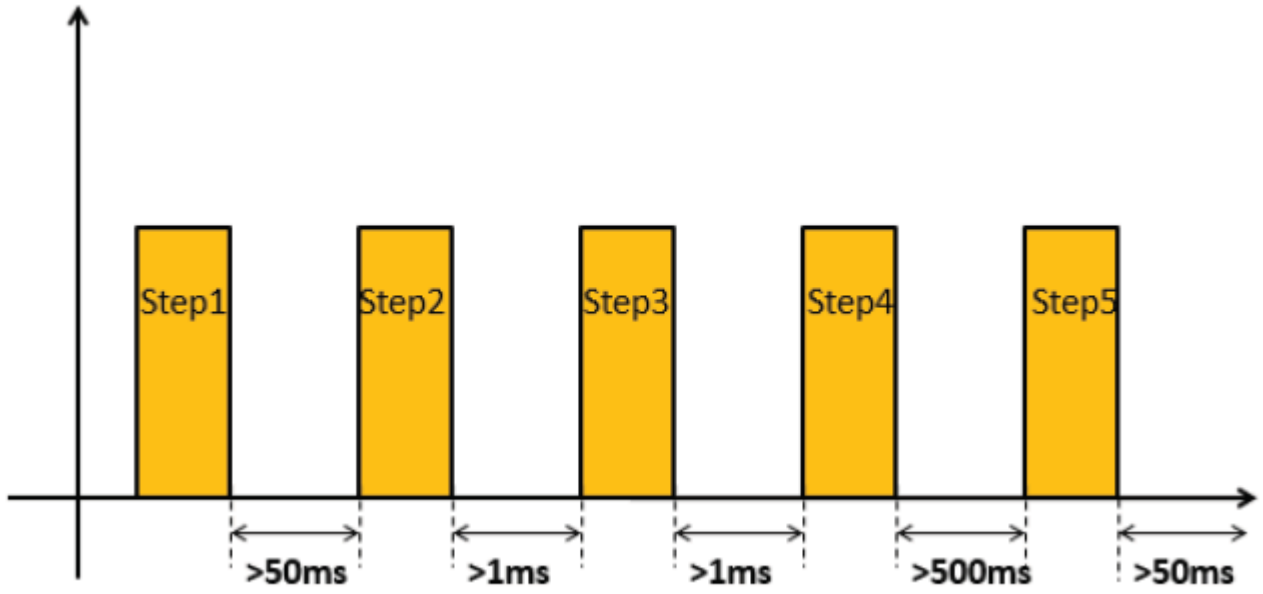
Step5 Reset

*Device Address is 0x74 or 0x75(7Bits)

S	Slave Address	W	A	Index Address 0	A	Control Byte	A	P
	1 1 1 0 1 0 0 0 0xE8 Device Address + W			0 0 0 0 0 0 0 0 0x00 Control Address		0 0 0 1 0 0 1 0 0x12 Reset + OUT_EN		

3.6 Interval of step to step

Step to step interval must follow below figure



4.0 INTERFACE CONNECTION

4.1 Open Cell Input Signal & Power

< Table 7. Open Cell Input Connector Pin Configuration >

Pin No	Symbol	Description	Pin No	Symbol	Description
1	NC	No Connection	21	GND	Ground
2	SDA	I²C Data	22	CH1[3]-	First pixel negative LVDS differential data input. Pair3
3	SCL	I²C Clock	23	CH1[3]+	First pixel positive LVDS differential data input. Pair3
4	NC	Not Connected	24	NC	Not Connected
5	NC	Not Connected	25	NC	Not Connected
6	NC	Not Connected	26	NC or GND	Not Connected
7	SELLVDS	Only Support VESA	27	NC	Not Connected
8	NC	Not Connected	28	CH2[0]-	Second pixel negative LVDS differential data input. Pair0
9	NC	Not Connected	29	CH2[0]+	Second pixel positive LVDS differential data input. Pair0
10	NC	Not Connected	30	CH2[1]-	Second pixel negative LVDS differential data input. Pair1
11	GND	Ground	31	CH2[1]+	Second pixel positive LVDS differential data input. Pair1
12	CH1[0]-	First pixel negative LVDS differential data input. Pair0	32	CH2[2]-	Second pixel negative LVDS differential data input. Pair2
13	CH1[0]+	First pixel positive LVDS differential data input. Pair0	33	CH2[2]+	Second pixel positive LVDS differential data input. Pair2
14	CH1[1]-	First pixel negative LVDS differential data input. Pair1	34	GND	Ground
15	CH1[1]+	First pixel positive LVDS differential data input. Pair1	35	CH2CLK-	Second pixel negative LVDS clock
16	CH1[2]-	First pixel negative LVDS differential data input. Pair2	36	CH2CLK+	Second pixel positive LVDS clock
17	CH1[2]+	First pixel positive LVDS differential data input. Pair2	37	GND	Ground
18	GND	Ground	38	CH2[3]-	Second pixel negative LVDS differential data input. Pair3
19	CH1CLK-	First pixel negative LVDS clock	39	CH2[3]+	Second pixel positive LVDS differential data input. Pair3
20	CH1CLK+	First pixel positive LVDS clock			

Pin No	Symbol	Description	Pin No	Symbol	Description
40	NC	Not Connected	46	GND	Ground
41	NC	Not Connected	47	NC	Not Connected
42	NC or GND	Not Connected	48	VCC	Input Voltage +12V
43	NC or GND	Not Connected	49	VCC	Input Voltage +12V
44	NC or GND	Ground	50	VCC	Input Voltage +12V
45	GND	Ground	51	VCC	Input Voltage +12V

Notes : 1. NC(Not Connected) : This pins are only used for BOE internal operations.
2. Input Level of LVDS signal is based on the IEA 664 Standard.

Rear view of LCM

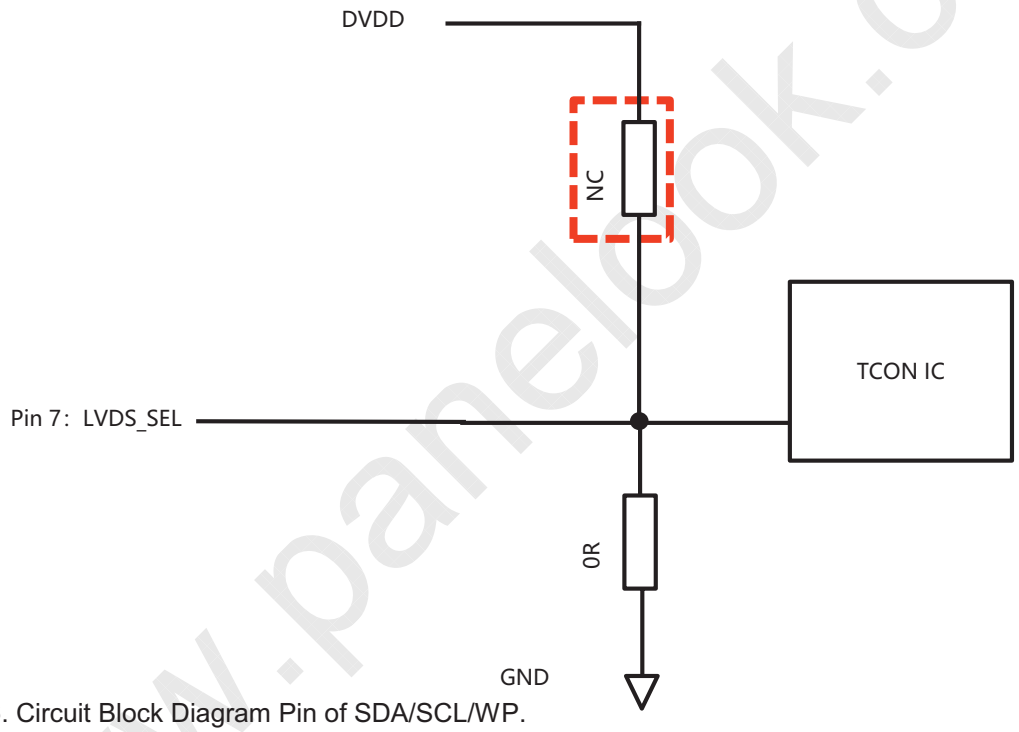
BIST Pattern

Notes : 1. NC(Not Connected) : This pins are only used for BOE internal operations.

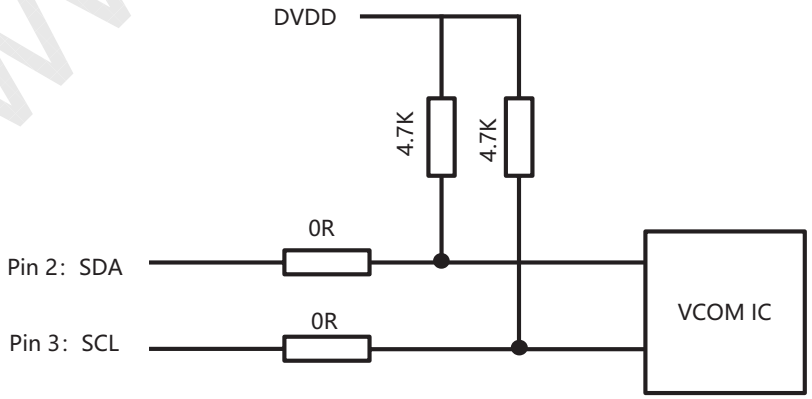
2. Input Level of LVDS signal is based on the IEA 664 Standard.

3. BIST : This pin is used for selecting display pattern mode when input DE or input CLOCK quits toggling.
   If this Pin : Low (GND) or Open (NC) → Free run mode(Black Pattern)
   Otherwise : High(3.3V) → BIST mode(BIST Pattern)
   Sequence : On = VDD ≥LVDS Option , BIST Option ≥Interface signal
   Off = Interface signal ≥ LVDS Option , BIST Option ≥ VDD

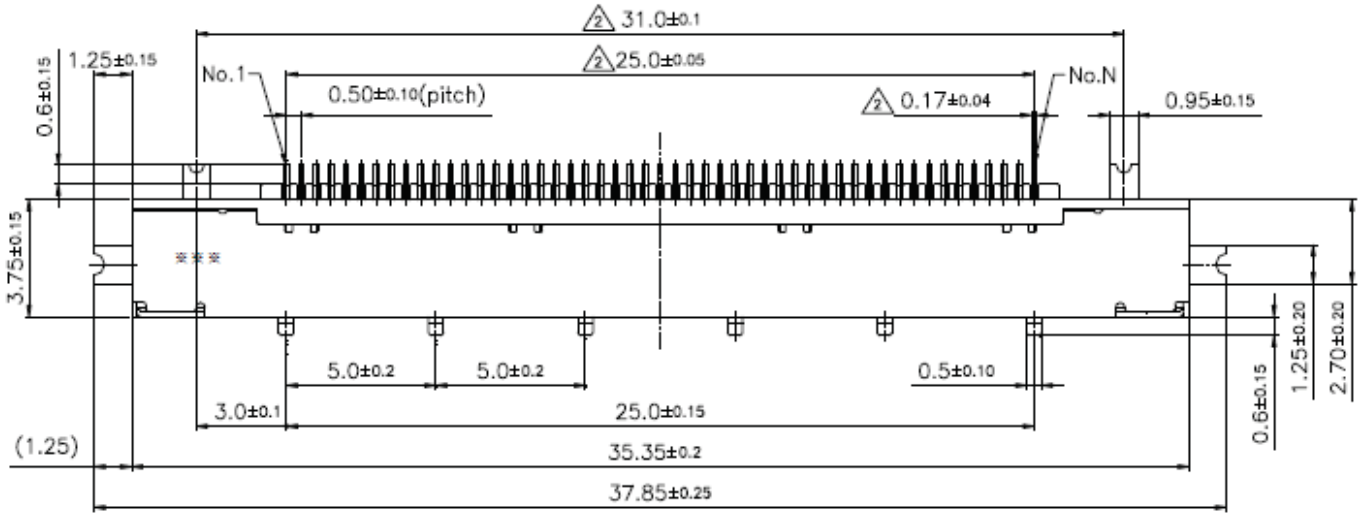
. 4 Circuit Block Diagram of LVDS_SEL.

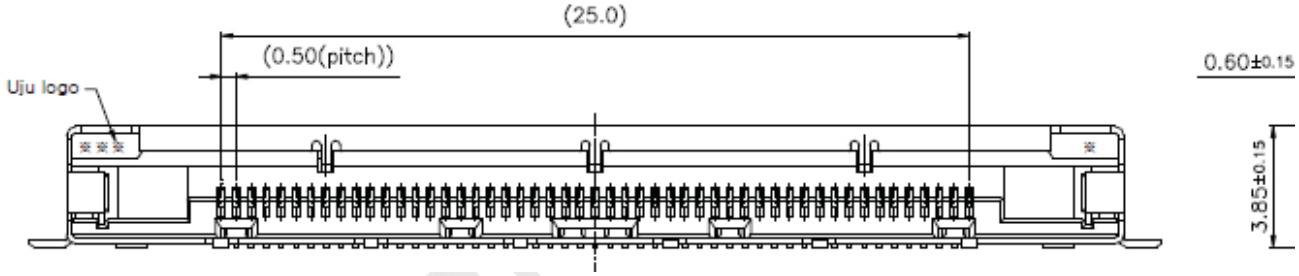


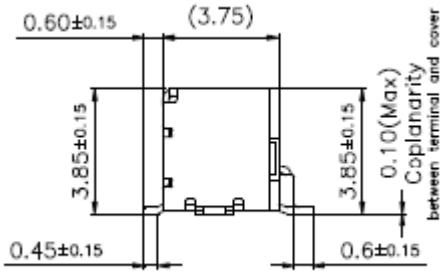
6. Circuit Block Diagram Pin of SDA/SCL/WP.



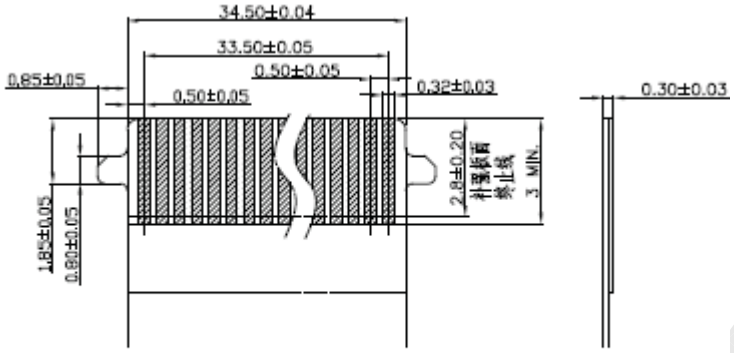
-51pin Connector: IS050-C51B-C39-S







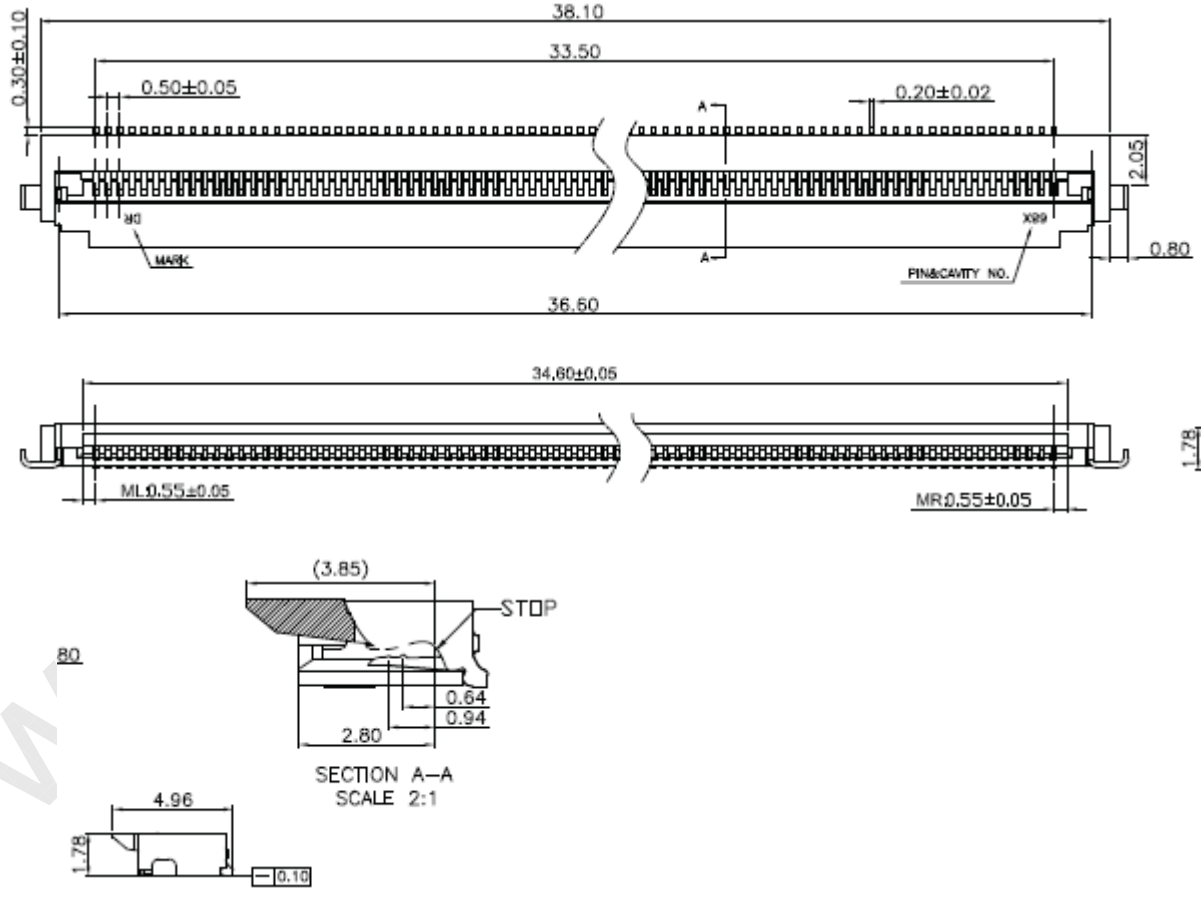
-68pin FFC



RECOMMENDED FPC/FFC DIM.
THICKNESS:0.3±0.03

Notes: This FFC drawing are supplied by the connector vendor.

-68pin Connector: CONN_40.1*4.96*1.78MM_68P_0.5MM



5.0 SIGNAL TIMING WAVEFORMS OF INTERFACE SIGNAL

5.1 LVDS Interface

<Table 9. LVDS Receiver : Timing Controller (LVDS Rx merged) / LVDS Data : Pixel Data>

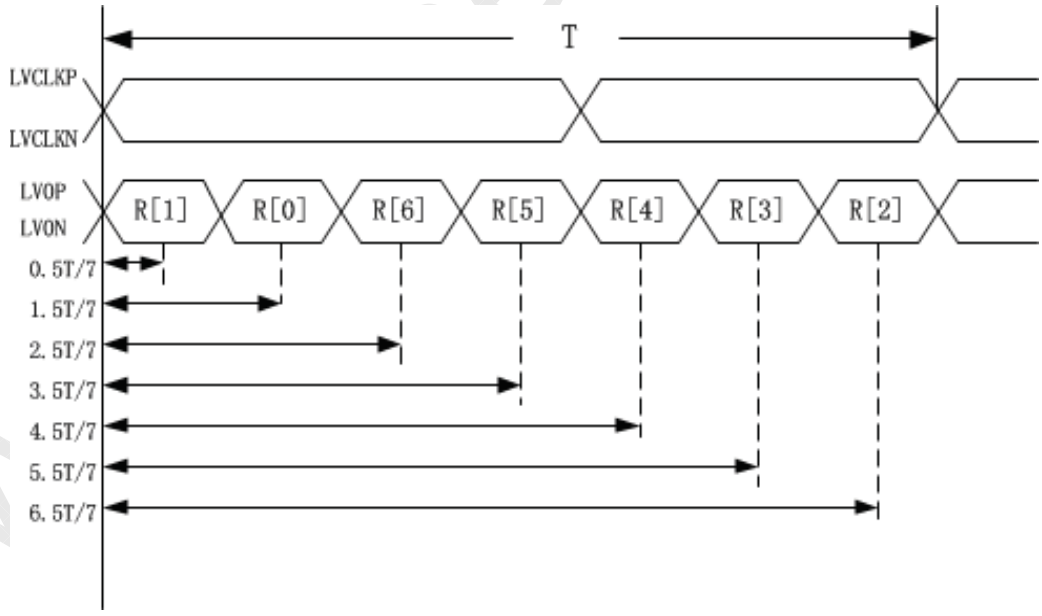
Channel No.	Data No.	8-bit LVDS Type	
		NS	JEIDA
0	Bit-0	R0	R2
	Bit-1	R1	R3
	Bit-2	R2	R4
	Bit-3	R3	R5
	Bit-4	R4	R6
	Bit-5	R5	R7
	Bit-6	G0	G2
1	Bit-0	G1	G3
	Bit-1	G2	G4
	Bit-2	G3	G5
	Bit-3	G4	G6
	Bit-4	G5	G7
	Bit-5	B0	B2
	Bit-6	B1	B3
2	Bit-0	B2	B4
	Bit-1	B3	B5
	Bit-2	B4	B6
	Bit-3	B5	B7
	Bit-4	HS	HS
	Bit-5	VS	VS
	Bit-6	DE	DE
3	Bit-0	R6	R0
	Bit-1	R7	R1
	Bit-2	G6	G0
	Bit-3	G7	G1
	Bit-4	B6	B0
	Bit-5	B7	B1
	Bit-6	-	-

5.2 LVDS Rx Interface Timing Parameter

The Specification of the LVDS Rx interface timing parameter is shown in Table10

< Table 10. LVDS Rx Interface Timing Specification >

Item	Symbol	Min	Typ	Max	Unit	Note
CLKIN Period	T	11.8	13.5	17.9	nsec	
Input Data0	tRCIP1	0.5T/7-0.4	0.5T/7	0.5T/7+0.4	nsec	
Input Data1	tRCIP0	1.5T/7-0.4	1.5T/7	1.5T/7+0.4	nsec	
Input Data2	tRCIP6	2.5T/7-0.4	2.5T/7	2.5T/7+0.4	nsec	
Input Data3	tRCIP5	3.5T/7-0.4	3.5T/7	3.5T/7+0.4	nsec	
Input Data4	tRCIP4	4.5T/7-0.4	4.5T/7	4.5T/7+0.4	nsec	
Input Data5	tRCIP3	5.5T/7-0.4	5.5T/7	5.5T/7+0.4	nsec	
Input Data6	tRCIP2	6.5T/7-0.4	6.5T/7	6.5T/7+0.4	nsec	



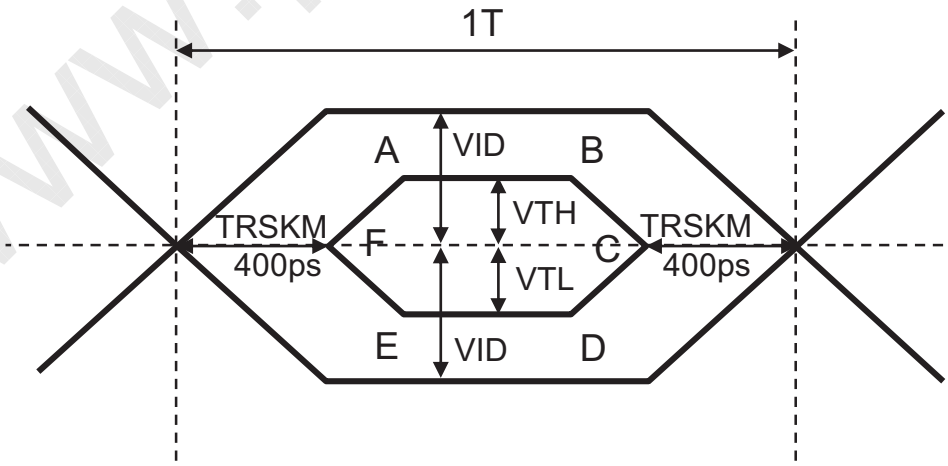
Notes: Input frequency range from 25MHz to 110MHz

5.3 LVDS Rx Interface Eye Diagram & DC SPEC

< Table 11. LVDS DC Specification>

Symbol	Min	Typ	Max	Unit	Remark
A	100	-	-	mV	
B	100	-	-	mV	
C	0	-	-	mV	
D	-100	-	-	mV	
E	-100	-	-	mV	
F	0	-	-	mV	
VTH	+100	-	-	mV	
VTL	-	-	-100	mV	
VID	±100	-	±600	mV	

Notes:
1. TRSKM: 600ps@65MHz, 510ps@75MHz, , 450ps@85MHz.
2. VID /VTH/VTL measure point is below timing. Vid measurement can be judge at the center of Eye.



6.0 SIGNAL TIMING SPECIFICATION

6.1 Timing Parameters

< Table 12. Timing Table >

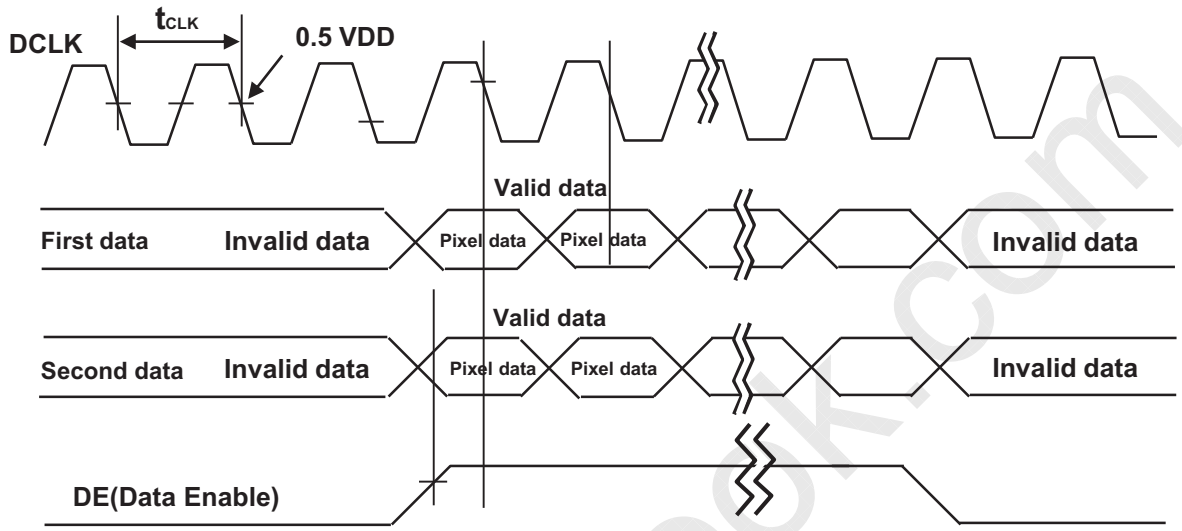
Item		Symbols		Min	Typ	Max	Unit
Clock	Frequency	1/Tc		58	74.25(92.8)	96.8	MHz
	High Time	Tch		-	4/7Tc	-	
	Low Time	Tcl		-	4/7Tc	-	
Frame Period		Tv		1100	1125	1300	lines
				47	60(75)	78	Hz
Horizontal Active Display Term		Valid	t_{HV}	-	960	-	t_{CLK}
		Total	t_{HP}	1060	1100	1200	t_{CLK}
Vertical Active Display Term		Valid	t_{VV}	-	1080	-	t_{HP}
		Total	t_{VP}	1100	1125	1300	t_{HP}

Notes: This product is DE only mode. The input of Hsync & Vsync signal does not have an effect on normal operation.

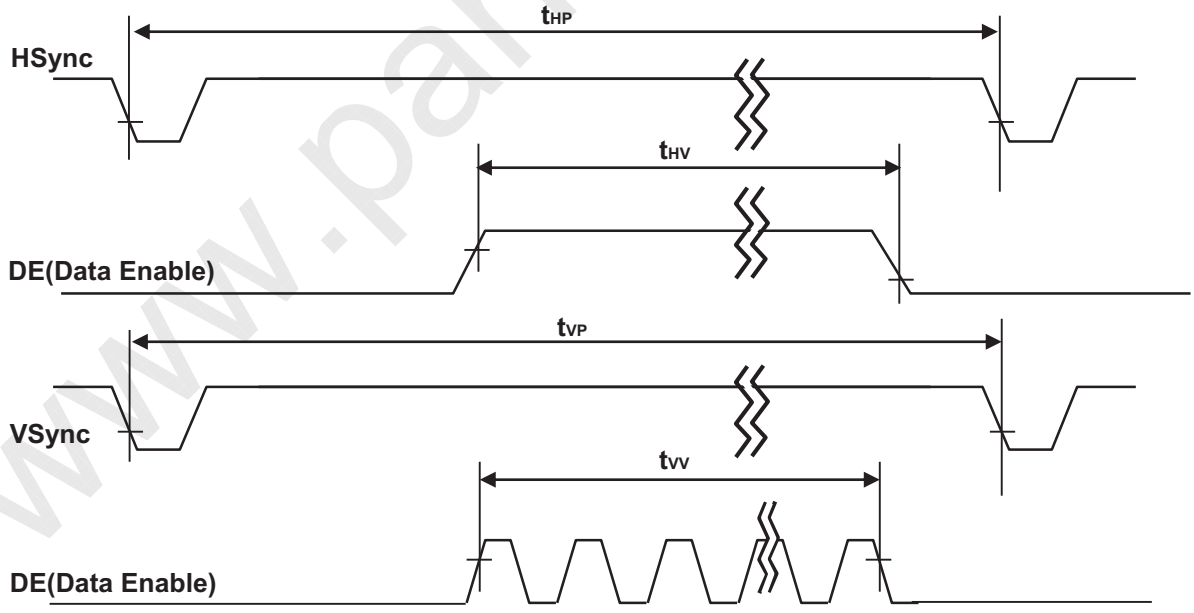
< Table 13. LVDS Input SSCG>

Symbol	Parameter	Condition	Min	Typ	Max	Unit
F	LVDS Input frequency	-	58	74.25 (92.8)	97	MHz
T_{LVSK}	LVDS channel to channel skew	F=100MHz V_{IC}=1.2V V_{ID}=±200mV	-(1/F)*30%	-	(1/F)*30%	ps
F_{LVMOD}	Modulating frequency of input clock during SSC	F=85MHz V_{IC}=1.2V V_{ID}=±200mV	0	-	200	KHz
F_{LVDEV}	Maximum deviation of input clock frequency during SSC		-3	-	+3	%
T_{CY-CY}	Cycle to Cycle jitter		-	-	50	ps

6.2 Signal Timing Waveform



Notes: This product is DE only mode. The input of Hsync & Vsync signal does not have an effect on normal operation.



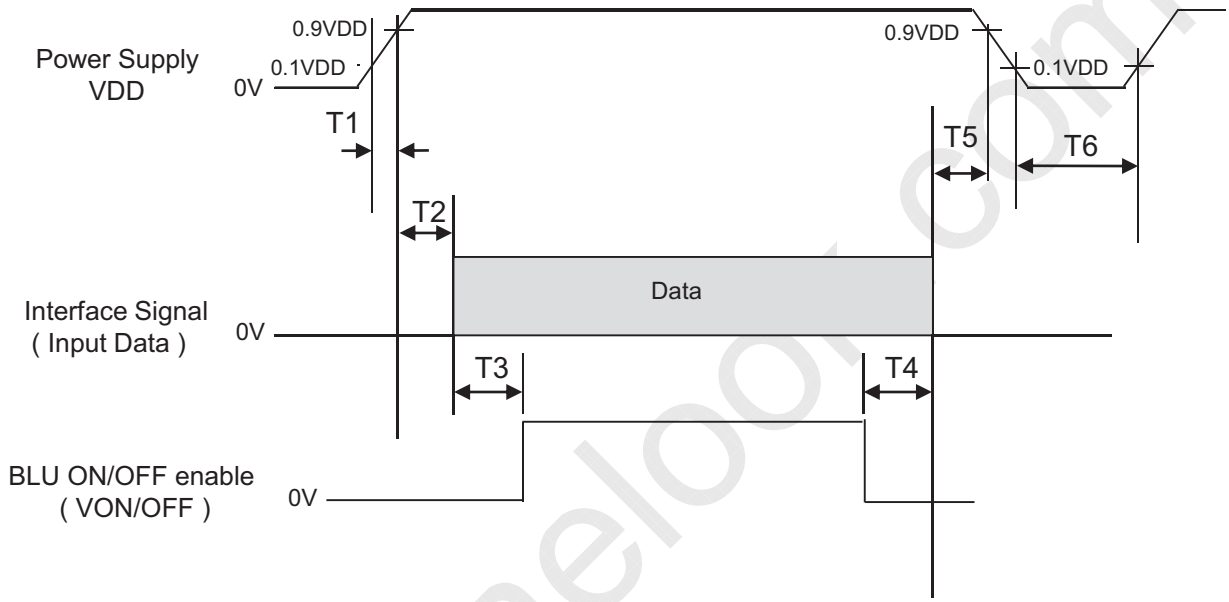
6.3 Input Signals, Basic Display Colors and Gray Scale of Colors

< Table 10. Input Signal and Display Color Table >

Color & Gray Scale		Input Data Signal																							
		Red Data								Green Data								Blue Data							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale of Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△					↑								↑								↑			
	▽					↓								↓								↓			
	Brighter	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	▽	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale of Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Darker	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	△					↑								↑								↑			
	▽					↓								↓								↓			
	Brighter	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	▽	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale of Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Darker	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	△					↑								↑								↑			
	▽					↓								↓								↓			
	Brighter	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	▽	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Gray Scale of White	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
	Darker	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0
	△					↑								↑								↑			
	▽					↓								↓								↓			
	Brighter	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1
	▽	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

6.4 Power Sequence

To prevent a latch-up or DC operation of the Open Cell, the power on/off sequence shall be as shown in below



< Table 7. Sequence Table >

Parameter	Values			Units
	Min	Typ	Max	
T1	0.5	-	20	ms
T2	10	-	50	ms
T3	250	-	-	ms
T4	100	-	-	ms
T5	0	-	50	ms
T6	1	-	-	s

Notes: 1. Even though T1 is over the specified value, there is no problem if I2T spec of fuse is satisfied.
2. Back Light must be turn on after power for logic and interface signal are valid.
3. If exceed T2(max), enter to BIST mode.

7.0 OPTICAL SPECIFICATION

The test of optical specifications shall be measured in a dark room (ambient luminance≤1 lux and temperature=25±2℃) with the equipment of Luminance meter system (Goniometer system and PR730) and test unit shall be located at an approximate distance 180cm from the LCD surface at a viewing angle of θ and Φ equal to 0°. We refer to $\theta_{Ø=0}$ (=θ_3) as the 3 o'clock direction (the "right"), $\theta_{Ø=90}$ (= θ_{12}) as the 12 o'clock direction ("upward"), $\theta_{Ø=180}$ (= θ_9) as the 9 o'clock direction ("left") and $\theta_{Ø=270}$(= θ_6) as the 6 o'clock direction ("bottom"). While scanning θ and/or Ø, the center of the measuring spot on the Display surface shall stay fixed. The measurement shall be executed after 30 minutes warm-up period. VDD shall be 12.0V +/-10% at 25°C. Optimum viewing angle direction is 6 'clock.

< Table 12. Optical Table >

[VDD = 12.0V, Frame rate = 60Hz, Ta =25±2 ℃]

Parameter		Symbol	Condition	Min	Typ	Max	Unit	Remark
Viewing Angle	Horizontal	Θ_3	CR > 10		89		Deg.	-
		Θ_9			89		Deg.	
	Vertical	Θ_{12}			89		Deg.	
		Θ_6			89		Deg.	
Contrast ratio		CR		1000:1	1200:1	-		-
Reproduction of color	White	W_x	Θ = 0° (Center) Normal Viewing Angle	TYP. - 0.03	0.280	TYP. + 0.03		Based on BOE Backlight
		W_y			0.290			
	Red	R_x			0.632			
		R_y			0.346			
	Green	G_x			0.303			
		G_y			0.636			
	Blue	B_x			0.150			
		B_y			0.047			
Response Time	G to G	T_g		-	8	10	ms	-
Gamma Scale				2.0	2.2	2.4		
Cell Transmittance				4.5	5.0		%	Note 5

Note :

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface.
2. Contrast measurements shall be made at viewing angle of θ= 0° and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. (See Figure 1 shown in Appendix) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. The color chromaticity coordinates specified in Table 12.shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel. The BLU is used by BOE.

4Response time Tg is the average time required for display transition by switching the input signal as below table and is based on Frame rate fV =60Hz to optimize.
Each time in below table shall be measured by switching the input signal for "any level of gra y(bright)"and "any level of gray(dark)"

Measured Response Time		Target																
		0	15	31	47	63	79	95	111	127	143	159	175	191	207	223	239	255
Start	0																	
	15																	
	31																	
	47																	
	63																	
	79																	
	95																	
	111																	
	127																	
	143																	
	159																	
	175																	
	191																	
	207																	
	223																	
	239																	
	255																	

5. Definition of Transmittance (T%) :
Module is with white(L255) signal input

$$\text{Transmittance} = \frac{\text{Luminance of LCD Module}}{\text{Luminance of BLU}} \times 100\ \%$$

8.0 RELIABILITY TEST

The Reliability test items and its conditions are shown in below.

< Table 13. Reliability Test Parameters >

No	Test Items	Conditions
1	High temperature storage test	Ta = 60 ℃, 240 hrs
2	Low temperature storage test	Ta = -20 ℃, 240 hrs
3	High temperature & high humidity operation test	Ta = 50 ℃, 80%RH, 240hrs
4	High temperature operation test	Ta = 50 ℃, 240hrs
5	Low temperature operation test	Ta = -5 ℃, 240hrs
6	Thermal shock	Ta = -20 ℃ ↔ 60 ℃ (0.5 hr), 100 cycle

This test condition is based on BOE module.

9.0 HANDLING & CAUTIONS

(1) Cautions when taking out the Panel

- Pick the pouch only, when taking out panel from a shipping package.

(2) Cautions for handling the panel

- As the electrostatic discharges may break the LCD panel, handle the LCD panel with care. Peel a protection sheet off from the LCD panel surface as slowly as possible.
- As the LCD panel and back - light element are made from fragile glass material, impulse and pressure to the LCD panel should be avoided.
- As the surface of the polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.
- Do not pull the interface connector in or out while the LCD panel is operating.
- Put the panel display side down on a flat horizontal plane.
- Handle connectors and cables with care.

(3) Cautions for the operation

- When the panel is operating, do not lose CLK, ENAB signals. If any one of these signals is lost, the LCD panel would be damaged.
- Obey the supply voltage sequence. If wrong sequence is applied, the panel would be damaged.

(4) Cautions for the atmosphere

- Dew drop atmosphere should be avoided.
- Do not store and/or operate the LCD panel in a high temperature and/or humidity atmosphere. Storage in an electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.

(5) Cautions for the panel characteristics

- Do not apply fixed pattern data signal to the LCD panel at product aging.
- Applying fixed pattern for a long time may cause image sticking.

9.0 HANDLING & CAUTIONS

(6) Other cautions

- In particular in winter, Before putting Panel boxes on the line, aging process is required to make the temperature of products similar to the temperature of workplace.
- Response time depends on the temperature.(In lower temperature, it becomes longer.)
- Do not disassemble and/or re-assemble LCD panel.
- Do not re-adjust variable resistor or switch etc.
- When returning the panel for repair or etc., Please pack the panel not to be broken. We recommend to use the original shipping packages.
- Product assembled into module should be stored in the bag(cover case).
- Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter causes circuit break by electro-chemical reaction.
- Be careful not to give any extra mechanical stress to the panel when designing the set, and BLU.
- Do not pull, fold or bend the source COF and the gate COF in any processes
- If the liquid crystal material leaks from the panel, this should be kept away from the eyes or mouth. If this contacts to hands, legs, or clothes, you must washed it away with soap thoroughly and see a doctor for the medical examination.

10.0 PRODUCT SERIAL NUMBER

1		2	3	4		5	6				7						
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

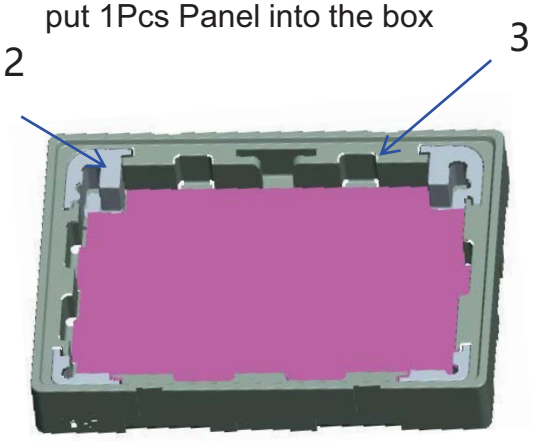
1. Control Number
2. Rank / Grade
3. Line Classification
4. Year (2011 : 11, 2012 : 12, …)
5. Month (1,2,3, … , 9, X, Y, Z)
6. Internal Use
7. Serial Number

11.0 PACKING

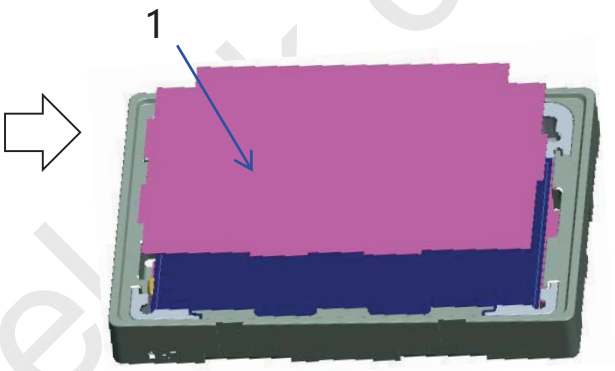
BOE provides the standard shipping container for customers, unless customer specifies their packing information. The standard packing method and Barcode information are shown in below.

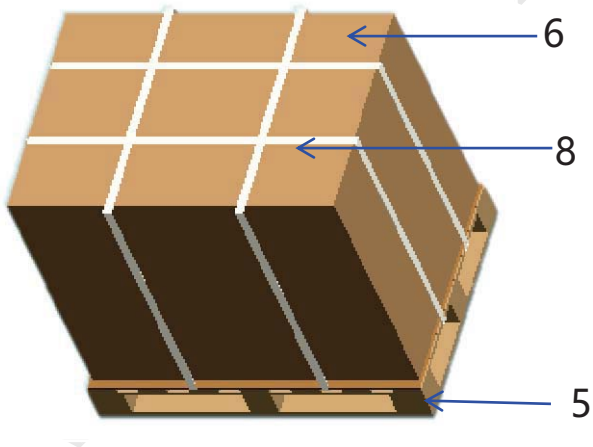
11.1 Packing Order

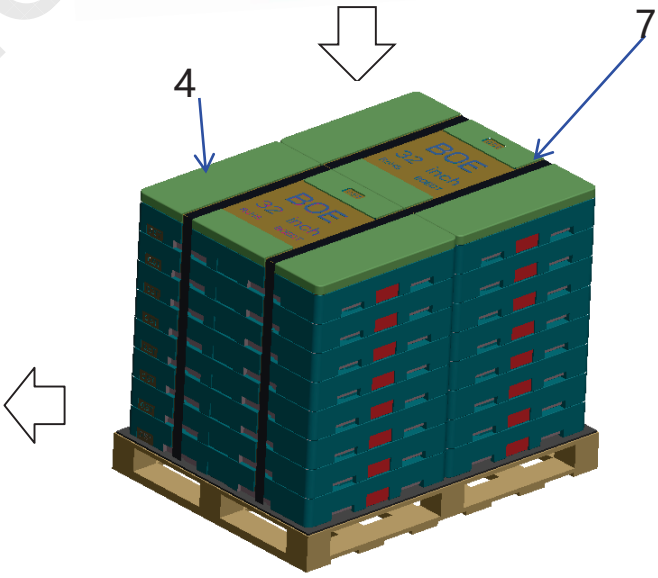
Put 1Pcs EPE Pad in the box, then put 1Pcs Panel into the box



Totally 17pcs panels and 18Pcs EPE Pad per box







Place out box and wrap film around t he boxes. Pack with 4 packing belts.

Put one paper pad on the pallet, Put totally 8 boxes and 1 cover, Pack with 2 Package belt. (8ea boxes per pallet)

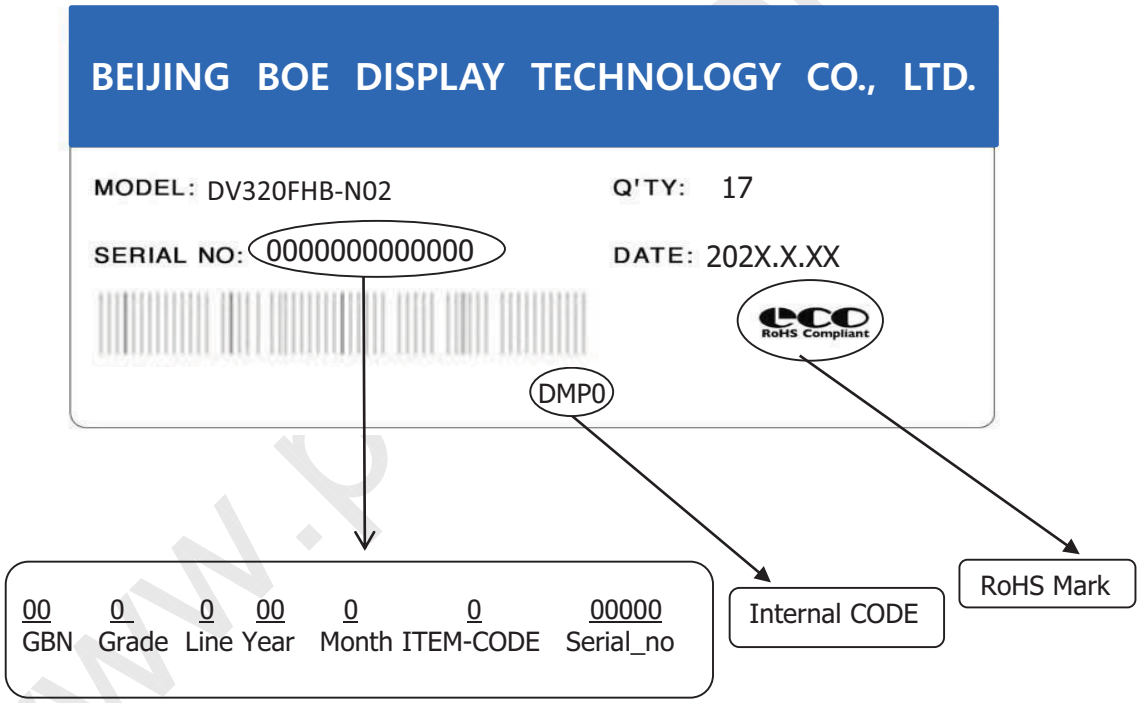
11.2 Packing Note

- Box Dimension : 860mmL×560mmW×123mmH
- Package Quantity in one Box : 17pcs

11.3 Box Label

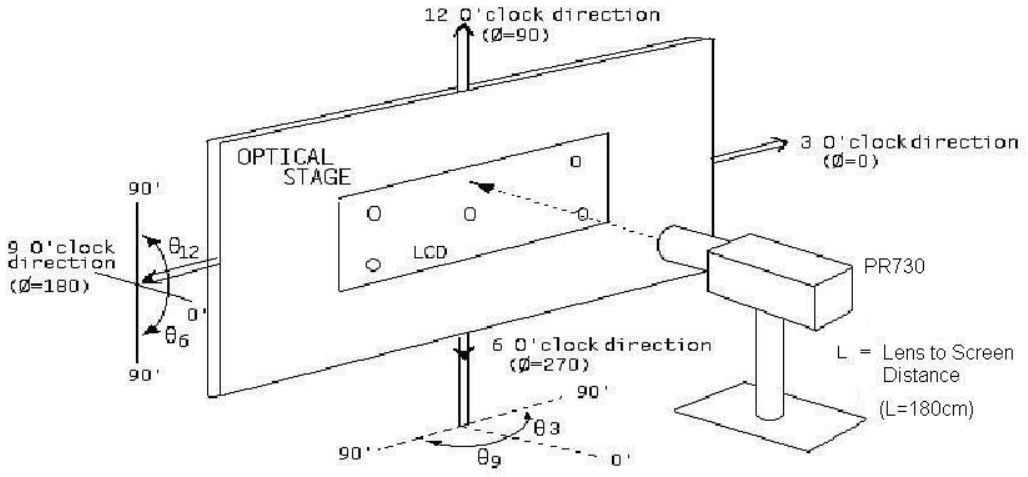
- Label Size : 110 mm (L) × 55 mm (W)
- Contents

  Model : DV320FHB-N02
  Q`ty : 17 Open Cell in one box.
  Serial No. : Box Serial No. See next page for detail description.
  Date : Packing Date
  FG Code : FG Code of Product

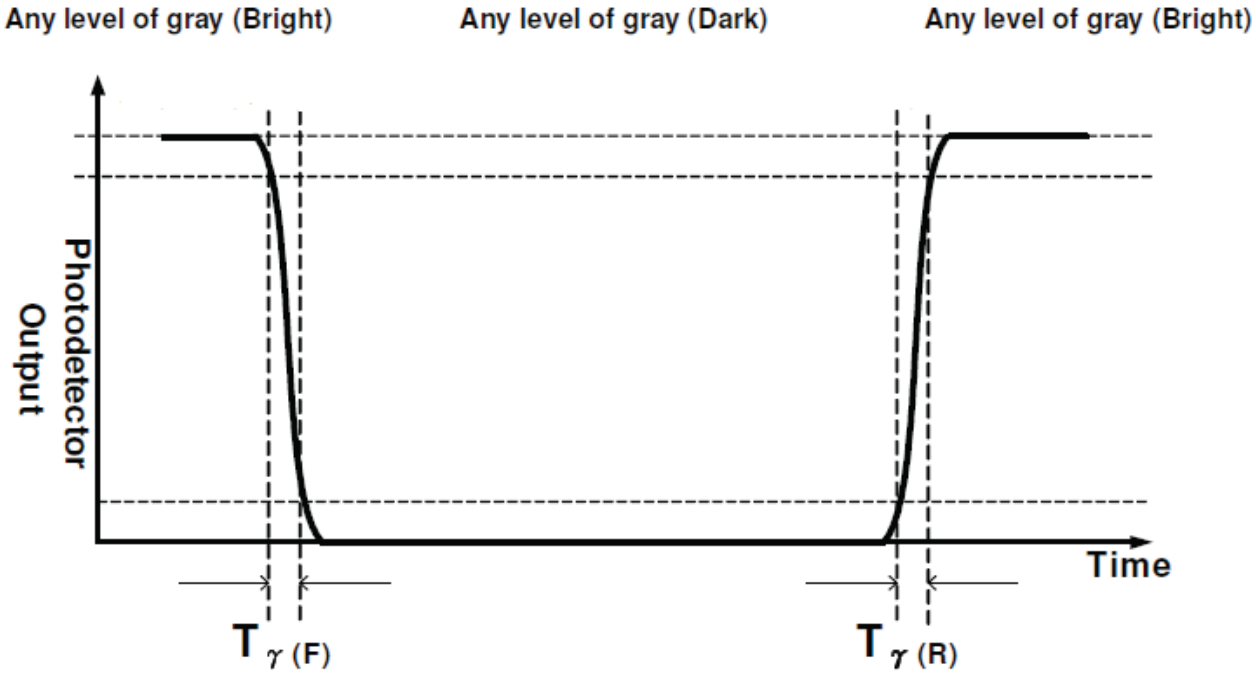


12.0 APPENDIX 1

< Figure 1. Measurement Set Up >

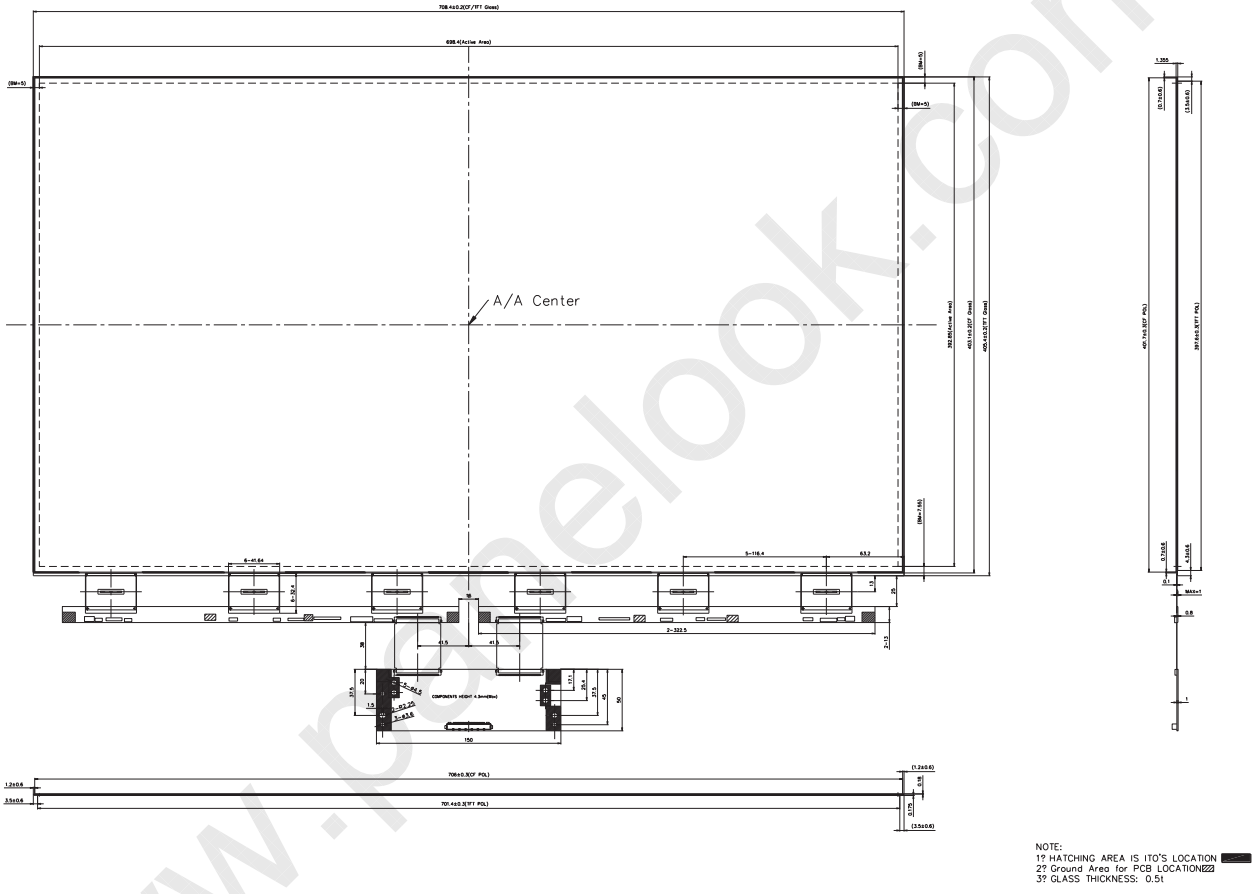


< Figure 2. Response Time Testing >



12.0 APPENDIX 2

< Figure 3. TFT-LCD Open Cell Outline Dimensions (Front View) >



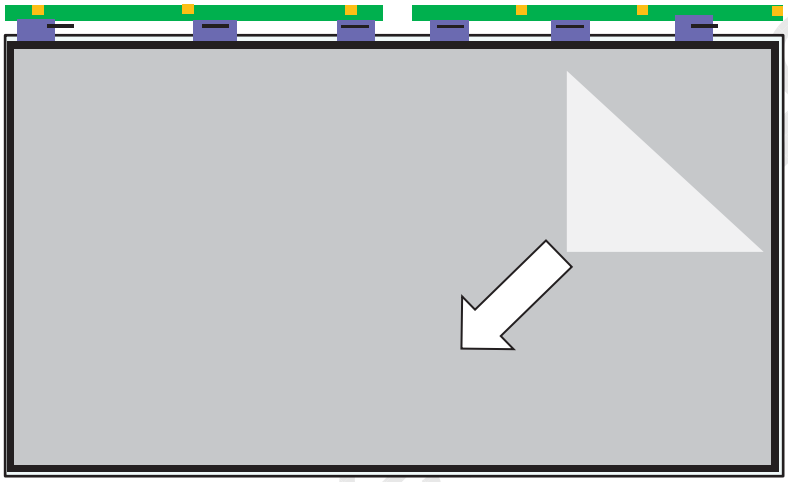
PANEL SIZE:
TFT-GLASS SIZE:708.4X405.4X0.5T
CF-GLASS SIZE:708.4X403.1X0.5T

TOLERANCE TABLE(±)

DIMENSION	1 GRADE	2 GRADE	3 GRADE	4 GRADE
L ≤ 20	0.05	0.1	0.1	0.2
20 < L ≤ 50	0.1	0.15	0.2	0.25
50 < L ≤ 100	0.15	0.2	0.25	0.3
100 < L ≤ 200	0.2	0.25	0.3	0.5
200 < L	0.25	0.3	0.5	0.8
UNLESS OTHERWISE SPECIFIED				

12.0 APPENDIX 3

< Figure 4. TFT POL Protect Film Peeling Method >

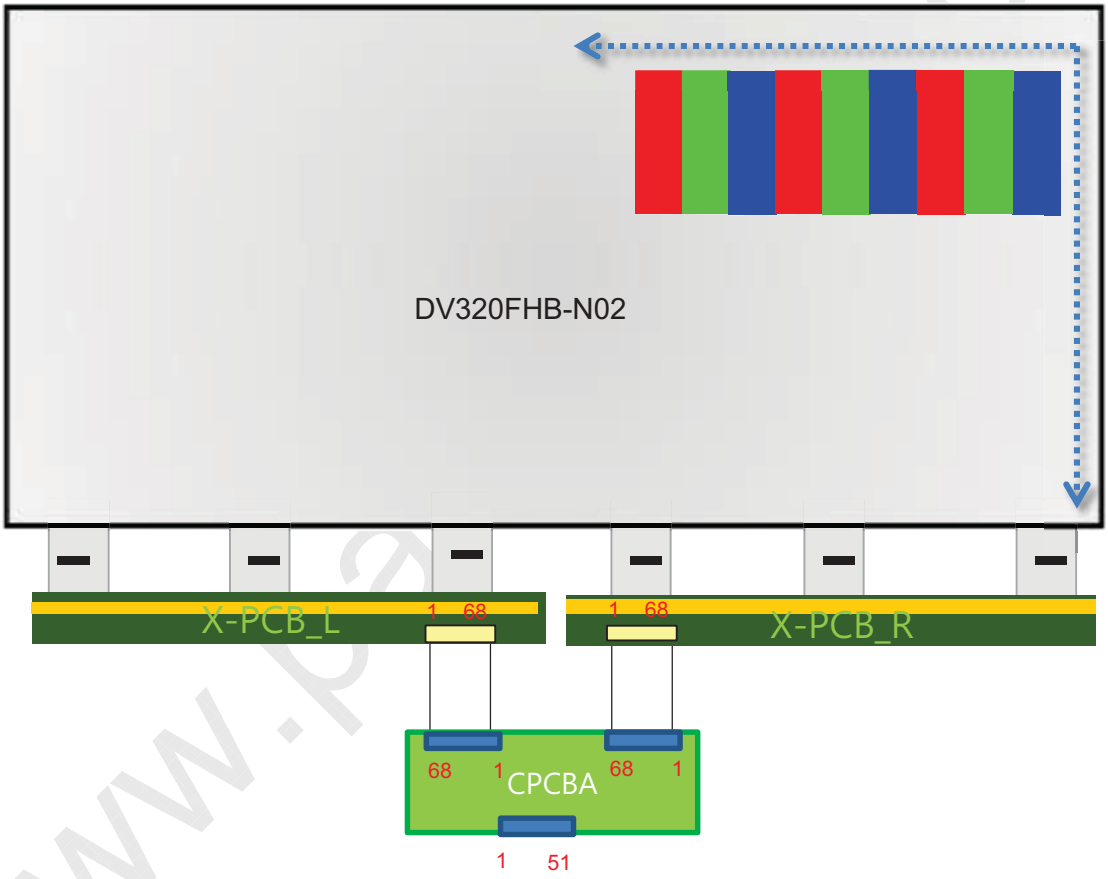


1. Be sure to peel off slowly(recommended more than 7sec) and constant speed.
2. Peeling direction shows in Figure 4.
3. Be sure to ground person with adequate methods such as the anti-static wrist band.
4. Be sure to ground each S-PCB while peeling off the protection film.
5. Ionized air should be blown over during peeling action.
6. The protection film must not touch drivers and S-PCBs.
7. If adhesive may remain on the polarizer after the protection film peeling off, please rem ove with isopropyl-alcohol.

12.0 APPENDIX 4

< Figure 5. Display Mode>

(a)This Product is Reverse type display. V by One data mapping scan direction : from left-up to right-down.



Notes : NC(Not Connected) : This pins are only used for BOE internal operations.