Product Specification

Model Name: G700FCP63.A

Description：7” (1920x 1080) AMOLED

Doc. Version：06

Customer：

Customer Part No：

□Approved for Preliminary Specification

□Approved for Final Specification

■Approved for Final Specification & Sample

Prepared	Checked	Approved
Lu Xinxin	Yongliang Zheng	Chen Sheng.

Customer’s Approval

Version History			
Version. No	Date	Contents	Remark
1	2023/8/18	First	Yan Shi
2	2024/7/4	修改 Electrical Specifications 增加 I/O connection & Block Diagram 增加 DDIC Electrical Characteristics 增加 TP Electrical Characteristics 增加 Outline Dimension Drawing	Wu Kang Liu Xiaoqing
3	2024/7/4	增加 Features IC 更新 Electrical Specifications 增加 Mechanical Specifications Thickness (Panel)	Wu Kang Liu Xiaoqing
4	2024/7/17	增加 Packing Specification	Liu Xiaoqing
5	2024/11/1	更新 Mode Video Signal Timing	Wu Kang
6	2025/4/30	更新 I/O Connection 更新 TP Connection 更新 Outline Dimension Drawing	Yu zhou Liu Xiaoqing

Contents

1. Scope

This specification defines AMOLED display manufactured by EverDisplay Optronics (Shanghai) Co., Ltd. (hereinafter this is referred as EDO). In the event that there occurs any doubt, discrepancy, and or unspecified term in this specification therein, the party may request to other party to cooperatively discuss to find mutual satisfactory solution.

2 Features

2.1 Product Applications

Automotive

2.2 Product Features

Display color	SPR 8bit
Display format	7” (1920RGB x 1080)
Pixel arrangement	Rendering
Interface	LVDS
IC	RM69C00/S7883

2.3 Model Name:

Code	Definiation	Description
G	Suppler Name	General industry display
700	Display Size	7 inch
F	Resolution	1920 x 1080
C	Technology	LTPS/ Rendering/Glass/Glass
P	Touch technology	On Cell
6	Delivery type	FOG
3	serial number	3
A	version number	A

3. General Information

Item	Specification	Unit	Note
Active area	155.06 (H)* 87.221 (V)	mm	
Diagonal size	7	inch	
Driver Element	LTPS TFT AMOLED Display		
Display mode	AMOLED		
Display Colors	8 bit		
Number of dots	1920*1080	dots	
Pixel Arrangement	Rendering 蝶形排列		

PPI	315/239（real）		
Pixel pitch	80.76	um	
Border L/R/U/D	2.25/2.25/1.5/4	mm	

4. Absolute Maximum Rating (Electrical Specifications)

The product or its functions may subject to permanent damage if it's stressed beyond those absolute maximum ratings listed below. Exposure to absolute maximum rating conditions for extended periods may affect display module reliability.

Table4 Absolute Maximum Rating (For each AMOLED)

Item		Symbol	Min.	Typ.	Max.	Unit	Note
Storage temperature		TSTG	-40	-	90	℃	-
Panel Surface Temperature		Tsurface		-	40	℃	1
Maximum Current		Output Current			0.363	A	2
Supply Voltage	System	VCC	3.2	3.3	3.4	V	-
	Panel power	ELVSS	-5.0	-4.3	-4.0	V	-
		ELVDD	4.5	4.6	4.7	V	
TP supply Voltage	TP	TP_VDD	3.0	3.3	3.6	V	
Current	consumption	I_{VCC}		0.9	1.5	A	
Power	Panel consumption	P_{ELVSS}		2.814	3.236	W	
		P_{ELVDD}				W	
TP consumption	Current	I_{TP_VDD}	33	34	38.5	mA	

Note 1: Ambient Temperature:25℃, RH=60%, and test pattern: Color bar，without IC and bonding area

Note 2：Ambient Temperature:25℃, Maximum Current (ELVDD/ELVSS)

5. Mechanical Specifications

6. Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	159.36	159.56	159.76	mm	Panel Only
	Vertical (V)	92.521	92.721	92.921	mm	
	Thickness (Panel)	1.841	2.091	2.341	mm	
Weight			-	TBD	g	

6. Electro-Optical Specification

Test condition：25℃±3℃，65±20%RH，Dark room.

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Brightness		Normal	630	700	770	cd/m^2	(1)

			(White mode)					
			A+ area	550			cd/m^2	
			A area	200			cd/m^2	
			B area	120			cd/m^2	
Brightness Uniformity			White (G255)	75	80	-	%	(2)
Contrast Ratio			Perpendicular	100000	-	-	-	(3)
			Contrast Ratio/Viewing cone (85/85/85/85)	1000				
			Contrast Ratio at 85°C for viewing angles Θ=Φ=0°	5000				
Color of CIE Coordinate	White	x	Normal Θ=Φ=0°	0.303	0.313	0.323	-	Reference data, actual typ. data needs measurements
		y		0.319	0.329	0.339	-	
	Red	x		0.666	0.686	0.706	-	
		y		0.293	0.313	0.333	-	
	Green	x		0.20	0.24	0.28	-	
		y		0.69	0.73	0.77	-	
	Blue	x		0.116	0.136	0.156	-	
		y		0.024	0.044	0.064	-	
Color Gamut			NTSC	100	105	-	%	(4)
Gamma			Normal Θ=Φ=0°@ 25 °C	2.0	2.2	2.4	-	(5)
Response time			@25° C		3		ms	Reference data, actual data needs measurement (6)
			@-20/-30°C		4		ms	
White Color Shift Δu'v'			θh=30°,θv=0°			5.5	JNCD	(7)
Flicker			Normal Θ=Φ=0°			-30	dB	(8)
AMOLED Surface reflection (SCI)			Only OLED with HC surface treatment			5.5	%	

Crosstalk	Normal Θ=Φ=0°			3	%	(9)
OLED Life Time	T80 @ 25℃	10,000	-	-	Hrs	(10)
	T80 @ 85℃ (w/ 50% De-rating)	1000			Hrs	

Note 1: Brightness

Environmental conditions：Temp.25℃±3℃, 65±20%RH, Dark Room.

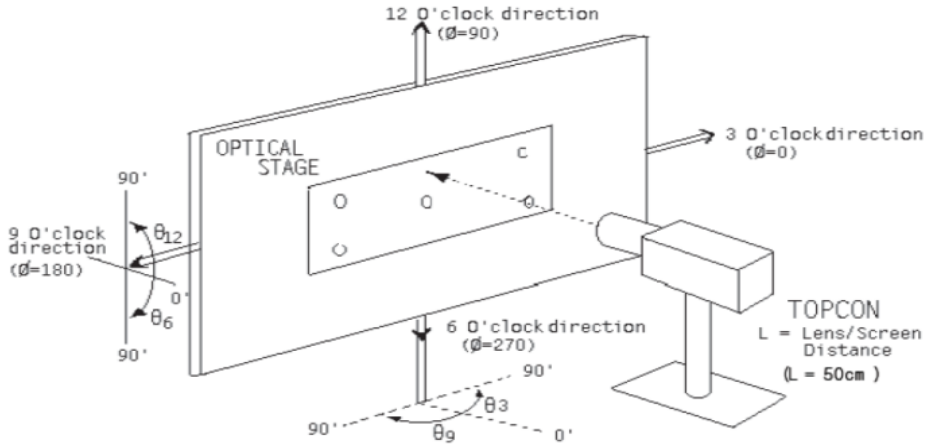
Distance of OLED display center to measuring machine is 50cm.

Test 32pcs manually；

Equipment：CS2000A

Method：Turn the machine around H direction, and measure the brightness of the middle of the panel.

A+ area (H=13°)/ A area (H=44°)/ B area (H=53°)



Note 2: Brightness uniformity

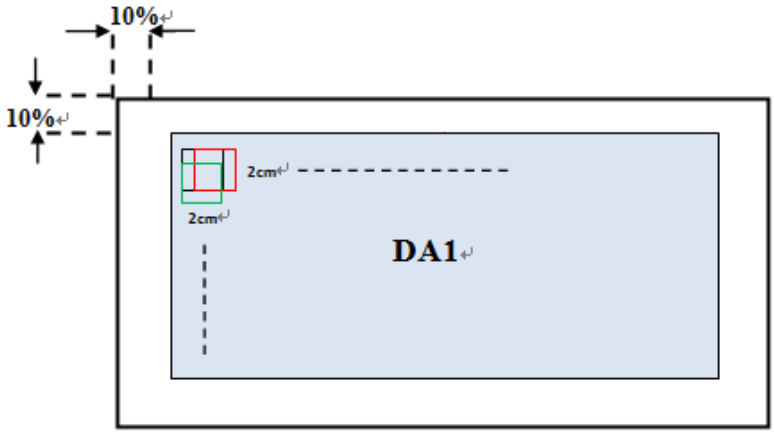
For brightness uniformity measure, EDO's request as below:

1. The test condition is at 25℃ and measured on the surface of Display panel module.
2. Measurement equipment: HYC E2000-12MEDO-SHHH or similar equipment.
3. The brightness uniformity is calculated by using following formula:

   Brightness Uniformity = Bp (Min.) / Bp (Max.)×100 (%)

   Bp (Max.) = Maximum brightness in display area DA1.

   Bp (Min.) = Minimum brightness in display area DA1.



Note 3: Contrast Ratio

Dark Room C.R=LW/LB

LW: full white brightness of display center P0;

LB: full black brightness of display center P0.

Note 4: Color Gamut

EDO's request as below:

1. Measurement equipment: CS2000A or similar equipment.
2. The color gamut is calculated by using following formula:

   Color Gamut % = $S_{coverage}$ / $S_{original\ color\ gamut}$

   $S_{coverage}$: The triangle area of the panel color gamut

   $S_{original\ color\ gamut}$: The triangle area of NTSC color gamut

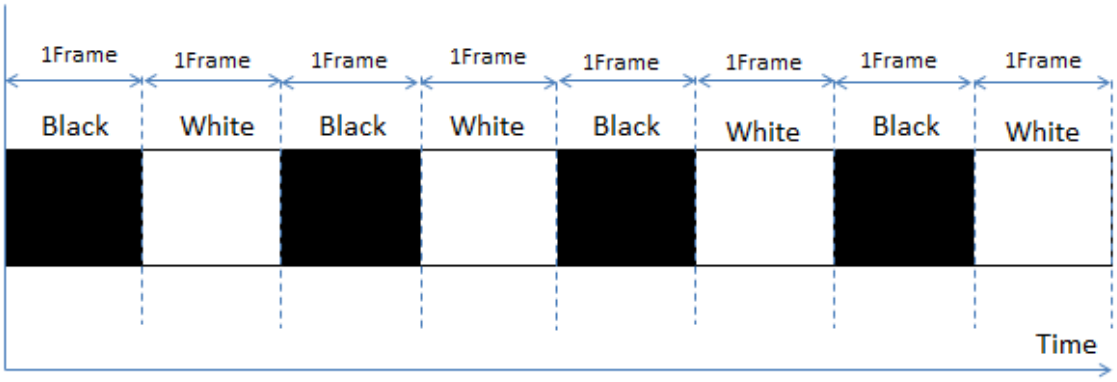
Note 5: Gamma

For gamma curve control, EDO's request as below:

1. Calibration the test instrument. Set the screen size parameters, and measure the center point.
2. EDO will test gray 16~gray240
3. Output the measure data. Data number normalization and draw the chart.
4. The whole screen should be complied with the gamma curve of gamma 2.0 or 2.4, it means +/-0.2 error is allowed. But if there are special requirements for the special project, its required specifications can be used as a standard value, please refer the project spec.

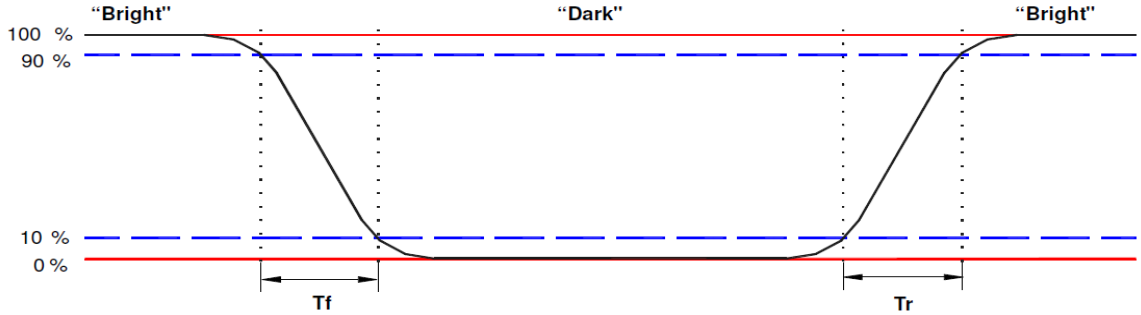
Note 6: Response Time

Response time=Pixel turn on and turn off time (White<=>Black).



Environmental conditions：Temp. 25℃、-20℃、-30℃

It is measuring transition time from 10% to 90% of luminance with single frame pattern.



Response time = Tf+Tr

Note 7: Color Shift

For color shift measure:

Fix on white pattern,

On the condition θh=0 θv=0°, we can get the color coordinate (u_1', v_1') and on θh=30° θv=0° we can get another color coordinate (u_2', v_2')

Delta = Square Root((u_2'-u_1')^2 + (v_2'-v_1')^2)

JNCD stands for "Just Noticeable Color Difference"

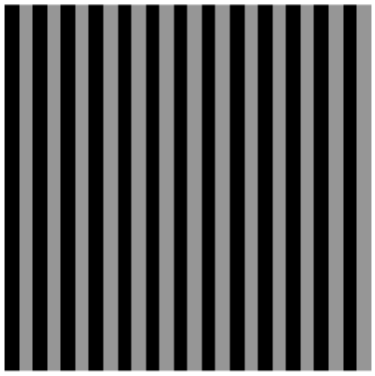
For the (u', v') color space 1 JNCD=0.0040

6 JNCD means Delta u'v'<0.0240.

This Requirement is from our customer and we have test some of our phone display and the result is OK.

Note 8: Flicker

Suggested Instruments: **Konica Minolta CA-310 or similar instrument**



Odd row : **L0** Black
Even row : **L186** gray level

Flicker Test Pattern

The flicker level is defined by **Fast Fourier Transformation (FTT)** as follows:

$$Flic\ker = 20\log_{10}\left(2\frac{f_{FFTC}(n)}{f_{FFTC}(0)}\right) + FS(Hz) \quad \text{(dB)}$$

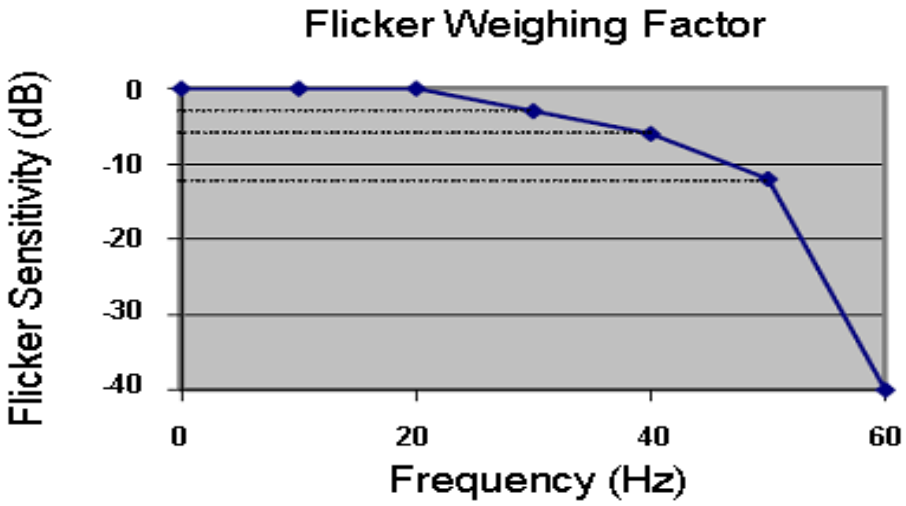
Where

$f_{FFTC}(n)$ is the n-th FFT coefficient.

$f_{FFTC}(0)$ is the 0-th FFT coefficient which is DC component.

FS(Hz) is the flicker sensitivity as a function of frequency.

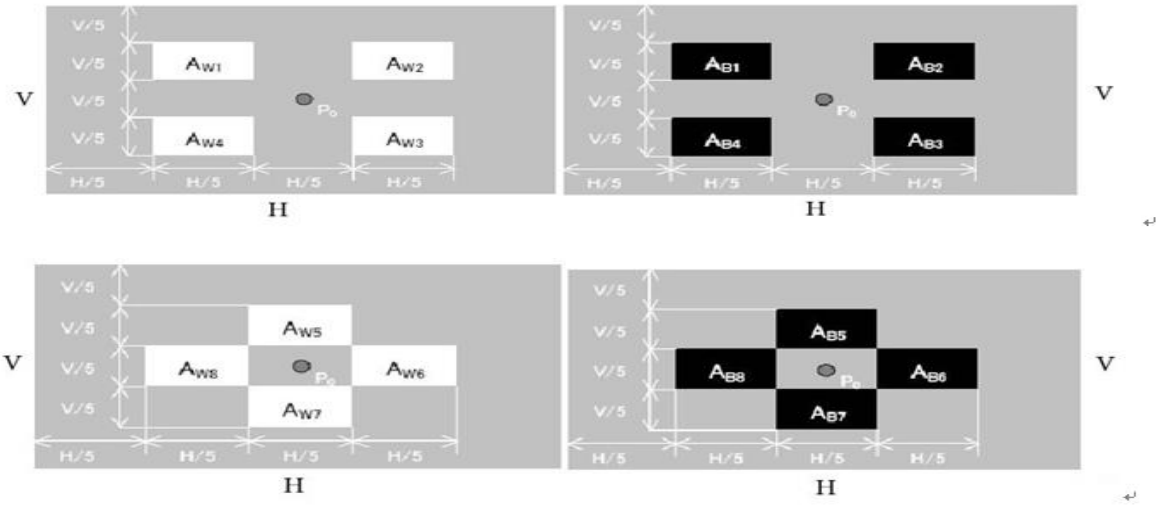
The peak flicker level shall be reported based on the calculation using above formula in which FS(Hz) is determined by the flicker weighing factor shown below.



Note 9: Crosstalk

For crosstalk measure, EDO's request as below:

1. 4% black or white window ， 127 gray background.



2. Calibrate the test instrument.

$$L_{W\_OFF} = \frac{L_{w1} + L_{w2} + L_{w3} + L_{w4}}{4}$$

$$L_{B\_OFF} = \frac{L_{B1} + L_{B2} + L_{B3} + L_{B4}}{4}$$

$$CT = \frac{|L_{Wi\_ON} - L_{W\_OFF}|}{L_{W\_OFF}} \times 100\% (i = 5\ to\ 8)$$

For white windows AWi (i = 5 to 8), and

$$CT = \frac{|L_{Bi\_ON} - L_{B\_OFF}|}{L_{B\_OFF}} \times 100\% (i = 5 \text{ to } 8)$$

For black windows ABi (i = 5 to 8).

The maximum cross-talk value shall be noted in the measurement report.

Note 10: OLED Life Time

The test procedure is as follows:

At room temperature(25℃), light the module with typical value brightness(Full white). After that, record the brightness of center point every 24 hours. Then test 600 hours or more to collect the raw data. Finally, use the raw data and the specific formulas to calculate and estimate the T80.

1. Test Temp.：85˚C；
2. Test Time：1000h
3. Method： 500h/check

(1000hrs T80@85℃, w/ 50% De-rating，change pattern)

7. I/O connection & Block Diagram

a) I/O Connection

No	Name	I/O	Description	备注
1	TEST1	I/O	CN or FPC state check	3.3V
2	NC			
3	ELVSS	P	ELVSS(Min:-5V,Typ:-4.3V,Max：-4.0V)	
4	ELVSS	P	ELVSS(Min:-5V,Typ:-4.3V,Max：-4.0V)	
5	ELVSS	P	ELVSS(Min:-5V,Typ:-4.3V,Max：-4.0V)	
6	ELVSS	P	ELVSS(Min:-5V,Typ:-4.3V,Max：-4.0V)	
7	NC1			
8	ELVDD	P	ELVDD(Min:4.5V,Typ:4.6V,Max：4.7V)	
9	ELVDD	P	ELVDD(Min:4.5V,Typ:4.6V,Max：4.7V)	
10	ELVDD	P	ELVDD(Min:4.5V,Typ:4.6V,Max：4.7V)	
11	ELVDD	P	ELVDD(Min:4.5V,Typ:4.6V,Max：4.7V)	
12	NC			
13	VCI	P	VCI(Min:3.2,Typ:3.3,Max:3.4V)	
14	VCI	P	VCI(Min:3.2,Typ:3.3,Max:3.4V)	
15	VCI	P	VCI(Min:3.2,Typ:3.3,Max:3.4V)	
16	Flash_IO1	I/O	QSPI IO IO1(如果不使用请拉低）	
17	Flash_IO0	I/O	QSPI IO IO0(如果不使用请拉低）	
18	Flash_CS	I/O	QSPI IO CS（如果不使用请拉高）	
19	Flash_SCLK	I/O	QSPI IO CLK(如果不使用请拉低）	
20	PM_EN	I/O	PMIC enable （PM_EN=1,打开 AVDD、VDDI、DVDD、Reset 上电时序电压) PM_EN=0,进入下电模式，关闭所有电压）	3.3V
21	QSPI_M	I/O	QSPI 模式选择 PIN (QSPI_M 拉高，后续透过 debug QSPI 路径的 TEST[7:2]读写： Flash QSPI_M 拉低，RM69C00 透过 Flash QSPI 路径的 Flash_IO 读写 Flash)	3.3V
22	GND		Ground	
23	ED3P	I	LVDS Even signal 3+	
24	ED3N	I	LVDS Even signal 3-	
25	GND		Ground	
26	ECLKP	I	LVDS Even signal C+	
27	ECLKN	I	LVDS Even signal C-	
28	GND		Ground	
29	ED2P	I	LVDS Even signal 2+	
30	ED2N	I	LVDS Even signal 2-	
31	GND		Ground	
32	ED1P	I	LVDS Even signal 1+	
33	ED1N	I	LVDS Even signal 1-	
34	GND		Ground	

35	ED0P	I	LVDS Even signal 0+	
36	ED0N	I	LVDS Even signal 0-	
37	GND		Ground	
38	OD3P	I	LVDS Odd signal 3+	
39	OD3N	I	LVDS Odd signal 3-	
40	GND		Ground	
41	OCLKP	I	LVDS Odd signal C+	
42	OCLKN	I	LVDS Odd signal C-	
43	GND		Ground	
44	OD2P	I	LVDS Odd signal 2+	
45	OD2N	I	LVDS Odd signal 2-	
46	GND		Ground	
47	OD1P	I	LVDS Odd signal 1+	
48	OD1N	I	LVDS Odd signal 1-	
49	GND13		Ground	
50	OD0P	I	LVDS Odd signal 0+	
51	OD0N	I	LVDS Odd signal 0-	
52	GND		Ground	
53	SDA	I/O	I2C interface	
54	SCL	I	I2C interface	
55	RESX	I	RSET DDIC (用于复位 Driver IC)	1.8V
56	VPP	P	OTP Power (不用时请 NC)	6V
57	GPO_0	O	TE（用于测试刷新频率）	
58	ERR0	O	Fail_det(安全问题错误反馈 PIN)	
59	NC			
60	TEST2	I/O	CN or FPC state check	3.3V

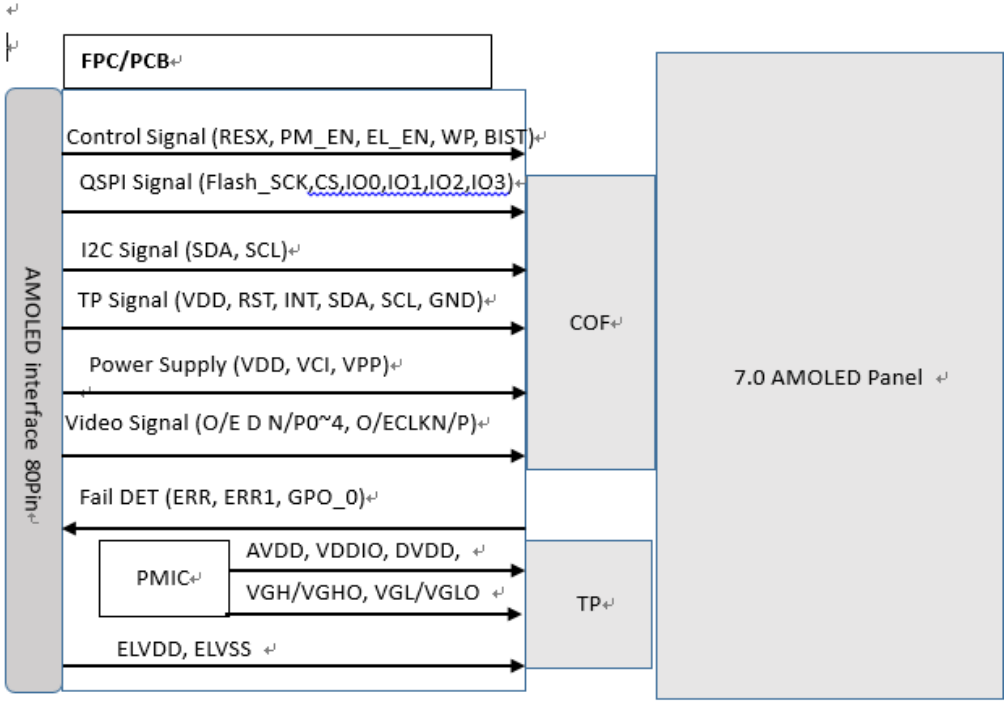
b) TP Connection

No	Name	I/0	Description	备注
1	GND		Ground	
2	TP_RESET	I	TP REST	3.3V
3	TP_INT	O	TP INT	
4	SDA	I/O	TP I2C interface(I/O 口电压为 3.3V)	Note1:
5	GND		Ground	
6	SCL	I	TP I2C interface(I/O 口电压为 3.3V)	Note1:
7	TP_VDD	P	TP_VDD(3.3V) interface	
8	TP_VDD	P	TP_VDD(3.3V) interface	
9	TP_VDD	P	TP_VDD(3.3V) interface	
10	GND		Ground	

Note1:

TP 模组中 I2C 已经上拉了。

c) Display Module Block Diagram



8. DDIC Electrical Characteristics

8.1 DC Characteristics

At Ta = 25 °C, VDDI=1.8V, GND=0V， VCI=3.3V。

Table 11: DC Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Related Pins
Analog Power Supply Voltage	VCI	Operation voltage	3.2	3.3	3.4	V	Note3
I/O pin Power Supply Voltage	VDDI	I/O supply voltage	1.65	1.8	1.95		Note2
Power supply current for Logic	I_{VDDI}	Operation current	-	TBD		mA	
Power supply current for Logic	Iv_{DD}	I/O current	-	TBD		mA	
Logic High level input voltage	VIH	VDDI = 1.65V ~ 3.6V	0.8* VDDI	-	VDDI	V	Note 1
Logic Low level input voltage	VIL	VDDI = 1.65V ~ 3.6V	0	-	0.2* VDDI	V	Note 1
Logic High level Output voltage	VOH	Iout = -1 mA	0.8* VDDI	-	VDDI	V	Note 1
Logic Low level Output voltage	VOL	Iout = +1 mA	0	-	0.2* VDDI	V	Note1
Logic High level input current	IIHD	Vin=0~VDDI=1.8 V			1	uA	Note 1

Logic Low level input current	IILD	Vin=0~VDDI=1.8 V	-1			uA	Note1

Notes:

1 Ta(ambient temperature) ranges from -40℃ to 105 ℃

2. Recommend VDDI/VDDI_FLASH=1.8V for power saving

3. VDD means VDDA, VDDL. And VSS means VSSA, VSSR, VSSL, AVSS. VDDA and VDDL should be the same input voltage level and larger than VDDI/VDDI_FLASH voltage.

Table 12: LVDS DC Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage	VDDL	Write	3.2	3.3	3.4	V
Differential Input common-mode range	VCM	VCM		1.2		V
Differential Input voltage	|VID|			400		mV

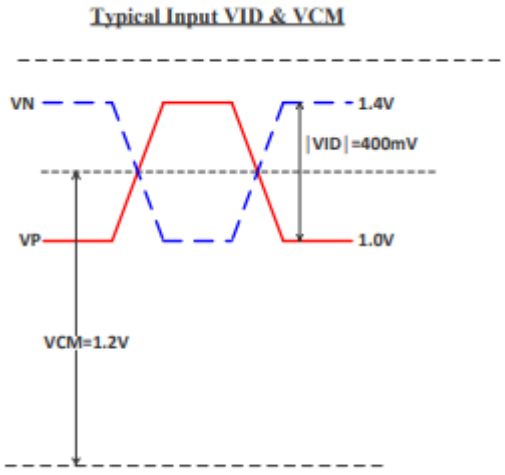


Figure 16, DC specification of LVDS input voltage levels

8.2. LVDS AC electrical characteristics

Table 13: AC characteristics of LVDS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Operation frequency	f_{LVDS}		20	-	125	MHz
1 Unit interval	UI			1/7		$1/f_{LVDS}$
D0 position	t_{RIP0}		-0.2	0	0.2	UI
D1 position	t_{RIP1}		0.8	0	1.2	UI
D2 position	t_{RIP2}		1.8	1	2.2	UI
D3 position	t_{RIP3}		2.8	2	3.2	UI
D4 position	t_{RIP4}		3.8	3	4.2	UI
D5 position	t_{RIP5}		4.8	4	5.2	UI
D6 position	t_{RIP6}		5.8	5	6.2	UI

Input data skew margin	t_{RSKM}	VID|=400mV, VCM=1.2V	0	6	0.2	UI
PLL wake-up time	t_{RPLL}			-	600	us

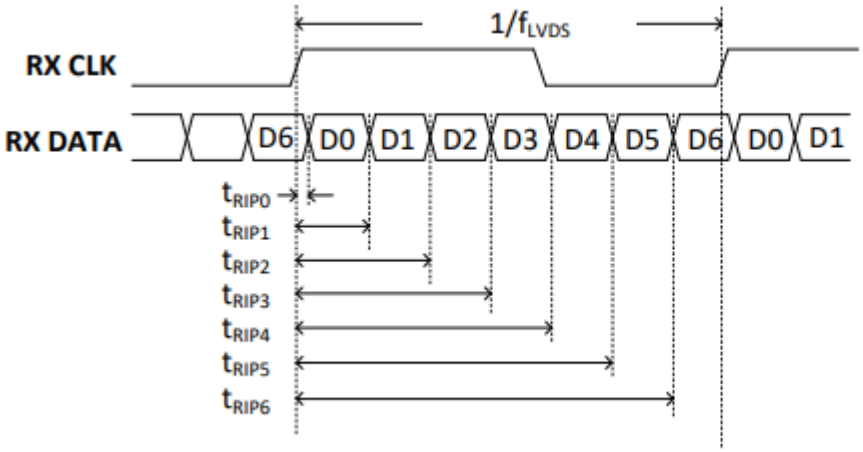


Figure 17, Timing spec for input bit stream with reference to the rising edge of RX- clock

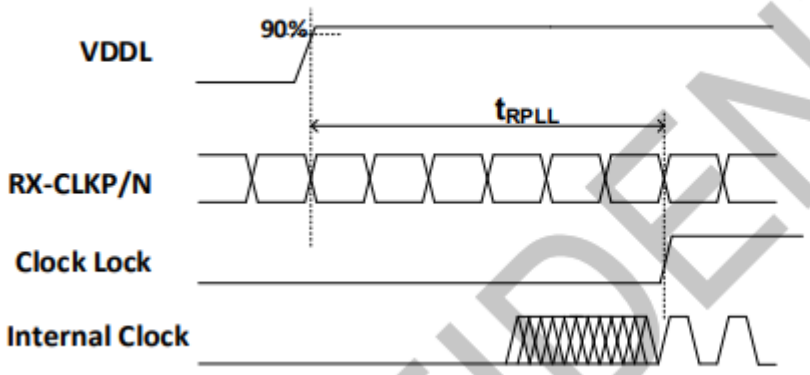


Figure 18, PLL wake-up timing

8.3 **LVDS Input Format**

➢ **4-Lane 24-bit Display Data Transmission (RGB-888)**

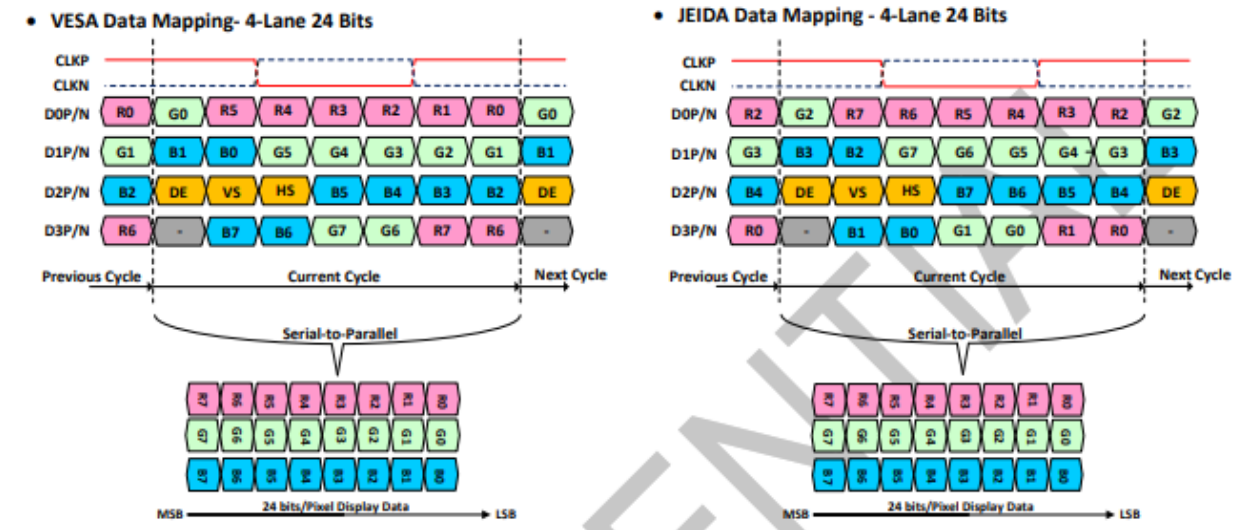


Figure 6, LVDS input data format for 4-Lane 24-bit application

8.4 **Mode Video Signal Timing**

Table14：Video-Mode Timing Parameters for 1920RGBx1080 (Two Port) – DE Mode

Symbol	Parameter	Condition(Two Port)	Min.	Typ.	Max.	Units
f_{DCLK}	DCLK Frequency	Data rate per lane is f_{DCLK}*7	70		125	MHz
HACT	Active pixels per line	1 pixel data transmission per DCLK		960		pixels
HDA	Horizontal Display Area			960		DCLK
HBP	Horizontal Back Porch			36		DCLK
HPW	Horizontal Pulse Width		1	4		
HFP	Horizontal front porch		40	40		DCLK
VDA	Vertical Display Area			1080		H
VBP	Vertical back porch	This parameter is dependent on GOA timing	16	34		H
VPW	Vertical Pulse Width		1	2		
VFP	Vertical front porch		16	36		H

➢ **LVDS DE Mode**

Under LVDS DE mode, there is no HSYNC or VSYNC information transmitted into the display module through LVDS interface. The HSYNC and VSYNC depicted in the following figure are generated internally.

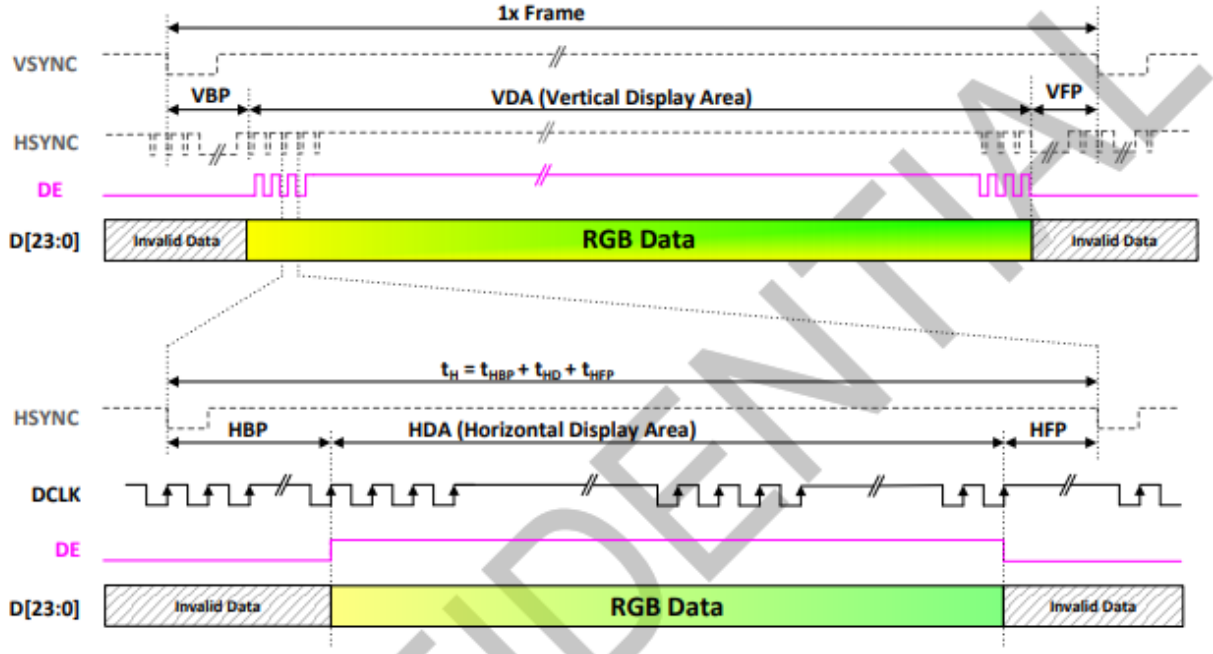


Figure 8, LVDS timing for DE mode

8.5 I2C Timing Characteristics

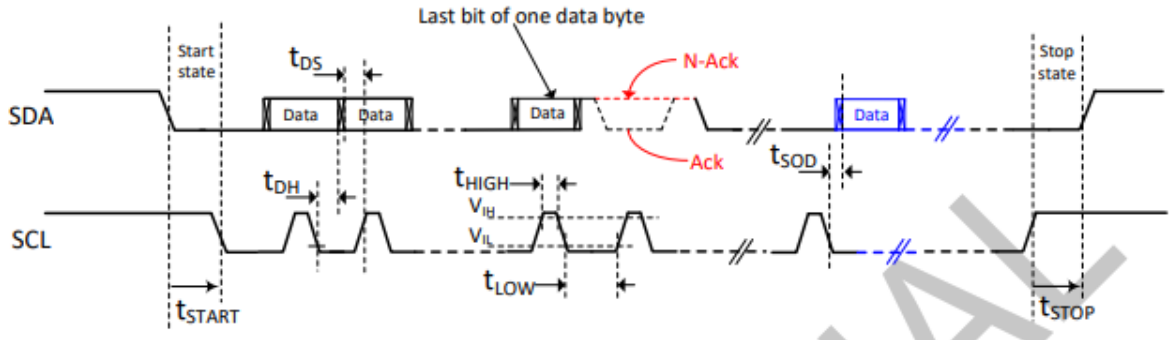


Figure 15, Illustration of I2C AC Characteristics

Table15: I2C Timing Specifications:

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
I2C SCL frequency	f_{SCL}		100		400	kHz
Start Sequence	t_{START}	SDA falling to SCL falling	0.6			us

Stop sequence	t_{STOP}	SDA rising to SDA falling	0.6			us
Low period of SCL	t_{LOW}		1.3			us
High period of SCL	t_{HIGH}		0.6			us
Data setup time	t_{DS}	To VIH of SCL's rising edge	100			ns
Data hold time	t_{DH}	From VIL of SCL's falling edge	200			ns
Access time of output data	t_{SOD}	(1) Output data is "low" (2) Output Capacitance < 15pF	15			ns
Clock rise time	$t_{R\text{-}SCL}$	0.2*VDDI -> 0.8*VDDI	2		300	ns
Clock fall time	$t_{F\text{-}SCL}$	0.8*VDDI -> 0.2*VDDI	2		300	ns
Capacitive Load	C_b	For each bus line			400	pF

Notes:

(1) Logic high and low levels are specified as 80% and 20% of VDDI for Input signals.

(2) During the read sequence, the transition time of SDA from low to high depends on the wire capacitance loading and pull-high resistance of the data bus. For example, the RC time constant of 4k pull-high resistance and 400pF bus capacitance is around 1.6us.

8.6. Reset Timing

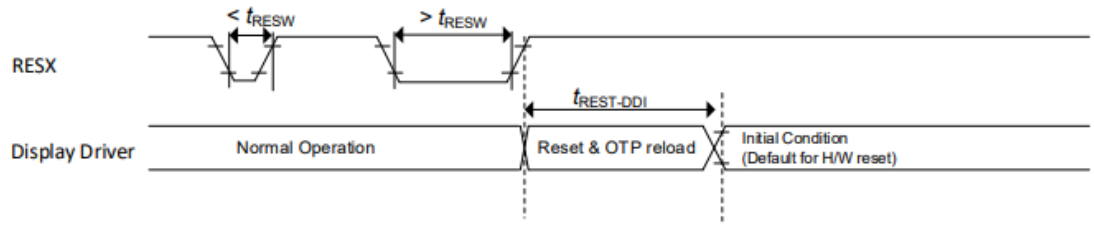
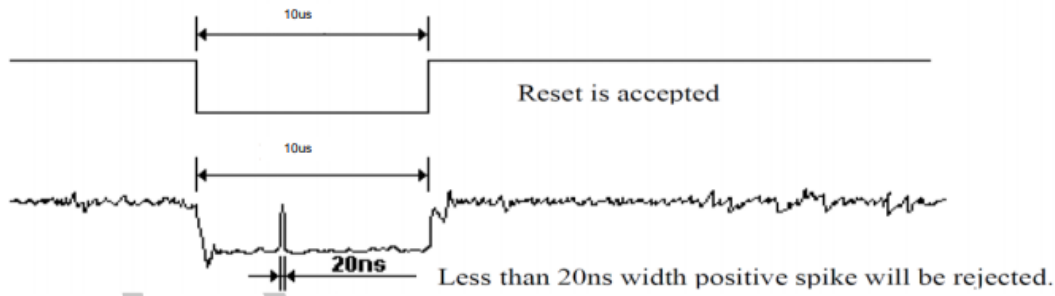


Figure 19, Illustration of reset timing for the whole chip

Table16: RESET Timing Specifications:

Parameter	Description	Min.	Typ.	Max	Unit
t_{RESW}	Low pulse width for RESX (1) Shorter than 5us: Reset Rejected (2) Longer than 30us: IC Reset (3) Between 5us and 30us: Unknown state (It depends on operation temperature and voltage)	30			us
$t_{REST\text{-}DDI}$	Reset complete time for display driver when reset is applied during Sleep-In mode	30			ms
	Reset complete time for display driver when reset is applied during Display-On mode	120			ms

Notes: Spike Rejection also applies during a valid reset pulse as shown below:



8.7. Power-On/Off Sequence for LVDS I/F

If the LVDS interface is used for video data transmission, and I2C can be used as command I/F. The following figure illustrates the power-on sequence by utilizing I2C I/F as command I/F. Moreover, if the device module had stored the initial code sufficient enough to light-on the panel, the host processor may not need to transmit any data to display module. Under this case, the host processor can activate the display module through HW pin “DISP”. The host processor shall transmit the video data to the display module before the DISPON command is sent to the display module or “DISP” goes high.

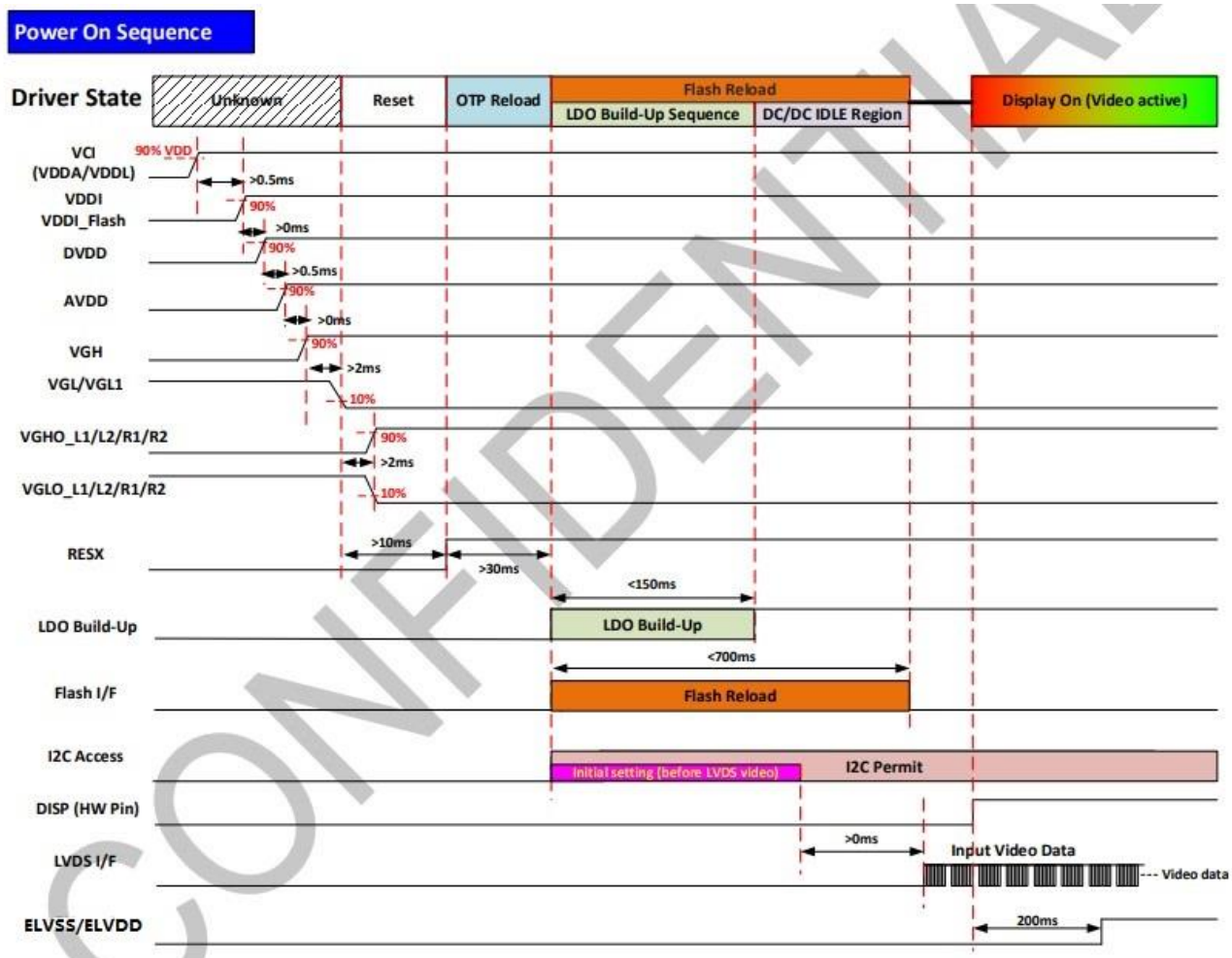


Figure 13, Normal Power-On Sequence for LVDS I/F

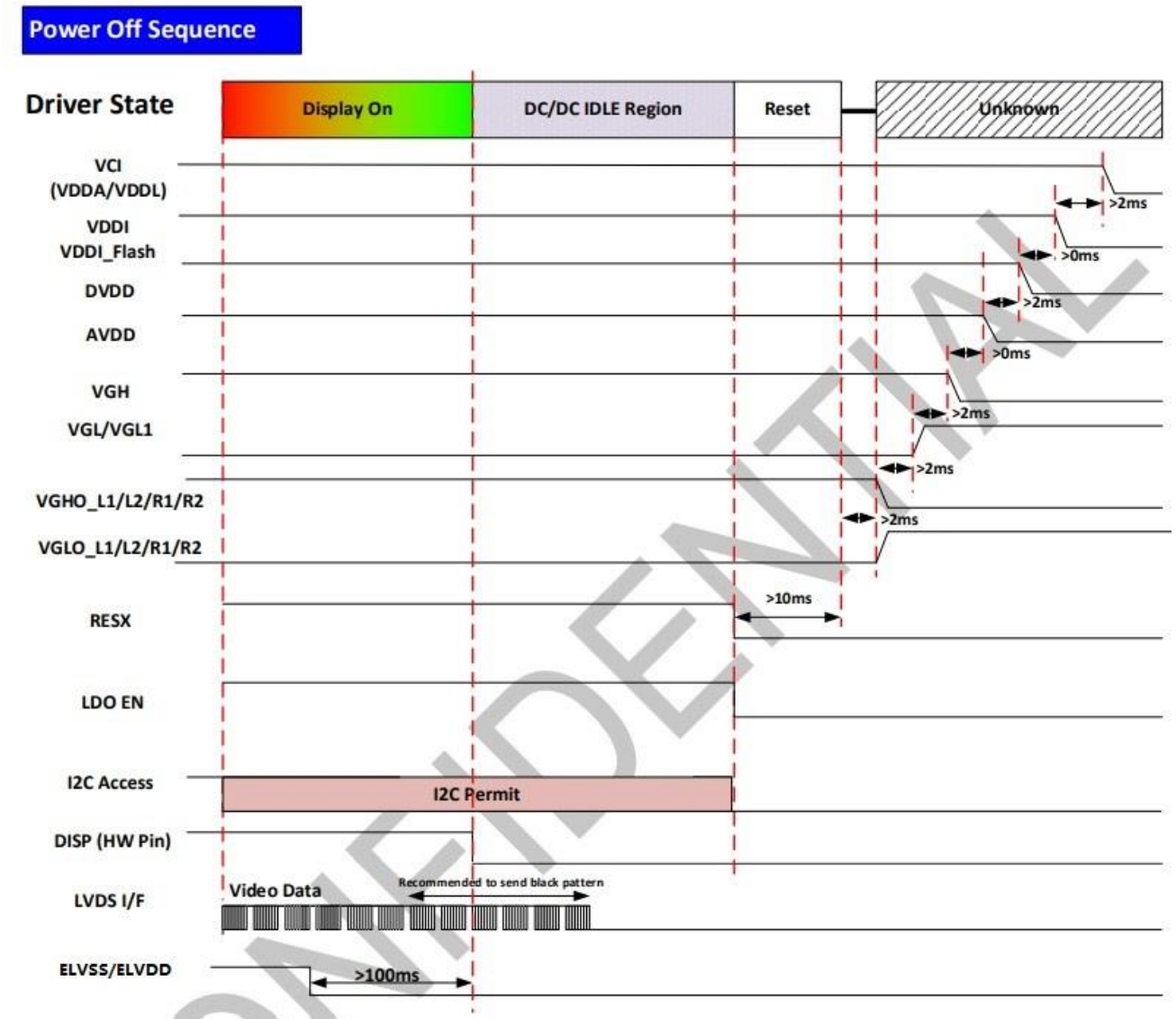


Figure 14, Normal Power-Off Sequence for LVDS I/F

9. TP Electrical Characteristics

9.1 TP I2C Timing Characteristics

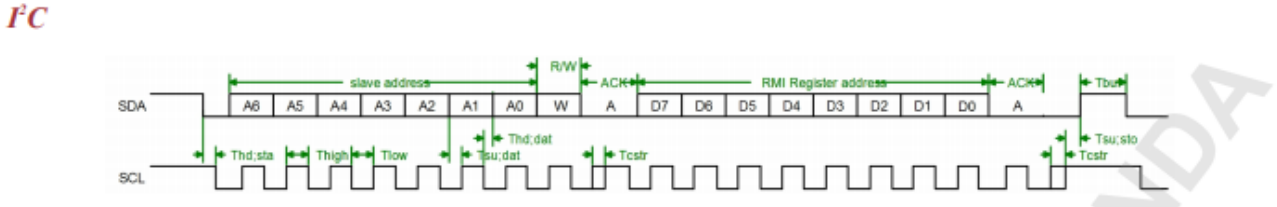


Figure 11. I²C timing

Table17: I2C parameters

Parameter	Symbol	Standard Mode			Fast Mode			Unit
		Min	Typ	Max	Min	Typ	Max	
SCL clock frequency	f_{SCL}	-	-	100	-	-	400	KHz
Clock stretch time	t_{CSTR}	-	<25	-	-	<25	-	us
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	$t_{HD;STA}$	4.0	-	-	0.6	-	-	us
Low period of the SCL clock	t_{LOW}	4.7	-	-	1.3	-	-	us
High period of the SCL clock	t_{HIGH}	4.0	-	-	0.6	-	-	us
Setup time for repeated START condition	$t_{SU:STA}$	4.7	-	-	0.6	-	-	us
Data hold time	$t_{HD:DAT}$	0	-	-	0	-	-	us
Data out valid time	$t_{VALID;DATO}$	-	-	3.45	-	-	0.9	us
Data setup time	$t_{SU;DAT}$	250	-	-	100	-	-	us
Rise time of SDA/SCL	t_r	-	-	1.000	$20+0.1G_B$	-	300	us
Fall time of SDA/SCL	t_f	-	-	300	$20+0.1G_B$	-	300	us
Setup time for STOP condition	$t_{SU:STO}$	4.0	-	-	0.6	-	-	us
Bus free time between a STOP and START condition	t_{BUF}	4.7	-	-	1.3	-	-	us
Capacitive load for each bus line	C_b	-	-	400	-	-	400	pf

9.2 TP Power-on and reset

Table19 Power-on sequence and external reset timing

Parameter	Min	Max	Unit
T_{attn_en}	5	21	ms
$T_{powerup}$	-	45	ms
Tstartup	-	45	ms
$T_{bl\_start\ (bootloader\ start)}$	-	30	ms
$T_{bl\_active\ (bootloader\ active)}$	-	15	ms
T_{reset}	100	-	ns

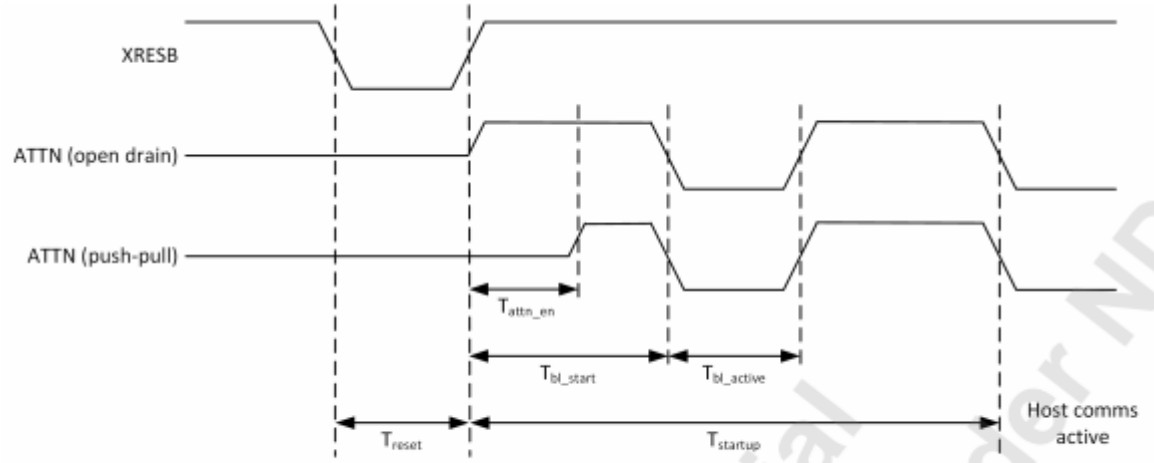


Figure 15. External reset timing diagram

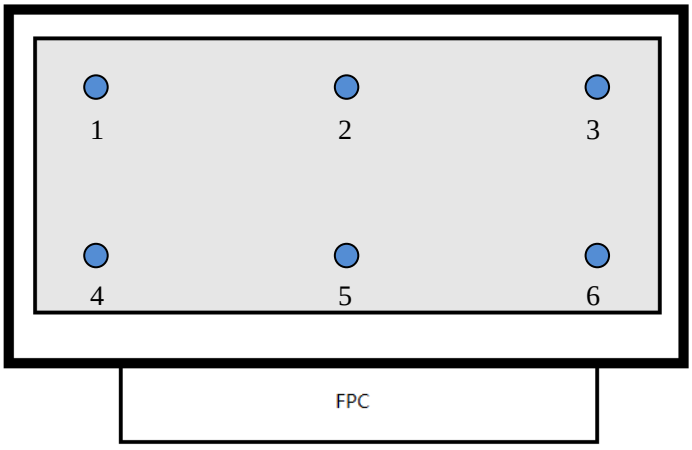
10.Reliability

序号	Item	Condition/Time/Cycle	判定标准	数量
1	高温存储试验	温度：90°C，湿度：<=45% 状态：不工作，1000hrs	在室温恢复 2hrs 后判定 无功能/外观类不良	6
2	低温存储试验	温度：-40°C， 状态：不工作，1000hrs	在室温恢复 2hrs 后判定 无功能/外观类不良	6
3	高温高湿耐久寿命试验	温度：60°C，湿度：93% 状态：工作，1000hrs 画面：R/G/B 黑/白/G127 循环播放	无功能/外观类不良； 前 500hrs 产品亮度 Decay 小于 20%，对比度/色坐标在产品规格内	6
4	高温运行耐久寿命试验	温度：85°C， 状态：工作，1000hrs 画面：R/G/B 黑/白/G127 循环播放	偏光片发黄，但无功能/外观类不良； 500hrs 产品亮度 Decay 小于 20%，对比度/色坐标在产品规格内	6
5	低温工作	温度：-40°C， 状态：工作，1000hrs 画面：R/G/B 黑/白/G127 循环播放	在室温恢复 2hrs 后判定 无功能/外观类不良； 前 500hrs 亮度 Decay 小于 20%，对比度/色坐标在产品规格内	6

6	温度循环试验	温度：-40°C→+85°C 1cycle：-40°C 停留 30mins，+85°C 停留 30mins ，transition time ≤5mins 状态：不工作，300cycle	在室温恢复 2hrs 后判定 无功能/外观类不良	6
7	ESD (Note 1)	不通电(FOG 状态)： 接触：C=100pF，R=1.5kΩ，±4KV 空气：C=100pF，R=1.5kΩ，±6KV	测试后通电可正常工作	5
		通电(FOG 状态)： 接触：C=150pF，R=330Ω，±6KV(显示) 空气：C=150pF，R=330Ω，±6KV（显示） FOG 状态下 TP ±4KV	Class B	5
		不通电(with CG)： 接触：C=150pF，R=2kΩ，±6KV 空气：C=150pF，R=2kΩ，±8KV	测试后通电可正常工作 （样品产出后，EDO 协助摸底测试，但不做为规格卡控）	5
		通电(with CG)： 接触：C=330pF，R=330Ω，±6KV 空气：C=330pF，R=330Ω，±8KV	Class B （样品产出后，EDO 协助摸底测试，但不做为规格卡控）	5

Note 1：ESD 测试说明

参考如下示意图选取 6 个放电点进行测试（AA，to AA edge＞8mm），每点测试 10 次，每次放电测试前完成静电释放，放电间隔时间 1s。



11.Handling Precautions

d) When cleaning ITO pad, avoid using hard and abrasive material or corrosive solution.

e) Keep module away from direct sunlight or fluorescent light, and keep it at room temperature and humidity.

f) Strong impact & pressure on module and packing is prohibited.

g) Following normal power on/off sequence is necessary for preventing abnormal display or permanent damage to display.

h) Optimal contrast ratio under ideal voltage is AMOLED module's characteristic, hence it is recommended a voltage control function available.

i) Image sticking may occur if an image displays for an extended period of time.

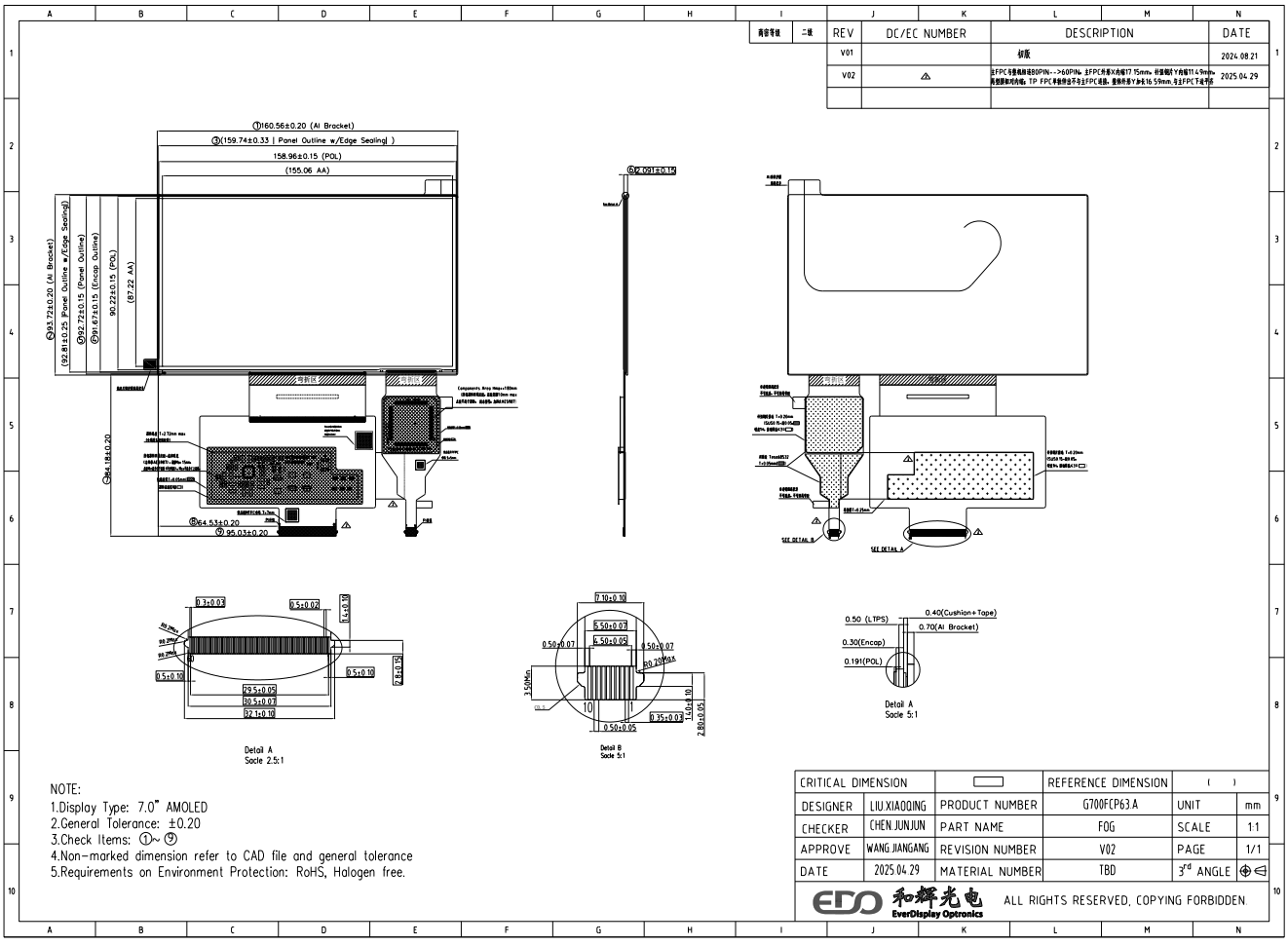
j) When interfered by system's overall mechanical design, an abnormal display may occur.

k) After considering emitting energy, you should plan your design to satisfy EMI standards.

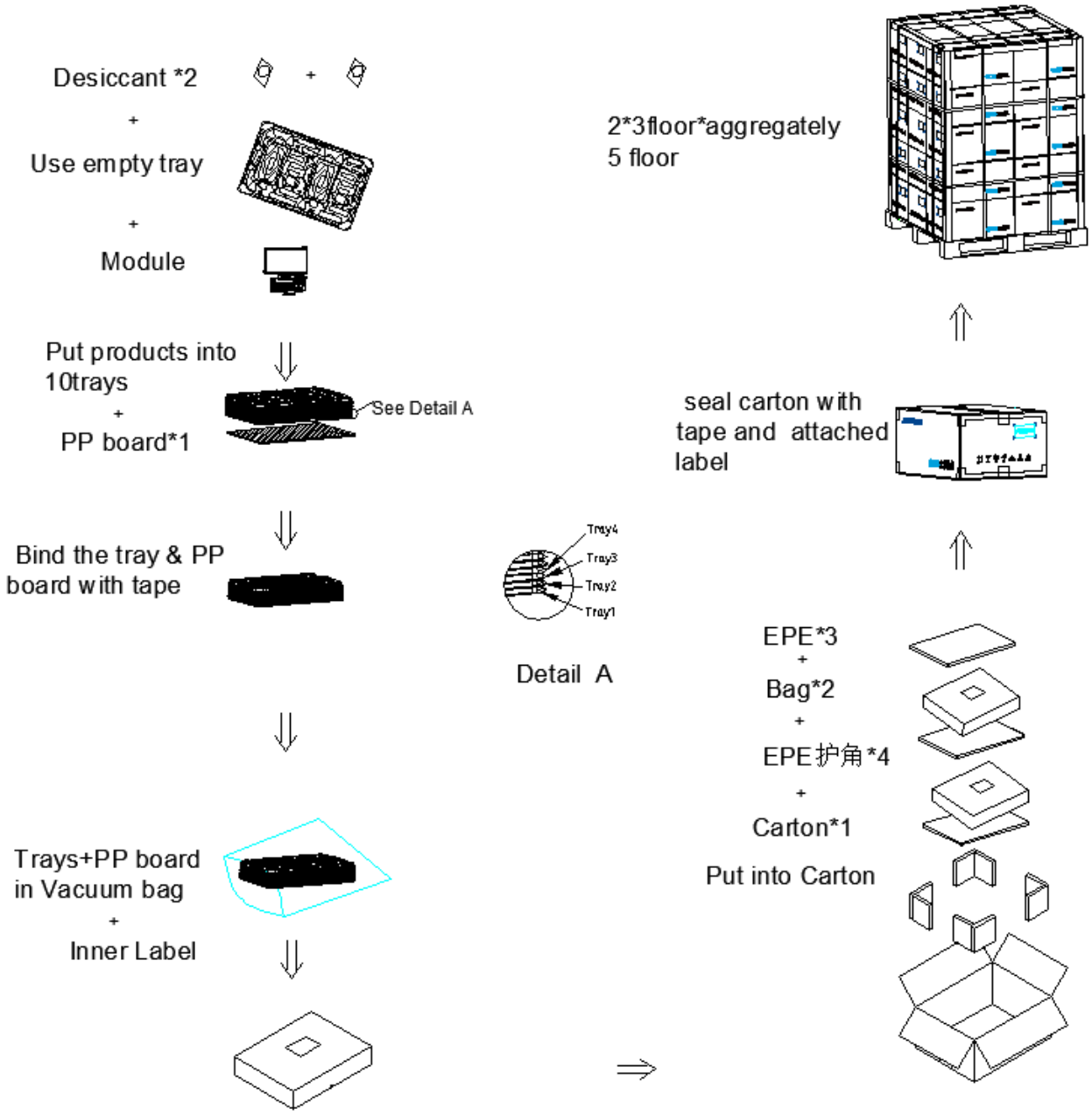
l) Host side should place a surge-prevent circuit at power trace (ie: VCI, Vddi) to protect AMOLED module.

12.Outline Dimension Drawing

Draft drawing



13.Packing Specification



14.The Control of Hazardous substances

The Control of Hazardous substances refer to EDO document《有害物质管控标准书》(Standard document for the Control of Hazardous substances) EDO-IS-110, last Version.