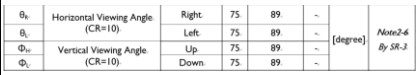
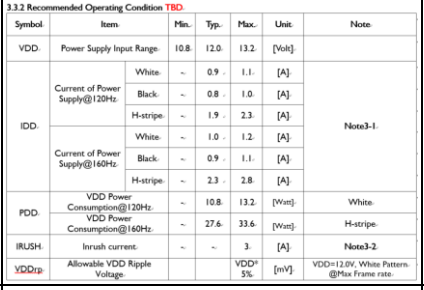
( ) Preliminary Specification
(V) Final Specification

Module	**32.0" Color TFT-LCD**
Model Name	**M320QAN02.D**

Customer	**Date**	**Approved by**	**Date**
		CH Lin	Jun 26,2023
Approved by		**Prepared by**	**Date**
		CJ Huang	Jun 26,2023
Note: This Specification is subject to change without notice.		AUO Corporation	

Contents

Record of Revision

Version	Date	Page	Old description	New Description	Remark
0.1	2023/2/13	All	First version release	-	
0.2	2023/4/7	9			
0.2	2023/4/7	18			
1.0	2023/7/26	All			

I Handling Precautions

1) Since polarizer is easily damaged, do not touch or press the surface of polorizer with hand.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open or modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) In case a TFT-LCD Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the LED lightbar edge. Otherwise the TFT-LCD Module may be damaged.
10) Insert or pull out the interface connector, be sure not to rotate nor tilt it of the TFT-LCD Module.
11) Do not twist nor bend the TFT -LCD Module even momentary. It should be taken into consideration that no bending/twisting forces are applied to the TFT-LCD Module from outside. Otherwise the TFT-LCD Module may be damaged.
12) Please avoid touching COF position while you are doing mechanical design.
13) When storing modules as spares for a long time, the following precaution is necessary: Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5°C and 35°C at normal humidity.
14) Do not apply the same pattern for a long time, it will enhance relevant defect.
15) When this reverse-type model(PCBA on bottom side) is used as forward-type model(PCBA on top side) , AUO can not guarantee any defects of LCM .

2 General Description

This specification applies to the 32.0 inch wide Color a-Si TFT-LCD Module M320QAN02.D. The display supports the UHD - 3840(H) x 2160(V) screen format and 1.07B colors(RGB 8bits +Hi-FRC). The input interface is 8-lanes eDP HBR2 and this module doesn't contain an driver board for backlight.

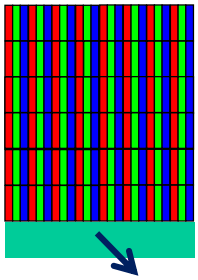
2.1 Display Characteristics

The following items are characteristics summary on the table under 25℃ condition:

ITEMS	Unit	SPECIFICATIONS
Screen Diagonal	[mm]	812.8 (32.0")
Active Area	[mm]	708.48 (H) x 398.52 (V)
Pixels H x V	-	3840(x3) x 2160
Pixel Pitch	[um]	184.5 (per one triad) × 184.5
Pixel Arrangement	-	R.G.B. Vertical Stripe ***Note 2-1***
Display Mode	-	AHVA Mode (Advances Hyper-Viewing Angle),Normally Black
White Luminance (Center of screen)	[cd/m^2]	350 (typ.)
HDR White Luminance (Center of screen	[cd/m^2]	400 (typ.)
HDR PEAK White Luminance (Center of screen	[cd/m^2]	400 (min.)
Contrast Ratio	-	1000 (Typ.)
Response Time	[msec]	5 (Typ., Gray to Gray)
Power Consumption (LCD Module + Backligh unit)	[Watt]	34.1 W (Typ.) LCD module : PDD(Typ.)= 12 W@white pattern,160Hz Backlight unit : PBLU (Typ.) = 22.1 W @Is= 85 mA
HDR PEAK Power Consumption (LCD Module + Backligh unit)	[Watt]	43.7 W (Typ.) LCD module : PDD(Typ.)= 12 W@white pattern,160Hz Backlight unit : PBLU (Typ.) = 31.7 W @Is= 120 mA
Weight	[Grams]	4800 +/- 240
Outline Dimension	[mm]	721.68 (H) x 417.93 (V) × 15.47 (D) Typ.
Electrical Interface	-	8 Lane eDP HBR2 10bits RGB data input with max frame rate 120Hz 8bits RGB data input with max frame rate 160Hz
Support Color	-	1.07B colors (RGB 8bits + Hi-FRC)
Surface Treatment	-	SAG25%, 3H

Temperature Range Operating Storage (Shipping)	[°C] [°C]	0 to +50 -20 to +60
RoHS Compliance	-	RoHS Compliance
Low Blue Light Compliance	-	The ratio of light in the range from 415nm~455nm compared to 400nm~500nm shall be less than 50%

Note 2-1: The following shows the figure of pixel arrangement



Source Board

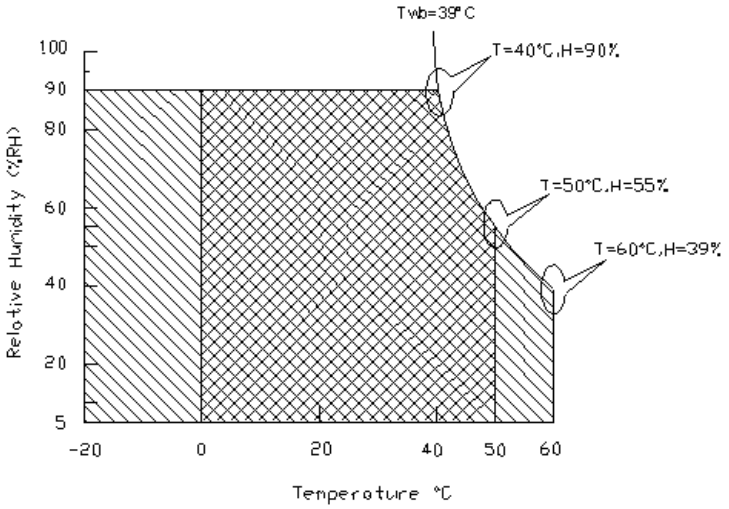
2.2 Absolute Maximum Rating of Environment

Permanent damage may occur if exceeding the following maximum rating.

Symbol	Description	Min.	Max.	Unit	Remark
TOP	Operating Temperature	0	+50	[°C]	***Note 2-2***
TGS	Glass surface temperature (operation)	0	+68	[°C]	***Note 2-2*** *Function judged only*
HOP	Operation Humidity	5	90	[%RH]	***Note 2-2***
TST	Storage Temperature	-20	+60	[°C]	
HST	Storage Humidity	5	90	[%RH]	

Note 2-2: Temperature and relative humidity range are shown as the below figure.

1. 90% RH Max (Ta ≦39℃)
2. Max wet-bulb temperature at 39℃ or less. (Ta ≦39℃)
3. No condensation



Operating Range Storage Range

2.3 Optical Characteristics

The optical characteristics are measured on the following test condition.

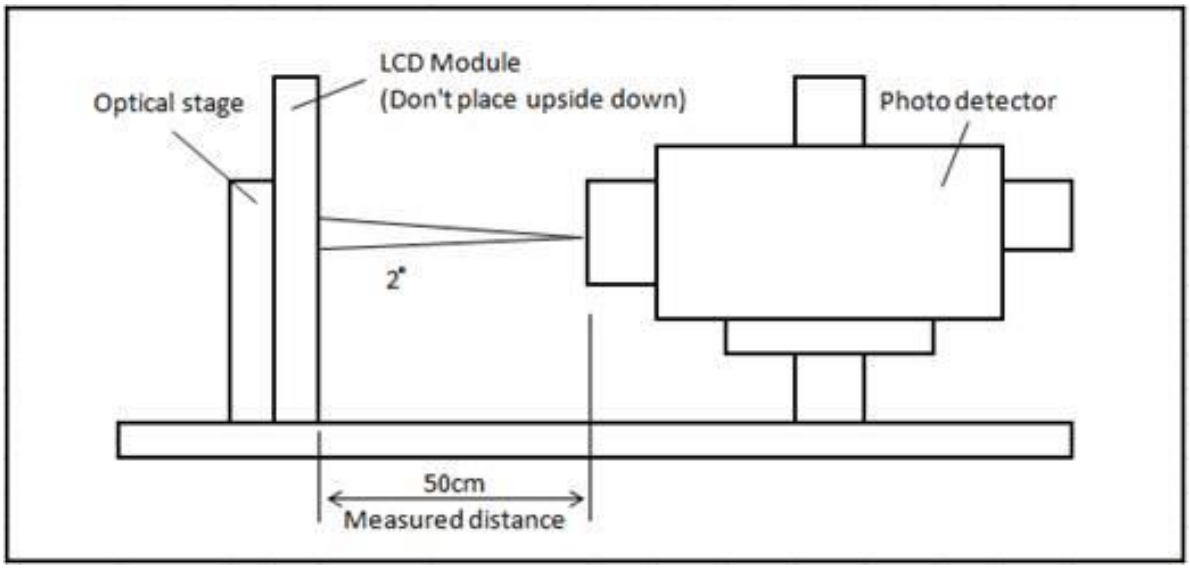
Test Condition:

1. Equipment setup: Please refer to ***Note 2-3.***
2. Panel Lighting time: 30 minutes
3. VDD=12.0V, Fv=120Hz, Ta=25°C

Symbol	Description		Min.	Typ.	Max.	Unit	Remark
L_w	White Luminance (Center of screen)		280	350	-	[cd/m2]	Is=85mA Note2-3 By SR-3
L_{WH}	HDR White Luminance (Center of screen)		320	400		[cd/m2]	Is=95mA Note2-3 By SR-3
L_{WP}	HDR PEAK White Luminance (Center of screen)		400		-	[cd/m2]	Is=120mA Note2-3 By SR-3
L_{UNI}	Luminance Uniformity (9 points)		75	80	-	[%]	***Note2-4*** *By SR-3*
CR	Contrast Ratio (Center of screen)		600	1000	-	-	***Note2-5*** *By SR-3*
θ_R	Horizontal Viewing Angle (CR=10)	Right	75	89	-	[degree]	***Note2-6*** *By SR-3*
θ_L		Left	75	89	-		
Φ_H	Vertical Viewing Angle (CR=10)	Up	75	89	-		
Φ_L		Down	75	89	-		
T_{GTG}	Response Time	Gray to Gray	-	5	-	[msec]	***Note2-7*** *By TRD-100*
R_x	Color Coordinates (CIE 1931)	Red x	0.654	0.684	0.714	-	*By SR-3*
R_y		Red y	0.280	0.310	0.340		
G_x		Green x	0.231	0.261	0.291		
G_y		Green y	0.624	0.654	0.684		
B_x		Blue x	0.112	0.142	0.172		
B_y		Blue y	0.032	0.062	0.092		
W_x		White x	0.283	0.313	0.343		
W_y		White y	0.299	0.329	0.359		
Ru'	Color Coordinates (CIE 1976)	Red u'		0.511		-	*By SR-3*
Rv'		Red v'		0.521			
Gu'		Green u'		0.101			

Gv'		Green v'		0.570			
Bu'		Blue u'		0.164			
Bv'		Blue v'		0.161			
Wu'		White u'		0.198			
Wv'		White v'		0.468			
sRGB coverage ratio (CIE 1931)				99		[%]	*By SR-3*
DCI P3 Coverage ratio (CIE1976)				95		[%]	*By SR-3*

Note 2-3: Equipment setup :

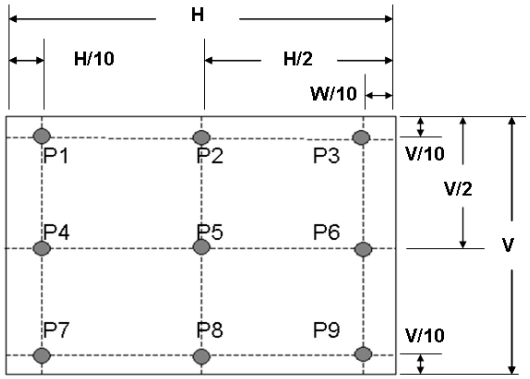


Note 2-4: Luminance Uniformity Measurement

Definition:

$$\text{Luminance Uniformit y} = \frac{\text{Minimum Luminance of 9 Points (P1 ~ P9)}}{\text{Maximum Luminance of 9 Points (P1 ~ P9)}}$$

a. Test pattern:White Pattern



Note 2-5: Contrast Ratio Measurement

Definition:

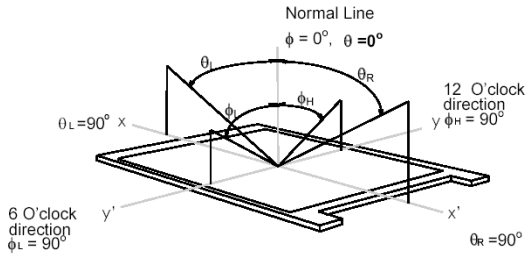
$$\text{Contrast Ratio} = \frac{\text{Luminance of White pattern}}{\text{Luminance of Black pattern}}$$

a. Measured position: Center of screen (P5) & perpendicular to the screen (θ=Φ=0°)

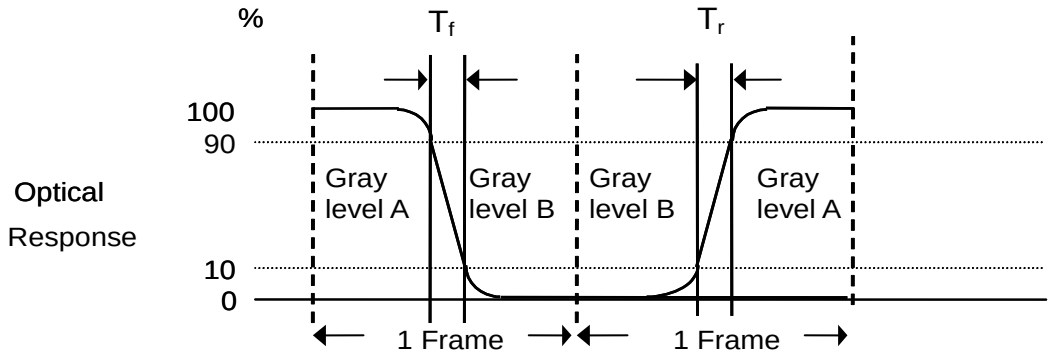
Note 2-6: Viewing angle measurement

Definition: The angle at which the contrast ratio is greater than 10 & 5.

a. Horizontal view angle: Divide to left & right (θ_L & θ_R)
Vertical view angle: Divide to up & down (Φ_H &Φ_L)



Note 2-7: Response time measurement



The output signals of photo detector are measured when the input signals are changed from "Gray level A" to "Gray level B" (falling time, TF), and from "Gray level B" to "Gray level A" (rising time, TR), respectively. The response time is interval between the 10% and 90% of optical response.

The gray to gray response time is defined as the following table.

Gray Level to Gray Level		Target gray level				
		L0	L63	L127	L191	L255
Start gray level	L0					
	L63					
	L127					
	L191					
	L255					

- T_{GTG_typ} is the total average time at rising time and falling time of gray to gray.

Note 2-8: Evaluation test and mass production inspection shall be applied with LED current I_S White Luminance condition if there is not specified condition.

2.8 Mechanical Characteristics

Symbol	Description	Min.	Max.	Unit	Remark
P_{bc}	Backside Compression	2.5	-	[Kgf]	***Note 2-9***

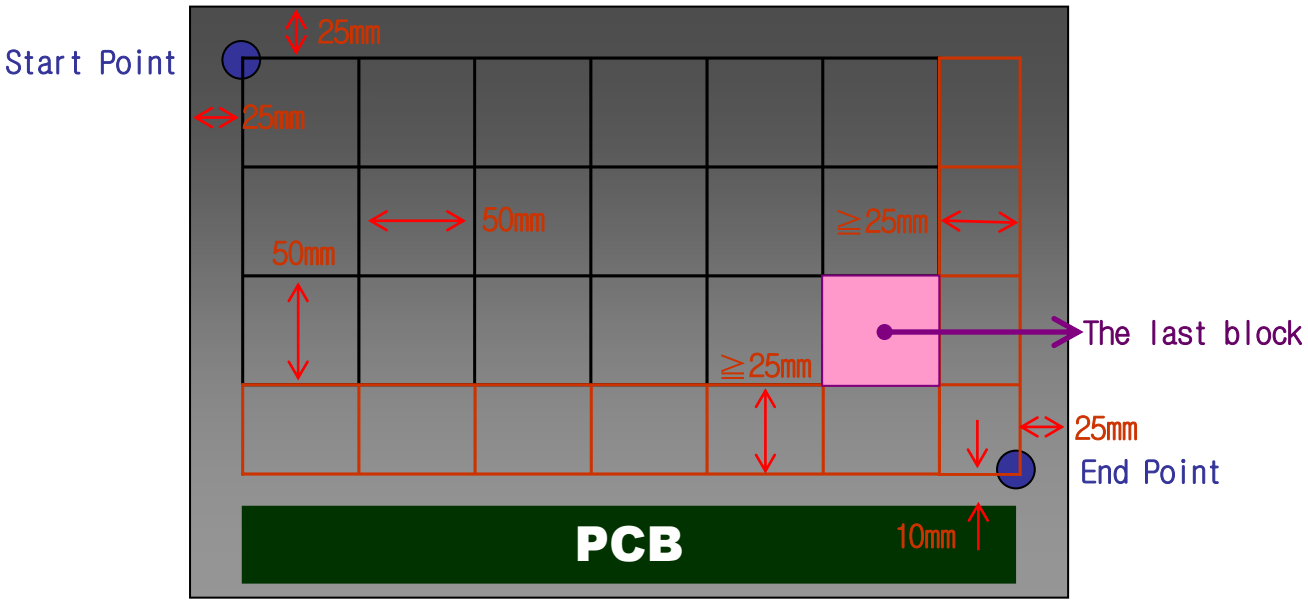
Note 2-9: a. Test Method:

The point is at a distance from right-downside 25mm x 25mm defined as the Start Point of Measure Points, and the point is at a distance 25mm from left-side & around 10mm from PCB defined as the End Point.

Align 50mm x 50mm block from Start Point on the Bezel Back, and the corners of each block are Measure Points.

If the distance from the last block to each side of the End Point ≧ 25mm, add other blocks to make sure that most area of Bezel Back can be measured.

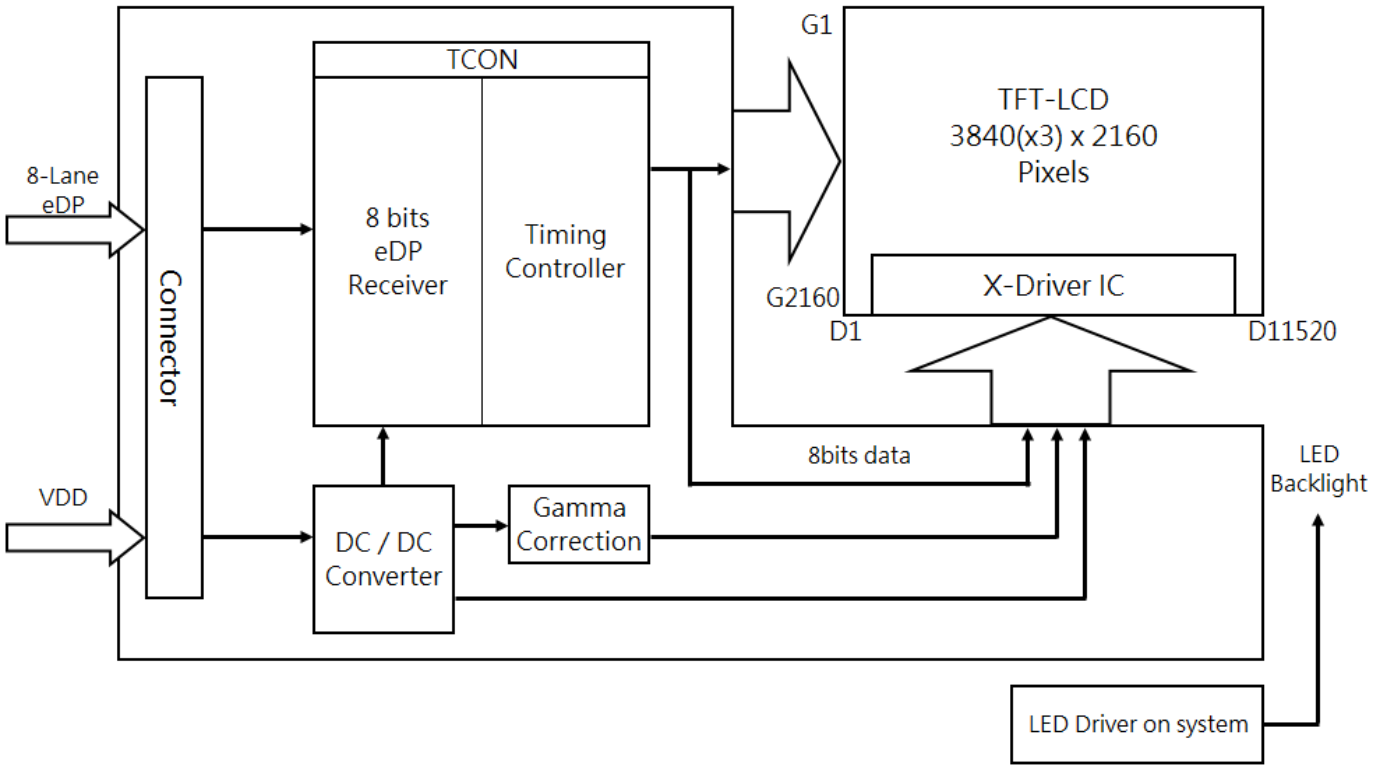
a. Test pattern: It is listed as following.



3 TFT-LCD Module

3.1 Block Diagram

The following shows the block diagram of the 32.0 inch Color TFT-LCD Module.



3.2 Interface Connection

3.2.1 Connector Type

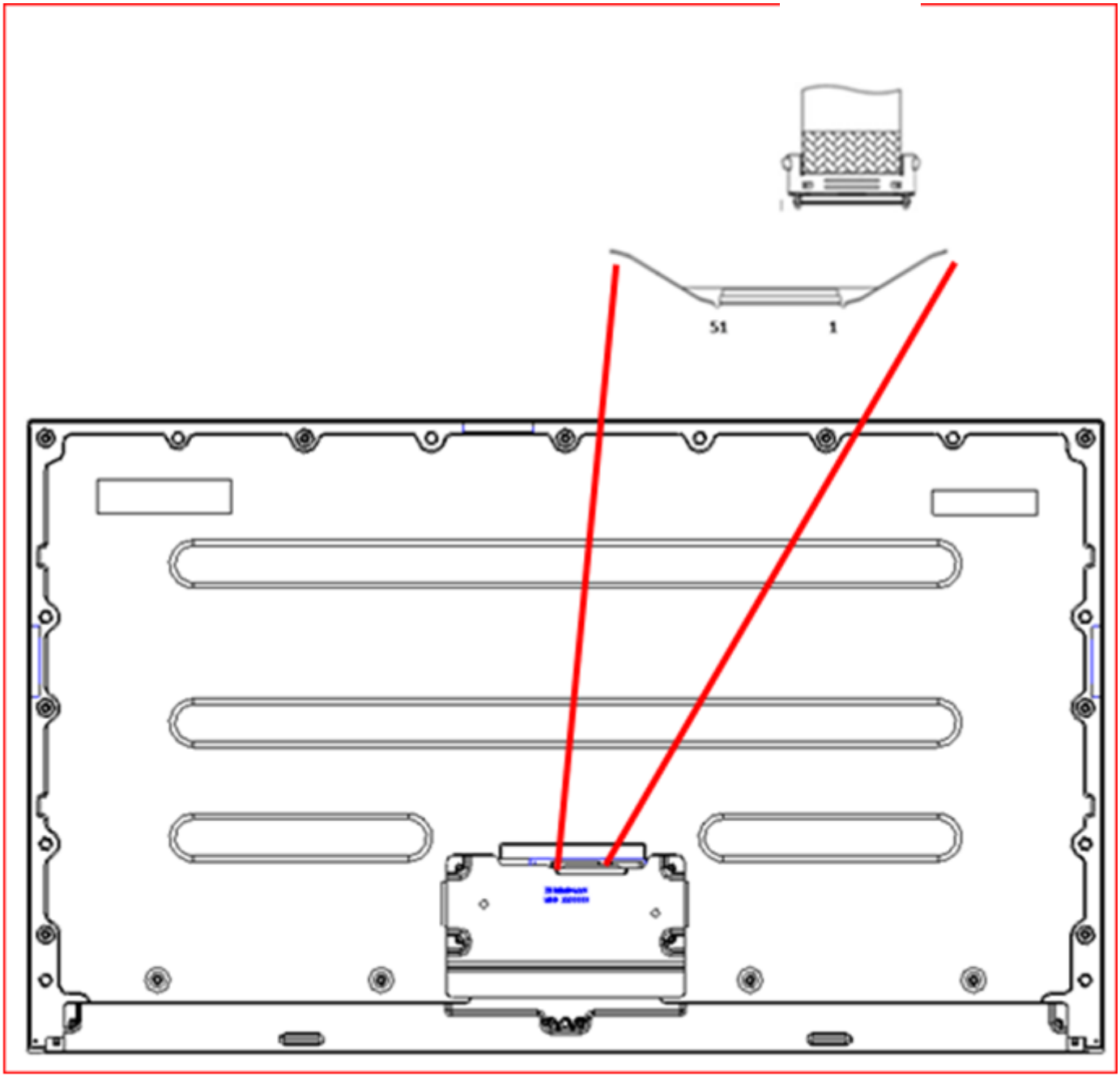
TFT-LCD Connector	Manufacturer	JAE	P-TWO	STARCONN (CHIEF LAND)
	Part Number	FI-RTE51SZ-HF	187059-5122	115E51-0000RA-M3-R
Mating Connector	Manufacturer	JAE or Compatible		
	Part Number	FI-RE51CL (Locked Type)		

3.2.2 Connector Pin Assignment

PIN #	Symbol	Description	Remark
1	VDD	Power +12V	
2	VDD	Power +12V	
3	VDD	Power +12V	
4	VDD	Power +12V	
5	VDD	Power +12V	
6	GND	Ground	
7	GND	Ground	
8	GND	Ground	
9	NC	No connection (for AUO test only. Do not connect)	
10	NC	No connection (for AUO test only. Do not connect)	
11	NC	No connection (for AUO test only. Do not connect)	
12	NC	No connection (for AUO test only. Do not connect)	
13	NC	No connection (for AUO test only. Do not connect)	
14	NC	No connection (for AUO test only. Do not connect)	
15	NC	No connection (for AUO test only. Do not connect)	
16	NC	No connection (for AUO test only. Do not connect)	
17	GND	Ground	
18	1st Lane3_N	Negative eDP differential data input	
19	1st Lane3_P	Positive eDP differential data input	
20	GND	Ground	
21	1st Lane2_N	Negative eDP differential data input	

22	1st Lane2_P	Positive eDP differential data input	
23	GND	Ground	
24	1st Lane1_N	Negative eDP differential data input	
25	1st Lane1_P	Positive eDP differential data input	
26	GND	Ground	
27	1st Lane0_N	Negative eDP differential data input	
28	1st Lane0_P	Positive eDP differential data input	
29	GND	Ground	
30	1st AUX_CH_P	Positive AUX Channel differential data input	
31	1st AUX_CH_N	Negative AUX Channel differential data input	
32	GND	Ground	
33	NC	No connection (for AUO test only. Do not connect)	
34	GND	Ground	
35	2nd Lane3_N	Negative eDP differential data input	
36	2nd Lane3_P	Positive eDP differential data input	
37	GND	Ground	
38	2nd Lane2_N	Negative eDP differential data input	
39	2nd Lane2_P	Positive eDP differential data input	
40	GND	Ground	
41	2nd Lane1_N	Negative eDP differential data input	
42	2nd Lane1_P	Positive eDP differential data input	
43	GND	Ground	
44	2nd Lane0_N	Negative eDP differential data input	
45	2nd Lane0_P	Positive eDP differential data input	
46	GND	Ground	
47	2nd AUX_CH_P	Positive AUX Channel differential data input	
48	2nd AUX_CH_N	Negative AUX Channel differential data input	
49	GND	Ground	
50	HPD	Hot plug detection	

51	GND	Ground	



3.3 Electrical Characteristics

3.3.1 Absolute Maximum Rating

Permanent damage may occur if exceeding the following maximum rating.

Symbol	Description	Min	Max	Unit	Remark
VDD	Power Supply Input Voltage	GND-0.3	14	[Volt]	Ta=25°C

3.3.2 Recommended Operating Condition

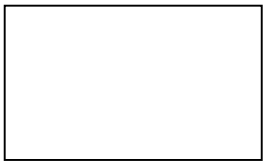
Symbol	Item		Min.		Typ.	Max.	Unit	Note
VDD	Power Supply Input Range		10.8		12.0	13.2	[Volt]	
IDD	Current of Power Supply@120Hz	White	-		0.9	1.1	[A]	**Note3-1**
		Black	-		0.8	1.0	[A]	
		H-stripe	-		1.9	2.3	[A]	
	Current of Power Supply@160Hz	White	-		1.0	1.2	[A]	
		Black	-		0.9	1.1	[A]	
		H-stripe	-		2.3	2.8	[A]	
PDD	VDD Power Consumption@120Hz		-		10.8	13.2	[Watt]	White
	VDD Power Consumption@160Hz		-		27.6	33.6	[Watt]	H-stripe
IRUSH	Inrush current		-		-	3	[A]	**Note3-2**
VDDrp	Allowable VDD Ripple Voltage					VDD *5%	[mV]	VDD=12.0V, White Pattern @Max Frame rate

Note 3-1: Test Condition:

(1) V_{DD} = Typical, (2) Temperature = 25 ℃

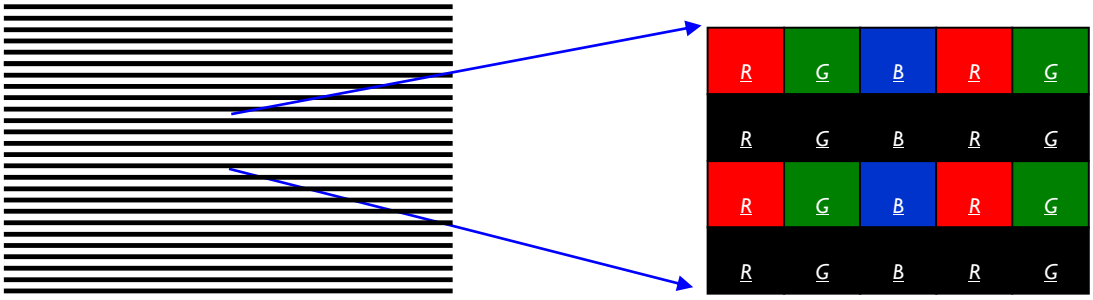
(3) Power dissipation check pattern. (Only for power design)

A. White



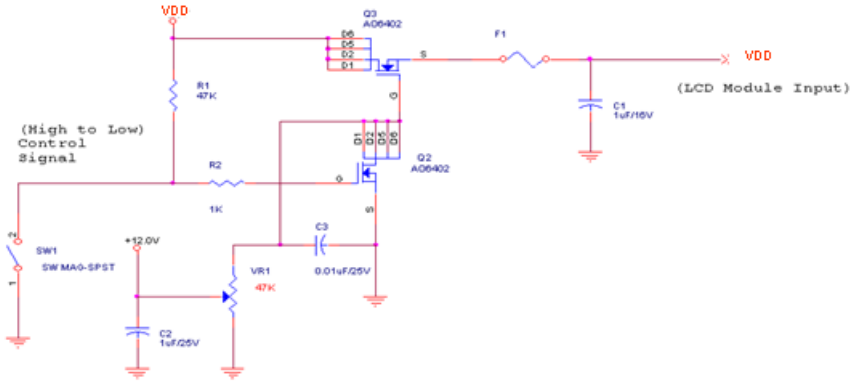
B. Black

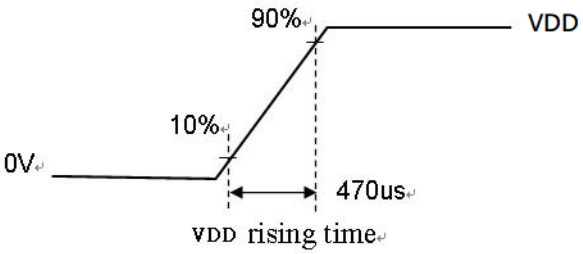
C. H-Stripe



Note 3-2: Inrush Current measurement:

Test circuit:



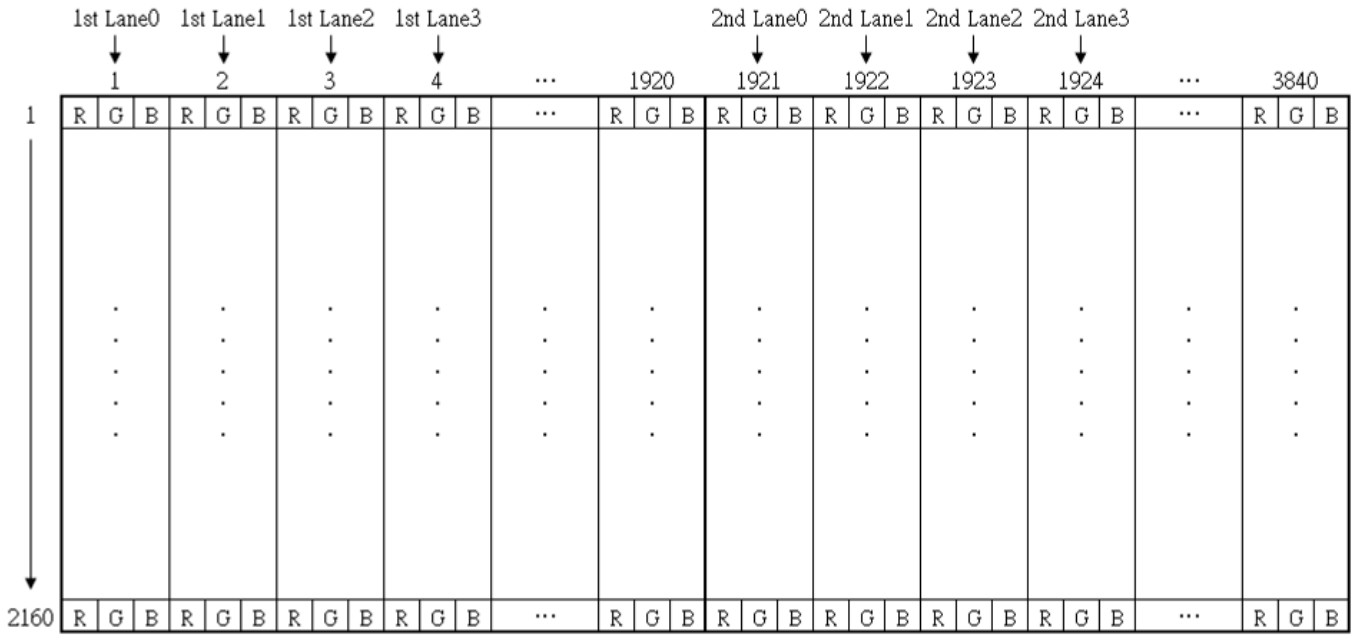


The duration of VDD rising time: 470us.

3.4 Signal Characteristics

3.4.1 LCD Pixel Format

Following figure shows the relationship between the input signals and LCD pixel format.



Note 3-3: The module use 8-Lanes eDP interface.

1st port:

1st Lane0：1+4n pixel

1st Lane1：2+4n pixel

1st Lane2：3+4n pixel

1st Lane3：4+4n pixel

2nd port:

2nd Lane0：1921+4n pixel

2nd Lane1：1922+4n pixel

2nd Lane2：1923+4n pixel

2nd Lane3：1924+4n pixel

n=0~479

3.4.2 eDP Data Format

1st Lane0	1st Lane1	1st Lane2	1st Lane3
R1-7:0	R2-7:0	R3-7:0	R4-7:0
G1-7:0	G2-7:0	G3-7:0	G4-7:0
B1-7:0	B2-7:0	B3-7:0	B4-7:0
R5-7:0	R6-7:0	R7-7:0	R8-7:0
G5-7:0	G6-7:0	G7-7:0	G8-7:0
B5-7:0	B6-7:0	B7-7:0	B8-7:0
R9-7:0	R10-7:0	R11-7:0	R12-7:0
G9-7:0	G10-7:0	G11-7:0	G12-7:0
B9-7:0	B10-7:0	B11-7:0	B12-7:0
.	.	.	.
.	.	.	.
.	.	.	.

2nd Lane0	2nd Lane1	2nd Lane2	2nd Lane3
R1921-7:0	R1922-7:0	R1923-7:0	R1924-7:0
G1921-7:0	G1922-7:0	G1923-7:0	G1924-7:0
B1921-7:0	B1922-7:0	B1923-7:0	B1924-7:0
R1925-7:0	R1926-7:0	R1927-7:0	R1928-7:0
G1925-7:0	G1926-7:0	G1927-7:0	G1928-7:0
B1925-7:0	B1926-7:0	B1927-7:0	B1928-7:0
R1929-7:0	R1930-7:0	R1931-7:0	R1932-7:0
G1929-7:0	G1930-7:0	G1931-7:0	G1932-7:0
B1929-7:0	B1930-7:0	B1931-7:0	B1932-7:0
.	.	.	.
.	.	.	.
.	.	.	.

3.4.3 Color versus Input Data

The following table is for color versus input data (8bit). The higher the gray level, the brighter the color.

.

Color	Gray Level	Color Input Data																								Remark
		RED data (MSB:R7, LSB:R0)								GREEN data (MSB:G7, LSB:G0)								BLUE data (MSB:B7, LSB:B0)								
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0	
Black	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
White	-	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
Gray 127	-	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	
Red	L0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Black
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	L255	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Green	L0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Black
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	L255	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	
Blue	L0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Black
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	L255	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	

3.4.4 eDP Specification (Follow as VESA DisplayPort Standard Version 1.1) (support 5.4Gbps for HBR2)

a. DisplayPort main link signal:

DisplayPort main link					
		Min	Typ	Max	unit
Frequency	Main link Frequency	-	5.4	-	Gbps
UI	Unit Interval	-	185	-	ps
VCM	RX input DC Common Mode Voltage	-	0	-	[Volt]
$VDiff_{P-P}$	Peak-to-peak Voltage at a receiving Device	70	-	-	[mVolt]
Down_Spread_Freq	Link clock down spread frequency	30	-	33	KHz
Down_Spread_Amplitude	Link clock down spread amplitude	-	-	0.5	%

Point	Time(UI)	Voltage
1	0.310	0
2	0.375~0.625	35mV
3	0.690	0
4	0.375~0.625	-35mV

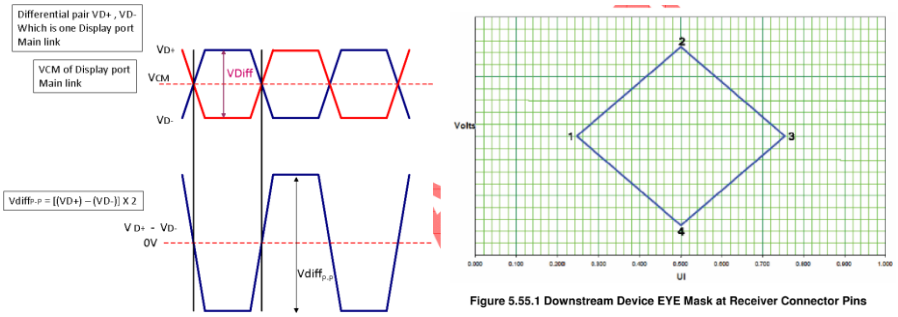
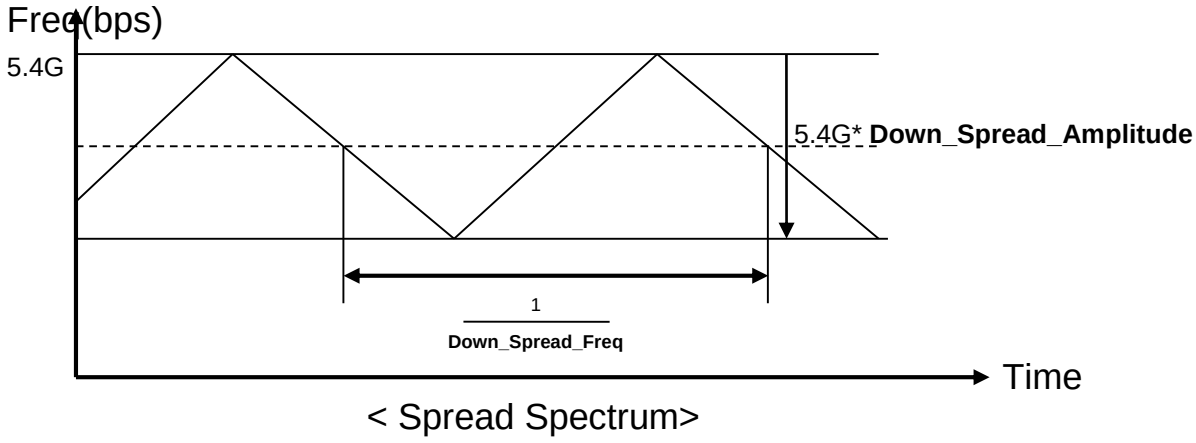


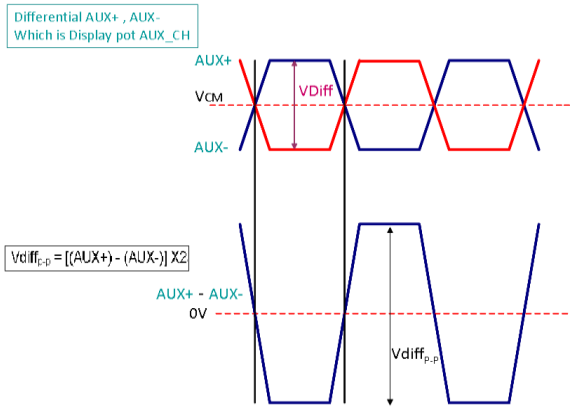
Figure 5.55.1 Downstream Device EYE Mask at Receiver Connector Pins



< Spread Spectrum>

b. DisplayPort AUX_CH signal:

DisplayPort AUX_CH					
		Min	Typ	Max	unit
VCM	AUX DC Common Mode Voltage	0	-	2.0	[Volt]
$VDiff_{P-P}$	AUX Peak-to-peak voltage at a receiving device	0.27	-	1.36	[Volt]



c. DisplayPort VHPD signal:

Display Port VHPD					
		Min	Typ	Max	unit
VHPD	HPD Voltage	2.25	-	3.6	[Volt]

d. Intra-Pair skew

LRX-SKEW-INTRA_PAIR					
		Min	Typ	Max	unit
LRX-SKEW-INTRA_PAIR	Lane Intra-pair Skew Tolerance	-	-	50	[ps]

e. Inter-Pair Skew

LRX-SKEW-INTER_PAIR					
		Min	Typ	Max	unit
LRX-SKEW-INTER_PAIR	Lane-to-Lane Skew at RX package pins	-	-	5200	[ps]

3.4.5 Input Timing Specification

The input timing is shown as the following table.

Symbol	Description		Min.	Typ.	Max.	Unit	Remark
Tv	Vertical Section	Period	2185	2200	7438	Th	
Tdisp (v)		Active	2160	2160	2160	Th	
Tblk (v)		Blanking	25	40	5278	Th	
Fv		Frequency	47	120	160	Hz	***Note 3-4*** ***Note 3-5***
Th	Horizontal Section	Period	2000	2100	2720	Tclk	
Tdisp (h)		Active	1920	1920	1920	Tclk	
Tblk (h)		Blanking	80	180	800	Tclk	
Fh		Frequency	180.0	264.0	352.0	kHz	***Note 3-6***
Tclk	Pixel Clock	Period	1.42	1.804	2.778	ns	1/Fclk
Fclk		Frequency	360.0	554.4	704.0	MHz	***Note 3-7***
Link Rate per Lane				5.4		Gbps	

Note 3-4: The optimal Vertical Frequency is 119~160 Hz for best picture quality. Some performance (such as Image stick, Flicker and Reliability) cannot be guaranteed if fixing at the refresh rate of 47~118 Hz. It just supports the gaming application at frequency change status.

Note 3-5: The max frame rate is 120Hz with 10bit data input application.

Note 3-6: The equation is listed as following. Please don't exceed the above recommended value.

Fh (Min.) = Fclk (Min.) / Th (Min.)
Fh (Typ.) = Fclk (Typ.) / Th (Typ.)
Fh (Max.)= Fclk (Max.) / Th (Min.)

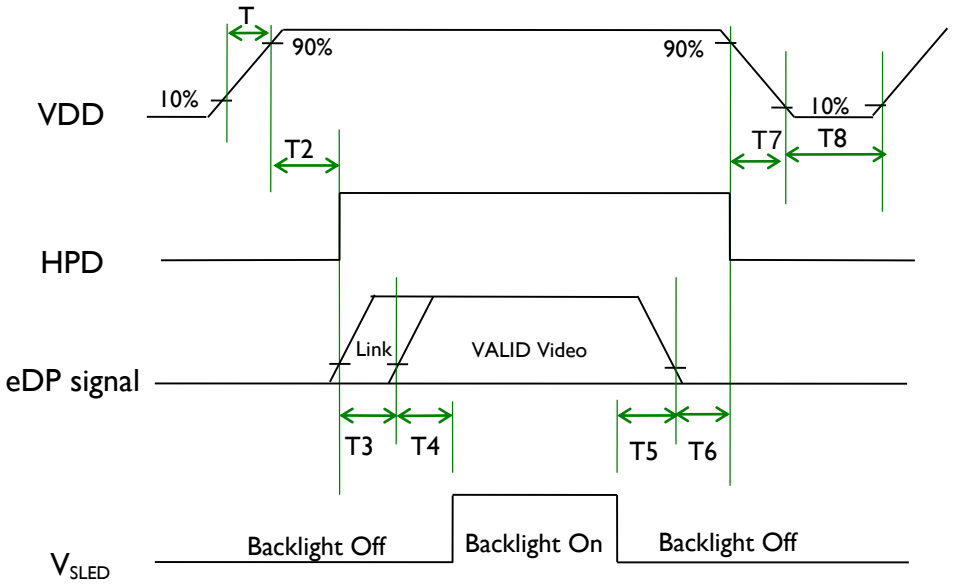
Note 3-7: The equation is listed as following. Please don't exceed the above recommended value.

Fclk (Typ.) = Fv (Typ.) x Th (Typ.) x Tv (Typ.)

Fclk (Min.) $\leqq$ Fv x Th x Tv $\leqq$ Fclk (Max.)

3.5 Power ON/OFF Sequence

VDD power,eDP signal and backlight on/off sequence are as following. eDP signals from any system tshall be Hi-Z state when VDD is off.



Power Sequence Timing

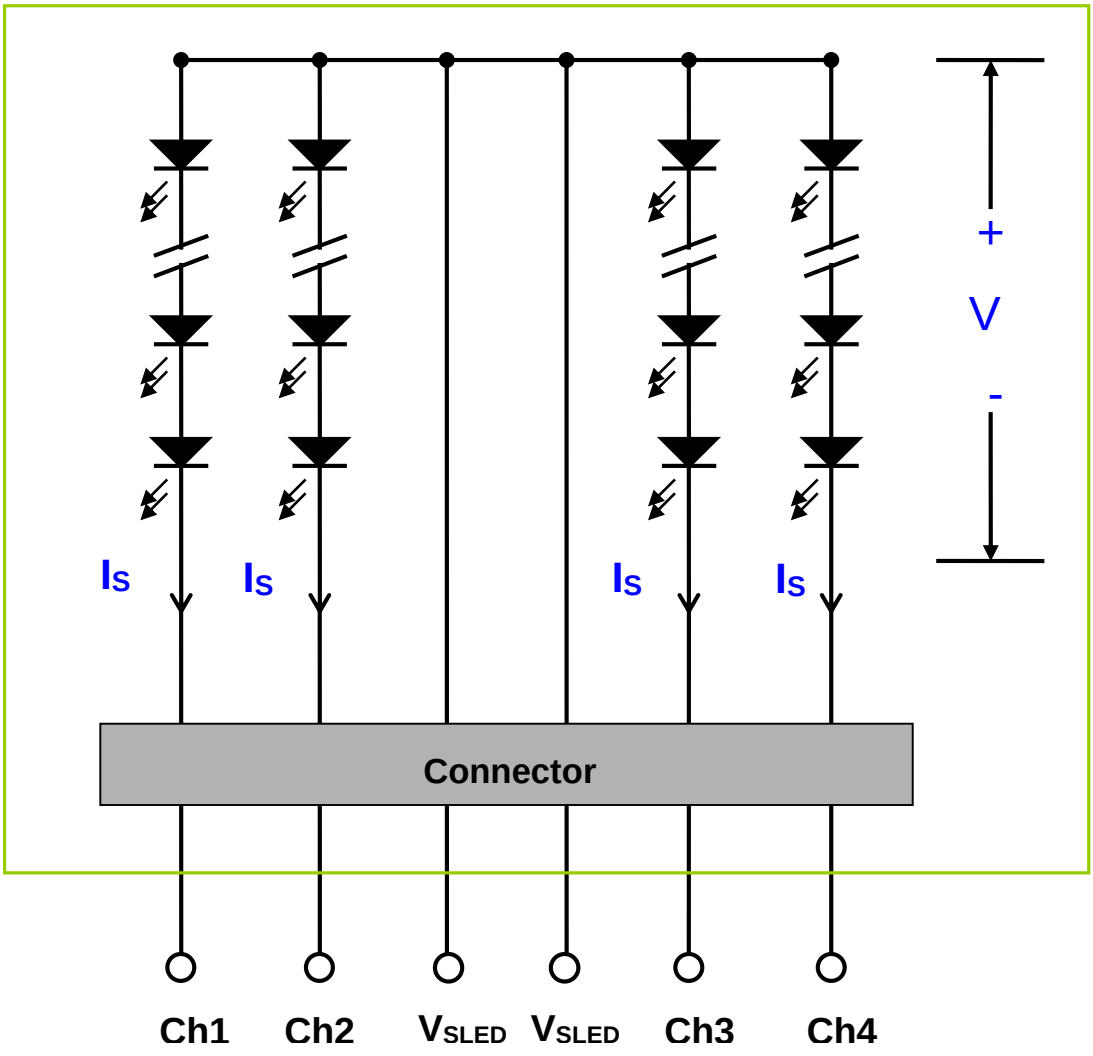
Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
T1	0.5	-	10	[ms]	
T2	0	-	200	[ms]	
T3	0	-	-	[ms]	***Note 3-8***
T4	500	-	-	[ms]	
T5	100		-	[ms]	
T6	0	-	50	[ms]	***Note 3-9*** ***Note 3-10***
T7	0	-	200	[ms]	***Note 3-10*** ***Note 3-11***
T8	1000	-	-	[ms]	

Note 3-8: During T3 period , eDP link training time by customer's system.
Note 3-9: Recommend setting T6 = 0ms to avoid electronic noise when VDD is off.
Note 3-10: During T6 & T7 period , please keep the level of input eDP signals with Hi-Z state.
Note 3-11: Voltage of VDD must decay smoothly after power-off.(customer system decide this value)

4 Backlight Unit

4.1 Block Diagram

The following shows the block diagram of the 32.0 inch Backlight Unit. And it includes 2 pcs LED light bar in Backlight Unit. Each LED light bar includes 44 pcs LED package. (= 4 strings; 11pcs LED for each string).



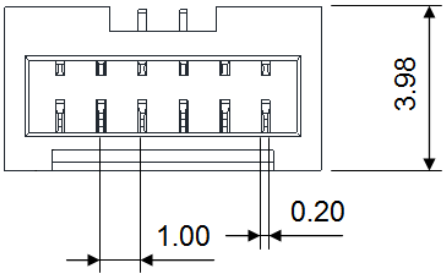
4.2 Interface Connection

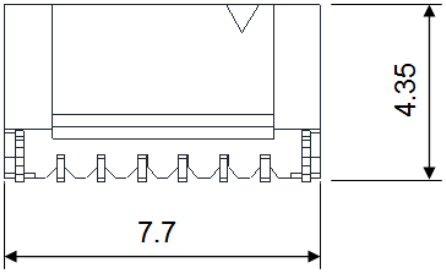
4.2.1 Connector Type

Backlight Connector	Manufacturer	Cvilux
	Part Number	CI1406M1VLD-NH
Mating Connector	Manufacturer	Cvilux
	Part Number	CI1406S0000-NH (Non-Locking type) CI1406SL000-NH (Locking type)

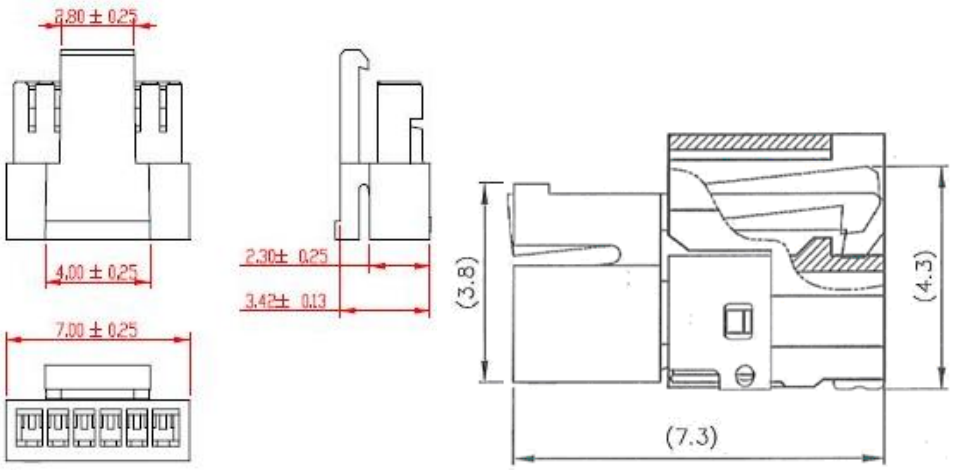
Backlight Connector dimension:

$H \times V \times D = 7.7 \times 3..98 \times 4.35, Pitch = 1.0(unit = mm)$



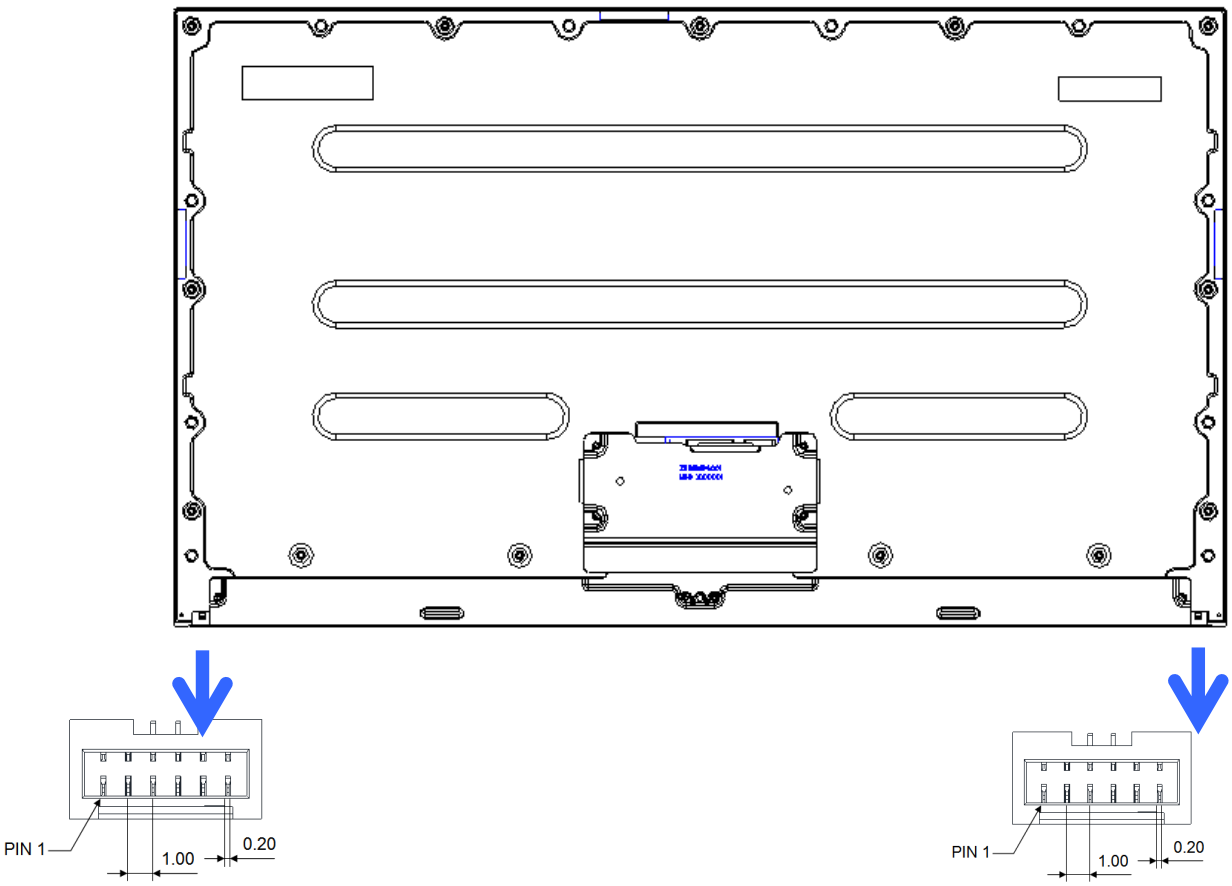


Mating Connector dimension:



4.2.2 Connector Pin Assignment

Pin#	Symbol	Description	Remark
1	Ch1	LED Current Feedback Terminal (Channel 1)	
2	Ch2	LED Current Feedback Terminal (Channel 2)	
3	V_{SLED}	LED Power Supply Voltage Input Terminal	
4	V_{SLED}	LED Power Supply Voltage Input Terminal	
5	Ch3	LED Current Feedback Terminal (Channel 3)	
6	Ch4	LED Current Feedback Terminal (Channel 4)	



4.3 Electrical Characteristics

4.3.1 Absolute Maximum Rating

Permanent damage may occur if exceeding the following maximum rating.

(Ta=25°C)

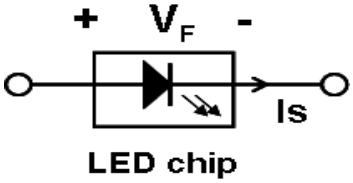
Symbol	Description	Min	Max	Unit	Remark
Is	LED String Current	0	150	[mA]	100% duty ratio

4.3.2 Recommended Operating Condition

Symbol	Description	Min.	Typ.	Max.	Unit	Remark
I_s	LED String Current		85	94	[mA]	100% duty ratio of LED chip; ***Note 4-7***
I_{SP}	HDR PEAK LED String Current		120	132	[mA]	100% duty ratio of LED chip; ***Note 4-7***
V_s	LED String Voltage	28.4	32.5	37.1	[Volt]	Is=85mA @ 100% duty ratio; ***Note 4-1&Note 4-5***
V_{SP}	HDR PEAK LED String Voltage	28.6	33.0	37.4	[Volt]	Is=120mA @ 100% duty ratio; ***Note 4-1&Note 4-5***
ΔVs	Maximum Vs Voltage Deviation of light bar			2.2	[Volt]	100% duty ratio of LED chip; ***Note 4-2***
P_{BLU}	LED Light Bar Power Consumption		22.1	25.2	[Watt]	Is=85mA ***Note 4-3***
P_{BLUP}	LED PEAK Light Bar Power Consumption		31.7	35.9	[Watt]	Is=120mA ***Note 4-3***
LT_{LED}	LED Life Time	30000			[Hour]	***Note 4-4***
OVP	Over Voltage Protection in system board	110% Vs(Max.)			[Volt]	***Note 4-5***

Note 4-1: Vs (Typ.) = V_F (Typ.) X LED No. (one string);

a. V_F: LED chip forward voltage @HDR off, V_F (Min.)=2.58, V_F(Typ.)=2.95, V_F(Max.)=3.37
b. The same euqation to calculate V_S(Min.) & V_S(Max.) for respective V_F(Min.) & V_F(Max.);
c. V_F: LED chip forward voltage @HDR on, V_F (Min.)=2.6, V_F(Typ.)=3.0, V_F(Max.)=3.4
d. The same euqation to calculate Vs(Min.) & Vs (Max.) for respective V_F (Min.) & V_F(Max.);



Note 4-2: ΔVs (Max.) = ΔV_F X LED No. (one string);

a. ΔV_F: LED chip forward voltage deviation (0.2V , each Bin of LED V_F)

Note 4-3: P_{BLU} (Typ.) = Vs (Typ.) X Is (Typ.) X 8 (8 is total String No. of BLU)

P_{BLU} (Max.) = Vs (Max.) X Is (Typ.) X 8

a. The same euqation to calculate P_{BLUP}(Typ.) & P_{BLUP}(Max.) for respective P_{BLU}(Typ.) & P_{BLU}(Max.);

Note 4-4: Definition of life time:

a. Brightness of LED becomes to 50% of its original value
b. Test condition: I_{SH} = 85 mA and 25°C (Room Temperature)

Note 4-5: Recommendation for LED driver power design:
Due to there are electrical property deviation in LED & monitor set system component after long time operation. AUO strongly recommend the design value of LED driver board OVP (over voltage protection) should be 10% higher than max. value of LED string voltage (Vs) at least.

Note 4-6: AUO strongly recommend "Analog Dimming" method for backlight brightness control for Wavy Noise Free. Otherwise, recommend that Dimming Control Signal (PWM Signal) should be synchronized with Frame Frequency

Note 4-7 Ensure that the LED light bar is not subjected either forward or reverse voltage while monitor set is on standby mode or not in use.

5 Reliability Test

AUO reliability test items are listed as following table. (*Bare Panel only*)

Items	Condition	Remark
Temperature Humidity Bias (THB)	Ta= 50°C, 80%RH, 300hours	
High Temperature Operation (HTO)	Ta= 50°C, 50%RH, 300hours	
Low Temperature Operation (LTO)	Ta= 0°C, 300hours	
High Temperature Storage (HTS)	Ta= 60°C, 300hours	
Low Temperature Storage (LTS)	Ta= -20°C, 300hours	
Vibration Test (Non-operation)	Frequency:10~57Hz/Vibration width(one side):0.075mm : 58~500Hz/Acceleration:9.8 m/s2 Sweep time: 11minutes Test period: 3 hours(1h for each direction of X,Y,Z)	
Shock Test (Non-operation)	Acceleration: 50 G Wave: Half-sine Active Time: 20 ms Direction: ±X, ±Y, ±Z (one time for each Axis)	
Thermal Shock Test (TST)	-20°C/30min, 60°C/30min, 100 cycles	***Note 5-1***
On/Off Test	On/10sec, Off/10sec, 30,000 cycles	
ESD (Electro Static Discharge)	Contact Discharge: ± 15KV, 150pF(330Ω) 1sec, 8 points, 25 times/ point.	***Note 5-2***
	Air Discharge: ± 15KV, 150pF(330Ω) 1sec 8 points, 25 times/ point.	
Altitude Test	Operation:18,000 ft Non-Operation:40,000 ft	

Note 5-1: a. A cycle of rapid temperature change consists of varying the temperature from -20°C to 60°C, and back again. Power is not applied during the test.
b. After finish temperature cycling, the unit is placed in normal room ambient for at least 4 hours before power on.

Note 5-2: EN61000-4-2, ESD class B: Certain performance degradation allowed
No data lost
Self-recoverable
No hardware failures.

ESD discharged points should avoid display area and periphery front bezel of display area. Suggest points were 4 side parallel edge of display area surface.

Metal front bezel must cover half area of BM (black matrix), and metal front bezel must connect with metal back bezel to protect source IC of panel by ESD damaged.

Note 5-3: Result Evaluation Criteria:
TFT-LCD panels test should take place after gradually cooling enough at room temperature.

In the normal application, there should be no particular problems that may affect the display function.

6 Shipping Label

The label is on the panel as shown below:

Note 6-1: For Pb Free products, AUO will add for identification.

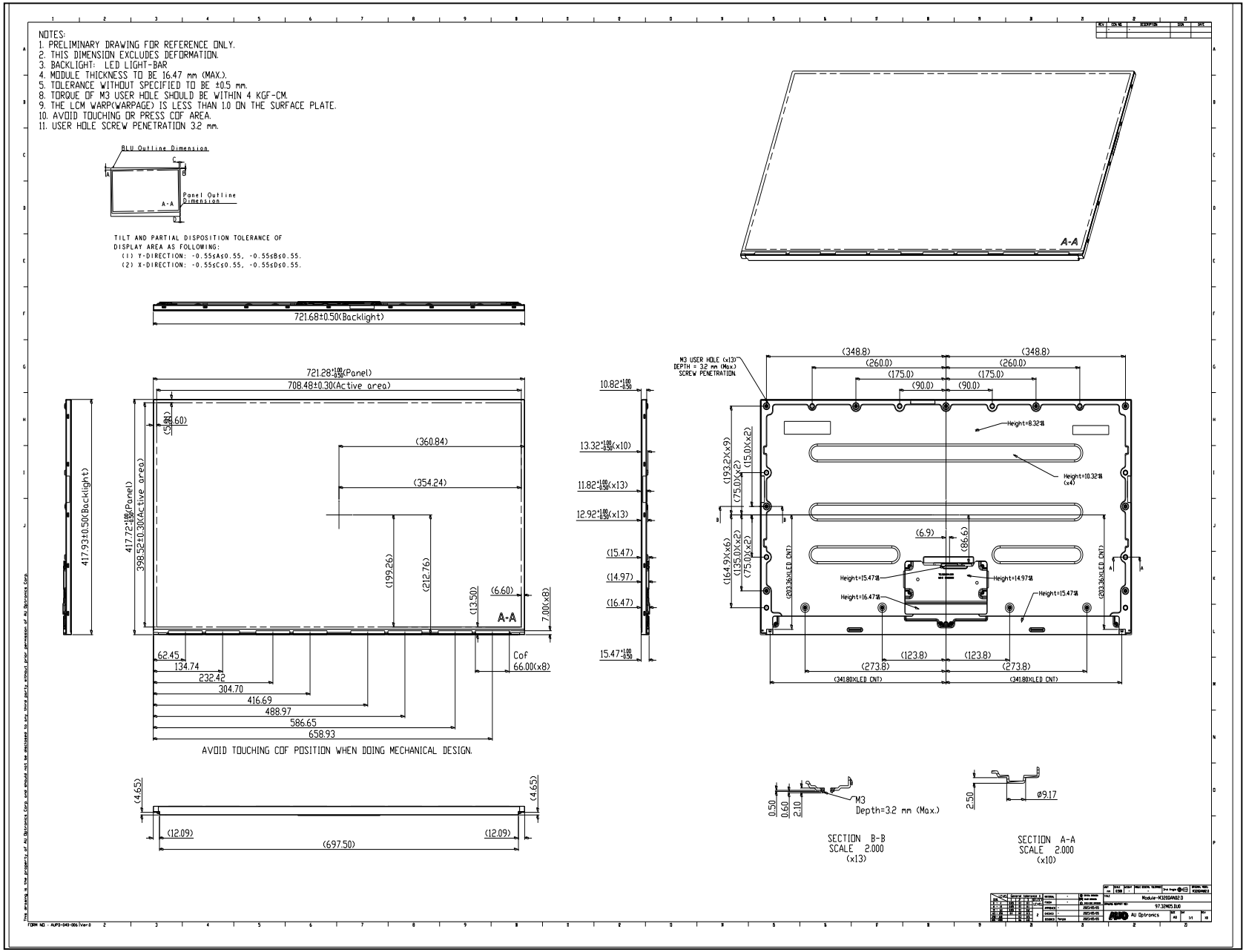
Note 6-2: For RoHS compatible products, AUO will add for identification.

Note 6-3: For China RoHS compatible products, AUO will add for identification.

Note 6-4: The Green Mark will be presented only when the green documents have been ready by AUO Internal Green Team.

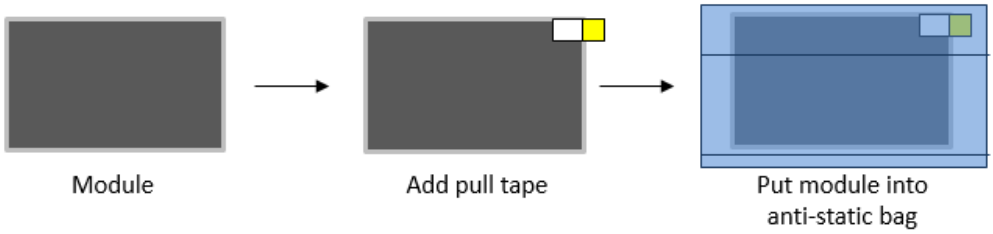
Note 6-5: To response ErP Lot5 regulation about "Cadmium (Cd) logo", display panel shall be labeled with additional new "Cd logo"

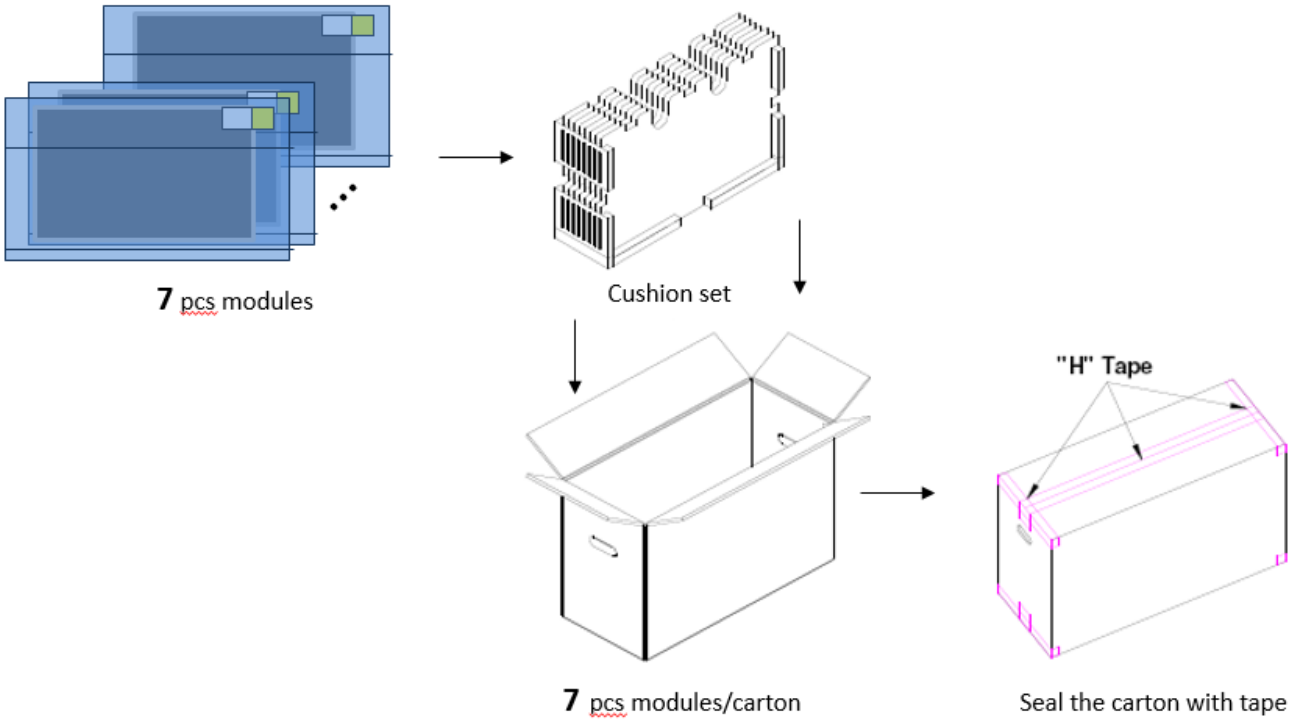
7 Mechanical Characteristics

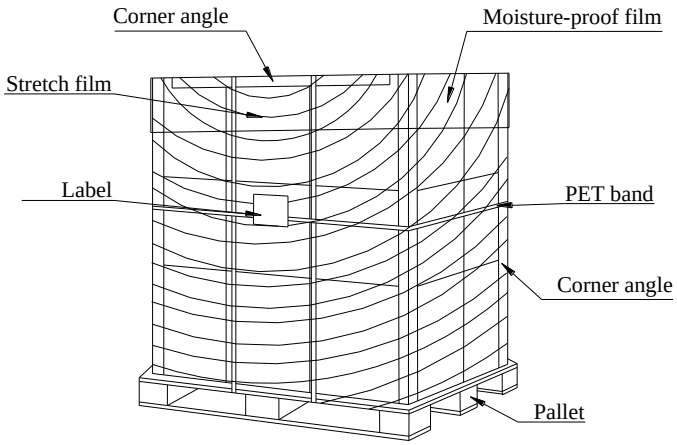


8 Packing Specification

8.1 Packing Flow







8.2 Pallet and shipment information

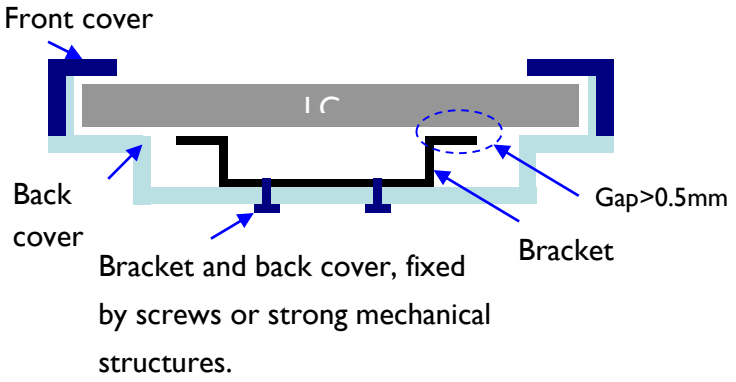
Item	Specification			Remark
	Q'ty	Dimension	Weight(kg)	
Panel	1	721.68mm (H) x 417.93mm (V) × 15.47mm (D) Typ.	4.8	
Cushion	1	-	4.54	
Box	1	805(L)mm x 280(W)mm x 514(H)mm		without Panel
Packing Box	7 pcs/Box	805(L)mm x 280(W)mm x 514(H)mm	38.14	with panel & cushion & Box
Pallet	1	1150(L)mm x 840(W)mm x 132(H)mm	13.6	
Pallet after Packing	8 boxes/pallet	1150(L)mm x 840(W)mm x 1160(H)mm	318.72	

9 Design Guide for System

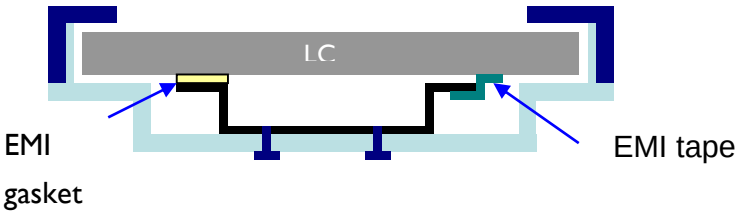
9.1 AHVA design guide

9.1.1 The gap between LCM and system rear bracket should be bigger than 0.5mm.

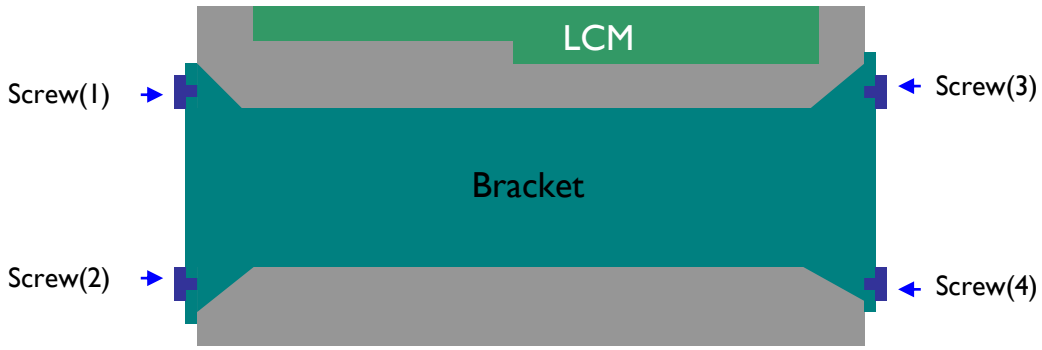
9.1.2 The system bracket should be fixed on back cover firmly.



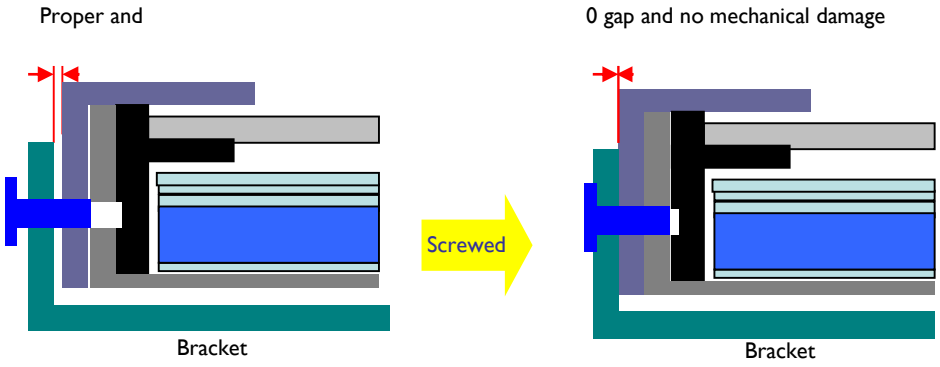
9.1.3 The EMI gasket should be uniform and not push panel strongly.



9.1.4 For stable assembly, the system bracket should use 4 screws to fix system and panel by dual sides.



9.1.5 The system bracket and panel should be in parallel with having no gap after inserting screws.



9.1.6 Avoid scratching LCM, the rib on system front-cover should not exceed the bottom edge of LCM's front-bezel.