A. General Description

C101UAN01.0 is an a-Si type Thin Film Transistor Liquid crystal Display (TFT-LCD) with AHVA (Advanced Hyper-Viewing Angle) technology. This model is composed of a TFT-LCD, driver ICs, FPCs, FPCA, backlight unit, and touch panel.

B. Features

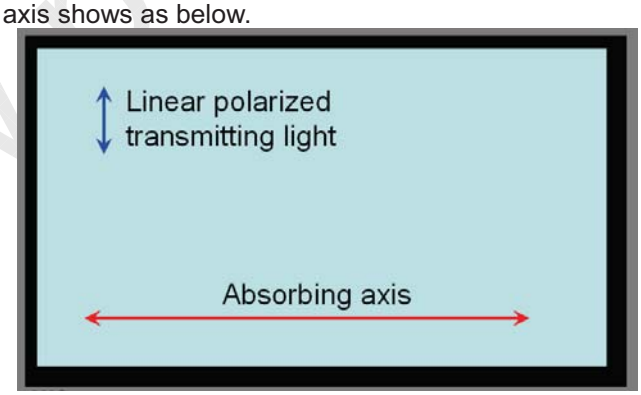
- 10.1" display
- 1920 x 1200 resolution in RGB stripe dot arrangement
- High brightness
- Interfaces: LVDS (8 bit, JEIDA/VESA, DE mode)
- AHVA – wide view technology
  RoHs compliance

C. Physical Specifications

1. TFT LCD Panel

NO.	Item	Unit	Specification	Remark
1	Display Resolution	dot	1920 RGB (H) x 1200 (V)	
2	Active Area	mm	217.44 (H) x 135.9 (V)	
3	Screen Size	inch	10.1 (Diagonal)	
4	Dot Pitch	μm	113.25	
5	Color Configuration	–	R. G. B. Stripe	
6	Color Depth	–	16.7M colors	
7	Overall Dimension	mm	236.96 (H) x 163 (V) x 8 (T)	Note. 1
8	Weight	g	425 g +/- 10%	
9	Display Mode	–	Normally Black	Note. 2

Note 1: FPC, PCBA, and screw bosses aren't included. 2D drawing is shown in Page 9.
Note 2: Transmission axis shows as below.



TFT-LCD Module Electrical Specifications

TFT LCD Panel Pin Assignment

Recommended Connector: FH41-60S-0.5SHED

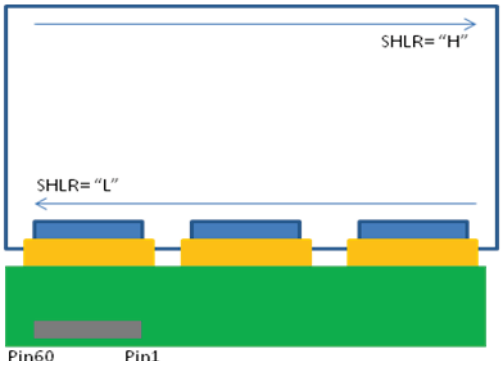
No.	Pin Name	I/O	Description	Remarks
1	NC	-	NC	
2	NC	-	NC	
3	LVFMT		LVDS format selection LVFMT = "H": VESA format LVFMT = "L": JEIDA format	Note 1
4	GND	G	Power Ground	
5	GND	G	Power Ground	
6	GND	G	Power Ground	
7	NC	-	NC	
8	VDD	I	3.3 V power supply	
9	VDD	I	3.3 V power supply	
10	VDD	I	3.3 V power supply	
11	NC	-	NC	
12	NC	I	AUO internal use	
13	NC	I	AUO internal use	
14	TP_SYNC	-	For TP used (output = HSYNC) Keep floating if no use in system side.	
15	SDA	I	Serial communication data input. (System side: pull High) Keep floating if no use in system side.	
16	NC	-	No Connect	
17	SCL	I	Serial communication clock input. (System side: pull High) Keep floating if no use in system side.	
18	IND_OUT	O	Abnormal signal detection Combine the source driver & gate driver detection result AB_IND="H",IC is at normal operation AB_IND="L",IC is at abnormal states	Note 2
19	NC	-	NC	
20	NC	-	NC	
21	NC	-	NC	
22	GND		Power Ground	
23	GND		Power Ground	
24	GND		Power Ground	
25	D13P		Positive LVDS differential input (Even)	
26	D13N		Negative LVDS differential input (Even)	
27	GND		Power Ground	
28	CLK1P		Positive LVDS differential clock input (Even)	

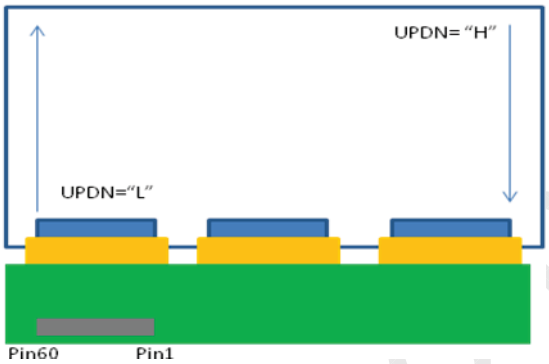
29	CLK1N		Negative LVDS differential clock input (Even)	
30	GND		Power Ground	
31	D12P		Positive LVDS differential input (Even)	
32	D12N		Negative LVDS differential input (Even)	
33	GND		Power Ground	
34	D11P		Positive LVDS differential input (Even)	
35	D11N		Negative LVDS differential input (Even)	
36	GND		Power Ground	
37	D10P		Positive LVDS differential input (Even)	
38	D10N		Negative LVDS differential input (Even)	
39	GND		Power Ground	
40	D03P		Positive LVDS differential input (Odd)	
41	D03N		Negative LVDS differential input (Odd)	
42	GND		Power Ground	
43	CLK0P		Positive LVDS differential clock input (Odd)	
44	CLK0N		Negative LVDS differential clock input (Odd)	
45	GND		Power Ground	
46	D02P		Positive LVDS differential input (Odd)	
47	D02N		Negative LVDS differential input (Odd)	
48	GND		Power Ground	
49	D01P		Positive LVDS differential input (Odd)	
50	D01N		Negative LVDS differential input (Odd)	
51	GND		Power Ground	
52	D00P		Positive LVDS differential input (Odd)	
53	D00N		Negative LVDS differential input (Odd)	
54	GND		Power Ground	
55	SHLR		Horizontal scan direction control	Note 3
56	UPDN		Vertical scan direction control	Note 4
57	GND		Power Ground	
58	NC		NC	
59	GND		Power Ground	
60	GND		Power Ground	
I: Digital signal input, **O**: Digital signal output, **G**: GND, **PI**: Power input; **T**: touch panel signal				

Note 1：
LVFMT = “H”: VESA forma (Default) ; LVFMT = “L”: JEIDA format.
Note 2：
IND_OUT = “L”: Abnormal states; IND_OUT = “H”: Normal operation. (If no used keep floating).
Note 3：
SHLR = “H”: Normal scanning (left-to-right) (Default); SHLR = “L”: Invert horizontal scanning (right-to-left).

Note 4：

UPDN = “H”: Normal scanning (up-down) (Default); UPDN = “L”: Invert vertical scanning (down-to-up).





Differential Input Data Format
VESA format

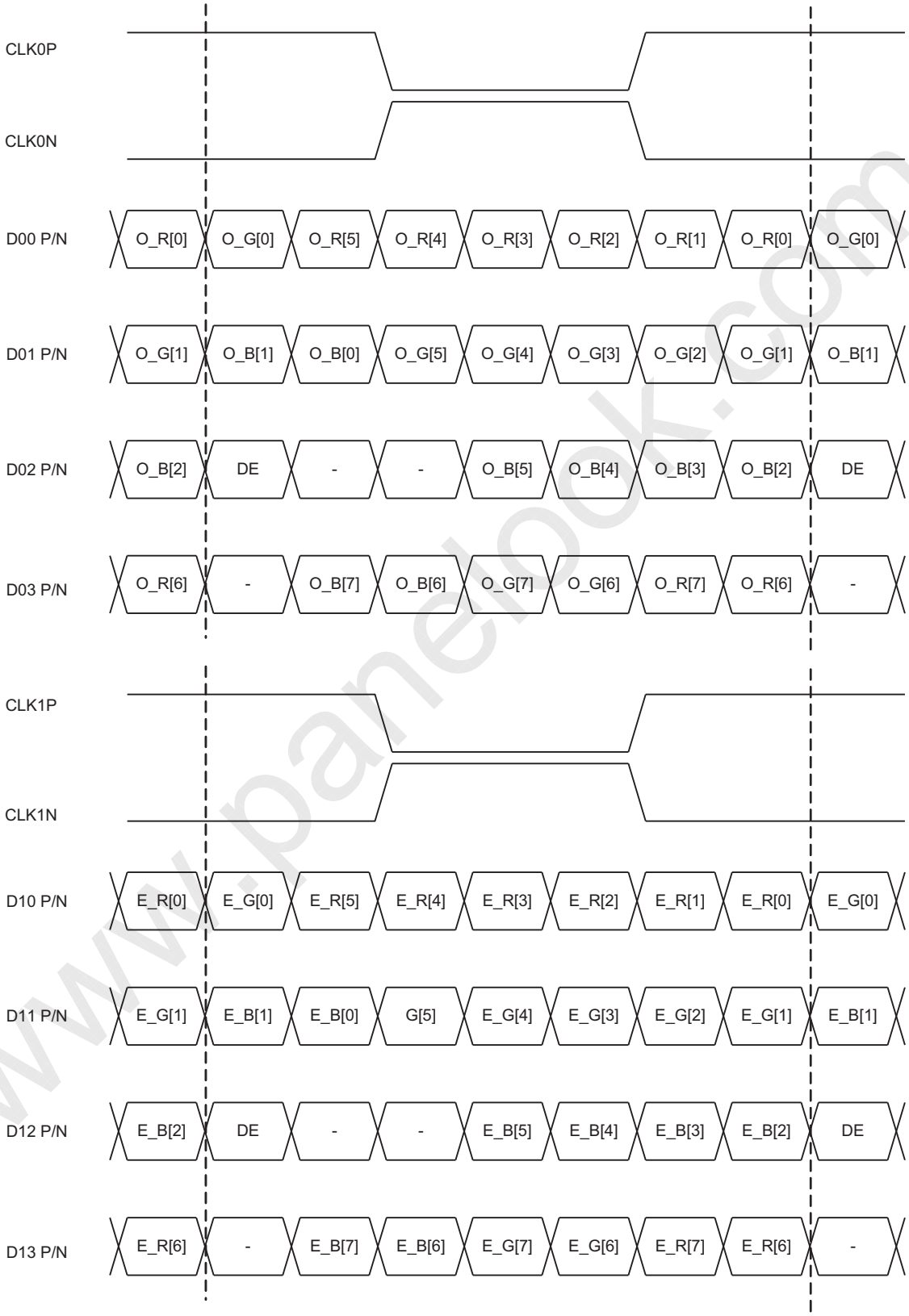


Fig. 1. LVDS input data VESA format

JEIDA format

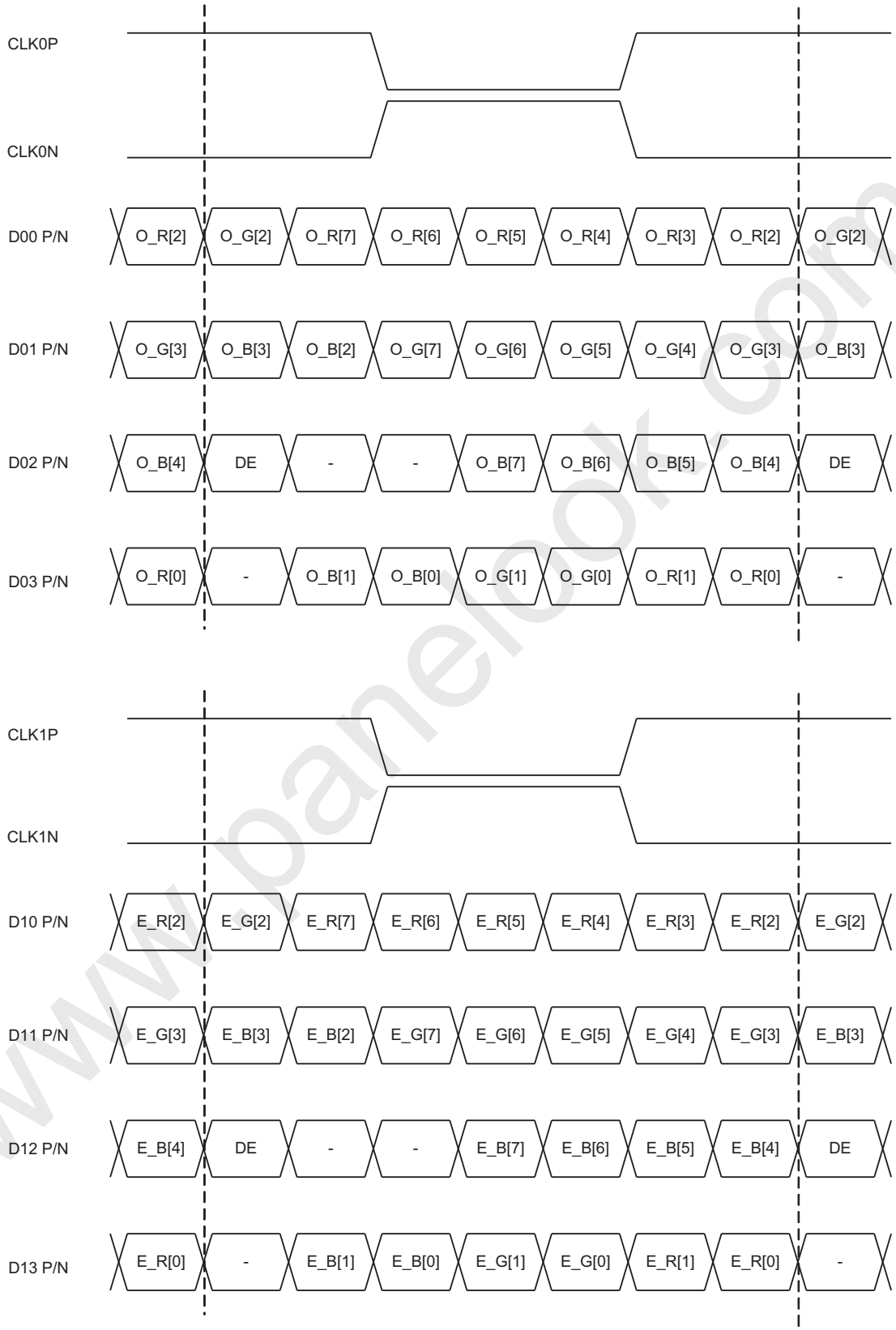
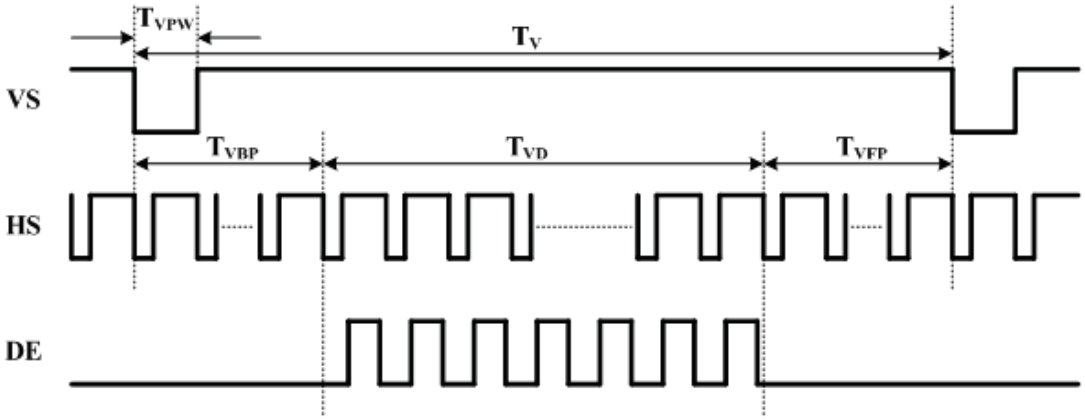
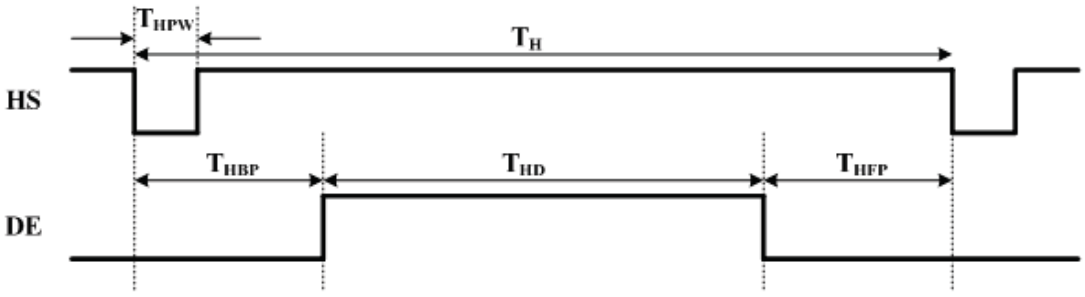
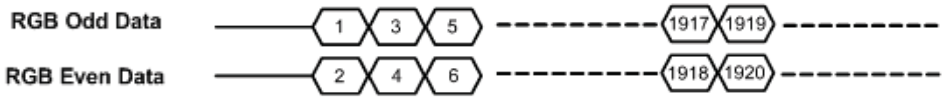


Fig. 2. LVDS input data JEIDA format

Input Timing Diagram







a. DE mode timing (Note 1)

Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark
CLK Frequency		F_{CLK}	73.9	74.2	85	MHz	
HSYNC	Period	T_H	1020	1024	1120	CLK	
	Horizontal display area	T_{HD}		960		CLK	
	Blanking	$T_{HBP} + T_{HFP}$	60	64	160	CLK	
VSYNC	Period	T_V	1206	1208	1265	HS	
	Vertical display area	T_{VD}		1200		HS	
	Blanking	$T_{VBP} + T_{VFP}$	6	8	65	HS	

Note 1: Both two ports of LVDS need to follow this timing chart

Absolute Maximum Ratings

Items	Symbol	Values		Unit	Condition
		Min.	Max.		
Power Voltage	VDD	-0.3	5	V	GND = 0 V
Input signal voltage	Vi	-0.3	VDD		
Operation Temperature	Topa	-30*	85	°C	Ambient
Storage Temperature	Tstg	-40	95	°C	Ambient

Note 1: Functional operation should be restricted under normal ambient temperature.
Note 2: *No permanent functional defect between -40 °C and -30 °C

DC Electrical Characteristics

The following items are measured under stable condition and suggested application circuit.

b. Power specification

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Power Supply	VDD	3	3.3	3.6	V	Note 1
	IVDD		500	700	mA	Note 1
	IVDD inrush current			1.2	A	

Note 1: Test pattern is the following picture.

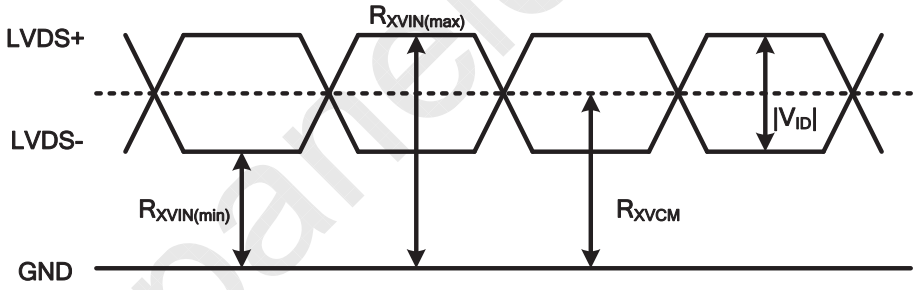
Fig. 3. Test pattern for power specification

Signal DC electrical characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Input high level voltage	V_{IH}	0.7VDD	-	VDD	V	Note 1
Input low level voltage	V_{IL}	GND	-	0.6	V	Note 1
Output high level voltage	V_{OH}	VDD - 0.4	-	VDD	V	Note 1
Output low level voltage	V_{OL}	GND	-	0.4V	V	Note 1
Differential input high threshold	R_{XVTH}	-	-	0.1	V	Note 2.3
Differential input low threshold	R_{XVTL}	-0.1	-	-	V	Note 2.3
Input differential voltage	$\|V_{ID}\|$	0.2	-	$(1.5 - R_{XVCM})*2$	V	Note 2.3
Differential Input Common Mode Voltage	R_{XVCM}	1	1.2	1.4	V	Note 2.3

Note 2: TTL interface signal DC characteristics
Note 3: LVDS interface signal DC characteristic
Note 4: The VID of transceiver suggest up to +/-400mV, this is better solution for receivers at high speed transmission

Single-end Signal



Differential Signal

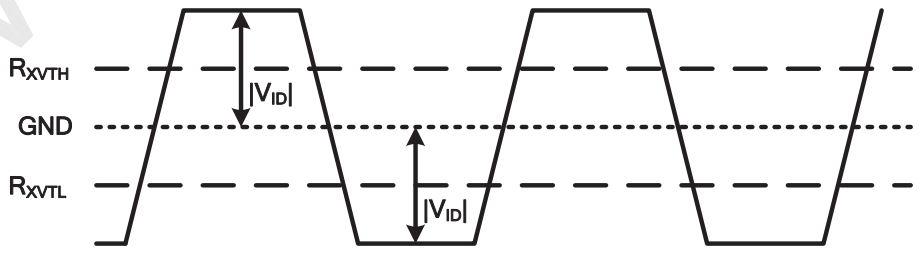


Fig. 4. LVDS DC characteristics diagram

AC Electrical Characteristics

c. Input AC characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
VDD power on slew time	T_{POR}	1	-	20	ms	From 0V to 90% VDD Note 1

Note 1: The inrush current spec should follow VDD power on slew time which min value is 1 ms and max value is 20 ms. Inrush current may be out of spec.

Fig. 6. VDD timing diagram

d. Repower ON / OFF

Parameter	Value			Unit
	Min.	Typ.	Max.	
T1	1000	--	-	ms

Note: VDD voltage **must be** less than 0.1V then can power on without following the minimum value.

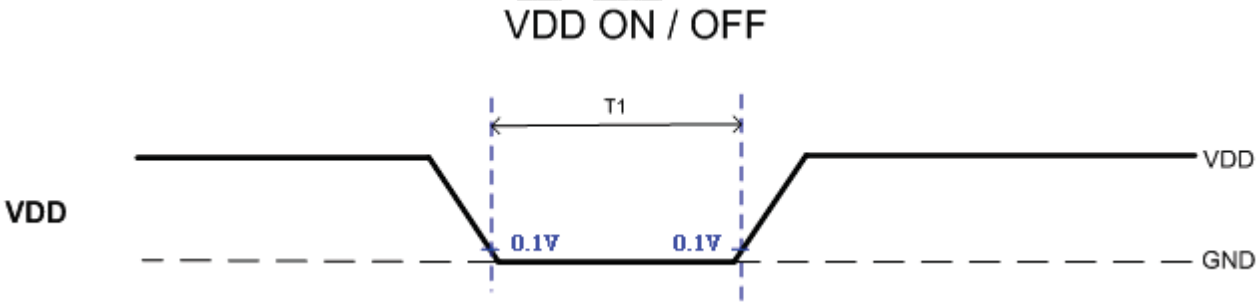


Fig. 7. VDD timing diagram

e. Differential signal AC characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Clock frequency	R_{xFCLK}	73.9	74.2	85	MHz	
Clock high time	T_{LVCH}	-	$4/(7*T_{LVCLK})$	-	ns	
Clock low time	T_{LVCL}	-	$3/(7*T_{LVCLK})$	-	ns	
Input data skew margin	T_{RSKM}	-	-	0.25	UI	VCC_IF=1.8V w/o SSC
1 Data bit time	UI	-	1/7	-	T_{LVCLK}	

Note 1: For the Data Skew Margin, "Input Signal Skew + Input Signal Jitter" must be smaller than TRSKM.

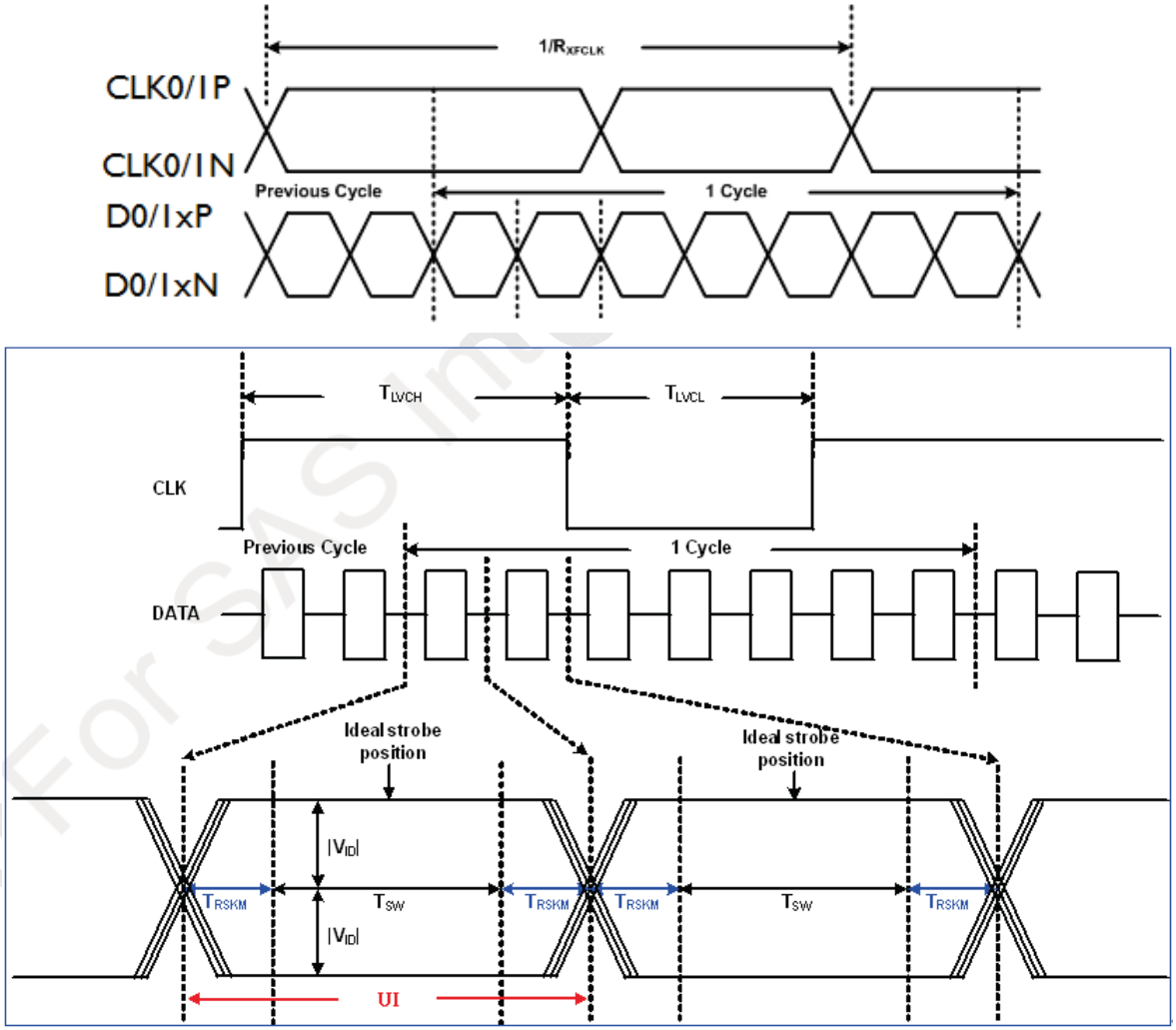
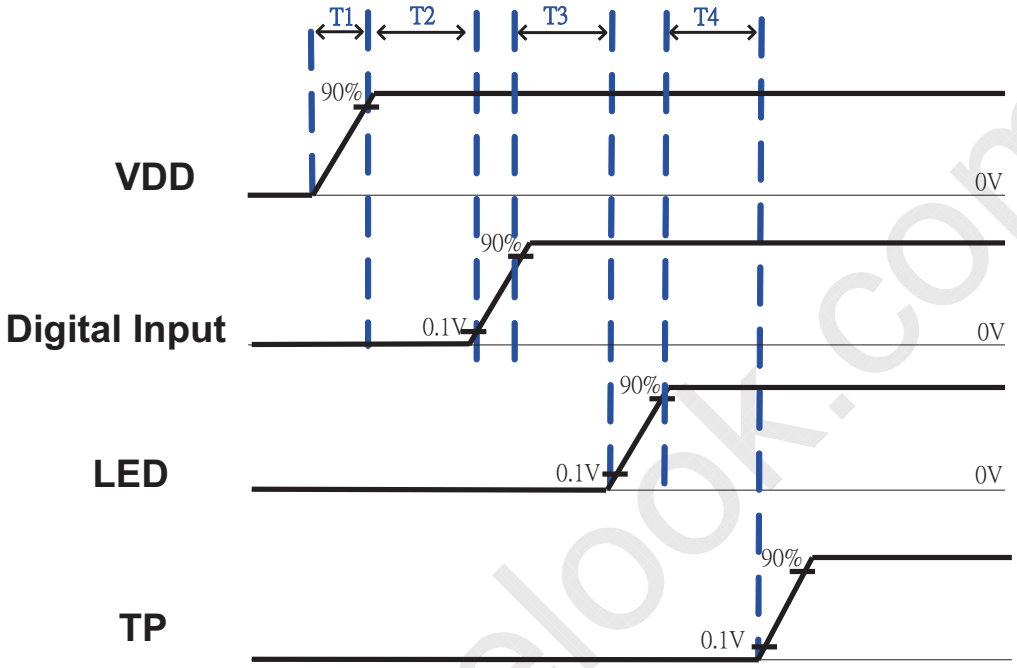


Fig. 8 LVDS AC characteristics diagram

Power On/Off Sequence

The LCD adopts high voltage driver IC, so it could be permanently damaged under a wrong power on/off sequence. The suggested LCD power sequence is below:

f. Power on sequence



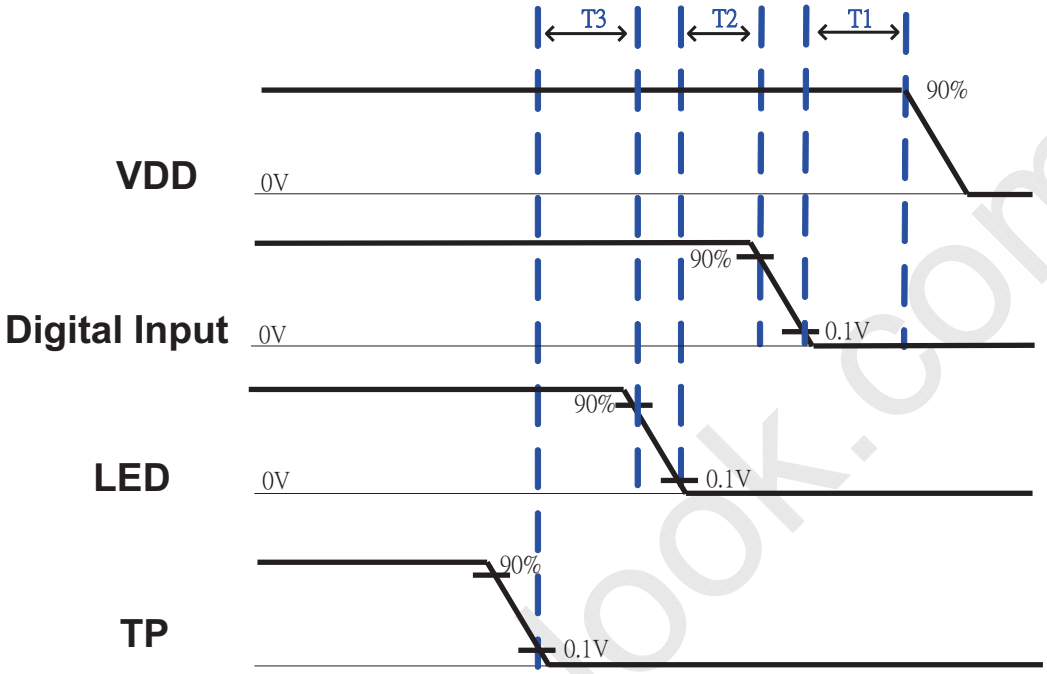
Power on timing:

Parameter	Value			Units
	Min.	Typ.	Max.	
T1	1		20	ms
T2	1			ms
T3	160			ms
T4	120			ms

Note: Digital Input are LVFMT, SHLR, UPDN and LVDS signals.

Power off sequence

Power off timing



Parameter	Value			Units
	Min.	Typ.	Max.	
T1	16.67			ms
T2	35			ms
T3	20			ms

Optical Specifications (Note 1, 2)

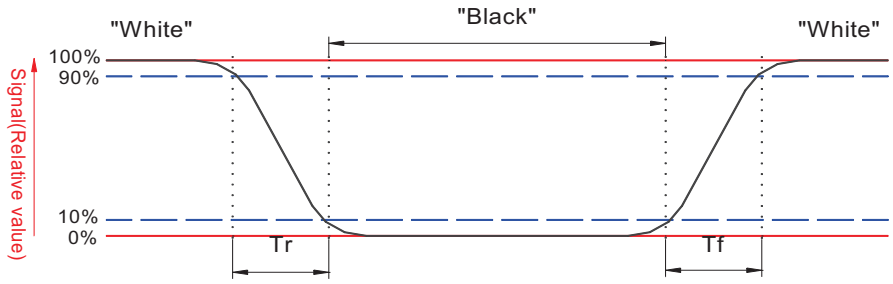
Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response Time (25°C)	Tr+ Tf	θ = 0°	-	-	25	ms	Note 3, 4
Response Time (-30°C)	Tr+ Tf	θ = 0°	-	-	350	ms	
Contrast ratio	CR	θ = 0°	1100	1500	-		Note 4, 5, 6
Viewing Angle Top Bottom Left Right		θ = 80°, Φ = 90° θ = 80°, Φ = 270° θ = 80°, Φ = 180° θ = 80°, Φ = 0°	CR ≧ 10	-	-	deg.	Note 5, 6, 7, 9
Brightness	Y_L	θ = 0°	1100	1400	-	cd/m^2	Note 1, 2, 8
White Chromaticity	X	θ = 0°	0.274	0.304	0.334		Note 9
	Y	θ = 0°	0.287	0.317	0.347		
Red Chromaticity	X	θ = 0°	0.634	0.664	0.694		
	Y	θ = 0°	0.281	0.311	0.341		
Green Chromaticity	X	θ = 0°	0.267	0.297	0.327		
	Y	θ = 0°	0.630	0.660	0.690		
Blue Chromaticity	X	θ = 0°	0.119	0.149	0.179		
	Y	θ=0°	0.031	0.061	0.091		
NTSC Ratio	-	-	80	85	-	%	
Uniformity of white pattern	-	-	80	-	-	%	Note 10

Note 1: Measurement should be performed in the dark room, optical ambient temperature = 25 °C

Note 2: To be measured in the center area of TFT-LCD with a field angle of 1° by Topcon luminance meter SR3, after 10 minutes operation and warm up 30 minutes.

Note 3: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black state” to “white state” (falling time) and from “white state” to “black state” (rising time), respectively.



Note 4: Based on liquid crystal characteristics, the response time will become slower and the color of panel will become darker than the above optical specification when ambient temperature is below 25 °C.

$$\text{Contrast ratio} = \frac{\text{Photo detector output when LCD is at "White" state}}{\text{Photo detector output when LCD is at "Black" state}}$$

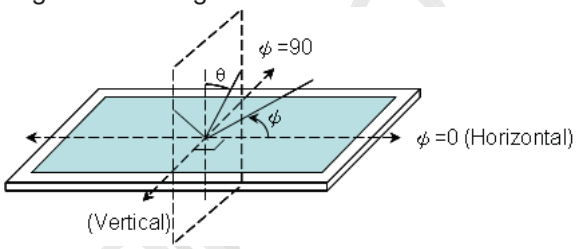
Note 5: Contrast ratio is calculated with the following formula.

White : White : RGB data = ”11111111” (V1 = 12.4 V & V18 = 0.6 V)

Black : RGB data = ”00000000” (V9 = 6.9 V & V10 = 6.1 V)

The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened

Note 6: Definition of viewing angle: refer to figure as below.

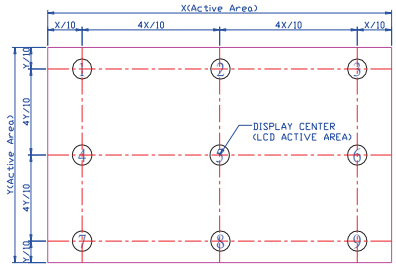


Note 7: Viewing angles are measured at the center of the panel when all the input terminals of LCD oanel are electrically opened.

Note 8: Brightness is measured at the center of the display.

Note 9: The viewing angles are measured at the center area of the panel when all the input terminals of LCD panel are electrically opened. If user finds that display is out of color range, AUO will proceed to RMA (Return Material Authorisation) process to exchange panel piece by piece without the failure rate counting.

Note 10: Luminance Uniformity of these 9 points is defined as below: (1 : 4 : 4 : 1)



$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

G. Reliability Test Items (Note 1 ~ 7)

No.	Test items	Conditions		Remark
1	High temperature storage	Ta= 95 °C	240 Hrs	
2	Low temperature storage	Ta= -40 °C	240 Hrs	
3	Low temperature operation	Ta= -30 °C	240 Hrs	
4	High temperature operation	Ta= 85 °C	240 Hrs	Note 5,6
5	High temperature and high humidity	Ta= 65 °C, 90 % RH	240 Hrs	Note 5,6
6	Thermal Shock	-40 °C (30min) ~ 85 °C (30min) / 632 cycles 1 Hrs/cycle		Note 5,6
7	Power Temperature Cycling	-30 °C ~ 85 °C / 3hr/cycle / 211 hrs		Note 5,6
8	Humid Heat Cyclic	-10 °C /+65 °C, 93% 10 days (240h)		Note 5,6
9	Shock	100 G, 6 ms, ±X, ±Y, ±Z 3 times for each direction		(Note 6)
10	Electrostatic Discharge	Contact = ± 8 kV, 1 sec, 8 point, 10 times/point class B (R = 330 Ω, C = 150 pF) Air = ± 15 kV, 1sec, 8 point, 10 times/point class B (R = 330 Ω, C = 150 pF)		IEC61000-4-2 (note 4,6)
11	Vibration	Frequency range	8 ~ 33.3 Hz	JIS D1601,A10 Condition A (Note 6)
		Stoke	1.3 mm	
		Sweep	2.9 G, 33.3 ~ 400Hz	
		Cycle	15 min.	
		2 hours for each direction of X, Z 4 hours for Y direction		
12	Vibration (with carton)	Random vibration: 0.015 G^2/Hz from 5 ~ 200 Hz –6 dB/Octave from 200 ~ 500 Hz		IEC 68-34
13	Drop (with carton)	Height: 60 cm 1 corner, 3 edges, 6 surfaces		

Note 1: Test techniques follow IEC61000-4-2 standard. Class B – Some performance degradation allowed.
No data lost. Self-recoverable. No hardware failures.