



L506 MINI PCIe Hardware Design

Version: V1.0

Date: 2016-07-08





Notice

Some features of the product and its accessories described herein rely on the software installed, capacities and settings of local network, and therefore may not be activated or may be limited by local network operators or network service providers.

Thus, the descriptions herein may not exactly match the product or its accessories which you purchase. Shanghai Mobiletek Communication Ltd reserves the right to change or modify any information or specifications contained in this manual without prior notice and without any liability.

Copyright

This document contains proprietary technical information which is the property of Shanghai Mobiletek Communication Ltd. copying of this document and giving it to others and the using or communication of the contents thereof, are forbidden without express authority. Offenders are liable to the payment of damages. All rights reserved in the event of grant of patent or the registration of a utility model or design. All specification supplied herein are subject to change without notice at any time.

DISCLAIMER

ALL CONTENTS OF THIS MANUAL ARE PROVIDED "AS IS". EXCEPT AS REQUIRED BY APPLICABLE LAWS, NO WARRANTIES OF ANY KIND, EITHER EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, ARE MADE IN RELATION TO THE ACCURACY, RELIABILITY OR CONTENTS OF THIS MANUAL.

TO THE MAXIMUM EXTENT PERMITTED BY APPLICABLE LAW, IN NO EVENT SHALL SHANGHAI MOBILETEK COMMUNICATION LTD BE LIABLE FOR ANY SPECIAL, INCIDENTAL, INDIRECT, OR CONSEQUENTIAL DAMAGES, OR LOSS OF PROFITS, BUSINESS, REVENUE, DATA, GOODWILL SAVINGS OR ANTICIPATED SAVINGS REGARDLESS OF WHETHER SUCH LOSSES ARE FORSEEABLE OR NOT.



Version History

Date	Version	Description of chage	Author
2016-07-08	V1.0	Initial	
	N		



Overview:

This document is suitable for products: L506 MINI PCIe Module.

From the detail introduce of L506 MINI PCIe module hardware interface, guide the user to the module hardware design, and more convenient kinds of wireless terminals in product design based on the modules.

Reader

This document is design for the people as below:

- System design engineer
- Structural Engineer
- Hardware Engineer
- Software Engineer
- Test Engineer

Content Introduction

This document include 5 chapters ,the content as below:

Chapter	Content
1 Summarize	Introduce the Technique Specification、the related
1 Summanze	reference of standards of L506 MINI PCIe module
2 Din Description	Introduce the name and function about the Pins on L506
2 Pin Description	MINI PCIe module
3 Hardware interface	Introduce the design of hardware interface on L506 MINI
3 Hardware interface	PCIe module.
4 Modular structure size	Introduction Appearance, structure, size and manufacturing
and production	considerations of L506 MINI PCIe module
5 Electrical	Introduction electrical work anyironment and DE
characteristics ,Reliability	Introduction electrical, work environment and RF
and RF characteristics	characteristics of L506 MINI PCIe module



Catalog

1	About this document	1
1.1	Range of Application	1
1.2	Referenced document	1
1.3	Shorthand	2
2	Introduction	3
2.1	Mechanical characteristics	4
2.2	Technical Parameters	6
2.3	Product Features Description	8
2.3.1	Baseband Features	8
2.3.2	RF characteristics Features introduce	9
3	Interface Introduction	
3.1	Definition of Pin	
3.1.1	Definition of Pin I/O parameter	
3.1.2	Deployment diagram of Pin	12
3.1.3	Pin description	13
3.2	Working conditions	20
3.3	Interface level features	20
3.4	The power interface	21
3.4.1	Power pin description	21
3.5	(U)SIM card interface	21
3.5.1	Pin description	21
3.5.2	Electrical characteristics	22
3.5.3	(U)SIM card Interface application	22
3.6	USB2.0 interface	23
3.6.1	Pin description	23
3.6.2	Electrical characteristics	23
3.6.3	USB Interface application	23



L506 MINI	PCIe Hardware Design	MobileTek →	
3.7	UART interface		24
3.7.1	Pin description		24
3.7.2	Electrical characteristics		25
3.8	PON_RST_N reset signal		25
3.8.1	Pin description		25
3.8.2	Interface application		26
3.9	LED_WWAN_N signal		26
3.9.1	Pin description		26
3.9.2	Interface application		
3.10	W_DISABLE_N signal		27
4	product electrical characteristics		28
4.1	Power characteristics		28
4.1.1	Power supply		28
4.1.2	Working current		
5	Design guidance		
5.1	General design rules and requirements		29
5.2	RF circuit design		29
5.2.1	RF antenna circuit design		29
5.2.2	Antenna design early considerations		30
5.3	Mini PCI Express connector		36
5.4	EMC and ESD design suggestion		36



Figure catalog

Figure 2-1	Real product Figure show	4
Figure 2-2	Size of module	5
Figure 2-3	System Connection frame structure diagram	9
Figure 3-1	Deployment diagram of Pin (Top view)	13
Figure 3-2	(U)SIM card interface application	23
Figure 3-3	USB Connection diagram	24
Figure 3-4	Module and AP(application device) Application processor	25
Figure 3-5	Reset circuit	26
Figure 3-6	Status indicator reference circuit	27
Figure 5-1	The radio frequency interface test (HRS U.FL-R-SMT-1)	30
Figure 5-2	Test cable	30
Figure 5-3	Deployment diagram of Pin	32
Figure 5-4	Main antenna matching circuit diagram (MAIN_ANT)	33
Figure 5-5	LTE Diversity antenna matching circuit diagram (AUX_ANT)	33
Figure 5-6	GNSS active antenna matching circuit diagram (GNSS_ANT)	34
Figure 5-7	GNSS passive antenna matching circuit diagram (GNSS_ANT)	34
Figure 5-8	Mini PCIe connector	36



Table catalog

Table 1-2	Shorthand list	2
Table 2-1	The main technical parameter:	6
Table 3-1	Definition of Pin I/O parameter	12
Table 3-2	Standard edition MINI PCIE Pin description(no codec)	13
Table 3-3	Integrate codec edition MINI PCIe Pin description	16
Table 3-3	Working conditions	20
Table 3-4	Digital signal v range	20
Table 3-5	(U)SIM card Signal group definition and description	21
Table 3-6	UART Signal definition	24
Table 3-7	Light state definition	27
Table 3-8	Light state definition	27
Table 4-1	Input voltage	28
Table 4-2	Working current	28
Table 5-1	Antenna pin definition	32



1 About this document

1.1 Range of Application

This document is a customers design for Wireless Internet access products, apply to hardware development guidance HSUPA Mini PCIe Module L506 products. Users need to according to the requirement and guidance in this document when design, the document applies only used to hardware application development L506 Mini PCIe products The purpose of writing

This document provides the design and development basis for the user of the module product. By reading this document, the user can have an overall understanding of the products, the technical parameters of the product have a clear understanding, and in this document based on the successful completion of the application development of wireless 3G Internet access products or equipment.

This document provides not only hardware development product features and technical parameters, but also provides product reliability testing and related testing standards, business functions to achieve the process, the RF circuit design performance and user guide.

Both provide a more comprehensive design reference to the user.

1.2 Referenced document

In addition to this hardware documentation, we also provide product development boards based on this operating instructions manual and software development instruction manual,

Table 1-1 is a list of supporting documentation.



Table 1-1 Supporting documentation list

No.	The name of document	
1	L506 AT Command User Guide.pdf	
2	L506 Hardware Design.pdf	

1.3 Shorthand

Table 1-2 is an explain for the shorthand in the document

Table 1-1 Shorthand list

shorthand	Full name
AP	Another name of DTE
BER	Bit Error Rate
DL	Downlink
DPCH	Dedicated Physical Channel
ESD	Electro-Static discharge
GPRS	General Packet Radio Service
GSM	Global Standard for Mobile Communications
I/O	Input/output
LED	Light Emitting Diode
PWL	Power Level
SIM	Subscriber Identification Module
SMT	SuRFace Mount Technology
SPI	Serial Peripheral Interface
UMTS	Universal Mobile Telecommunication System
WCDMA	Wideband Code Division Multi Access
HSUPA	High Speed Uplink Packet Access



2 Introduction

This product is a 4G wireless Internet access with Mini PCIe interface, this product has the advantages about , Internet-speed, small size, light weight, high reliability, can be applied to various products and devices with wireless Internet access function widely. The features of modules are as follows :

- 1) Support frequency range: UMTS/HSDPA/HSUPA 900(850)/2100(1900)MHz、 GSM/GPRS/EDGE 850/900/1800/1900MHz ;
- 2) Provide High-speed data access services with GSM/GPRS/EDGE、UMTS/HSDPA/HSUPA under CMCC.
 - 3) Support SMS;
 - 4) Provide USIM card interface (3.0V/1.8V); USB2.0 interface. UART interface.

W_DISABLE_N \ LED_WWAN_N interface and so on;





Figure 2-1 Real product Figure show

2.1 Mechanical characteristics

The size of the produce module is 51*30mm , height is 5.2mm. Figure 2-2 is the Dimensions type map about this produce module.



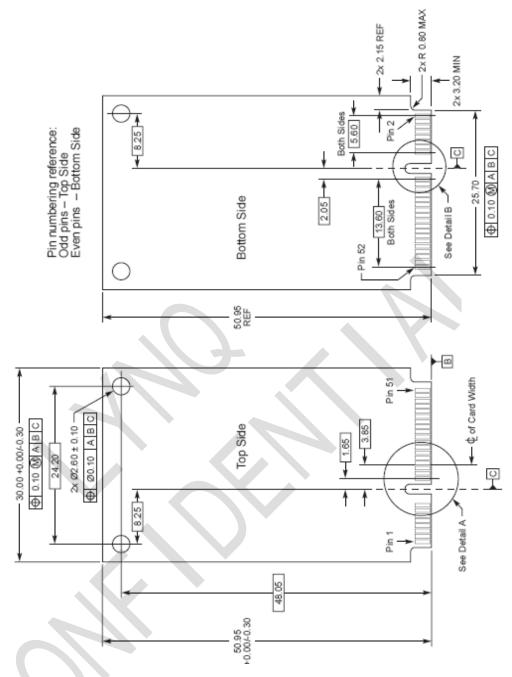


Figure 2-2 Size of module



2.2 Technical Parameters

The main characteristics of the product is Mechanical characteristics, baseband, RF, technical standards and environmental characteristics. Table 2-1 is the main technical parameter and characteristics which the product support.

Table 2-1 The main technical parameter:

Title	Parameters of the item	Specifications	
Mechanical characteristics	Size(L*W*H)	51mm * 30mm * 5.2mm	
	Weight	About 10g	
	Encapsulation type	52Pin Mini PCIE interface	
	Processor architecture	MDM 9x07(Qualcomm)	
	(U)SIM/SIM	Support 3V SIM card and 1.8V SIM card	
	USB interface	USB 2.0 HIGH SPEED	
Baseband	Maximum power consumption 1	1.9W	
	Voltage	3.0-3.6V, special3.3V	
	Electric current 2	peak current ≤ 2A	
		The average current when normal work ≤ 600mA	
		The average current when normal work(without task) ≤ 30mA	
		standby current ≤ 6mA	
		TDD-LTE B38/B39/B40/B41	
		FDD-LTE B1/B3/B7/B8/B20	
		TD-SCDMA B34/B39	
	Frequency Range	UMTS/HSDPA/HSPA+ B1/B8	
		GSM/GPRS/EDGE 900/1800 MHz	
RF		GPS/BEIDOU/GLONASS	
	·	AGPS	
	Diversity reception	TDD-LTE B38/B39/B40/B41	
	frequency range	FDD-LTE B1/B3/B7/B8/B20	



		LTE OAT
		LTE CAT4
		Uplink up to 50Mbps,
		Downlink up to 150Mbps
		TD-HSDPA/HSUPA
		Uplink up to 2.2 Mbps,
		Downlink up to 4.2 Mbps
		TD-SCDMA
		Uplink up to 128Kbps,
	Data rate	Downlink up to 384Kbps
	Data rate	HSPA+
		Uplink up to 5.76 Mbps,
		Downlink up to 42 Mbps
		UMTS
		Uplink/Downlink up to 384Kbps
		EDGE Class12:
	(7	Max. 236.8Kbps(DL),Max. 236.8Kbps(UL)
		GPRS Class12:
		Max. 85.6Kbps(DL), Max. 85.6Kbps(UL)
technical standards	Operation system	Windows XP (SP2 and later)
		Windows Vista
		Windows 7
		Linux
		Android
	operating temperature	-30 to 75° C
	storage temperature	-40 to 90° C
	humidity	5%~ 95%
Environmental	RAS dial	Support
characteristics		
	SMS	Support
	Lock Network	Support
Application	SIM READER	Support
	AT Commands	Compatible 3GPP TS 27.007, 27.005 and AT command
	Upgrade	Support

\mathbf{m}	Attention:	
	Auennon.	



- 1: The maximum power consumption get from the average value under the maximum transmitted power
- 2: The peak current、the average current when normal work、the average current when normal work(without task) are get the largest data when the module is test under the maximum power consumption. The standby current data is get from the test under SLEEP mode.
- 3: Beyond the limits of the application conditions, it can permanently damage the module..

2.3 Product Features Description

2.3.1 Baseband Features

The baseband features include the follow signal on the product: the signal of USB interface, the signal of USIM card interface, the signal of UART interface, the signal of Network Status Indicator, the signal of Reset and the control signal of WAKE_N, the signal of W_DISABLE_N, power, floor and so on. Figure 2-3 is System Connection frame structure diagram.

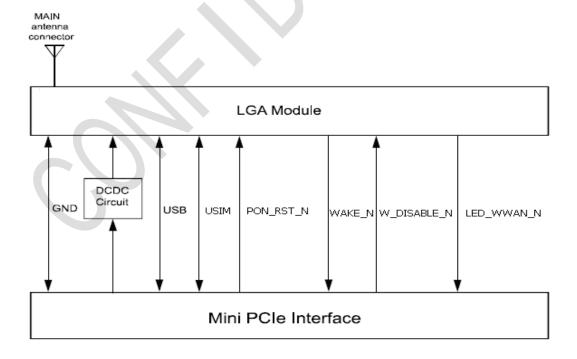




Figure 2-3 System Connection frame structure diagram

2.3.2 RF characteristics Features introduce

RF Function Overview:

- Four-Band TDD-LTE B38/B39/B40/B41
- Five-Band FDD-LTE B1/B3/B7/B8/B20
- Dual-Band TD-SCDMA B34/B39
- Dual-Band UMTS/HSDPA/HSPA+ B1/B8
- GSM/GPRS/EDGE 900/1800 MHz
- GPS/BEIDOU/GLONASS

The operating frequency range of the transmitter is shown in table 2-2.

Table 2-2 RF frequency band

Working band	Upstream band (Uplink)	Downlink frequency (Downlink)
UMTS900	890 MHz — 915MHz	925 MHz — 960 MHz
UMTS1900	1850 MHz — 1910 MHz	1930 MHz — 1990 MHz
GSM900 <	890 MHz — 915MHz	925 MHz — 960MHz
GSM1800	1710 MHz — 1785MHz	1805 MHz — 1880MHz
TD-SCDMA B34	2010 ~ 2025 MHz	2010 ~ 2025 MHz
TD-SCDMA B39	1880 ~ 1920 MHz	1880 ~ 1920 MHz
TDD_LTE B38	2570 MHz~2620 MHz	2570 MHz~2620 MHz
TDD_LTE B39	1880 MHz~1920 MHz	1880 MHz~1920 MHz
TDD_LTE B40	2300 MHz~2400 MHz	2300 MHz~2400 MHz
TDD_LTE B41	2555 ~ 2655 MHz	2555 ~ 2655 MHz
FDD_LTE B1	1920 MHz~1980 MHz	2110 MHz~2170 MHz
FDD_LTE B3	1710 MHz~1785 MHz	1805 MHz~1880 MHz
FDD_LTE B7	2500 MHz~2570 MHz	2620 MHz~2690 MHz
FDD_LTE B8	880 MHz~915 MHz	925 MHz~960 MHz
FDD_LTE B20	832 MHz~862 MHz	791 MHz~821 MHz
GPS L1 BAND	-	1574.4 ~ 1576.44 MHz
GLONASS	-	1598 ~ 1606 MHz
BEIDOU B1	-	1559.05 ~ 1563.14 MHz

Table 2-3 Conducted transmission power

Working Band	Max Power	Min Power
UMTS900	24dBm +1/-3dB	<-50dBm



UMTS1900	24dBm +1/-3dB	<-50dBm
GSM900	33dBm ±2dB	5dBm ± 5dB
DCS1800	30dBm ±2dB	0dBm ± 5dB
GSM900(8-PSK	27dBm ±3dB	5dBm ± 5dB
)		
DCS1800(8-PS	26dBm +3/-4dB	0dBm ± 5dB
K)		
TD-SCDMA B34	24dBm +1/-3dB	<-50dBm
TD-SCDMA B39	24dBm +1/-3dB	<-50dBm
TDD_LTE B38	23dBm +/-2.7dB	<-40dBm
TDD_LTE B39	23dBm +/-2.7dB	<-40dBm
TDD_LTE B40	23dBm +/-2.7dB	<-40dBm
TDD_LTE B41	23dBm +/-2.7dB	<-40dBm
FDD_LTE B1	23dBm +/-2.7dB	<-40dBm
FDD_LTE B3	23dBm +/-2.7dB	<-40dBm
FDD_LTE B7	23dBm +/-2.7dB	<-40dBm
FDD_LTE B8	23dBm +/-2.7dB	<-40dBm
FDD_LTE B20	23dBm +/-2.7dB	<-40dBm

Table 2-4 Conducted receive sensitivity

Table 2-4 Conducted receive sensitivity								
Working Band	Receive sensitivity(Typical)	Receive sensitivity(MAX)						
WCDMA B1	< -109dBm	3GPP						
WCDMA B8	< -109dBm	3GPP						
GSM900	< -109dBm	3GPP						
DCS1800	< -108dBm	3GPP						
TD-SCDMA B34	< -110dBm	3GPP						
TD-SCDMA B39	< -110dBm	3GPP						

Table 2-5 Reference sensitivity (QPSK)

Channel bandwidth										
E-UTRA Band	1.4 MHz	3 MHz	5 MHz	10 MHz	15 MHz	20 MHz	Duplex Mode			
1			-100	-97.2	-96.2	-95	FDD			
3	-102.2	-99.7	-98	-95	-94.2	-93	FDD			
7			-98	-95	-93.2	-92	FDD			
8	-103.2	-101.7	-100.2	-97.2			FDD			
20			-97	-94	-91.2	-90	FDD			
38			-100	-97	-95.2	-94	TDD			



39	 	-100	-97	-95.2	-94	TDD
40	 	-100	-97	-95.2	-94	TDD
41	 	-100	-97	-95.2	-94	TDD





3 Interface Introduction

3.1 Definition of Pin

3.1.1 Definition of Pin I/O parameter

Definition of Pin I/O parameter as Table 3-1.

Table 3-1 Definition of Pin I/O parameter

symbols about Pin attribute identifies	Describe
DI	Digital signal input pin
DO	Digital signal output pins
Al	Analog signal input pin
AO	Analog signal output pins
В	Bidirectional digital port, CMOS input
Z	High-impedance output
P1	Pin Group 1, power supply voltage VDD P1
P2	Pin Group 2, power supply voltage VDD P2

3.1.2 Deployment diagram of Pin



The define about the order of interface pins on the product as the Figure 3-1.

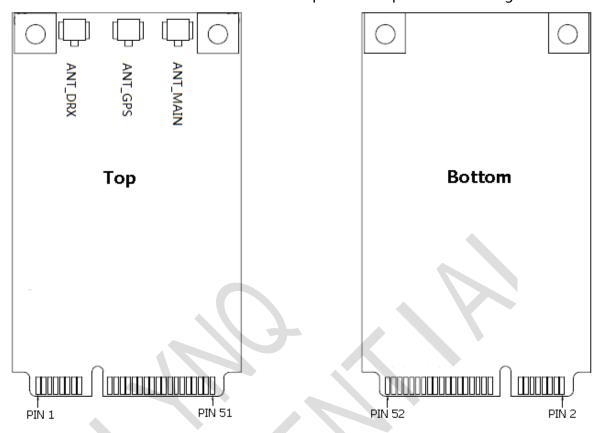


Figure 3-1 Deployment diagram of Pin (Top view)

3.1.3 Pin description

Table 3-2 Standard edition MINI PCIE Pin description(no codec)

Pin No.	L506 Pin define	Pin voltage	I/O	Pin Properties	Standard mini PCle Pin define	Note
1	WAKE_N	P1	DO	Wake up the host signal	WAKE#	Down is Active
2	V_MAIN			System power supply	3.3Vaux	3.0-3.6V
3	NC				COEX1	
4	GND			Floor	GND	
5	RESERVED			Reserved	COEX2	
6	NC				1.5V	
7	RESERVED			Reserved	CLKREQ#	



Pin No.	L506 Pin define	Pin voltage	I/O	Pin Properties	Standard mini PCle Pin define	Note
8	VREG_UIM	P1/P2		USIM card power signal	UIM_PWR	
9	GND	P1	DO	Floor	GND	
10	UIM_DATA	P1/P2	В	USIM card data signal	UIM_DATA	
11	UART1_RX	P1	DI	USART1 data reception	REFCLK-	
12	UIM_CLK	P1/P2	DO	USIM card clock signal	UIM_CLK	
13	UART1_TX	P1	DO	UART1 transmit data	REFCLK+	
14	UIM_RST	P1/P2	DO	USIM card reset signal	UIM_RESET	
15	GND			Floor	GND	
16	FORCE_USB_B OOT	P1	DO	Module mandatory USB download	UIM_VPP	Pull up to 1.8V enter force USB Boot mode
17	UART1_RI	P1	DO	UART1 ringing signal	RESERVED	
18	GND			Floor	GND	
19	UIM_PRESENT	P1	DI	USIM card hot plug detect signal	RESERVED	Low effective. Have internal pulled up
20	W_DISABLE_N	P1	DI	Fly mode	W_DISABLE#	Down is Active.
21	GND			Floor	GND	
22	PON_RESET_N		Al	Module reset signal	PERST#	Down is Active
23	UART1_CTS	P1	DI	UART1 allowed to send data	PERn0	
24	V_MAIN			Main power	3.3Vaux	3.0-3.6V.



Pin No.	L506 Pin define	Pin voltage	I/O	Pin Properties	Standard mini PCle Pin define	Note
				supply		
25	UART1_RTS	P1	DO	UART1 ready to receive	PERp0	
26	GND			Floor	GND	
27	GND			Floor	GND	
28	NC				1.5V	
29	GND			Floor	GND	
30	I2C_SCL	P1		I2C Clock	SMB_CLK	Have internal pulled-up
31	UART1_DTR	P1	DI	UART1 interrupt ready	PETn0	
32	I2C_SDA	P1		I2C Data	SMB_DATA	Have internal pulled-up
33	UART1_DCD	P1	DO	UART1 Carrier Detect	РЕТр0	
34	GND	-	-/	Floor	GND	
35	GND			Floor	GND	
36	USB_DM		AI/A O	USB differential data lines (-)	USB_D-	$\begin{array}{ll} \text{need} & \text{to} \\ \text{take} & 90\Omega \\ \text{impedanc} \\ \text{e line}. \end{array}$
37	GND			Floor	GND	
38	USB_DP		Al/A O	USB differential data lines (+)	USB_D+	$\begin{array}{ll} \text{need} & \text{to} \\ \text{take} & 90\Omega \\ \text{impedanc} \\ \text{e line}. \end{array}$
39	VMAIN			Main power supply	3.3Vaux	3.0-3.6V.
40	GND			Floor	GND	



Pin No.	L506 Pin define	Pin voltage	I/O	Pin Properties	Standard mini PCle Pin define	Note
41	VMAIN			Main power supply	3.3Vaux	3.0-3.6V.
42	LED_WWAN_N		Al	Work status indication	LED_WWAN#	
43	GND			Floor	GND	
44	NC			-	LED_WLAN#	
45	PCM_CLK	P1	DO	PCM Clock	RESERVED	Connect to the PCM audio decoder chip
46	NC				LED_WPAN#	
47	PCM_IN	P1	DI	PCM Data in	RESERVED	Connect to the PCM audio decoder chip
48	NC			-	1.5V	
49	PCM_OUT	P1	DO	PCM Data out	RESERVED	Connect to the PCM audio decoder chip
50	GND	-	\	Floor	GND	
51	PCM_SYNC	P1	DO	PCM Sync signal	RESERVED	Connect to the PCM audio decoder chip
52	VMAIN	-		Main power supply	3.3Vaux	

Table 3-3 Integrate codec edition MINI PCIe Pin description

Pin No.	L506 Pin define	Pin voltage	I/O	Pin Properties	Standard mini PCle Pin define	Note	
1	WAKE_N	P1	DO	Wake up the host signal	WAKE#	Down Active	is
2	V_MAIN			System power supply	3.3Vaux	3.0-3.6V	,
3	NC			-	COEX1		
4	GND			Floor	GND		



Pin No.	L506 Pin define	Pin voltage	I/O	Pin Properties	Standard mini PCle Pin define	Note
5	SPK_OUT_P		АО	The positive difference speaker output signal	COEX2	Analog difference line
6	NC				1.5V	
7	SPK_OUT_N		АО	Negative difference speaker output signal	CLKREQ#	Analog difference line
8	VREG_UIM	P1/P2		USIM card power signal	UIM_PWR	
9	GND	P1	DO	Floor	GND	
10	UIM_DATA	P1/P2	В	USIM card data signal	UIM_DATA	
11	UART1_RX	P1	DI	USART1 data reception	REFCLK-	
12	UIM_CLK	P1/P2	DO	USIM card clock signal	UIM_CLK	
13	UART1_TX	P1	DO	UART1 transmit data	REFCLK+	
14	UIM_RST	P1/P2	DO	USIM card reset signal	UIM_RESET	
15	GND		-	Floor	GND	
16	FORCE_USB_B OOT	P1	DO	Module mandatory USB download	UIM_VPP	Pull up to 1.8V enter force USB Boot mode
17	UART1_RI	P1	DO	UART1 ringing signal	RESERVED	
18	GND			Floor	GND	
19	UIM_PRESENT	P1	DI	USIM card hot plug detect signal	RESERVED	Low effective. Have internal pulled up
20	W_DISABLE_N	P1	DI	Fly mode	W_DISABLE#	Down is Active.



Pin No.	L506 Pin define	Pin voltage	I/O	Pin Properties	Standard mini PCle Pin define	Note
21	GND			Floor	GND	
22	PON_RESET_N		Al	Module reset signal	PERST#	Down is Active
23	UART1_CTS	P1	DI	UART1 allowed to send data	PERn0	
24	V_MAIN			Main power supply	3.3Vaux	3.0-3.6V.
25	UART1_RTS	P1	DO	UART1 ready to receive	PERp0	
26	GND	-		Floor	GND	
27	GND	-	-	Floor	GND	
28	NC			-	1.5V	
29	GND	-		Floor	GND	
30	MIC_P	Al	-	MIC Positive input	SMB_CLK	Routing differential
31	UART1_DTR	P1	DI	UART1 interrupt ready	PETn0	
32	MIC_N	Al		MIC Negative input	SMB_DATA	Routing differential
33	UART1_DCD	P1	DO	UART1 Carrier Detect	РЕТр0	
34	GND			Floor	GND	
35	GND			Floor	GND	
36	USB_DM		AI/A O	USB differential data lines (-)	USB_D-	$\begin{array}{ll} \text{need} & \text{to} \\ \text{take} & 90\Omega \\ \text{impedanc} \\ \text{e line}. \end{array}$
37	GND			Floor	GND	
38	USB_DP		AI/A	USB	USB_D+	need to



Pin No.	L506 Pin define	Pin voltage	I/O	Pin Properties	Standard mini PCle Pin define	Note
			0	differential data lines (+)		take 90Ω impedanc e line.
39	VMAIN			Main power supply	3.3Vaux	3.0-3.6V.
40	GND			Floor	GND	
41	VMAIN			Main power supply	3.3Vaux	3.0-3.6V.
42	LED_WWAN_N		Al	Work status indication	LED_WWAN#	
43	GND			Floor	GND	
44	NC				LED_WLAN#	
45	RESERVED			Reserved	RESERVED	
46	NC	-		-	LED_WPAN#	
47	RESERVED			Reserved	RESERVED	
48	NC			-	1.5V	
49	RESERVED			Reserved	RESERVED	
50	GND			Floor	GND	
51	RESERVED			Reserved	RESERVED	
52	VMAIN	-		Main power supply	3.3Vaux	

Attention:

"NC" means Not Connected, Internal module is not connected; "RESERVED" means Internal module connected but is temporarily unavailable.P1. P2 arePower supply signal level group1 and group 2.No useless Pins can hang up.



3.2 Working conditions

Table 3-4 Working conditions

Signal	describe	lowest	special	highest	unit
V_MAIN	The main power supply module	3.0	3.3	3.6	V
VDD_P1	Power supply voltage pin group P1	1.7	1.8	1.9	V
VDD_P2	Power supply voltage pin group P2	2.71	2.85	2.99	V

Attention:

- 1. Typical voltage value indicates that the product of P1, P2, set the default pin input and output voltage value, the external input pin is required to provide the interface of the voltage value for this purpose.
- 2. The external interface circuit voltage design must pin voltage matching with the products.

3.3 Interface level features

Table 3-5 Digital signal v range

Symb	ool	Describe	Lowest	Highest	Unit
VIH		High input voltage level	0.65*VDD_PX	VDD_PX+0.3	V
VIL		Low input voltage level	-0.3	0.35* VDD_PX	V
VOH		High level output voltage	VDD_PX-0.45	VDD_PX	V
VOL		Low output voltage level	0	0.45	V



3.4 The power interface

3.4.1 Power pin description

Pin number: 2,24,39,41,52 are the signal of V_MAIN (3.3Vaux), The positive signal for power supply of 3.3 V.

Pin number: 4/9/15/18/21/26/27/29/34/35/37/40/43/50 are the signal of GND.

This is the product of power supply and signal, all need to connect to the system board on the ground plane.GND signal connection is not complete will have an impact on the performance of this product.

3.5 (U)SIM card interface

3.5.1 Pin description

L506 Mini PCIe module integrates accord with standard of ISO 7816-2 (U) SIM card interface, support, and can automatically detect 3.0 V and 1.8 V (U) SIM card, (U) SIM card interface signal as shown in Table 3-5.

Table 3-6 (U)SIM card Signal group definition and description

Pin NO.	Protocol signal name	Signal definition	Signal description
8	VREG_UIM	SIM card power	Module output the USIM card power
10	UIM_DATA	SIM card Data pin	USIM card DATA signal,Two-way signal
12	UIM_CLK	SIM card clock pin	Module output the USIM card clock pin signal
14	UIM_RST	SIM card reset pin	Module output the USIM card reset pin signal
8	VREG_UIM	SIM card power	Module output the USIM card power
10	UIM_DATA	SIM card Data pin	USIM card DATA signal , Two-way signal
12	UIM_CLK	SIM card clock pin	Module output the USIM card clock pin



signal

3.5.2 Electrical characteristics

Detailed definition (U) SIM card each signal as shown in Table 3-5.Near (U) SIM kaka on the lines of design, please pay attention to the need to increase the ESD protection devices.

In order to meet the 3 GPP TS 51.010 1 protocol and EMC certification requirements, recommend (U) SIM booth arrangement near the location of the SIM card interface module, to avoid running for too long, lead to serious deformation of waveform signal integrity.

UIM_CLK and UIM_DATA signal line suggested package to protect. In a parallel between VREG_UIM &gnd 1 UF and 33 PF capacitor, UIM_CLK, UIM_RST, UIM_DATA with 33 PF capacitor in parallel between GND, filter the RF signal interference.

3.5.3 (U)SIM card Interface application

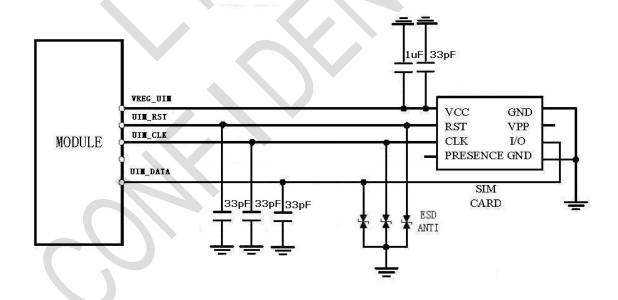




Figure 3-2 (U)SIM card interface application

Note: Pull up resistors of UIM_DATA signal lines has been in the module design, no need other connected resistance.

3.6 USB2.0 interface

3.6.1 Pin description

This product has a high-speed USB2.0 interface, support for low speed, full - speed and high - speed mode, a main processor (AP) and mainly through the USB interface for data transmission between modules.

3.6.2 Electrical characteristics

The USB interface module in line with the USB2.0 specification and electrical properties.

Support the low - speed, full - speed and high - speed three work modes. Main processor (AP) and the module of data between the interaction is mainly completed through the USB interface.

Attention:

USB differential data must be controlled impedance matching in 90 ohms.

3.6.3 USB Interface application

USB bus is mainly used for data transmission, software upgrades, detection module program. Work under the mode of high - speed USB line, if you need to ESD design, must satisfy the junction capacitance value of ESD protection devices < 2 pf, or larger junction capacitance will cause waveform distortion, affect the bus communication.



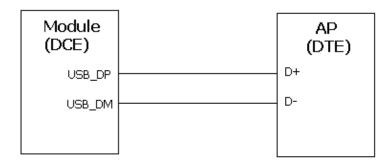


Figure 3-3 USB Connection diagram

3.7 UART interface

3.7.1 Pin description

This product provide 1 road UART serial communication interface, accord with the RS - 232 interface protocols, support 8 line serial bus interface, the module can be through the UART interface for serial communication with the outside world and the AT command input, etc. The UART port supports programmable data width, programmable data stop bits, parity bit of programmable, independent of the TX and RX FIFOs (128 bytes), the default baud rate to 115200 BPS, pin signal is defined as shown in Table 3-6.

Pin No. Signal name I/O type Function 11 UART1_RX DI UART1 receive data 13 UART1_TX DO UART1 send data 16 UART1 DSR DI UART1 data is ready 17 UART1_RI DO **UART1** Ringing indicating UART1_CTS DI DTE allow module send data 23 Module is ready to receive, DTE can 25 UART1_RTS DO send. UART1_DTR 31 DO DCE is ready 33 UART1_DCD DO **UART1** Carrier detect

Table 3-7 UART Signal definition



3.7.2 Electrical characteristics

In order to have a grab the log in the process of software alignment function, we recommend that users keep reserved the interface and test points in design. If the module is used together with the application processor, and match level at 1.8 V, connection as shown in figure 3-4, can use 4 line way or two ways to connect. Module interface level is 1.8 V, if you don't match with AP interface level, suggest increase level conversion circuit.

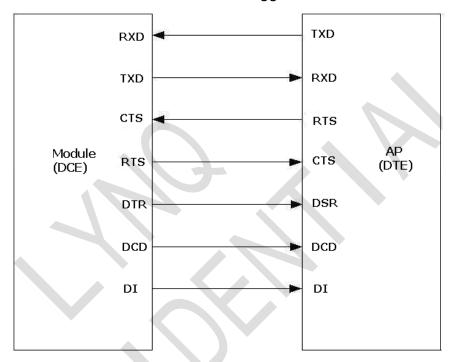


Figure 3-4 Module and AP(application device) Application processor

3.8 PON_RST_N reset signal

3.8.1 Pin description

PON_RST_N pin is used to reset the module, the PON_RST_N pin down after 200 ms, then the tube feet dangling or high, can be reset.



3.8.2 Interface application

PON_RST_N circuit can refer to figure 3-5 in the design of the circuit.

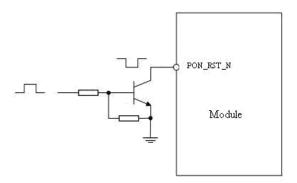


Figure 3-5 Reset circuit

3.9 LED_WWAN_N signal

3.9.1 Pin description

Module LED_WWAN_N signal is used to control the LED light, can be used in network connection status. By different status lights flashing mode, represent different network status. The pin using GPIO control, external an NPN triple tube. External connect VBAT can directly drive leds. Drive current capacity varies according to external NPN model, recommend DTC143ZEBTL, and the MAX current can reach 100 mA.

3.9.2 Interface application

Figure 3-6 is the reference circuit design, light condition defined as shown in Table 3-7.



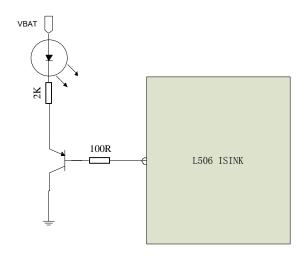


Figure 3-6 Status indicator reference circuit

Table 3-8 Light state definition

Module working state	Light state	Note	
On	Not bright		
Search network	3Hz shining	Searching the network now	
IDLE	1Hz shining	Has Registered to the network	
Traffic (call、surf)	5Hz shining	Calling in/GPRS data transmission	
		>	

3.10 W_DISABLE_N signal

W_DISABLE_N signals for radio frequency (RF) can make the switch for access to flight mode and normal mode. As shown in Table 3 - 8.

Table 3-9 Light state definition

Module work mode	W_DISABLE_N signal	note
Normal mode	High level	Module can work normally
Fly mode	Low level	Close the RF function



4 product electrical characteristics

4.1 Power characteristics

4.1.1 Power supply

This product is a DC input voltage range of 3.0 V to 3.6 V, the typical value of 3.3 V, as shown in Table 4-1.

Table 4-1 Input voltage

Parameter	Lowest	Typical value
Input voltage	3.0V	3.3V

4.1.2 Working current

Working current scope of the product as shown in table 4-2, IDLE mode means no business module of power consumption, at the same time, we present the data in the GSM and WCDMA working current scope of business.

Table 4-2 Working current

Model	State	Average value	Note
GSM	Current under no business mode	5mA	IDLE mode
GSIVI	Current under data transmission	300mA	GPRS/EDGE mode
WCDMA	Current under no business mode	6mA	IDLE mode
WCDIVIA	Current under data transmission	600mA	HSPA mode
TD-SCDMA	Current under no business mode	6mA	IDLE mode
TD-SCDIVIA	Current under data transmission	320mA	HSPA mode
TDD LTE	Current under no business mode	6mA	IDLE mode
TDD_LTE	Current under data transmission	450mA	HSPA mode
EDD LTE	Current under no business mode	8mA	IDLE mode
FDD_LTE	Current under data transmission	700mA	HSPA mode

Attention:



1. The average current is under the condition of maximum transmitted power testing, test the value of the different environment may have error, please refer to our actual situation.

5 Design guidance

This chapter provides a general design of the products instruction, the user can refer to design guidance for design, make products to achieve better performance.

5.1 General design rules and requirements

Users in the design of this product is peripheral circuit, the first to ensure the external power supply circuit can provide enough power supply capacity, and the requirements for high speed signal lines USB control 90 ohm impedance differential. For general signal interface, require the user to us in strict accordance with the requirements of design, in line with the interface signal level matching, in case the level of damage to the module. This product its own radio frequency index is good, customers need to design in accordance with the requirements the main board side antenna circuit and corresponding impedance control, otherwise it will affect the whole RF index.

5.2 RF circuit design

5.2.1 RF antenna circuit design

This product's access part adopts radio frequency antenna RF connector. The current selection of RF connector test is HRS company U.F L - R - SMT - 1, as shown in Figure 5-1.



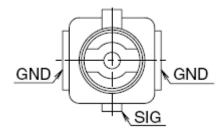


Figure 5-1 The radio frequency interface test (HRS U.FL-R-SMT-1)

If access to part of the main antenna using RF connector, RF interface that corresponds to the cable, suggested that chooses HRS company U.F L - LP - 04 n, as shown in Figure 5-2, adopt the way of connection and antenna RF connector can directly on the module of RF test, saves module of RF switching between the port and antenna interface.



Figure 5-2 Test cable

5.2.2 Antenna design early considerations

1. The early stage of the project evaluation

Antenna position of the first choice to keep antenna and the base station in horizontal direction, so that the highest efficiency; Second, try to avoid placed in switching power supply or cable, such as chip may produce electromagnetic interference device or around the chip. Also should avoid hand should be placed on the antenna position, thus preventing human body attenuation on the antenna; But also to reduce the radiation and realizability of the structure into consideration. Therefore, at the beginning of the design need to structure, ID, circuit layout evaluation, antenna engineers.



2.Antenna placement suggestion

Antenna placement for notebook products, ideal place is located in the top left or top right of the LCD, this position is relatively far away from the main board, by electromagnetic interference small, 2 it is considering the relatively far away from the body, easy to satisfy the SAR index; The second good place is to the right or left of LCD. Other products such as routers, ebook concrete evaluation according to the characteristics of the product itself.

3.Antenna need size suggestion

Due to the different antenna manufacturer may adopt different forms, so different antenna room.3 g frequency five main antenna: 5 mm (thickness) * 12 mm (width) * 80 mm (long)

4.Antenna RF cables

Antenna RF cables go line short as far as possible, considering the transmission loss, the proposal USES a bit coarse RF line. RF line also try to stay away from the FSB, chips and memory, power interface, data line may produce the EMI module and device interfaces, Connect the antenna with the 3 g module of RF cables can't walk right around the corner, can't be squeezed, wear and tear; RF line walk line is best close to the main board.

5. Antenna RF line and RF connector selection

Antenna RF cables usually use Taiwan GBE ShenYu (TW) and the mainland, also can consider Japan Somitomo, Shin Din, 3 g antenna RF cables usually use 1.37 mm wire diameter. Antenna RF connector generally adopt Japan IPX, also has with HRS, but the price a little on the high side.

6. RF signal PCB layout guide

L506 provides RF antenna interface. Customer's antenna should be located in the host board and connected to module's antenna pad through micro-strip line or other types of RF trace and the trace impedance must be controlled in 50Ω . we recommends that the total insertion loss between the antenna pad and antenna should meet the following requirements:



- GSM900/GSM850<0.5dB
- DCS1800/PCS1900 < 0.9dB
- WCDMA 2100/1900 < 0.9dB
- WCDMA 900/850 < 0.5 dB
- LTE (F<1GHz) <0.5dB
- LTE (1GHz<F<2GHz) <0.9dB
- LTE (2GHz<F) <1.2dB

To facilitate the antenna tuning and certification test, a RF connector and an antenna matching circuit should be added. The following figure is the recommended circuit.

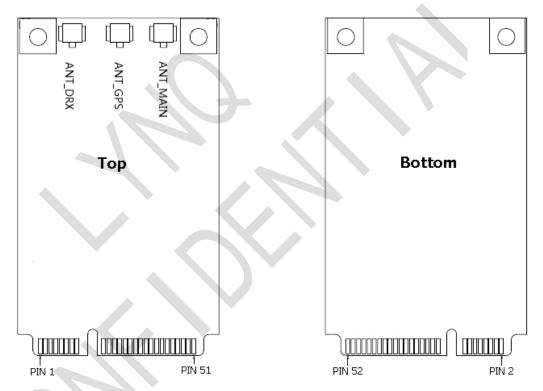


Figure 5-3 Deployment diagram of Pin

Table 5-1 Antenna pin definition

Signal	I/O Typ.	Description
MAIN_ANT	AI/AO	Module main antenna
AUX_ANT	AI	LTE diversity antenna feed point
GNSS_ANT	AI	GNSS antenna feeder connector



7. applications

For convenience of antenna tuning and certification test, should increase RF connectors and the antenna matching circuit, below is a recommended circuit:

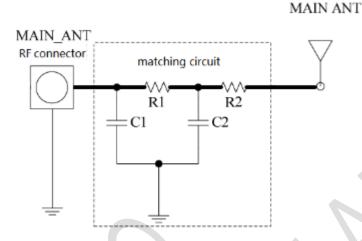


Figure 5-4 Main antenna matching circuit diagram (MAIN_ANT)

In this figure, the components R1, C1, C2 and R2 is used for antenna matching, the value of components can only be got after the antenna tuning, usually, they are provided by antenna vendor. By default, the R1, R2 are 0 Ohm resistors, and the C1, C2 are reserved for tuning.

The RF test connector in the figure is used for the conducted RF performance test, and should be placed as close as to the module's antenna pin. The traces impedance between components must be controlled in 50ohm.

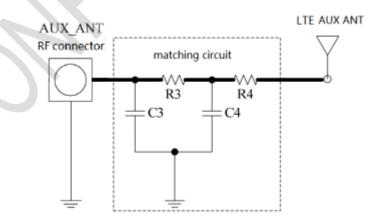


Figure 5-5 LTE Diversity antenna matching circuit diagram (AUX_ANT)



Note: LTE diversity antenna recommend leaving. Because there are many high frequencies of TDD LTE design, such as band38 band40 and Band41. Due to the high insertion loss RF line, if there is no diversity antenna, receiving sensitivity of the spectrum in the certification will be a risk.

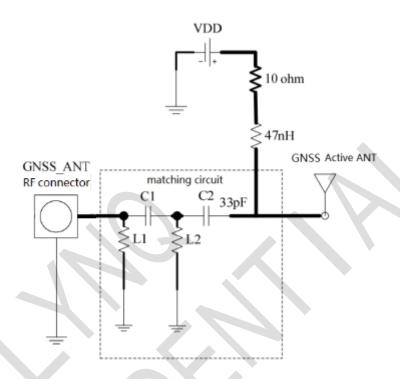


Figure 5-6 GNSS active antenna matching circuit diagram (GNSS_ANT)

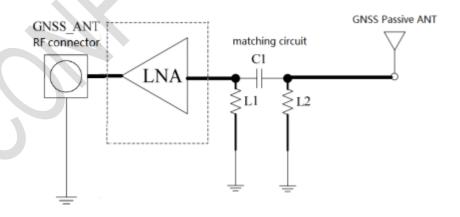


Figure 5-7 GNSS passive antenna matching circuit diagram (GNSS_ANT)



In above figures, the components C1 and L1, L2 are used for antenna matching, the values of the components can only be obtained after the antenna tuning usually, and they are provided by antenna vendor.C2 in Figure 5-6 is used for DC isolation. In active antenna circuit, users must use an external LDO/DCDC to provide VDD voltage whose value should be taken according active antenna characteristic, and VDD can be shut down to avoid consuming additional current when not being used. GNSS can be used by NMEA port. User can select NMEA as output through UART or USB. NMEA sentences are automatic and no command is provided. NMEA sentences include GSV, GGA, RMC, GSA, and VTG. Before using GNSS, user should configure L506 in proper operating mode by AT command. Please refer to related document for details. L506 can also get position location information through AT directly.

In the diagram above, component C1, L1 and L2 for antenna match, the element's value depends on the antenna after debugging. In figure 5-7, C2 for dc isolation. In the active antenna circuit, the user must use an external "/ DCDC VDD voltage, its value should be according to the properties of the active antenna, VDD can close to avoid without additional current consumption when using GNSS. In Figure 5-7, the user can increase a external LNA gain to get better.

L506 merges GNSS (GPS/GLONASS) satellite and network information to provide a high-availability solution that offers industry-leading accuracy and performance. This solution performs well, even in very challenging environmental conditions where conventional GNSS receivers fail, and provides a platform to enable wireless operators to address both location-based services and emergency mandates.

Tracking sensitivity -159 dBm (GPS) -158 dBm (GLONASS)

AcquisitionSensitivity -148dBm

Cold-start sensitivity -142 dBm

C/N0 = S - (-170) S= Input Signal Intensity

Accuracy (Open Sky) 2.5m (CEP50)

TTFF (Open Sky) Hot start <1s Cold start 35s

Receiver Type 16-channel, C/A Code

GPS L1 Frequency (1575.42±1.023MHz),

GLONASS: 1597.5~1605.8 MHz

Update rate Default 1 Hz

GNSS data format NMEA-0183

GNSS Current consumption (WCDMA/GSM Sleep mode) 100mA (Total supply current)



5.3 Mini PCI Express connector

In connection with a standard of the 52 user board pin Mini PCI Express connector. Recommended Molex company's 67910-0002 series connectors, as shown in Figure 5-3.

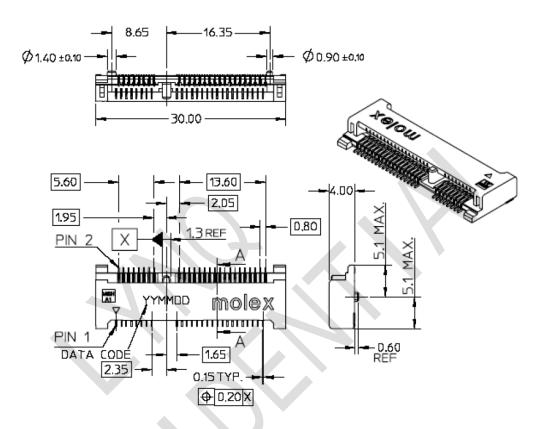


Figure 5-8 Mini PCIe connector

5.4 EMC and ESD design suggestion

Users in the machine design should fully consider the EMC problems triggered by signal integrity and power integrity, in the module of peripheral circuit layout line, for a walk the line, such as power supply and signal lines to keep the double line spacing width, can effectively reduce the coupling between the signal, make the signal has a "clean" return path. Peripheral power circuit design, the decoupling capacitor to put close to the module power supply pin, high-frequency high-speed circuit and sensitive circuit should be far away from the edge of PCB, and between the layout of the isolation as far as possible,



reduce the interference between each other, and to protect sensitive signals to the system board side possible interference module circuit or device with shielding design work.

This product is embedded in the system board, the design need to pay attention to ESD protection, the key input and output signal interface, such as (U) SIM card, in areas such as the signal interface to nearby place ESD protection device, in addition the main board, require the user to the reasonable design. Structure and PCB layout, to guarantee the metal Shielding case fully ground, such as a set for the electrostatic discharge unobstructed discharge channel.

Contact address: Shanghai Mobiletek Communication Ltd Shanghai xuhui district field state road 99, 9 building, room 201

Zip code: 200233

Telephone: + 86 21 5108 5108

Fax: + 86 21 5445 5445

Url: WWW. Mobiletek. Cn

Business contact: sales@mobiletek.cn