

- Tentative Specification
- Preliminary Specification
- Approval Specification

MODEL NO.: G133HCE
SUFFIX: EH1

Customer:	
APPROVED BY	SIGNATURE
Name / Title _____	_____
Note	

Please return 1 copy for your confirmation with your signature and comments.	

Approved By	Checked By	Prepared By
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REVISION HISTORY

Version	Date	Page	Description
Ver 1.0	18 Jul ,2025	All	Preliminary Specification was first issued.
Ver 1.1	14 Aug,2025	P5	1.4 GENERAL SPECIFICATIONS Modify Module Power Consumption 11.8W change to 13.246W
		P11	3.3.1 TFT LCD MODULE Modify Power Supply Current white min value160=>400 typ value 180=>420 max value 200=>450 Modify Power Supply Current Black min value145=>170 typ value 165=>185 max value 185=>200
		P13	3.3.2 BACKLIGHT UNIT Modify Converter input current Typ value 0.93 change to 0.988 & Max value 1.0 change to 1.054 Modify Input Power Consumption Typ value 11.16change to 11.86 & Max value NA change to 12.65

1. GENERAL DESCRIPTION

1.1 OVERVIEW

G133HCE-EH1 is a 13.3" TFT Liquid Crystal Display IA module with LED Backlight units and 40 pins eDP interface. This module supports 1920 x 1080 FHD mode and can display 16.7M colors.

The PSWG is to establish a set of displays with standard mechanical dimensions and select electrical interface requirements for an industry standard 13.3" FHD LCD panel and the LED driving device for Backlight is built in PCBA.

1.2 FEATURE

- FHD (1920 x 1080 pixels) resolution
- PSWG (Panel Standardization Working Group)
- Wide operating temperature.
- RoHS compliance

1.3 APPLICATION

- TFT LCD Monitor
- Factory Application
- Amusement

1.4 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	293.76 (H) x 165.24(V) (13.3" diagonal)	mm	(1)
Driver Element	a-Si TFT active matrix	-	-
Pixel Number	1920 x R.G.B x 1080	pixel	-
Pixel Pitch	0.153(H) x 0.153(W)	mm	-
Pixel Arrangement	RGB vertical Stripe	-	-
Display Colors	16,777,216	color	-
Display Mode	Normally Black	-	-
Surface Treatment	Hard Coating (3H), Glare	-	-
Module Power Consumption	13.246	W	Typ

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal(H)	315.47	315.97	316.47	mm	(1)
	Vertical(V)	181.88	182.38	182.88	mm	
	Depth(w/o PCBA)	7.12	7.62	8.12	mm	
	Depth(PCBA)	---	---	9.23	mm	(1)
Active Area	Horizontal	---	293.76	---	mm	
	Vertical	---	165.24	---	mm	
Weight		490	516	542	g	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

2. ABSOLUTE MAXIMUM RATINGS

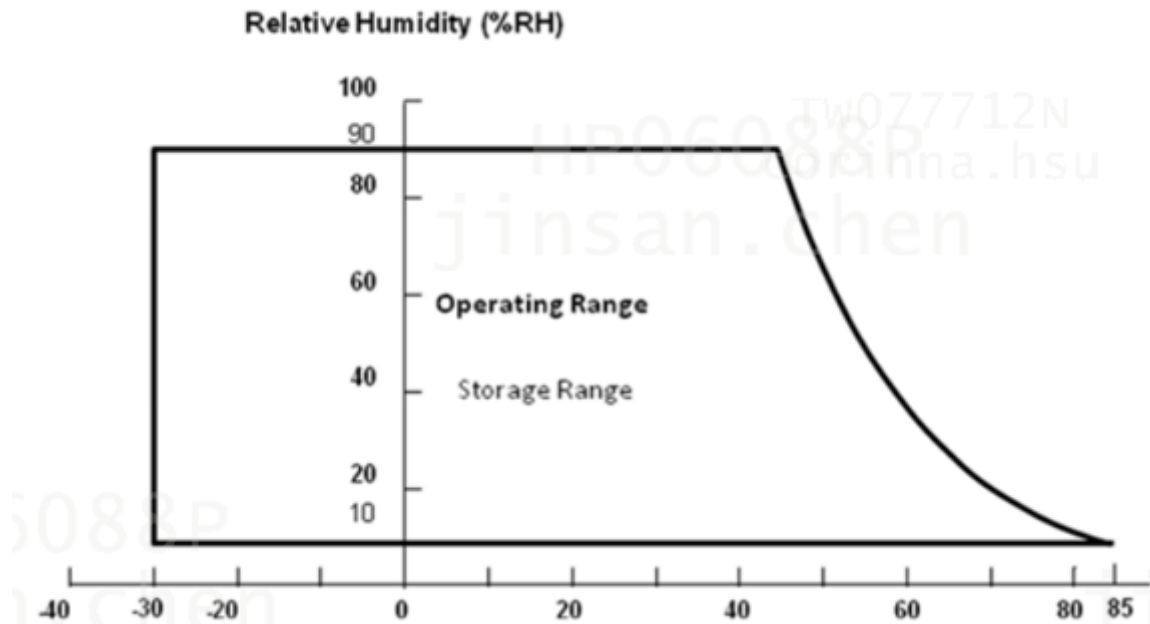
2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Operating Ambient Temperature	TOP	-30	+85	°C	(1)(2)(3)
Storage Temperature	TST	-30	+85	°C	(1)(2)(3)

Note (1)

- (a) 90 %RH Max.
- (b) Wet-bulb temperature should be 39 °C Max.
- (c) No condensation.

Note (2) Panel surface temperature should be 0°C min. and 85°C max under VCCS=3.3V, fr =60Hz, typical LED string current, 25°C ambient temperature, and no humidity control . Any condition of ambient operating temperature ,the surface of active area should be keeping not higher than 85°C.



2.2 ELECTRICAL ABSOLUTE RATINGS

2.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCCS	-0.3	4	V	(1)

2.2.2 BACKLIGHT UNIT

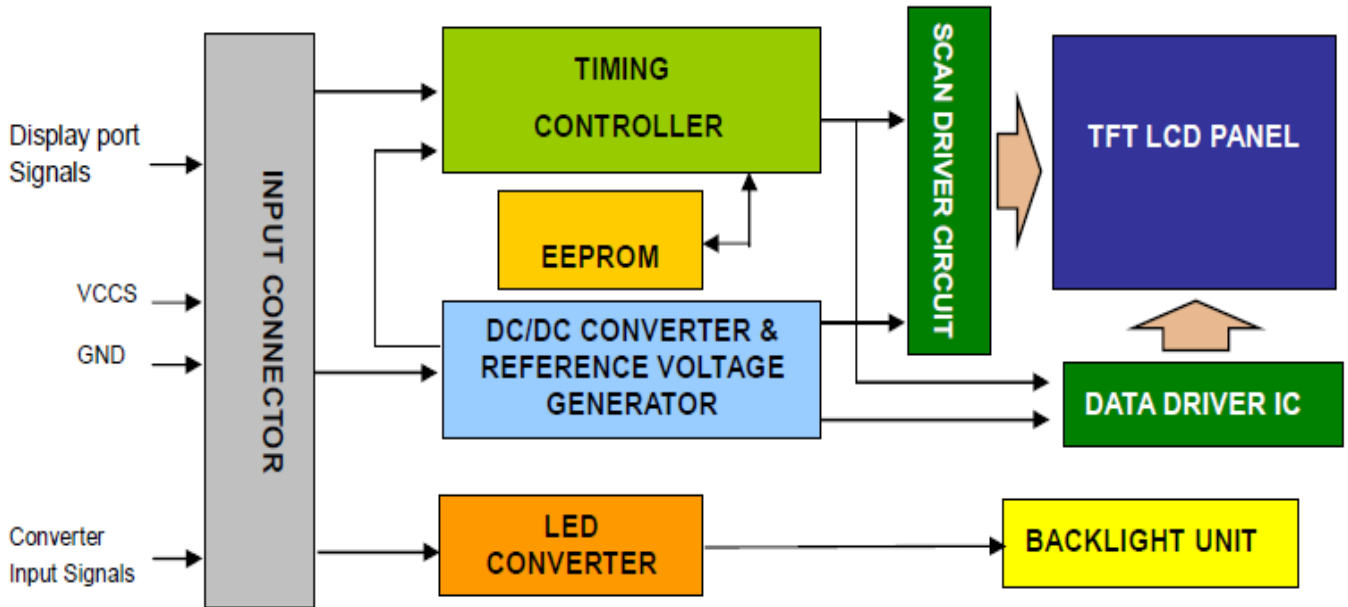
Item	Symbol	Value		Unit	Note
		Min.	Max.		
Converter Voltage	LED_VCCS	-0.3	18	V	(1), (2)
Enable Voltage	LED_EN	-0.3	5.5	V	
Backlight Adjust	LED_PWM	-0.3	5.5	V	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) Specified values are for LED (Refer to 3.3.2 for further information).

3. ELECTRICAL CHARACTERISTICS

3.1 TFT LCD MODULE



Note (1) Display port signals include eDP interface signals & BIST control signal Converter Input Signals include LED_VCCS, LED_EN, LED_PWM & LED_GND.

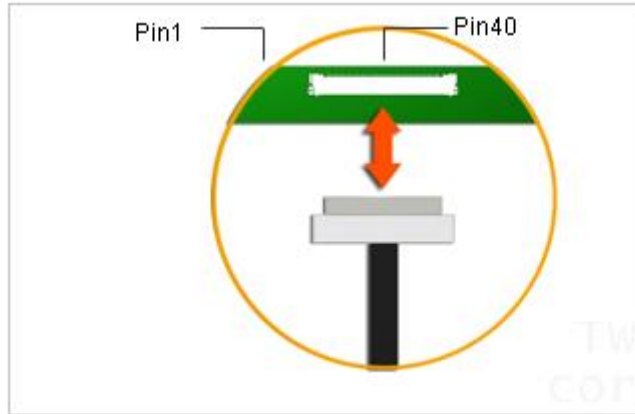
3.2 INPUT TERMINAL PIN ASSIGNMENT

PIN ASSIGNMENT of Input Connector

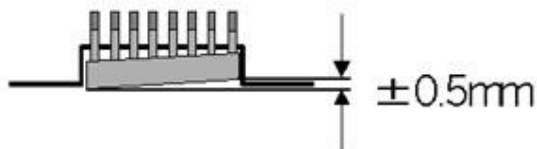
Pin No.	Pin Define	Description	Note
1	NC	No Connection	
2	LED_VCCS	LED Power Supply +12V (typical)	
3	LED_VCCS	LED Power Supply +12V (typical)	
4	LED_VCCS	LED Power Supply +12V (typical)	
5	LED_VCCS	LED Power Supply +12V (typical)	
6	NC	No Connection	
7	NC	No Connection	
8	LED_PWM	PWM Control Signal of LED Converter	(3)
9	LED_EN	Enable Control Signal of LED Converter	(3)
10	LED_GND	LED Ground	
11	LED_GND	LED Ground	
12	LED_GND	LED Ground	
13	LED_GND	LED Ground	
14	HPD	Hot Plug Detect	
15	GND	Ground	
16	GND	Ground	
17	GND	Ground	
18	GND	Ground	
19	BIST	LCM Built-in self-test patterns selection L: Disable (default) H: Enable	
20	VCCS	Power Supply +3.3 V (typical)	
21	VCCS	Power Supply +3.3 V (typical)	
22	VCCS	Power Supply +3.3 V (typical)	
23	VCCS	Power Supply +3.3 V (typical)	
24	GND	Ground	
25	AUX_N	Complement Signal-Auxiliary Channel	
26	AUX_P	True Signal-Auxiliary Channel	
27	GND	Ground	
28	Lane0_P	True Signal-Main Lane 0	
29	Lane0_N	Complement Signal-Lane 0	
30	GND	Ground	
31	Lane1_P	True Signal-Main Lane 1	
32	Lane1_N	Complement Signal-Lane 1	
33	GND	Ground	
34	NC	No Connection	
35	NC	No Connection	
36	GND	Ground	
37	NC	No Connection	
38	NC	No Connection	
39	GND	Ground	
40	NC	No Connection	

Note (1) Connector Part No.: 1st : STM MSAK24025P40MB (slivery), 2nd: IPEX 20455-040E-76 (golden)

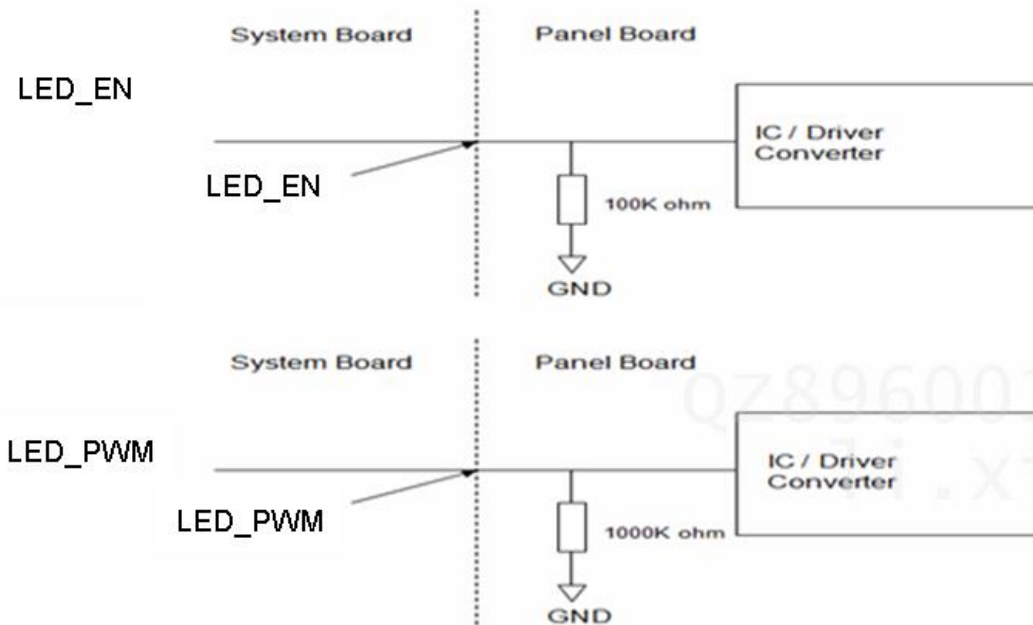
Note (2) User's connector Part No.: IPEX 20453-040T-0 or equivalent.



Mounting inclination of a connector carries out as follows



Note (3) There are PL resistors on LED_EN & LED_PWM in Panel control PCBA, refer to the following figure.



3.3 ELECTRICAL CHARACTERISTICS

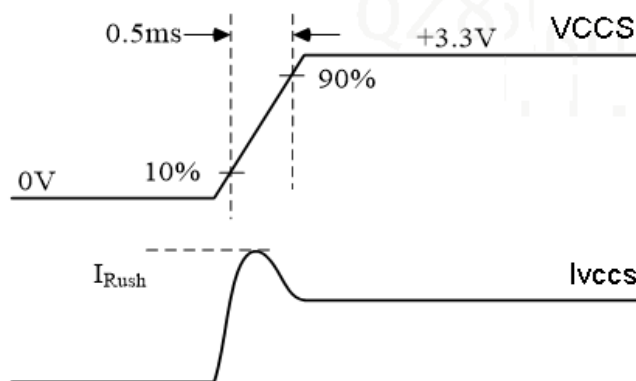
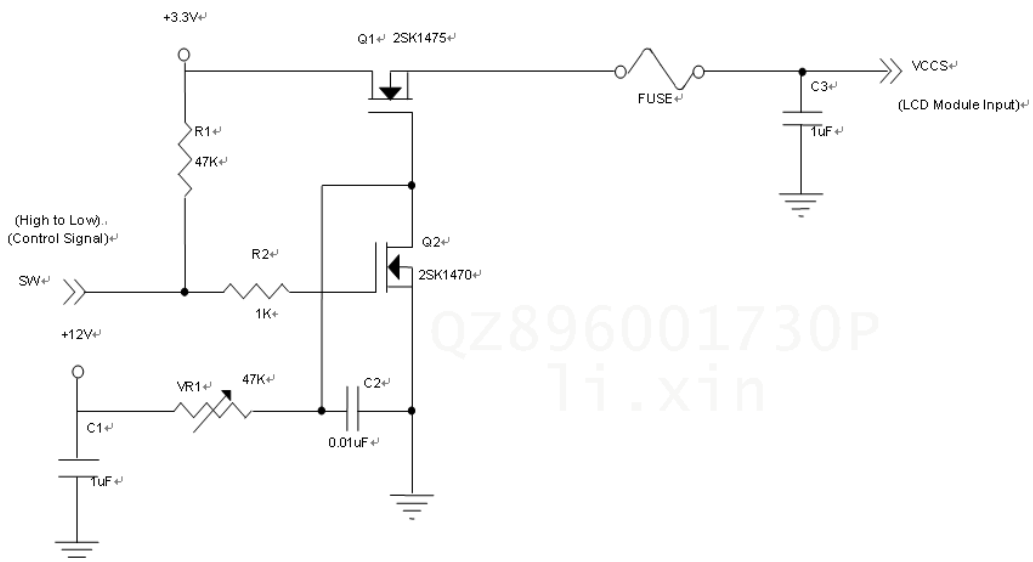
3.3.1 TFT LCD MODULE

Parameter	Symbol	Value			Unit	Note	
		Min.	Typ.	Max.			
Power Supply Voltage	VCCS	3.0	3.3	3.6	V	-	
Ripple Voltage	V _{RP}	-	50	150	mVp-p		
Inrush Current	I _{INRUSH}	-	-	1.5	A	(2)	
Power Supply Current	I _{VCCS}	White	160	180	200	mA	(3)a
		Black	145	165	185	mA	(3)b
HPD Impedance	R _{HPD}	30K			ohm		
HPD	High Level	V _{IH}	2.25	-	2.75	V	-
	Low Level	V _{IL}	0	-	0.4	V	-

Note (1) The module should be always operated within above ranges and the ambient temperature is Ta = 25 ± 2 °C.

Note (2) I_{INRUSH}: the maximum current when VCCS is rising

Measurement Conditions: Shown as the following figure. Test pattern: White



Note (3) The specified power supply current is under the conditions at $V_{CCS} = 3.3V$, $T_a = 25 \pm 2 \text{ }^\circ\text{C}$, DC Current and $f_v = 60 \text{ Hz}$, whereas a power dissipation check pattern below is displayed.

a. White Pattern



Active Area

b. Black Pattern

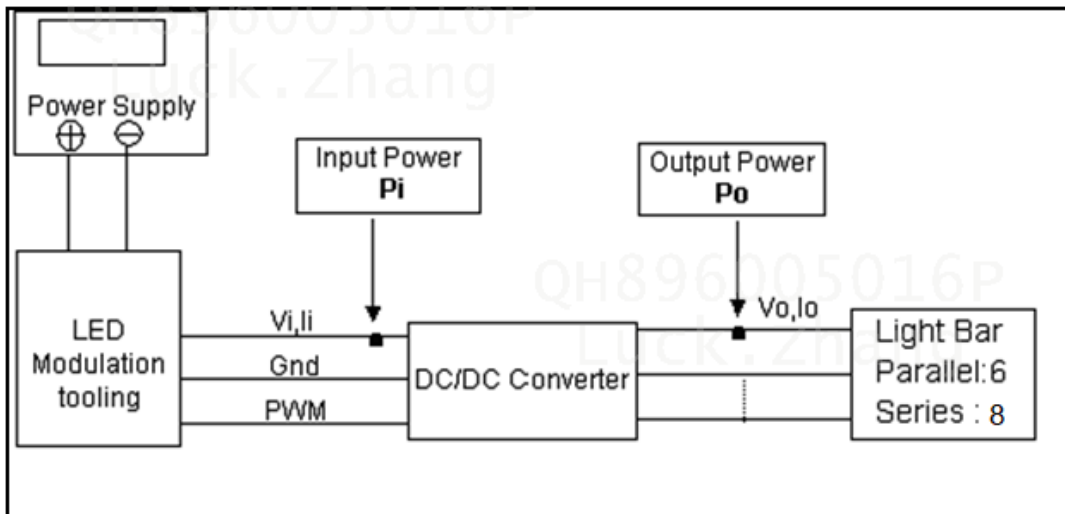


Active Area

3.3.2 BACKLIGHT UNIT

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Converter input voltage	LED_VCCS	10.8	12.0	13.2	V	(Duty 100%)
Converter input ripple voltage	V _{LED_VCCS_PP}	-	-	500	mV	
Converter input current	I _{LED_VCCS}	-	0.988	1.054	A	LED_VCCS= 12V @ LED_PWM Duty= 100%
Converter inrush current	I _{RUSH_LED_VCCS}	-	-	3.0	A	@ LED_VCCS rising time=10ms (LED_VCCS=12V)
Input Power Consumption	P _{LED_VCCS}	-	11.86	12.65	W	(1)
EN Control Level	LED_EN	2.5	3.3	5.0	V	
	Backlight off	0	---	0.3	V	
PWM Control Level	LED_PWM	2.5	---	5.0	V	
	PWM Low Level	0	---	0.3	V	
PWM Noise Range	V _{LED_PWM_PP}	-	-	0.1	V	
PWM Control Frequency	f _{LED_PWM}	190	200	20k	Hz	(2)
PWM Control Duty Ratio	-	1		100	%	(2).@ 190Hz<f _{LED_PWM} <20K Hz
LED Life Time	L _{LED}	50000	-	-	Hrs	(3)

Note (1) LED current is measured by utilizing a high frequency current meter as shown below:



Note (2) If the PWM control duty ratio is less than 10%, there is some possibility that acoustic noise or backlight flash can be found. And it is also difficult to control the brightness linearity.

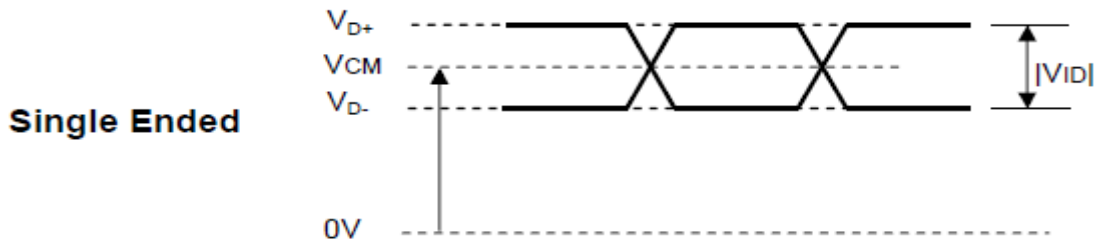
Note (3) The lifetime of LED is estimated data and defined as the time when it continues to operate under the conditions at Ta = 25 ±2 °C and Duty 100% until the brightness becomes ≤ 50% of its original value. Operating LED at high temperature condition will reduce life time and lead to color shift.

3.4 DISPLAY PORT INPUT SIGNAL TIMING SPECIFICATIONS

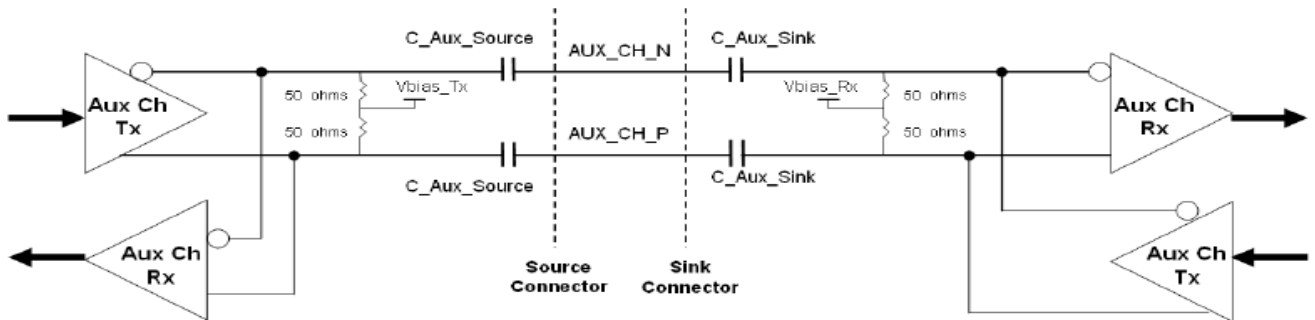
3.4.1 ELECTRICAL SPECIFICATIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Differential Signal Common Mode Voltage(MainLink and AUX)	VCM	0		2	V	(1)(4)
AUX AC Coupling Capacitor	C_Aux_Source	75		200	nF	(2)
Main Link AC Coupling Capacitor	C_ML_Source	75		200	nF	(3)

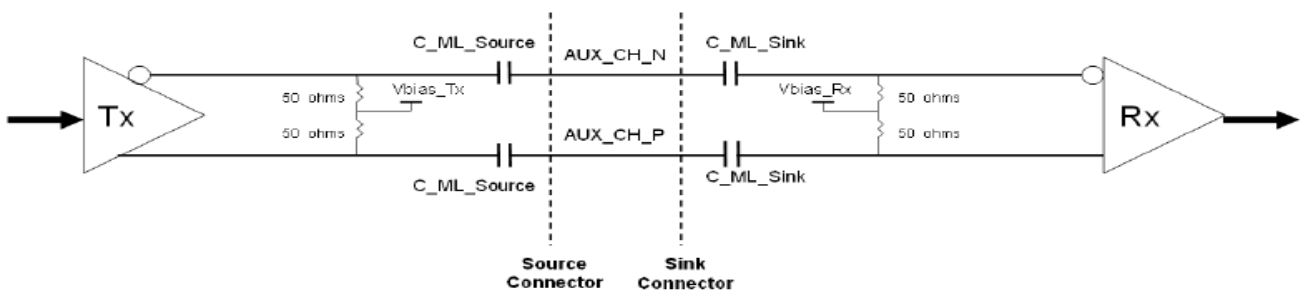
Note (1) Display port interface related AC coupled signals should follow VESA DisplayPort Standard Version 1. Revision 1a and VESA Embedded DisplayPort™ Standard Version 1.2. There are many optional items described in eDP1.2. If some optional item is requested, please contact us.



Note (2) Recommended eDP AUX Channel topology is as below and the AUX AC Coupling Capacitor (C_Aux_Source) should be placed on the source device.



Note (3) Recommended Main Link Channel topology is as below and the Main Link AC Coupling Capacitor (C_ML_Source) should be placed on the source device.



Note (4) The source device should pass the test criteria described in DisplayPortCompliance Test Specification (CTS) 1.1.

3.4.2 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
Gray Scale Of Red	Red(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Red(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Red(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮			
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮			
	Red(253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Red(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
Gray Scale Of Green	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0		
	Green(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0		
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮			
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮			
	Green(253)	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0		
	Green(254)	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0		
	Green(255)	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0		
Gray Scale Of Blue	Blue(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1		
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1		
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮			
	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮			
	Blue(253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0		
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0		
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1		

Note (1) 0: Low Level Voltage, 1: High Level Voltage

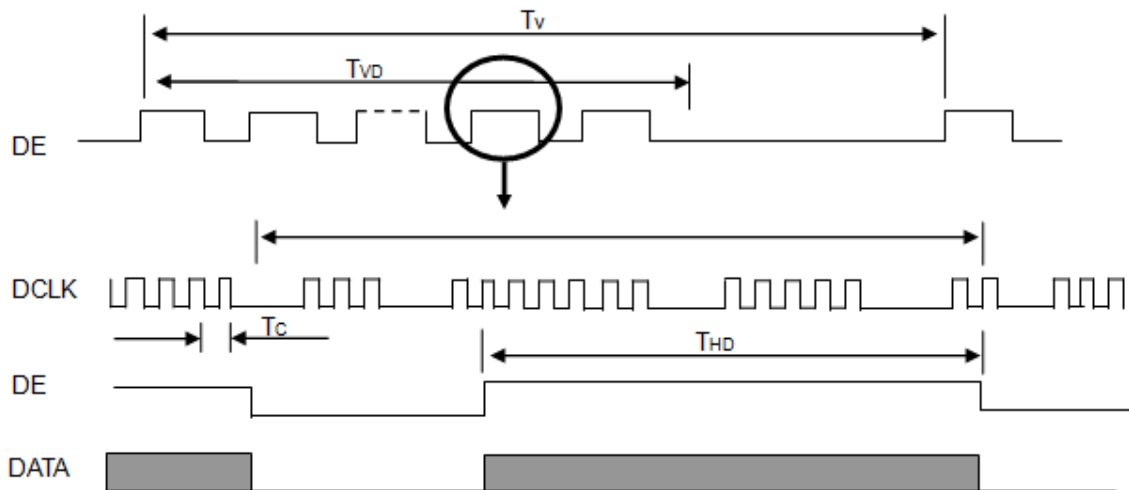
3.5 INTERFACE TIMING

3.5.1 INPUT SIGNAL TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

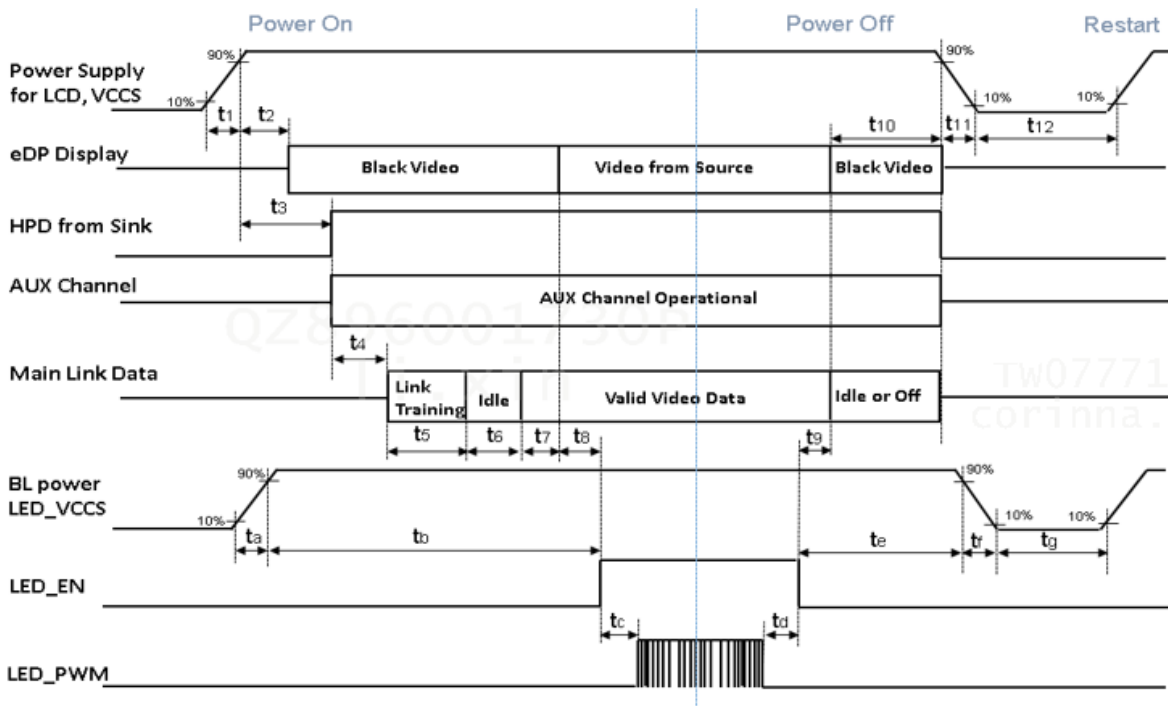
Signal	Item	Symbol	Typ.	Unit	Note
Frame rate	Frequency	Fr	60	Hz	-
DCLK	Clock frequency	Fc	138.78	MHz	-
Vertical Display Term	Total	Tv	1112	Th	Tv=Tvd+Tvb
	Active Display	Tvd	1080	Th	-
	Blank	Tvb	32	Th	-
Horizontal Display Term	Total	Th	2080	Tc	Th=Thd+Thb
	Active Display	Thd	1920	Tc	-
	Blank	Thb	160	Tc	-

INPUT SIGNAL TIMING DIAGRAM



3.6 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD assembly, the power on/off sequence should be as the diagram below.



Timing Specification

Symbol	Description	Value		Unit
		Min	Max	
t1	VCCS Power rail rise time, 10% to 90%	0.5	10	ms
t2	Delay from LCD,VCCS to black video generation	0	200	ms
t3	Delay from LCD,VCCS to HPD high	0	200	ms
t4	Delay from HPD high to link training initialization	0	500	ms
t5	Link training duration	0	500	ms
t6	Link idle	0	500	ms
t7	Delay from valid video data from Source to video on display	0	50	ms
t8	Delay from Valid Video Data to BL_EN enable	200	500	ms
t9	Delay from BL_EN disable to Black Video	200	500	ms
t10	Delay from end of valid video data from Source to power off	0	500	ms
t11	VCCS Power rail fall time, 90% to 10%	0.5	10	ms
t12	LCD power off to Restart	500	-	ms
ta	BL Power rail rise time, 10% to 90%	0.5	10	ms
tb	BL Power ON to BL_EN signal enable	20	-	ms
tc	Delay from BL_EN enable to BL_PWM on	10	-	ms
td	Delay from BL_PWM off to BL_EN disable	10	-	ms
te	Delay from BL_EN disable to BL power off	20	-	ms
tf	BL Power Power rail fall time, 90% to 10%	0.5	10	ms
tg	BL power off to Restart	500	-	ms

Note (1) Please don't plug or unplug the interface cable when system is turned on.

Note (2) It is recommended that the backlight power must be turned on after the power supply for LCD and the interface signal is valid.

4. OPTICAL CHARACTERISTICS

4.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	oC
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	According to typical value and tolerance in "ELECTRICAL CHARACTERISTICS"		
Input Signal			
PWM Duty Ratio	D	100	%

4.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 4.2 and all items are measured at the center point of screen except white variation. The following items should be measured under the test conditions described in 4.1 and stable environment shown in Note (5).

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note	
Color Chromaticity	Red	Rx	0.595	0.645	0.695	-	(1), (5)	
		Ry	0.285	0.335	0.385			
	Green	Gx	0.251	0.301	0.351			
		Gy	0.567	0.617	0.667			
	Blue	Bx	0.101	0.151	0.201			
		By	0.017	0.067	0.117			
	White	Wx	0.263	0.313	0.363			
		Wy	0.279	0.329	0.379			
Center Luminance of White	Lc	$\theta_X=0^\circ, \theta_Y=0^\circ$ Grayscale Maximum	1000	1200	-		(4), (5)	
Contrast Ratio	CR		700	1000	-		(2), (5)	
Response Time	T _R +T _F	$\theta_x=0^\circ, \theta_y=0^\circ$		25	35	ms	(3)	
White Variation	δW	$\theta_x=0^\circ, \theta_y=0^\circ$	75	80	-	%	(5), (6)	
Viewing Angle	Horizontal	θ_{x+}	CR \geq 10	80	89	-	Deg.	(1), (5)
		θ_{x-}		80	89	-		
	Vertical	θ_{y+}		80	89	-		
		θ_{y-}		80	89	-		

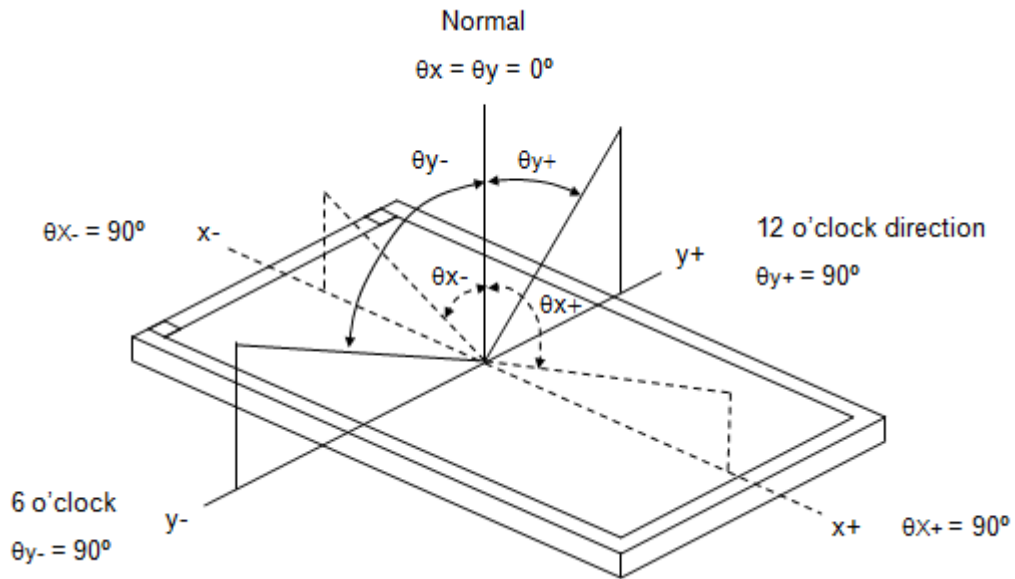
Definition :

Grayscale Maximum : Grayscale 255 (10 bits: grayscale 1023 ; 8 bits : grayscale 255 ; 6 bits: grayscale 63)

White : Luminance of Grayscale Maximum (All R,G,B)

Black : Luminance of grayscale 0 (All R,G,B)

Note (1) Definition of Viewing Angle (θ_x , θ_y):

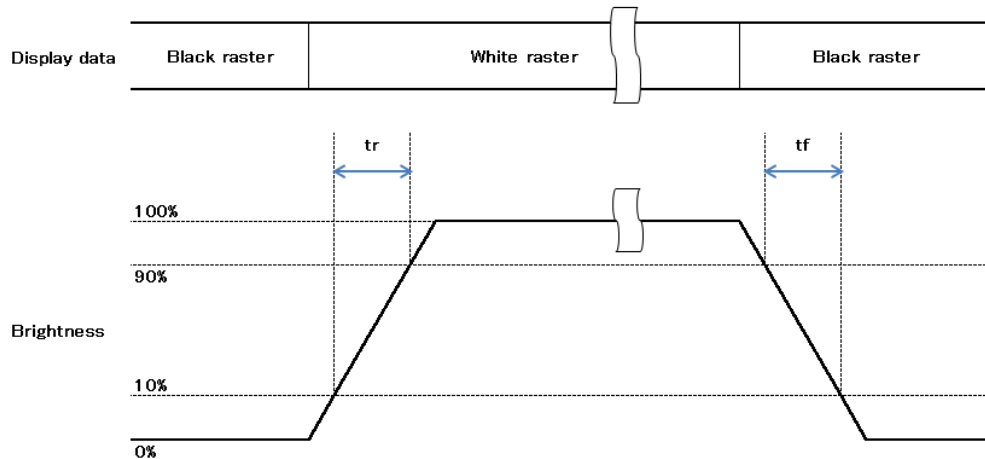


Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression at center point.

$$\text{Contrast Ratio (CR)} = \text{White} / \text{Black}$$

Note (3) Definition of Response Time (TR, TF):

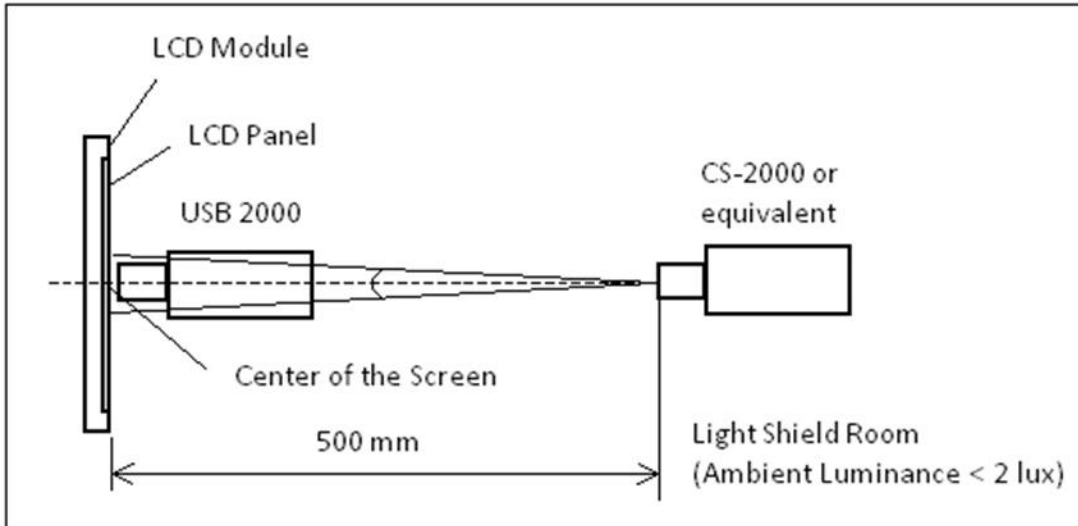


Note (4) Definition of Luminance of White (LC):

Measure the luminance of White at center point.

Note (5) Measurement Setup:

The LCD module should be stabilized at given temperature to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 40 minutes in a windless room. The measurement placement of module should be in accordance with module drawing.

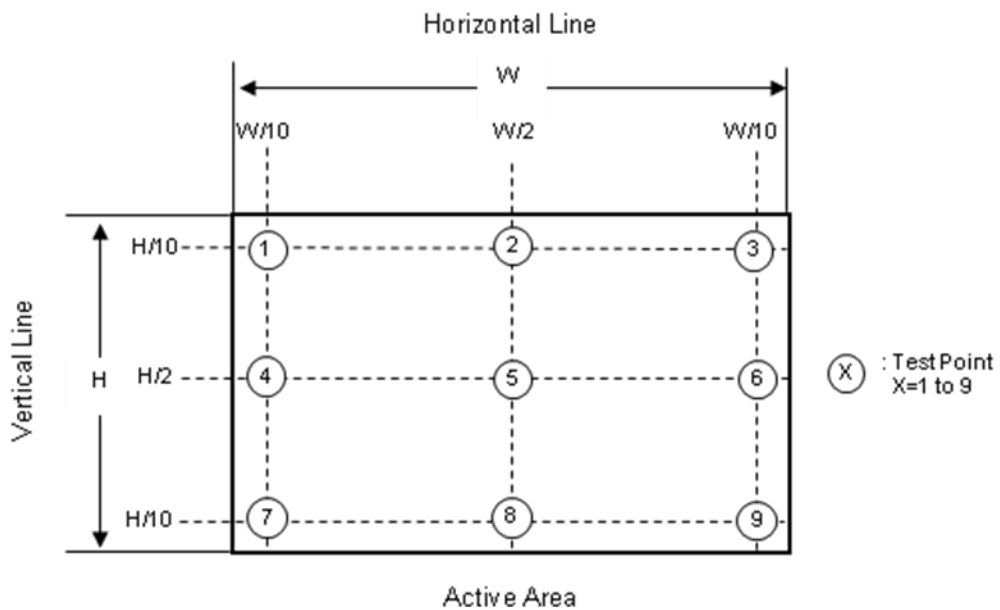


Note (6) Definition of White Variation (δW):

Measure the luminance of White at 9 points.

Luminance of White : $L(X)$, where X is from 1 to 9

$$\delta W = \frac{\text{Minimum [} L(1) \text{ to } L(9) \text{]}}{\text{Maximum [} L(1) \text{ to } L(9) \text{]}} \times 100\%$$



5. RELIABILITY TEST CRITERIA

Test Item	Test Condition	Note
High Temperature Storage Test	85°C, 240 hours	(1),(2) (4),(5)
Low Temperature Storage Test	-30°C, 240 hours	
Thermal Shock Storage Test	-20°C, 0.5 hour ↔ 60°C, 0.5 hour; 100cycles, 1 hour/cycle)	
High Temperature Operation Test	85°C, 240 hours	
Low Temperature Operation Test	-30°C, 240 hours	
High Temperature & High Humidity Operation Test	50°C, RH 80%, 240 hours	
ESD Test (Operation)	150pF, 330Ω, 1 sec/cycle Condition 1 : panel contact, ±8 KV Condition 2 : panel non-contact ±15 KV	(1), (4)
Shock (Non-Operating)	50G, 11ms, half sine wave, 1 time for ± X, ± Y, ± Z direction	(2), (3)
Vibration (Non-Operating)	1.5G, 10 ~ 300 Hz sine wave, 10 min/cycle, 3 cycles each X, Y, Z direction	

Note (1) There should be no condensation on the surface of panel during test.

Note (2) Temperature of panel display surface area should be 50°C Max.

Note (3) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

Note (4) In the standard conditions, there is no function failure issue occurred. All the cosmetic specification is judged before reliability test.

Note (5) Before cosmetic and function test, the product must have enough recovery time, at least 24 hours at room temperature.

6. PACKAGING

6.1 PACKING SPECIFICATIONS

- (1) 22pcs LCD modules / 1 Carton
- (2) Box dimensions: 565 (L) X 450 (W) X 275 (H) mm
- (3) Weight: approximately 16.9Kg (22 modules per carton)

6.2 PACKING METHOD

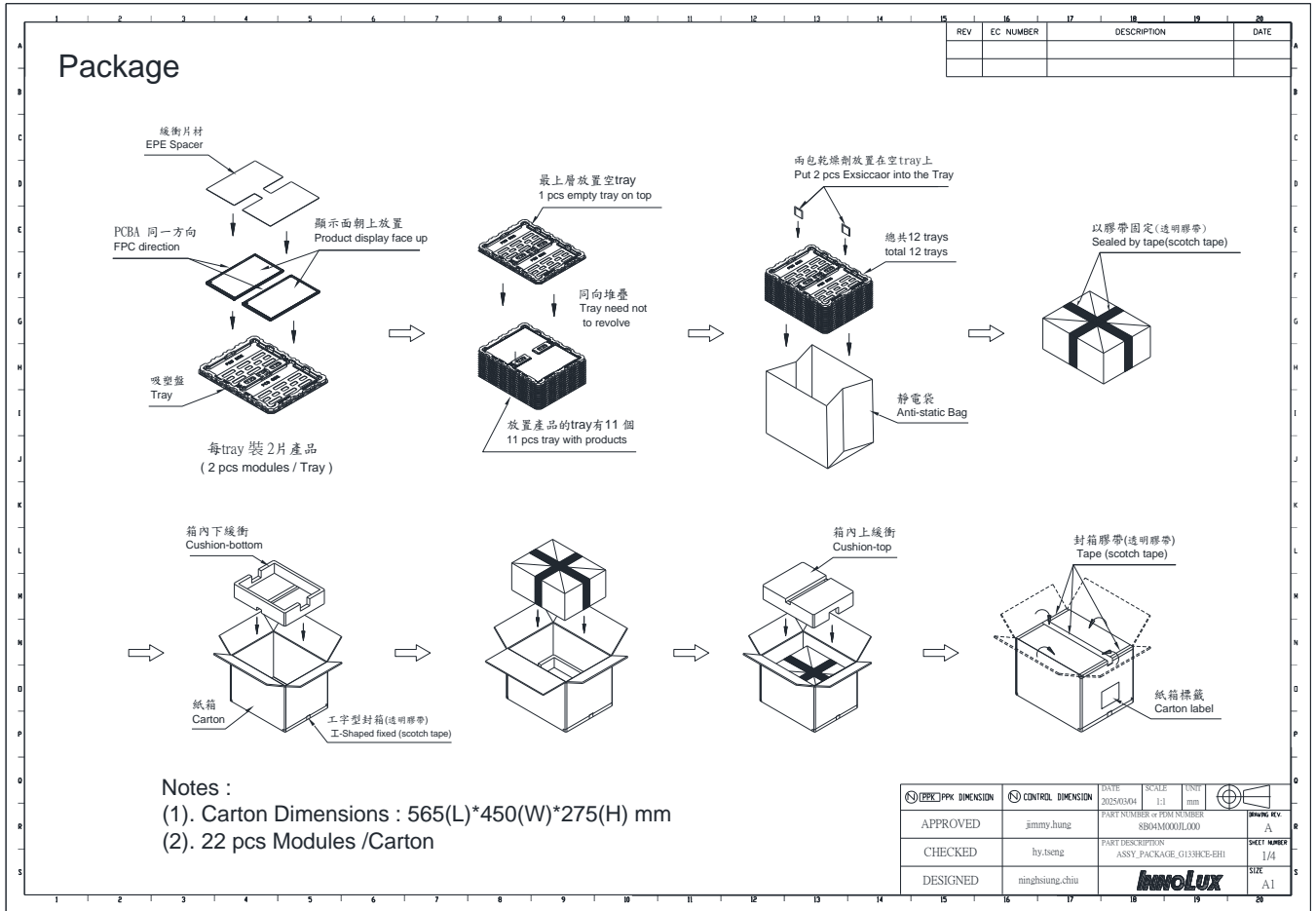


Figure. 6-1 Packing method

6.3 SHIPPING METHOD

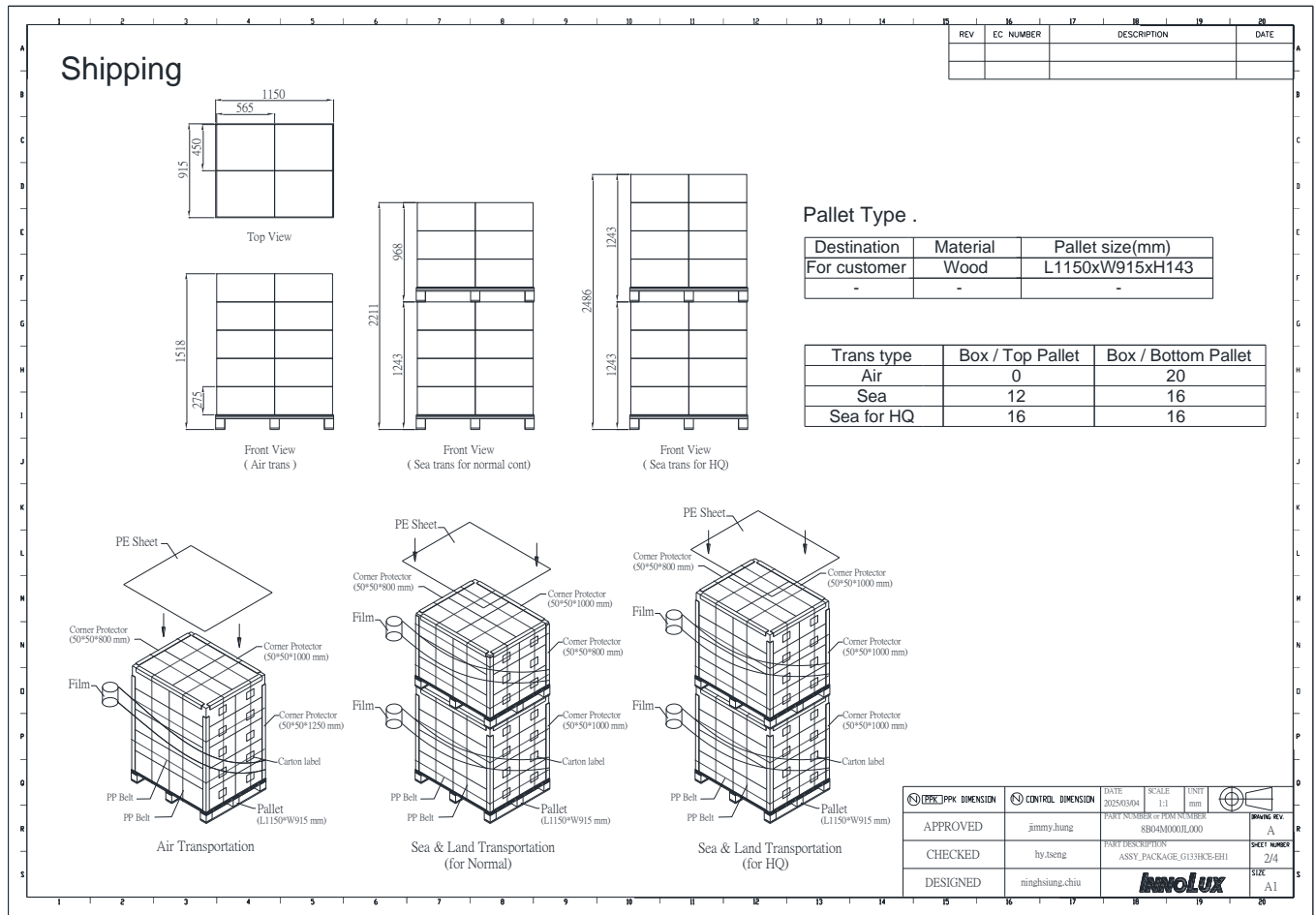
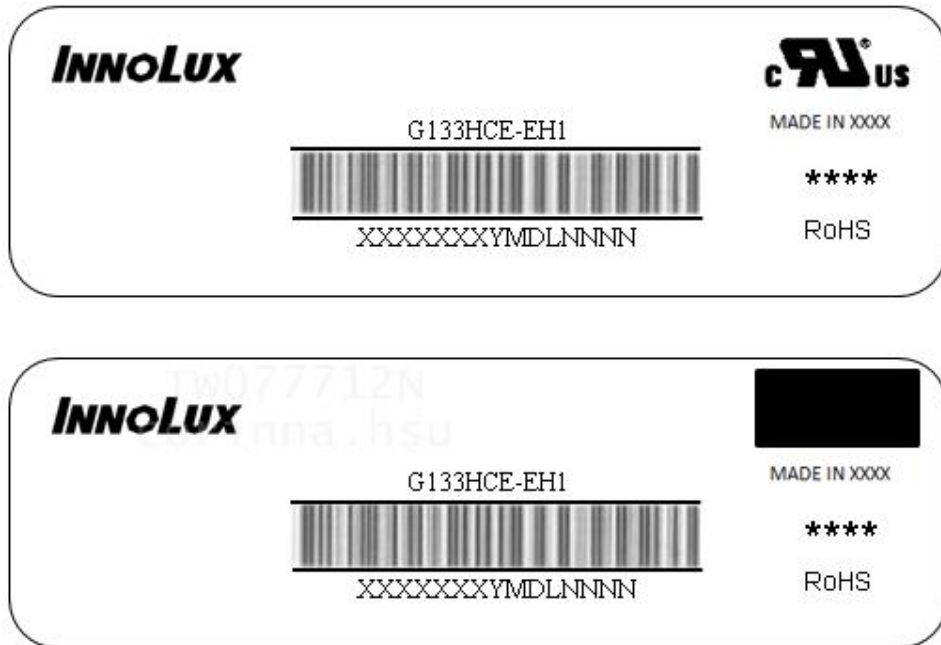


Figure. 6-2 Packing method

7. DEFINITION OF LABELS

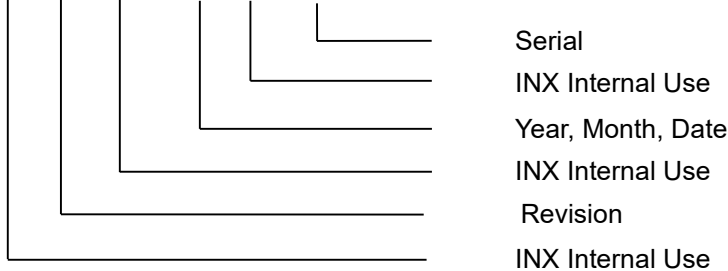
7.1 INX MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



Note (1) Safety Compliance(UL logo) will open after C1 version.

- (a) Model Name: G133HCE-EH1
- (b) * * * * : Factory ID
- (c) Serial ID: X X X X X X Y M D X N N N N



Serial ID includes the information as below:

- (a) Manufactured Date: 1~9, for 2021~2029
 Month: 1~9, A~C, for Jan. ~ Dec.
 Day: 1~9, A~Y, for 1st to 31st, exclude I , O and U
- (b) Revision Code: cover all the change
- (c) Serial No.: Manufacturing sequence of product

8. PRECAUTIONS**8.1 ASSEMBLY AND HANDLING PRECAUTIONS**

- (1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.
- (2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.
- (3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.
- (4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.
- (5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.
- (6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.
- (7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.
- (8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.
- (9) Do not disassemble the module.
- (10) Do not pull or fold the lamp wire.
- (11) Pins of I/F connector should not be touched directly with bare hands.

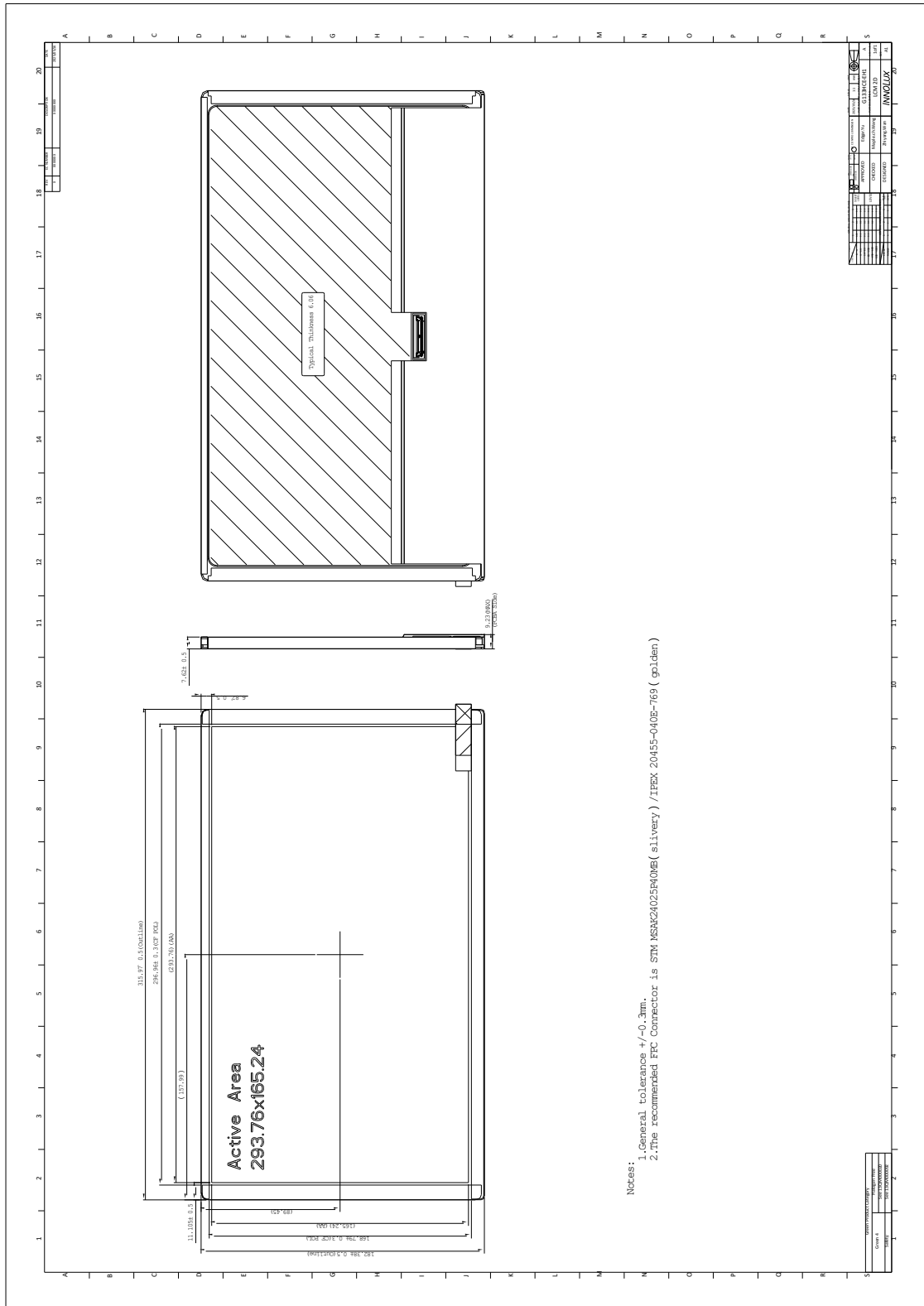
8.2 STORAGE PRECAUTIONS

- (1) When storing for a long time, the following precautions are necessary.
 - (a) Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5°C and 30°C at humidity 50+/-10%RH.
 - (b) The polarizer surface should not come in contact with any other object.
 - (c) It is recommended that they be stored in the container in which they were shipped.
 - (d) Storage condition is guaranteed under packing conditions.
 - (e) The phase transition of Liquid Crystal in the condition of the low or high storage temperature will be recovered when the LCD module returns to the normal condition
- (2) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.
- (3) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.
- (4) It may reduce the display quality if the ambient temperature is lower than 10 °C. For example, the response time will become slowly, and the starting voltage of lamp will be higher than the room temperature.
- (5) Storage must be in a fully packaged state (PET bag) and do not expose the sample (module).




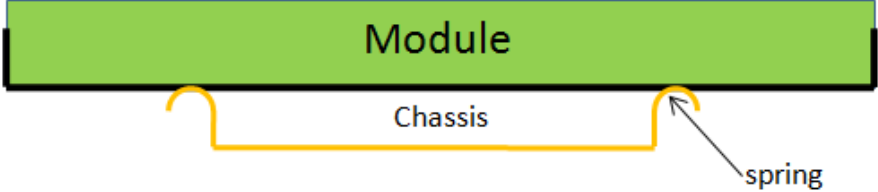
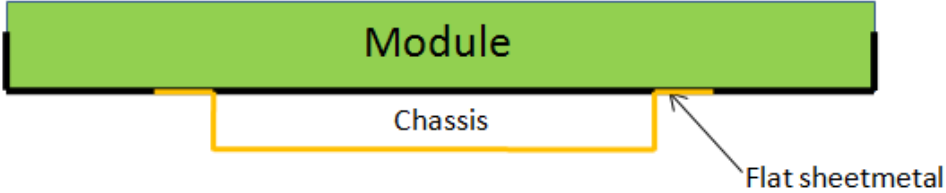
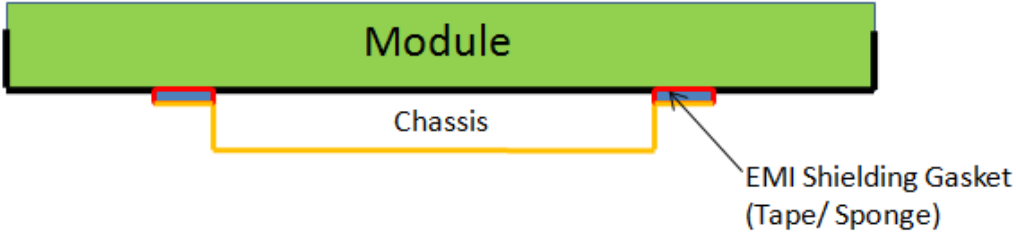
8.3 OTHER PRECAUTIONS

- (1) Normal operating condition
 - (a) Display pattern: dynamic pattern (Real display)
(Note) Long-term static display can cause image sticking.
- (2) Operating usages to protect against image sticking due to long-term static display
 - (a) Suitable operating time: under 16 hours a day.
 - (b) Static information display recommended to use with moving image.
 - (c) Cycling display between 5 minutes' information (static) display and 10 seconds' moving image.
- (3) Abnormal condition just means conditions except normal condition.

9. MECHANICAL CHARACTERISTICS

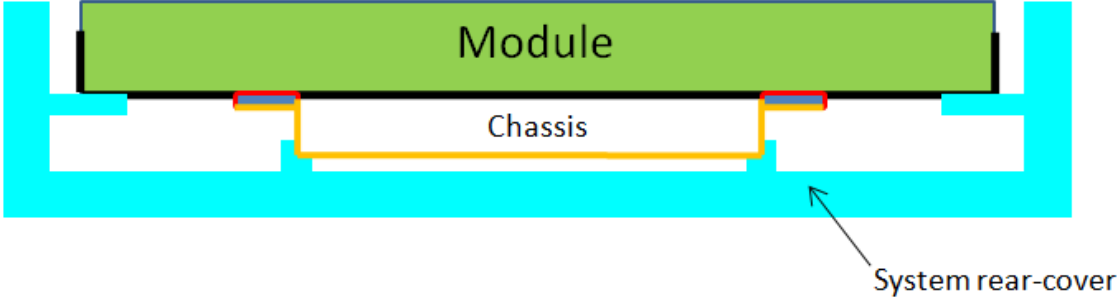


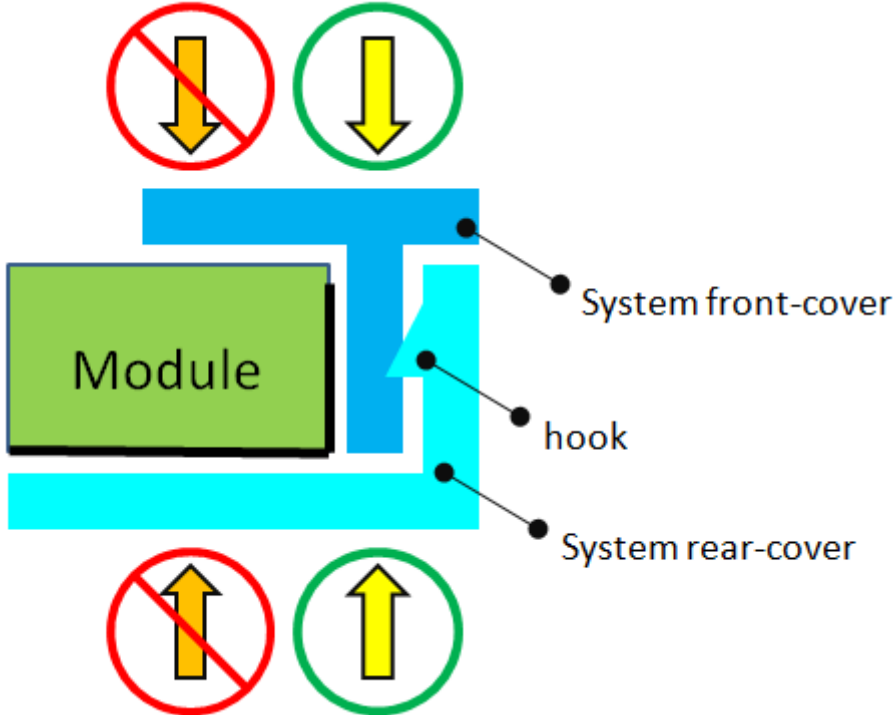
Appendix. SYSTEM COVER DESIGN NOTICE

1	Set Chassis and IA Module touching Mode
  	  
Definition	<p>a. To prevent from abnormal display & white spot after mechanical test, it is not recommended to use spring type chassis.</p> <p>b. We suggest the contact mode between Chassis and Module rear cover is Tape/Sponge, second is Flat sheet metal type chassis.</p>

2	Tape/Sponge design on system inner surface
<p>The diagrams illustrate the correct and incorrect placement of Tape/Sponge on the system inner surface. The top diagram shows a cross-section of a Module on a Chassis, with Tape/Sponge placed between them and a System rear bezel. Below are two top-down views: one with four L-shaped Tape/Sponge pieces (marked with a red X) and one with a single square Tape/Sponge piece (marked with a blue circle).</p>	
Definition	<p>a. To prevent from abnormal display & white spot after mechanical test, we suggest using Tape/Sponge as medium between chassis and Module rear cover could reduce the occurrence of white spot.</p> <p>b. When using the Tape/Sponge, we suggest it be lay over between set chassis and Module rear cover. It is not recommended to add Tape/Sponge in separate location. Since each Tape/Sponge may act as pressure concentration location.</p>

3	System inner surface examination
Definition	<p>a. The hatch area on Module PCBA should keep at least 1mm gap(X,Y,Z direction) to any structure with system cover inner surface.</p> <p>b. Burr, Step, PCB protrusion may cause stress concentration. White spot may occur during reliability test.</p>

4	Material used for system rear-cover
	
Definition	<p>System rear-cover material with high rigidity is needed to resist deformation during scuffing test, hinge test, pogo test or backpack test. Abnormal display, white spot, pooling issue may occur if low rigidity material is used. Pooling issue may occur because screw's boss position for module's bracket are deformed open-close test.</p> <p>Solid structure design of system rear-cover may also influence the rigidity of system rear-cover. The deformation of system rear-cover should not caused interference.</p>

5	Assembly SOP examination for system front-cover with hook structure
	
Definition	<p>To prevent panel crack during system front-cover assembly process with hook structure, it is not recommended to press panel or any location that relate directly to the panel.</p>

6	Permanent deformation of system cover after reliability test
<p>○</p> <p>×</p> <p>○</p> <p>×</p> <p>×</p> <p>×</p>	<p>● System front-cover</p> <p>● System rear-cover</p> <p>Module</p> <p>deformation</p> <p>● System front-cover</p> <p>● System rear-cover</p> <p>Module</p> <p>deformation</p> <p>● System front-cover</p> <p>● System rear-cover</p> <p>Module</p> <p>deformation</p> <p>● System front-cover</p> <p>● System rear-cover</p> <p>Module</p> <p>0 gap</p> <p>● System front-cover</p> <p>● System rear-cover</p> <p>Module</p> <p>● System front-cover</p> <p>● System rear-cover</p> <p>Module</p> <p>deformation</p>
Definition	<p>System cover including front cover and rear cover may deform during reliability test. Permanent deformation of system front cover and rear cover after reliability test should not interfere with panel. Because it may cause issue such as pooling, abnormal display, white spot and also cell creak.</p> <p>Note: If the interference cannot be avoided, please feel free to contract INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.</p>

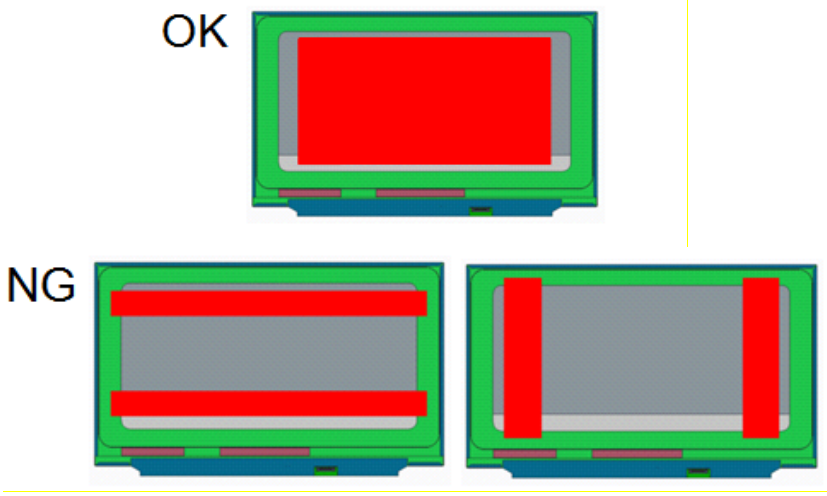

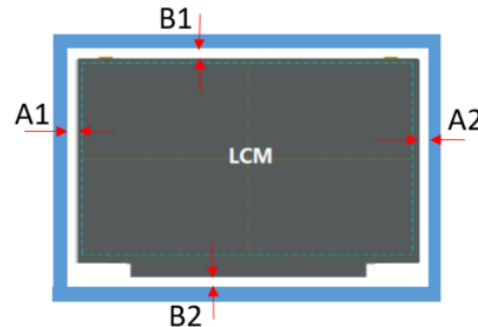
7	Design gap A between panel & any components on system rear-cover
Definition	<p>System cover including front cover and rear cover may deform during reliability test. Permanent deformation of system front cover and rear cover after reliability test should not interfere with panel. Because it may cause issue such as pooling, abnormal display, white spot and also cell creak.</p> <p>Note: If the interference cannot be avoided, please feel free to contract INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.</p>

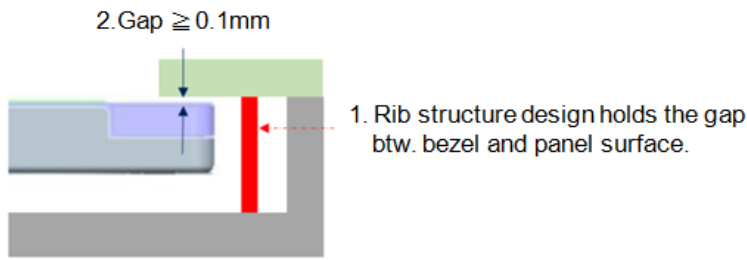
8	Design gap B between system front-cover & panel surface
Definition	<p>Gap between system front-cover & panel surface is needed to prevent pooling or glass broken. Zero gap or interference such as burr and warpage from mold frame may cause pooling issue near system front-cover opening edge. This phenomenon is obvious during swing test, hinge test, knock test or during pooling inspection procedure.</p> <p>To remain sufficient gap, design with system rib higher than maximum panel thickness is recommended.</p> <p>Note: If the interference cannot be avoided, please feel free to contract INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.</p>

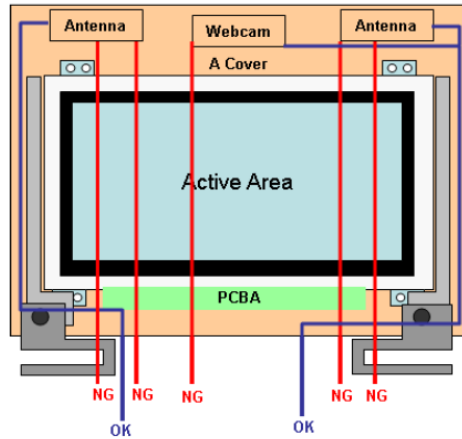
9	Design gap C between panel & system front-cover or protrusions
Definition	<p>Gap between panel & system front-cover or protrusions is needed to prevent shock test failure. Because system front-cover or protrusions with small gap may hit panel during the test. Issue such as cell crack, abnormal display may occur.</p> <p>The gap should be large enough to absorb the maximum displacement during the test.</p> <p>Note: If the interference cannot be avoided, please feel free to contract INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.</p>

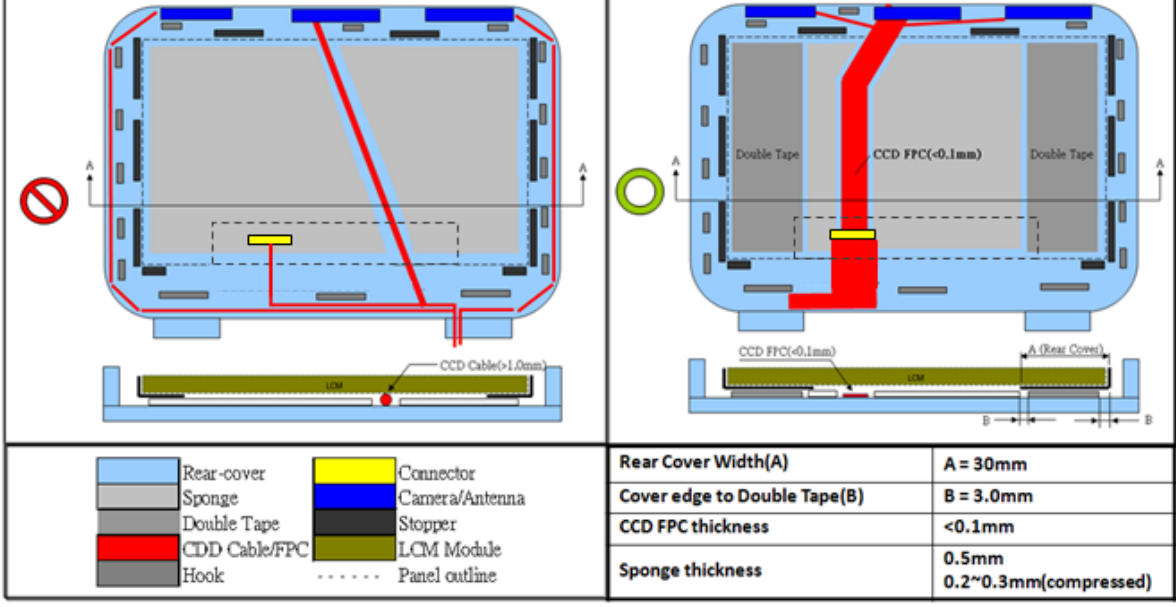
11	Use OCR Lamination
<p>The diagram illustrates two methods for avoiding line pooling in OCR lamination. The top diagram, marked with a red 'X', shows 'Line pooling' occurring at the edges of the 'TP or Cover Glass' layer. The bottom diagram, marked with a green circle, shows 'OCR overflow' and 'Add Side glue' at the edges, which prevents line pooling. A detailed inset shows the 'TP' and 'OCR' layers meeting at the edge with 'OCR overflow' and 'Add Side glue'.</p>	
Definition	<ol style="list-style-type: none"> 1.OCR glue as possible beyond module, in order to avoid Line Pooling 2.Add side glue to avoid Line Pooling

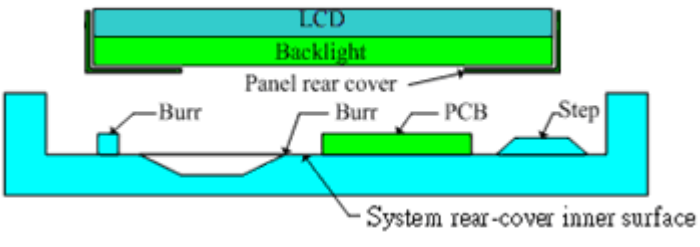
12	Use OCA Lamination
<p>The diagram illustrates two methods for OCA lamination. The top diagram, marked with a red 'X', shows 'Line pooling' occurring at the edges of the 'TP or Cover Glass' layer. The bottom diagram, marked with a green circle, shows 'Add Side glue' applied to the edges to prevent 'Line Pooling'. Both diagrams show a cross-section of the display assembly with layers including 'TP or Cover Glass', 'OCA', and various substrate layers. A 'Display Area' is indicated between two vertical dashed lines. An upward arrow 'F' indicates the direction of force applied during lamination.</p>	
Definition	<p>1.OCA glue as possible plastered throughout the module, in order to avoid Line Pooling. 2.Add side glue to avoid Line Pooling</p>

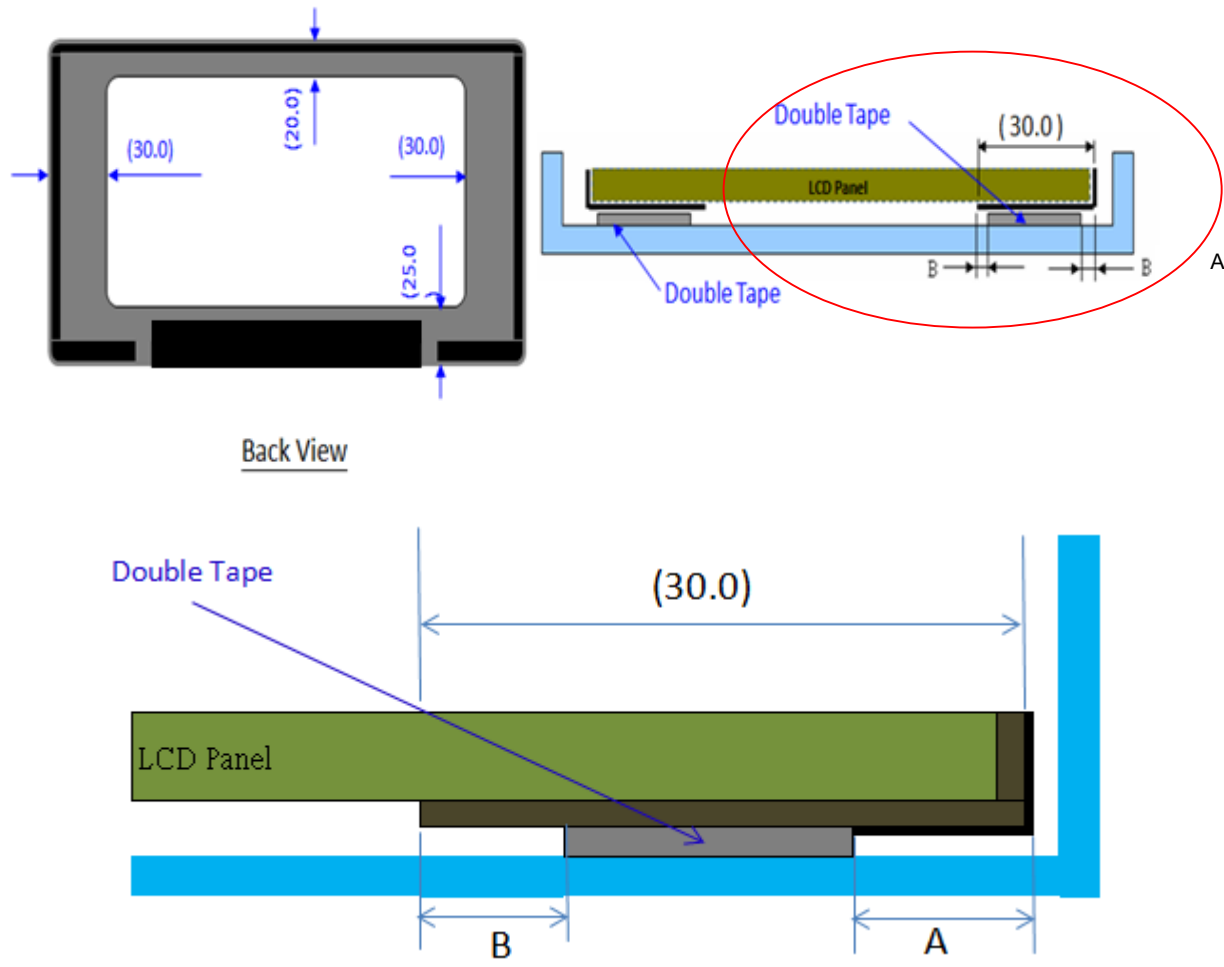
1	Sponge area design behind panel												
													
Definition	Sponge area design behind panel can not be across the panel metal rear and the reflector at the same time. It can be on the reflector area only.												
2	Gap between system rear-cover & panel												
													
Definition	The maximum thickness of sponge on the system rear-cover can not interfere to the maximum thickness of panel. Because the interference may cause stress concentration. Issues such as pooling, abnormal display, white spot, and cell crack may occur. Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.												
3	Gap Design between panel & around structure												
 <table border="1" data-bbox="766 1668 1404 1825"> <thead> <tr> <th>Item</th> <th>Suggestion</th> <th>Remark</th> </tr> </thead> <tbody> <tr> <td>A1</td> <td>A1 ≥ 0.5</td> <td rowspan="4">Gap ≥ Panel outline max. tolerance + Assembly max. tolerance</td> </tr> <tr> <td>A2</td> <td>A2 ≥ 0.5</td> </tr> <tr> <td>B1</td> <td>B1 ≥ 0.5</td> </tr> <tr> <td>B2</td> <td>B2 ≥ 0.8</td> </tr> </tbody> </table>		Item	Suggestion	Remark	A1	A1 ≥ 0.5	Gap ≥ Panel outline max. tolerance + Assembly max. tolerance	A2	A2 ≥ 0.5	B1	B1 ≥ 0.5	B2	B2 ≥ 0.8
Item	Suggestion	Remark											
A1	A1 ≥ 0.5	Gap ≥ Panel outline max. tolerance + Assembly max. tolerance											
A2	A2 ≥ 0.5												
B1	B1 ≥ 0.5												
B2	B2 ≥ 0.8												
Definition	Gap Design between panel & around structure needs to consider the maximum tolerances of panel outline and assembly at the same time. Gap Design suggestion is shown as A1/A2/B1/B2 on the chart.												

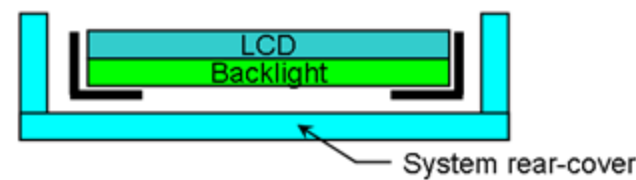
4	Gap between panel & bezel
	
Definition	<p>The gap between system bezel & panel surface is needed to prevent pooling or glass broken. Zero gap or interference such as burr and warpage from mold frame may cause pooling issue near system front-cover opening edge. This phenomenon is obvious during swing test, hinge test, knock test, or during pooling inspection procedure.</p> <p>To remain the sufficient gap, design with system rib higher than maximum panel thickness is recommended.</p> <p>The sufficient gap design is greater or equal to 0.1mm.</p>

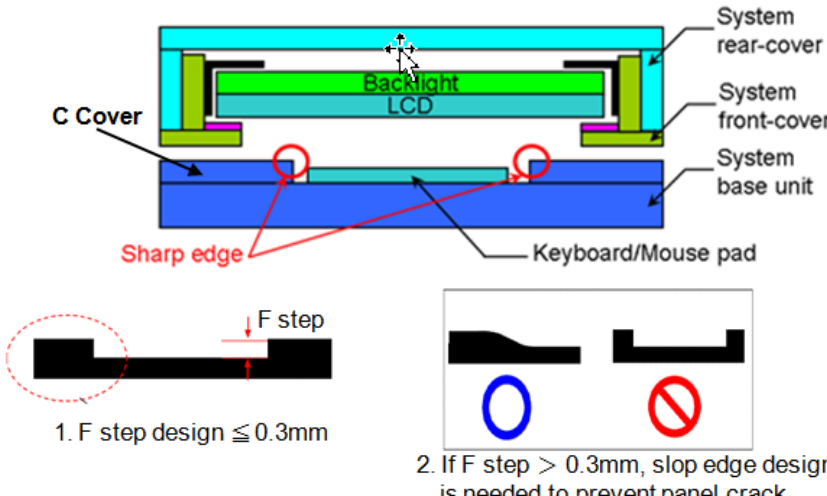
5	Cable routing behind panel
	
Definition	<p>It is strongly recommended that cables route around the panel outline, not overlap with the panel outline (including PCB). Because issue such as abnormal display & white spot after backpack test, hinge test, twist test or pogo test may occur.</p> <p>If any routings across panel outline are needed, we suggest design as below:</p> <ul style="list-style-type: none"> -Using FFC/FPC to replace cables. -Routing at the right or left area of panel metal rear. -Avoid any routings at the step of panel or A cover. -No interference to panel. -It should not overlap TCON, COF/FPC, Driver IC

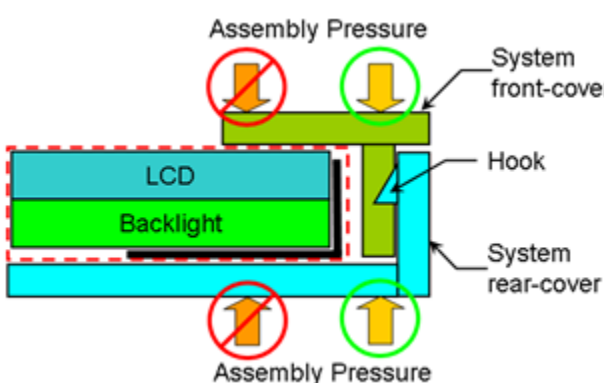
6	Interference examination of antenna cable and Web Cam wire								
<ul style="list-style-type: none"> To prevent panel damage, we suggest using CCD FPC to replace CCD cable Using double tape to fix LCM module for no bracket design. 									
 <table border="1" data-bbox="853 884 1428 1041"> <tr> <td>Rear Cover Width(A)</td> <td>A = 30mm</td> </tr> <tr> <td>Cover edge to Double Tape(B)</td> <td>B = 3.0mm</td> </tr> <tr> <td>CCD FPC thickness</td> <td><0.1mm</td> </tr> <tr> <td>Sponge thickness</td> <td>0.5mm 0.2~0.3mm(compressed)</td> </tr> </table>		Rear Cover Width(A)	A = 30mm	Cover edge to Double Tape(B)	B = 3.0mm	CCD FPC thickness	<0.1mm	Sponge thickness	0.5mm 0.2~0.3mm(compressed)
Rear Cover Width(A)	A = 30mm								
Cover edge to Double Tape(B)	B = 3.0mm								
CCD FPC thickness	<0.1mm								
Sponge thickness	0.5mm 0.2~0.3mm(compressed)								
Definition	<p>If the antenna cable or Web Cam wire must overlap with the panel outline, both sides of the antenna cable or Web Cam wire must have a sponge(Sponge material can not contain NH3) and sponge require higher antenna cable or Web Cam wire. (Antenna cable or Web Cam wire should not overlap with TCON,COF/FPC,Driver IC)</p> <p>Note: If the interference can not be avoided, please feel free to contact INX FAE Engineer for collaboration design. We can help to verify and pass risk assessment for customer reference.</p>								

7	System rear-cover inner surface examination
	
Definition	<p>Burr at logo edge, steps, protrusions or PCB board may cause stress concentration. White spot or glass broken issue may occur during reliability test.</p>

8	Tape/sponge design on system inner surface
 <p>The diagrams illustrate the tape/sponge design on the system inner surface. The top left shows a 'Back View' of the LCD panel with dimensions: (30.0) for the width, (20.0) for the height, and (25.0) for the bottom bezel thickness. The top right shows a cross-section of the LCD Panel (green) attached to a blue system inner surface with 'Double Tape'. The total width of the tape is (30.0), with 'A' representing the bezel tape length and 'B' representing the double tape attaching tolerance. The bottom diagram is a detailed cross-section showing the 'LCD Panel' (green) and 'Double Tape' (blue) with dimensions (30.0) for the total tape width, 'B' for the double tape attaching tolerance, and 'A' for the bezel tape length.</p>	
Definition	<p>To prevent peeling the bezel tape in rework process. The length of double tape is $30 - (A+B)$, A is bezel tape length and B is the double tape attaching tolerance. Ex :A :2mm, B:2mm, the length of double tape is $30-(2+2)=26\text{mm}$.</p>

9	Material used for system rear-cover
 <p>The diagram shows the LCD Backlight (green) assembly mounted on the System rear-cover (cyan). The System rear-cover material is Al-Mg alloy and has a thickness of 1.5mm.</p>	
Definition	<p>System rear-cover material with high rigidity is needed to resist deformation during scuffing test, hinge test, pogo test, or backpack test. Abnormal display, white spot, pooling issue may occur if low rigidity material is used. Solid structure design of system rear-cover may also influence the rigidity of system rear-cover. The deformation of system rear-cover should not caused interference.</p>

10	C cover shape design
 <p>The diagram illustrates the assembly of the C cover. Components shown include the System rear-cover, System front-cover, System base unit, Backlight LCD, and Keyboard/Mouse pad. A 'Sharp edge' is highlighted in red. Below the main diagram, two edge design options are shown: a standard 'F step' design and a 'slop edge' design. A blue circle indicates the preferred design, while a red circle with a slash indicates the disallowed design.</p> <p>1. F step design $\leq 0.3\text{mm}$</p> <p>2. If F step $> 0.3\text{mm}$, slop edge design is needed to prevent panel crack.</p>	
Definition	The F step design on C Cover less than or equal to 0.3mm is recommended. If F step exceeds 0.3mm, the slop edge design is necessary to prevent panel crack.

11	Assembly SOP examination for system front-cover with Hook design
 <p>The diagram shows the assembly process for the system front-cover with a hook design. It includes the System front-cover, Hook, System rear-cover, LCD, and Backlight. 'Assembly Pressure' is indicated by arrows. Red arrows with slashes indicate incorrect pressure points on the panel, while green arrows indicate correct pressure points on the hook and front-cover frame.</p>	
Definition	To prevent panel crack during system front-cover assembly process with hook design, it is not recommended to press panel or any location that related directly to the panel.

12	Adhesive design between panel & bezel
<div style="display: flex; justify-content: space-around;"> <div style="border: 1px solid black; padding: 5px; width: 45%;"> <p style="text-align: center;">OK</p> <p style="text-align: center;">1.00mm</p> <p style="text-align: center;">B-Cover</p> <p style="text-align: center;">CF Pol.</p> <p style="text-align: center;">Adhesive</p> <p>• Risk : Bezel Tape Peeling happened in a rework or reassembly process.</p> </div> <div style="border: 1px solid black; padding: 5px; width: 45%;"> <p style="text-align: center;">NG</p> <p style="text-align: center;">B-Cover</p> <p style="text-align: center;">CF Pol.</p> <p style="text-align: center;">Adhesive</p> <p>• Risk : Pooling or light leakage due to stress concentration at B-cover opening</p> </div> </div>	
Definition	<p>To prevent panel crack during system front-cover assembly process with double tape design, When system applied adhesive between B-Cover and LCD module, please design a distance 1.00mm between B-Cover's adhesive and CF pol. Do NOT put adhesive on CF pol. Adhesive material need be qualified to prevent from doing damage to cell tape after rework. Adhesive material need be qualified to prevent abnormal noise when hinge swinging test.</p>

13	System front-cover assembly reference with Double tape design
<p style="text-align: center;">0.1 mm</p> <p style="text-align: center;">A.A.</p> <p style="text-align: center;">B-Cover</p> <p style="text-align: center;">CF Pol.</p>	
Definition	<p>To prevent system front-cover peeling at double tape contact area, A gap between B-Cover & CF-Pol. Is 0.1mm min.</p>

14	System front-cover opening area reference with TFT-LCD module
<p style="text-align: center;">≥ 0.65mm</p> <p style="text-align: center;">A.A.</p> <p style="text-align: center;">B-Cover</p> <p style="text-align: center;">CF Pol.</p> <p style="text-align: center;">CF Glass</p>	
Definition	<p>To prevent panel the noise of B-cover & CF Pol. Distance from CF Pol. edge to front-cover more than 0.65mm.</p>

15	Color of system front-cover material
	<p>The diagrams illustrate the importance of front-cover material color in preventing light leakage. The top part shows cross-sections of the LCD and backlight assembly. In the first case, a light grey front cover allows light to leak out, indicated by orange arrows and the label 'Light Leakage'. In the second case, a black front cover prevents light leakage. The bottom part shows top-down views of the panel module. In the first case, a light grey front cover or TP (Touch Panel) allows light to leak out from the edges, indicated by yellow arrows and the label 'Light leakage'. In the second case, a black front cover or TP prevents light leakage.</p>
Definition	To prevent light leakage is seen at system front-cover due to material transparency, we suggest using dark color material (black) for system front-cover design.

16	Design Gap between System Front-cover & TOD LCD module surface
<p style="text-align: center;">$0.15 \leq \text{Gap A} \leq 0.20 \text{ mm}$</p>	
Definition	<p>Gap A between system front-cover & TOD LCD module surface is needed to prevent pooling or glass broken. Zero gap or interference such as burr and warpage from mold frame may cause pooling issue near system font-cover opening edge. This phenomenon is obvious during swing test, hinge test, knock test, or during pooling inspection procedure.</p> <p>To remain sufficient gap for first graph, design value for front-cover depth is recommended higher than module wing depth.</p>

17	System Front-cover dimension suggestion												
<table border="1"> <thead> <tr> <th>System Front Cover Open TOP to CF Pol. (A)</th> <th>System Front Cover Chamfer (B)</th> <th>System Front Cover Open to AA (C)</th> <th>Bezel Tape Edge to Double Tape (D)</th> <th>System Front Cover thickness (E)</th> <th>Double Tape Thickness (F)</th> </tr> </thead> <tbody> <tr> <td>0.8mm Max</td> <td>8~20°</td> <td>$0.7 \leq (C) \leq 0.9\text{mm}$</td> <td>1.0 mm Min</td> <td>1.2mm MAX</td> <td>$0.05 \leq (F) \leq 0.08\text{mm}$</td> </tr> </tbody> </table>		System Front Cover Open TOP to CF Pol. (A)	System Front Cover Chamfer (B)	System Front Cover Open to AA (C)	Bezel Tape Edge to Double Tape (D)	System Front Cover thickness (E)	Double Tape Thickness (F)	0.8mm Max	8~20°	$0.7 \leq (C) \leq 0.9\text{mm}$	1.0 mm Min	1.2mm MAX	$0.05 \leq (F) \leq 0.08\text{mm}$
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<p>CAUTION : In order to avoid the risk of bezel tape peeling, INX suggest not to attach any double tape on bezel tape; if necessary, the location of double tape attach must follow INX design guidance.</p>													
Definition	To achieve better touch sensibility, INX suggests to follow design value as recommended , Recommended dimension is shown in above graph.												