Approval Sheet

■ **Preliminary specification**

☐ **Final specification**

Customer Name	
Product Description	**0.39inch XGA Micro-OLED PCB Module**
Version	
Supplier	**BOE**
Module Code	**VX039X0M-NH0**

Customer Approval		**BOE Approval**	
SIGNATURE/TITLE	**DATE**	**SIGNATURE/TITLE**	**DATE**
PREPARED BY		**PREPARED BY**	
REVIEWED BY		**REVIEWED BY**	
APPROVED BY (R&D)		**APPROVED BY (R&D)**	
APPROVED BY (QA)		**APPROVED BY (QA)**	

Yunnan Invensight Optoelectronics Technology Co., Lt

目录

Version	Date	Description
V0.1	2023.04.26	Initial release

1.0 cm (Type 0.39) Active Matrix Color OLED Panel Module

1. Overview/Application

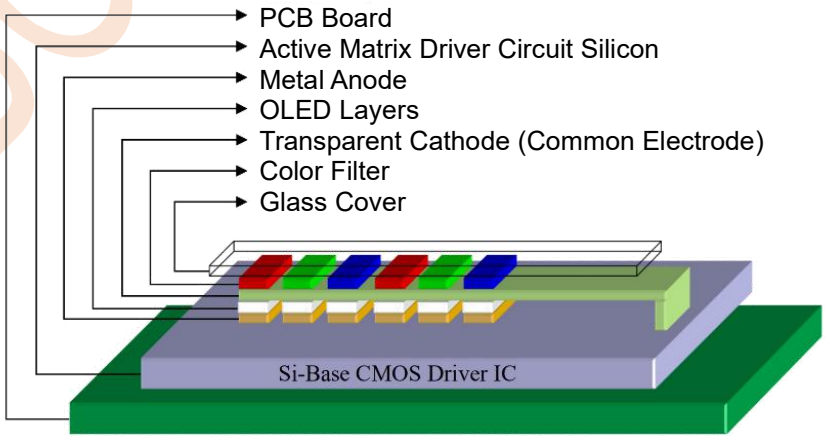
VX039X0M-NH0 is a 0.39 inch (1cm) diagonal, resolution1024 x768), active matrix color OLED (Organic Light Emitting Display) panel module based on single crystal silicon backplane. The pixel circuits and driving IC are integrated on the silicon backplane to get the compact size and very low power consumption.

2. Features

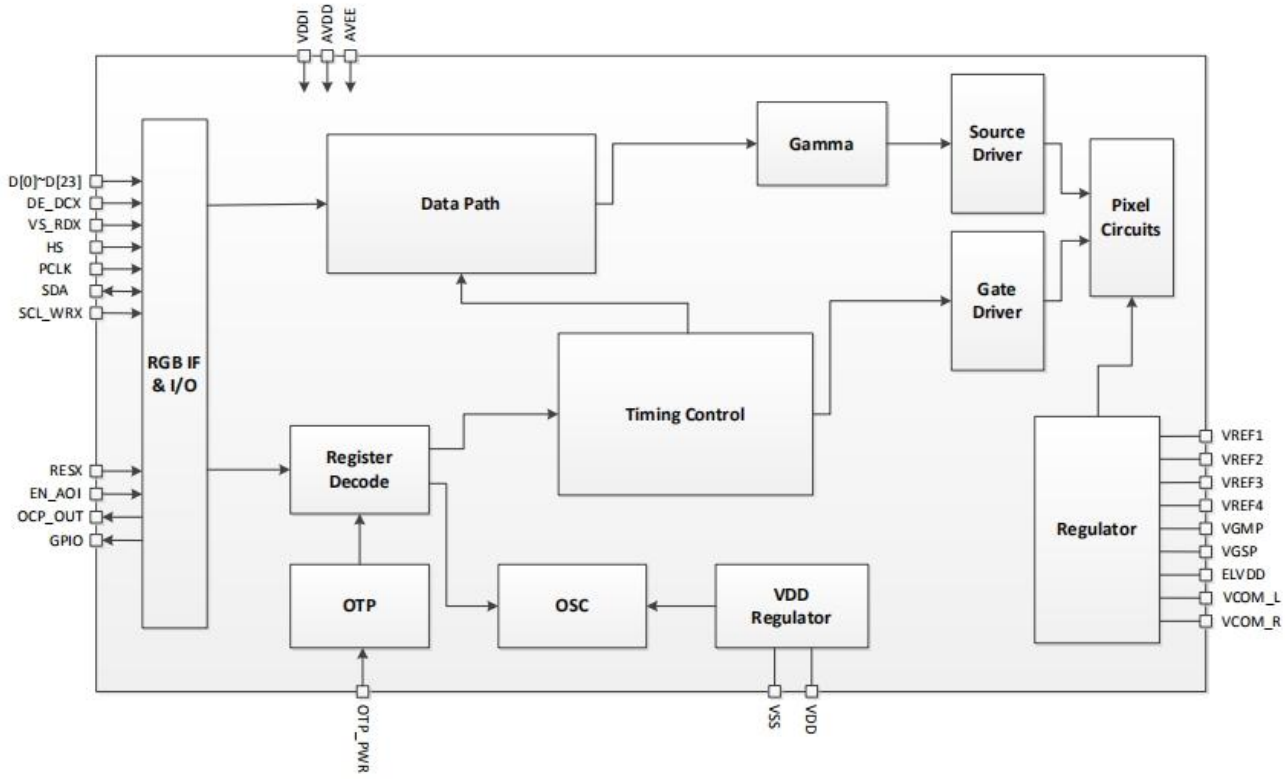
- Small-size, high resolution 0.39 XGA Display PPI=3282
- AP Operated Resolution (4*M, M=160~256) x RGB x (4*N, N=120~192)
- Full color mode, 16.7M colors
- Fast response
- Pattern Shift (Pixel Shift)
- Thin and light in weight
- Color enhancement, Sharpness enhancement
- High contrast mode
- High fluency mode
- Power-saving (PS) mode
- Scan direction selection, up or down
- Interface: RGB interface is for video data transmission
  I^2C interface is for command setting

3. Module Structure

- Active matrix color OLED display with on-chip driver based on single crystal silicon transistors

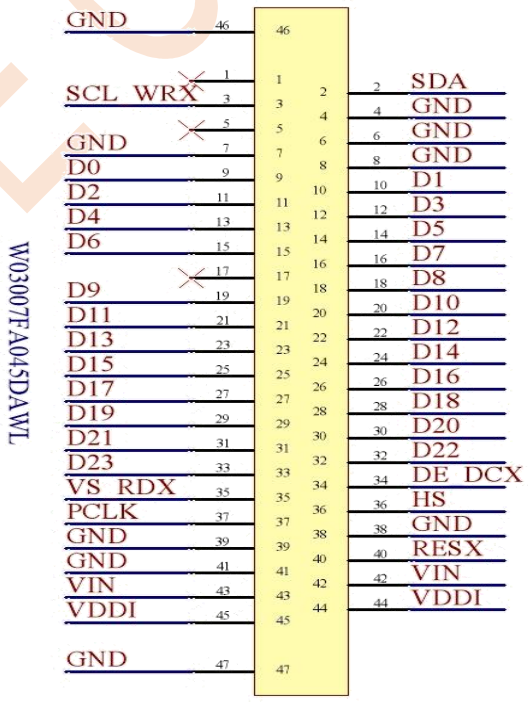


4. System Block Diagram



5. Pin Description

5.1 Pin Assignment of PCB Module



5.2 Pin description of PCB Module

PIN No.	Symbol	Type	Description
1	NC	Dummy pin	-
2	SDA	Input/ Output	Bi-direction data PIN in I2C I/F If this pin is not used, please connect to VDDI
3	SCL_WRX	Input	Synchronous clock signal in I2C I/F If this pin is not used, please connect to VDDI
4	GND	Power Supply	Circuit ground
5	NC	Dummy pin	-
6	GND	Power Supply	Circuit ground
7	NC	Dummy pin	-
8	GND	Power Supply	Circuit ground
9	D0	Input	This pin is video data signals in RGB interface. If not used, please connect to vss.
10	D1	Input	This pin is video data signals in RGB interface. If not used, please connect to vss.
11	D2	Input	This pin is video data signals in RGB interface. If not used, please connect to vss.
12	D3	Input	This pin is video data signals in RGB interface. If not used, please connect to vss.
13	D4	Input	This pin is video data signals in RGB interface. If not used, please connect to vss.
14	D5	Input	This pin is video data signals in RGB interface. If not used, please connect to vss.
15	D6	Input	This pin is video data signals in RGB interface. If not used, please connect to vss.
16	D7	Input	This pin is video data signals in RGB interface. If not used, please connect to vss.
17	NC	Dummy pin	-
18	D8	Input	This pin is video data signals in RGB interface. If not used, please connect to vss.
19	D9	Input	This pin is video data signals in RGB interface. If not used, please connect to vss.
20	D10	Input	This pin is video data signals in RGB interface. If not used, please connect to vss.
21	D11	Input	This pin is video data signals in RGB interface. If not used, please connect to vss.
22	D12	Input	This pin is video data signals in RGB interface. If not used, please connect to vss.
23	D13	Input	This pin is video data signals in RGB interface. If not used, please connect to vss.
24	D14	Input	This pin is video data signals in RGB interface. If not used, please connect to vss.
25	D15	Input	This pin is video data signals in RGB interface. If not used, please connect to vss.
26	D16	Input	This pin is video data signals in RGB interface. If not used, please connect to vss.
27	D17	Input	This pin is video data signals in RGB interface. If not used, please connect to vss.
28	D18	Input	This pin is video data signals in RGB interface. If not used, please connect to vss.
29	D19	Input	This pin is video data signals in RGB interface. If not used, please connect to vss.
30	D20	Input	This pin is video data signals in RGB interface. If not used, please connect to vss.
31	D21	Input	This pin is video data signals in RGB interface. If not used, please connect to vss.
32	D22	Input	This pin is video data signals in RGB interface. If not used, please connect to vss.
33	D23	Input	This pin is video data signals in RGB interface. If not used, please connect to vss.
34	DE_DCX	Input	Video data enable signal in RGB interface. If not used, please connect to vss.
35	VS_RDX	Input	Vertical sync signal in RGB interface. If not used, please connect to vss.
36	HS	Input	Horizontal sync signal in RGB interface. If not used, please connect to vss.
37	PCLK	Input	Pixel clock signal in RGB interface. If not used, please connect to vss.
38	GND	Power Supply	Circuit ground
39	GND	Power Supply	Circuit ground
40	RESX	Input	Reset the device and must be applied to properly initialize the chip. Active low.
41	GND	Power Supply	Circuit ground

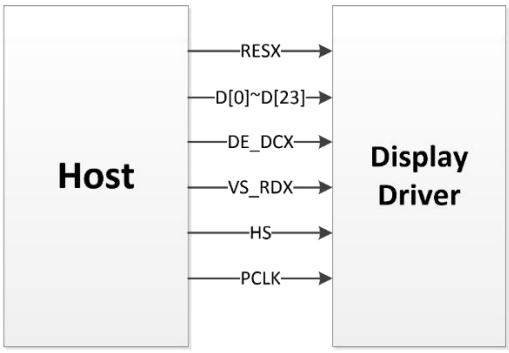
42	VIN	Power Supply	Power supply for analog system.
43	VIN	Power Supply	Power supply for analog system.
44	VDDI	Power Supply	Power supply for interface system except for MIPI interface.
45	VDDI	Power Supply	Power supply for interface system except for MIPI interface.
46	GND	Dummy pin	-
47	GND	Dummy pin	-

5.3 Video Data Interface

Pin No.	Video Data	RGB 8:8:8	Pin No.	Video Data	RGB 8:8:8	Pin No.	Video Data	RGB 8:8:8
33	D23	R[7]	25	D15	G[7]	16	D7	B[7]
32	D22	R[6]	24	D14	G[6]	15	D6	B[6]
31	D21	R[5]	23	D13	G[5]	14	D5	B[5]
30	D20	R[4]	22	D12	G[4]	13	D4	B[4]
29	D19	R[3]	21	D11	G[3]	12	D3	B[3]
28	D18	R[2]	20	D10	G[2]	11	D2	B[2]
27	D17	R[1]	19	D9	G[1]	10	D1	B[1]
26	D16	R[0]	18	D8	G[0]	9	D0	B[0]

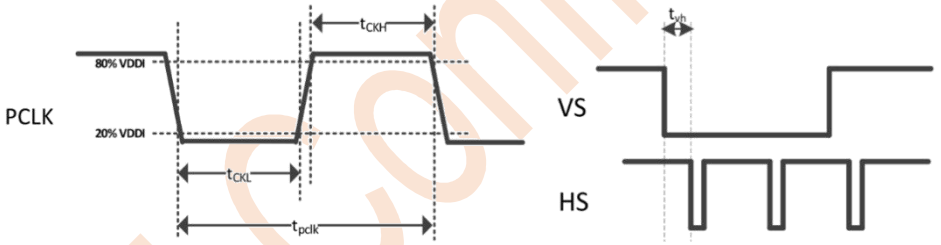
6. RGB Interface

RGB interface is a parallel interface that transmits 8-bits of red, green and blue data to each pixel. There are two mode for video data transmission, RGB video mode 1 use DE signal to mark valid data area. RGB video mode 2 do not use DE pin, instead of that, user have to set RGB_HBP register in command 1 to inform driver IC the end of HBP.

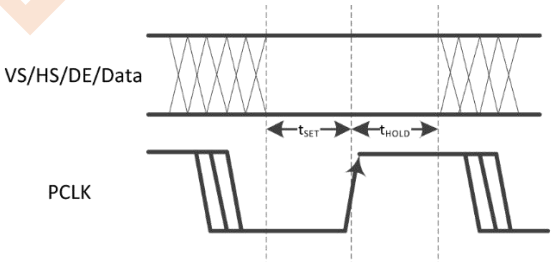


6.1 RGB Signal Timing Characteristics

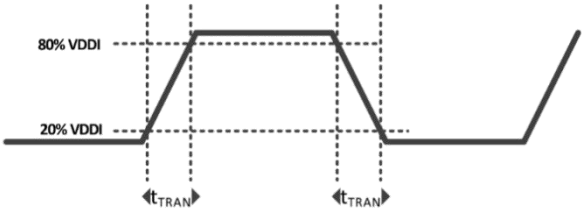
Symbol	Parameter	Min	Typ.	Max	Unit
t_{pclk}	Pclk Period	10	T	-	ns
t_{clk}	Pclk input low time	0.4T	0.5T	0.6T	ns
t_{ckh}	Pclk input high time	0.4T	0.5T	0.6T	ns
t_{hv}	Phase difference of Sync Signal Falling Edge	0	-	W	t_{pclk}



Symbol	Parameter	Min	Typ.	Max	Unit
t_{SET}	Data Setup Time	2	-	-	ns
t_{HOLD}	Data hold Time	2	-	-	ns



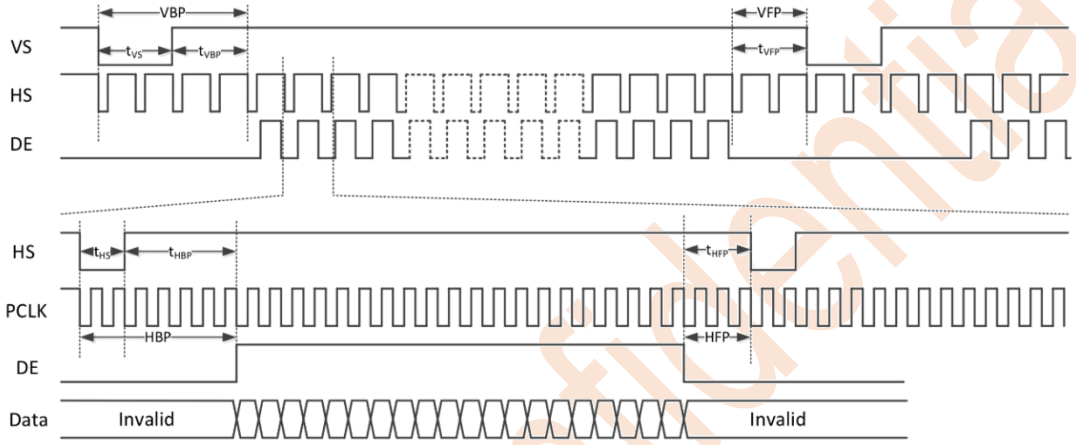
Symbol	Parameter	Min	Typ.	Max	Unit
t_{TRANS}	Transition time	-	-	2	ns



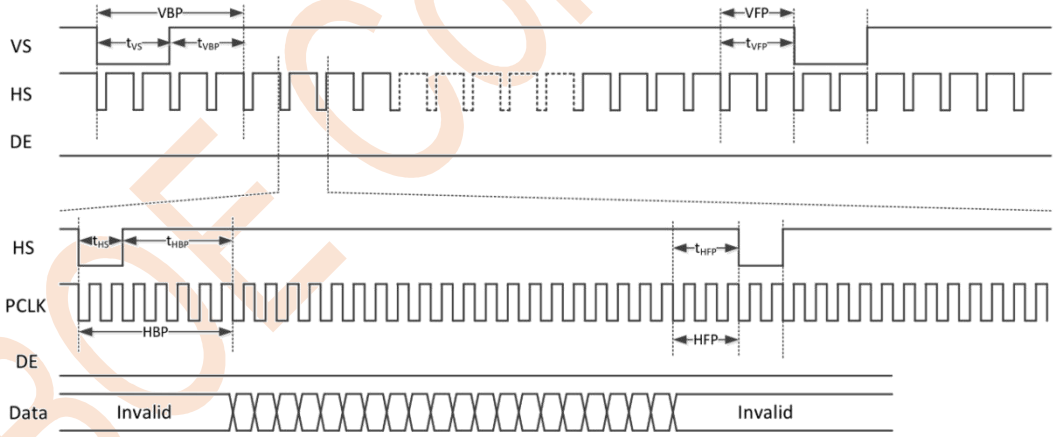
6.2 Video Operation Timing Characteristics

Symbol	Parameter	Min	Typ.	Max	Unit
t_{VS}	Vertical Sync input pulse width	1	-	-	H
t_{VBP}	Vertical back porch	1	-	-	H
t_{VFP}	Vertical front porch	1	-	-	H
$t_{VS} + t_{VBP} + t_{VFP}$	Vertical porch total line	8	-	-	H
t_{HS}	Horizontal Sync input pulse width	2	-	-	pclk
$t_{HS} + t_{HBP}$	Horizontal Sync + Horizontal back porch	4	-	-	pclk
t_{HFP}	Horizontal front porch	1	-	-	pclk

RGB Video Mode 1: with DE Signal



RGB Video Mode 2: without DE Signal



Note: HBP shall be precisely set for RGB Video Mode 2. See 11.1.5 RGB Interface Mode.

7. I2C Interface

The I2C-bus is for bi-directional, two-line communication between different ICs or modules. The two lines are the Serial Data Line (I2C_SDA) and Serial Clock Line (I2C_SCL). Both lines must be connected to a positive power supply via pull-up resistors. Data transfer can be initiated only when the bus is not busy. The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. The master generates all clock pulses, including the acknowledge ninth clock pulse.

7.1 I2C-Bus Protocol

Before any data is transmitted on the I2C-bus, the device which should response is addressed first. There are several slave addresses can be selected by MCU. The slave addressing is always carried out with the first byte transmitted after the START procedure.

Definition:

-Transmitter: The device which sends the data to the bus.

-Receiver: The device which receives the data from the bus.

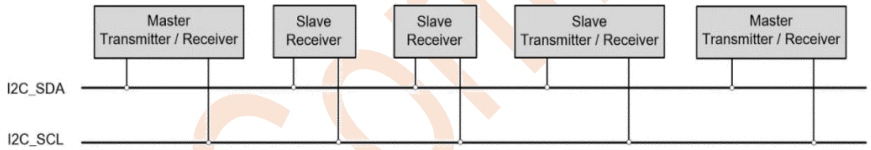
-Master: The device which initiates a transfer, generates clock signals and terminates a transfer.

-Slave: The device addressed by a master.

-Multi-master: More than one master can attempt to control the bus at the same time without corrupting the message.

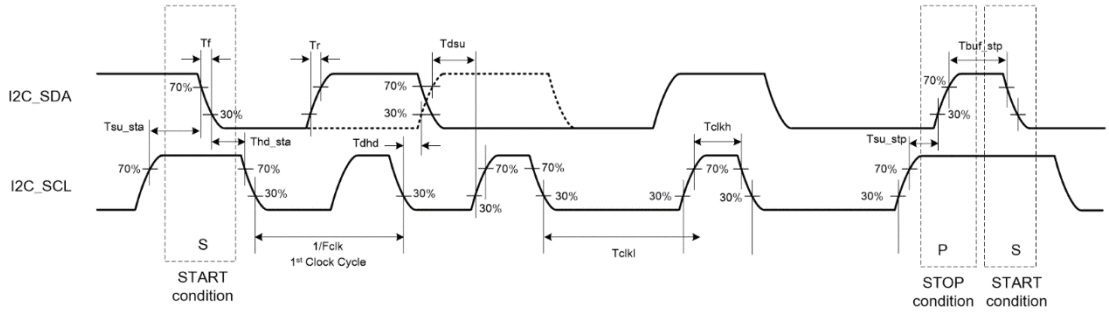
-Arbitration: Procedure to ensure that. If more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted.

-Synchronization: Procedure to synchronize the clock signals of two or more devices.



7.2 I2C Interface Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
I2C Clock Frequency	Fclk	-	-	400	kHz
I2C Clock Low	Tclkl	1300	-	-	ns
I2C Clock High	Tclkh	600	-	-	ns
I2C Data Rising Time	Tdr	-	-	300	ns
I2C Data Falling Time	Tdf	-	-	300	ns
I2C Data Setup Time	Tdsu	100	-	-	ns
I2C Data Hold Time	Tdhd	-	-	TBD	ns
I2C Setup Time (Start Condition)	Tsu_sta	600	-	-	ns
I2C Hold Time (Start Condition)	Thd_sta	600	-	-	ns
I2C Setup Time (Stop Condition)	Tsu_stp	600	-	-	ns
I2C Bus Free Time (Stop Condition)	Tbuf_stp	1300	-	-	ns



No.	ITEM	Description	Note
1	Slave address	0x4C	
2	Pull-up resistor	4.7KΩ@100Kbps	
3	Read bit	Setting “1” for write	
4	Write bit	Setting “0” for write	
5	Start condition	SDA is setting from “1” to “0” when SCL is “1”	
6	Stop condition	SDA is setting from “0” to “1” when SCL is “1”	

7.3 I2C Interface Waveform

7.3.1 Write Sequence

0.39" Micro OLED supports register write sequence via I2C-bus transfer. The register writing supports single register write mode. The detailed transfer sequences are illustrated and described as below.

(1) Data transfer for register writing should follow the format shown as below:

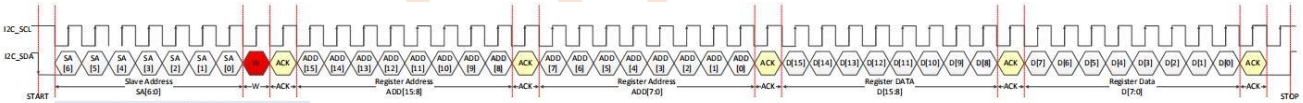
(2)After the START condition, a slave address is sent. R/W̄ bit is setting to “0” for Write.

(3)The slave issues an ACK to the master.

(4)8-bits register address transfer first then transfer the register data parameter.

(5)A data transfer is always terminated by a STOP condition.

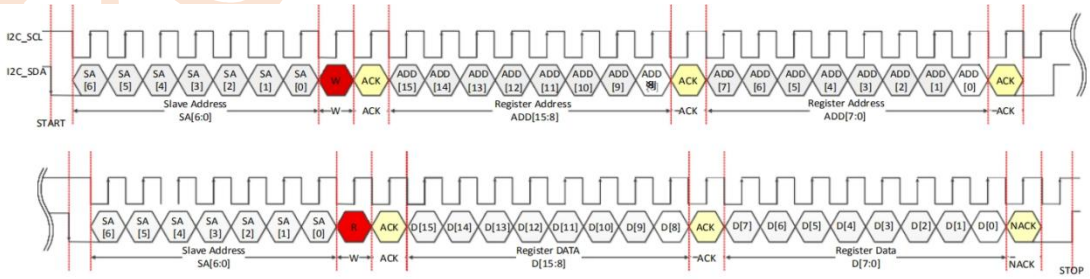
(6) The chip SA[6:0]=100_1100



W : Write Bit, W=” 0 ” here.
ACK : Acknowledge Bit, ACK=” 0 ” here
SA[6:0] : Slave Address.
ADD[15:0] : Register Address.
D[15:0] : : Register Data.

7.3.2 Read Sequence

0.39" Micro OLED supports register read sequence via I2C-bus transfer. The register reading supports single register read mode. The register data reading transfer are shown as below.



W : Write Bit, W=” 0 ” here.
R : Read Bit, R=” 1 ” here.
ACK : Acknowledge Bit, ACK=” 0 ” here
SA[6:0] : Slave Address.
ADD[15:0] : Read Register Address.
D[15:0] : : Read Register Return Data.
NACK: Non-ACK Bit, NACK=” 1 ” here

8. Absolute Maximum Ratings

The absolute maximum rating is listed on the below table. When the Driver IC of 0.39” is used beyond the absolute maximum ratings, it may be permanently damaged. It is strongly recommended use the driver IC within the following specified limits for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the driver IC will malfunction and cause poor reliability.

Item	Symbol	Typ. Value	Max Value	Unit
Power Supply Voltage	VDDI	1.8	5.5	V
	VIN	5	5.5	V
$V_{I/O}$	Digital Signal Voltage	1.8	5.5	V
Operating temperature	Topr	-20 ~ 60		°C
Storage temperature	Tstg	-30 ~ 70		°C

Note: The environment temperature is not a reliable test temperature.

9. Electrical Characteristics

9.1 DC Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Power & Operation Voltage						
VIN Input Level	VIN	--	3.3	5	5.5	V
Digital I/O Power Supply	VDDI	--	--	1.8	--	V
Digital I/O Input Level@Logic High	VIH	VDDI=1.65V ~ 1.95V	0.7*VDDI	--	VDDI	V
Digital I/O Input Level@Logic Low	VIL	VDDI=1.65V ~ 1.95V	0	--	0.3*VDDI	V
Digital I/O Output Level @Logic High	VOH	Iout = -1mA	0.8*VDDI	--	VDDI	V
Digital I/O Output Level @Logic Low	VOL	Iout = +1mA	0	--	0.2*VDDI	V
Digital I/O Input leakage @Logic High	IIHD	Vin = VDDI			1	uA
Digital I/O Input leakage @Logic Low	IILD	Vin = 0	-1			uA

9.2 AC Characteristics

9.2.1 Video Timing Specification.

1024*768@60Hz					
H	Hsync	2	V	Vsync	6
	HBP	8		VBP	29
	Hactive	1024		Vactive	768
	HFP	4		VFP	3
1024*768@25Hz					
H	Hsync	4	V	Vsync	6
	HBP	16		VBP	29
	Hactive	1024		Vactive	768
	HFP	10		VFP	3

Note: This parameter is a typical example illustrating the display timing. BOE cannot assume responsibility for any problems arising out of the use of the circuit.

9.3 Power Consumption

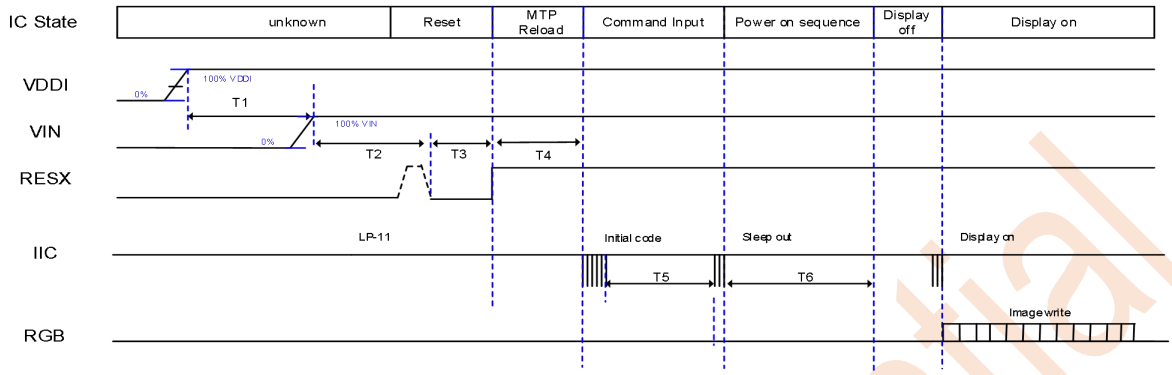
Item	Condition	Typ.	Unit
Power consumption	200cd/m2，Tpnl = 40°C	100	mW

Note: All white raster display, 1024 * 768, frame rate = 60Hz. White.

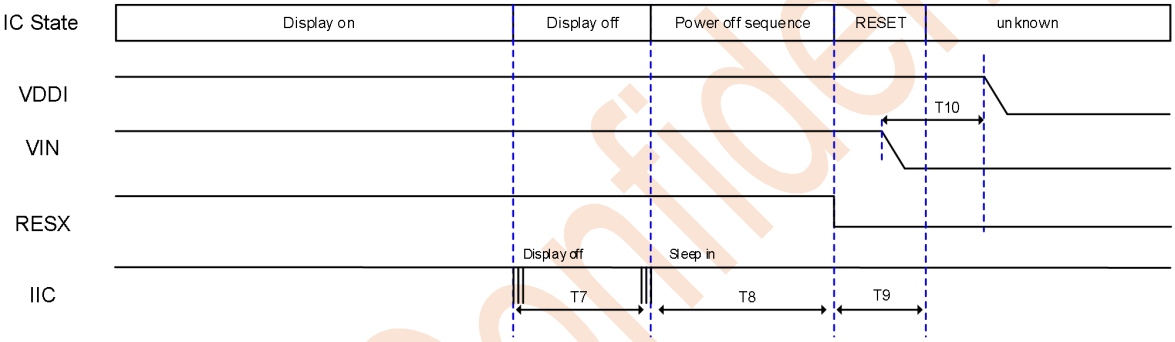
10. Power Supply Sequence

10.1 Power On/Off Sequence

◆ Power On sequence



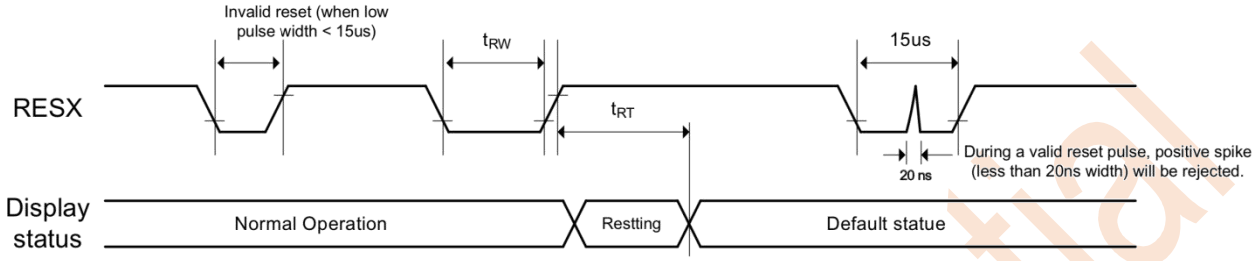
◆ Power Off sequence



Symbol	Min.	Typ.	Max.	Unit	Description
T1	1	-	-	ms	Power on time between VIN and VDDI
T2	20	-	-	Ms	Power on time between VIN and RESX
T3	1	-	-	ms	Effective hardware reset period
T4	20	-	-	ms	MTP reload time
T5	0	-	-	ms	The time is between initial code finished and sleep-out command
T6	2	-	8	VS	Power on sequence, the period can be modified
T7	1	-	-	VS	Blanking region
T8	-	1	-	VS	Power off sequence, the period can be modified
T9	1	-	-	ms	Effective hardware reset period
T10	1	-	-	ms	Power off time between VIN and VDDI

10.2 Rest Timing Characteristics

When Reset happens in Sleep-out mode, the driver IC will enter blanking sequence with the maximum time 120 msec. Then driver IC will remain in blanking state and return IC's default state. During reset complete time (tRT), data in OTP will be re-loaded and latched to internal registers. This data re-load is done every time when there is an H/W reset and completes within 20 msec after the rising edge of RESX. Therefore, it is necessary to wait at least 20 msec after releasing the RESX before sending commands. Moreover, the Sleep-out command cannot be sent in 120 msec. Spike (less than 20ns width) Rejection can also be applied during a valid reset pulse.



Reset time @ VDDI=1.65V to 1.95V, AVSS=VSS=MVSS=0V, Ta=-40°C to 85°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Description
t_{RW}	Reset low pulse width	15	-	-	us	Power on time between VIN and VDDI
t_{RT}	Reset Complete time	-	-	20	ms	When reset applied at sleep-in mode
		-	-	120	ms	When reset applied at sleep-out mode

11. Description of Function

11.1 Display Mode

11.1.1 Power Mode

ITEM	Code value
Sleep In	1000h
Sleep Out	1100h
Display On	2900h
Display Off	2800h

11.1.2 Idle Mode

ITEM	Code value
Idle On	3900h
Idle Off	3800h

11.1.3 Command Enable Mode

◆ **MAUCCTR (F0h): Manufacture Command Enable**

<table>
<tr><td>F000H</td><td colspan="11">MAUCCTR</td></tr>
<tr><td rowspan="2">Instruction</td><td rowspan="2">R/W</td><td>Address</td><td colspan="10">Parameter</td></tr>
<tr><td>IIC</td><td>D15-D8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td rowspan="2">MAUCCTR</td><td rowspan="2">W</td><td>F000h</td><td>--</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>F001h</td><td>--</td><td>-</td><td>-</td><td>-</td><td>EN_CMD2</td><td colspan="4">PAGE[3:0]</td></tr>
<tr><td>Description</td><td colspan="11">This command is used to enable the access of CMD2 page.
<table>
<tr><th>Bit</th><th>Symbol</th><th>Description</th><th>Comment</th></tr>
<tr><td>D4</td><td>EN_CMD2</td><td>Enable access of CMD2 page</td><td>1= enable
0= disable</td></tr>
<tr><td>D[3:0]</td><td>PAGE[3:0]</td><td>CMD2 Page selection</td><td>0=CMD2 Page0
1=CMD2 Page1
2=CMD2 Page2
3=CMD2 Page3
4=CMD2 Page4
5=CMD2 Page5
6=CMD2 Page6
Others=Reserved</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="11">-</td></tr>
<tr><td>Default</td><td colspan="11">
<table>
<tr><th>Status</th><th>Default Value</th><th></th></tr>
<tr><td rowspan="2">Power On Sequence</td><td>F000h</td><td>0xAA</td></tr>
<tr><td>F001h</td><td>0x00</td></tr>
</table></td></tr>
</table>

11.1.4 BIST Mode

◆ **BISTONOFF(C4h, CMD2-P1): BIST On/Off Control**

<table>
<tr><td rowspan="2">Instruction</td><td rowspan="2">R/W</td><td>Address name</td><td colspan="9">Parameter</td></tr>
<tr><td>IIC</td><td>D15-D8</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr>
<tr><td rowspan="4">BISTONOFF</td><td rowspan="4">R/W</td><td>C400h</td><td>--</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>C401h</td><td>--</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>C402h</td><td>--</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>BION1</td></tr>
<tr><td>C403h</td><td>--</td><td>BION2</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td><td>-</td></tr>
<tr><td>Description</td><td colspan="11">This command is used to control BIST function (Free Run mode).
BIST function enable step:
1. Enter Sleep-In (10h) mode.
2. Setting PATENICYC[1:0] and BISTPATEN[11:0] to control the display cycle time and pattern.
3. Setting BION1=”1” and BION2=”1”, the driver IC will start to run the BIST function.
BIST function disable step:
1. Setting BION1=”0” and BION2=”0”, the driver IC will return to normal function.
2. Sending MIPI video data and enter Sleep-Out (11h) mode for normal display.</td></tr>
<tr><td>Restriction</td><td colspan="11">-</td></tr>
<tr><td>Default</td><td colspan="11"><table><tr><td>Status</td><td colspan="2">Default Value</td></tr><tr><td rowspan="4">Power On Sequence</td><td>C400h</td><td>AAh</td></tr><tr><td>C401h</td><td>55h</td></tr><tr><td>C402h</td><td>00h</td></tr><tr><td>C403h</td><td>00h</td></tr></table></td></tr>
</table>

◆ BISTSET (C5h, CMD2-P1): BIST CTR

Instruction	R/W	Address name	Parameter								
		I2C	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
BISTSET	R/W	C500h	--	-	PATENICYC[2:0]			BISTPATEN[11:8]			
		C501h	--	BISTPATEN[7:0]							
		C502h	--	GRAY_LEVEL[7:0]							

escription

This command is used to set the display pattern in BIST function.

PATENICYC[2:0] : Cycle time between each display pattern.

PATENICYC[2:0]	Pattern cycle time
0h	256 Frame
1h	512 Frame
2h	1024 Frame
3h	2048 Frame

BISTPATEN[11:0] : Select the display pattern in BIST function.

BISTPATEN[9:0]	Description
BISTPATEN[0]	Red pattern.
BISTPATEN[1]	Green pattern.
BISTPATEN[2]	Blue pattern.
BISTPATEN[3]	Black pattern.
BISTPATEN[4]	Gray Level pattern. (Set by BIST_GRAY_LEVEL[7:0])
BISTPATEN[5]	Vertical Gradation pattern.
BISTPATEN[6]	Horizontal Gradation pattern.
BISTPATEN[7]	Color Bar pattern.
BISTPATEN[8]	Crosstalk with boundary pattern.
BISTPATEN[9]	Source CP Pattern
BISTPATEN[10]	Gamma CP Pattern
BISTPATEN[11]	Checker 4*4

Note1: the patterns which the bit number of BISTPATEN[9:0] is set to "1" will display and change automatically.

Note2: When BISTPATEN[11:0]=12'h000, display pattern will be black pattern.

GRAY_LEVEL[7:0] : Set the gray level when BISTPATEN[4]="1" in BIST function.

GRAY_LEVEL[7:0]	Description
0h	Gray Level : 00h
1h	Gray Level : 01h
2h	Gray Level : 02h
:	:
FDh	Gray Level : FDh
FEh	Gray Level : FEh
FFh	Gray Level : FFh

Restriction: -

Default

Status	Default Value	
Power On Sequence	C500h	00h
	C501h	08h
	C502h	FFh

11.1.5 RGB Interface Mode:

◆ **RGBMOD (83h, CMD1): RGB Interface Mode Control**

Instruction	R/W	Address name	Parameter								
		IIC	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
BISTONOFF	R/W	8300h	--	RGB_DE_OPT	--	--	--	--	--	--	RGB_HBP[8]
		8301h	--	RGB_HBP[7:0]							

Description

This command is used to set panel type and display resolution.

Bit	Symbol	Description	Comment
D7	RGB_DE_OPT	RGB video mode select	RGB_DE_OPT = 0: RGB video mode 1 RGB_DE_OPT = 1: RGB video mode 2
D[8:0]	RGB_HBP[8:0]	Horizontal back porch pixel number for RGB video mode 2	

RGB_HBP[8:0]	HBP number
0h	1 pixel
1h	2 pixel
2h	3 pixel
…	…
1FDh	510 pixel
1FEh	511 pixel
1FFh	512 pixel

Restriction: -

Default

Status	Default Value	
Power On Sequence	8300h	00h
	8301h	20h

◆ **DISPCTL (B8h, CMD2-P0): Display CTR**

Instruction	R/W	Address	Parameter								
		IIC	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
DISPCTL	R/W	B800h	--	-	-	-	-	CRGB	CTB	CRL	1

Description

CRGB: Select color order of sub-pixel of true RGB type.

CTB	Scan Direction
0h	R-G-B
1h	B-G-R

Note: The display corresponds to the result of CTB^ RSMY (CMD1, 36h)

CRL: Vertical Flip.

CTB	Scan Direction
0h	Normal Display
1h	Vertical Flip

Note: The display corresponds to the result of CTB^ RSMY (CMD1, 36h)

CTB: Horizontal Flip.

CRL	Scan Direction
0h	Normal Display
1h	Horizontal Flip

Note: The display corresponds to the result of CRL ^ *RSMX (CMD1, 36h).*

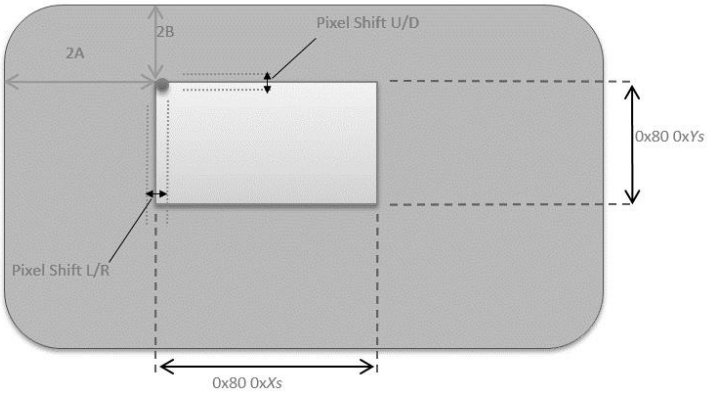
Restriction: -

Default

Status	Default Value	
Power On Sequence	B800h	01h

11.2 Display Active-Area (AA) Control

ITEM	Description	Code Value
Resolution	X-direction: Support 4N, N=120~192 Y-direction: support 4M, M=160~256	CMD1 ： 0x80(NC[7:0] NL[7:0])
Active-Area(AA) control	Display start pointer	Xs: CMD1: 0x2A ; Ys: CMD1: 0x2B
	Pixel shift ：±12pixel ； step=1pixel	CMD2 Page0: 0xB4



◆ **RESCTRL1(80h, CMD1)：Resolution CTRL1**

8000H	RESCTRL1									
Instruction	R/W	Address	Parameter							
		IIC	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
RESCTRL1	R/W	8000h	--	-	-	-	-	-	-	-	D0
		8001h	--	NC[7:0]							
		8002h	--	NL[7:0]							
		8003h	--	-	-	-	NC[8]	-	-	-	NL[8]
		8004h	--	NC_DEC[7:0]							
		8005h	--	-	-	-	-	-	NC_DEC[10:8]		

Description

This command is used to set panel type and display resolution.

Bit	Symbol	Description	Comment
D0	OSC_FREQ_SEL	OSC frequency selection	1= 60MHz 0= 45MHz
D[8:0]	NC[8:0]	X-axis resolution	X-axis resolution= NC[8:0]*4
D[8:0]	NL[8:0]	Y-axis resolution	Y-axis resolution= NL[8:0]*4
D[8:0]	NC_DEC[8:0]	X-axis resolution for input image size	X-axis resolution for input size = NC_DEC[8:0]*1

Restriction: Resolution switch is only valid in *SLPIN* mode.

Status	Default Value	
Power On Sequence	8000h	01h
	8001h	00h
	8002h	C0h
	8003h	10h
	8004h	00h
	8005h	40h

◆ RESCTRL2(81h, CMD1)：Resolution CTRL2

8100H	RESCTRL2										
Instruction	R/W	Address IIC	Parameter D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
RESCTRL2	R/W	8100h	--	-	-	-	-	-	-	T1A[9:8]	
		8101h	--	T1A[7:0]							
		8102h	--							VBPDA[9:8]	
		8103h	--	VBPDA[7:0]							
		8104h	--							VFPDA[9:8]	
		8105h	--	VFPDA[7:0]							
		8106h	--	-	-	-	-	-	PSELA[2:0]		

Description

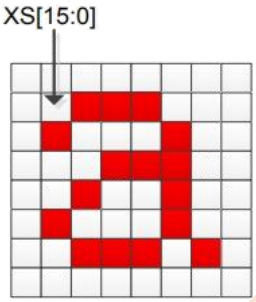
This command is used to set panel type and display resolution.

Bit	Symbol	Description	Comment
D[7:0]	T1A[9:0]	Clock number of 1-Hsync for data path in normal mode	T1A[9:0] = Number of clock; 0h = 1-dpclk; 1h = 2-dpclk; …… = ……; 3FFh = 1024-dpclk
D[7:0]	VBPDA[9:0]	VBP line number in nor云南省曲靖市mal mode	VBPDA[9:0] = Line Number of VBP; 0~1h = Reserved; 2h = 2-line; …… = ……; 3FBh = 1019-line; 3FC~3FFh = Reserved
D[7:0]	VFPDA[9:0]	VFP line number in normal mode	VBFPDA[9:0] = Line Number of VFP; 0~1h = Reserved; 2h = 2-line; …… = ……; 3FEh = 1022-line; 3FFh = 1023-line
D[2:0]	PSELA[2:0]	OSC divisor for data path in normal mode	PSELA[2:0] = Line Number of VBP; 0h = 1; …… = ……; 7h = 10

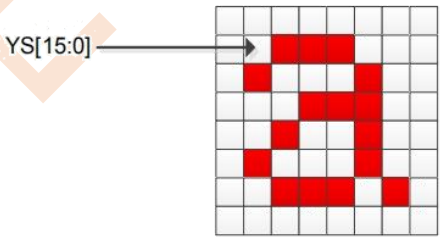
Default

Status	Default Value	
	8000h	02h
	8001h	23h
	8002h	00h
	8003h	08h
	8004h	00h
	8005h	08
	8006h	01hh

◆ CASET(2Ah, CMD1): Column Address Set

2A00H	WRCTRLD									
Instruction	R/W	Address	Parameter							
		IIC	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
CASET	W	2A00h	--	XS[15:8]							
		2A01h	--	XS[7:0]							
Description	This command indicates display start position of display module in columns. XS[15:0]: Display line start position 									
Restriction	1. When display module is on distribute driving mode, XS and XE should follow the rule as below: XS= 0 + 4N, N=integer									
Default	Status	Default Value								
	Power On Sequence	2A00h	00							
		2A01h	00							

◆ RASET(2Bh, CMD1): Row Address Set

2B00H	WRCTRLD									
Instruction	R/W	Address	Parameter							
		I2C	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
RASET	W	2B00h	--	YS[15:8]							
		2B01h	--	YS[7:0]							
Description	This command indicates display start position of display module in rows. YS[15:0]: Display line start position 									
Restriction	1. When display module is on distribute driving mode, YS and YE should follow the rule as below: YS= 0 + 4N, N=integer									
Default	Status	Default Value								
	Power On Sequence	2B00h	00h							
		2B01h	00h							

◆ PXLSHIFT CTR (B4h, CMD2-P0): Pixel Shift Control

Instruction	R/W	Address	Parameter								
		IIC	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
PXLSHIFT CTR	R/W	B400h	--	PIXEL_SHIFT_X_DIR	-		-	PIXEL_SHIFT_X_COUNT[3:0]			
		B401h	--	PIXEL_SHIFT_Y_DIR	-	-	-	PIXEL_SHIFT_Y_COUNT[3:0]			
		B402h	00	PIXEL_SHIFT_X_TOTAL[7:0]							
		B403h	00	PIXEL_SHIFT_Y_TOTAL[7:0]							

Description

PIXEL_SHIFT_X_DIR: Pixel shift direction of X-axis

PIXEL_SHIFT_X_DIR	The percentage of EM_STV01 for DBV
0h	Left
1h	Right

PIXEL_SHIFT_X_COUNT[3:0]: Pixel shift of X-axis

PIXEL_SHIFT_X_COUNT[3:0]	Pixel Shift of X-axis
0h	1pixels
1h	2-pixels
2h	3-pixels
Ah	10-pixels
Bh	11-pixels
Ch	12-pixels
Others	Reserved

PIXEL_SHIFT_Y_DIR: Pixel shift direction of Y-axis

PIXEL_SHIFT_Y_DIR	Pixel Shift Direction of Y-axis
0h	Up
1h	Down

PIXEL_SHIFT_Y_COUNT[3:0]: Pixel shift of Y-axis

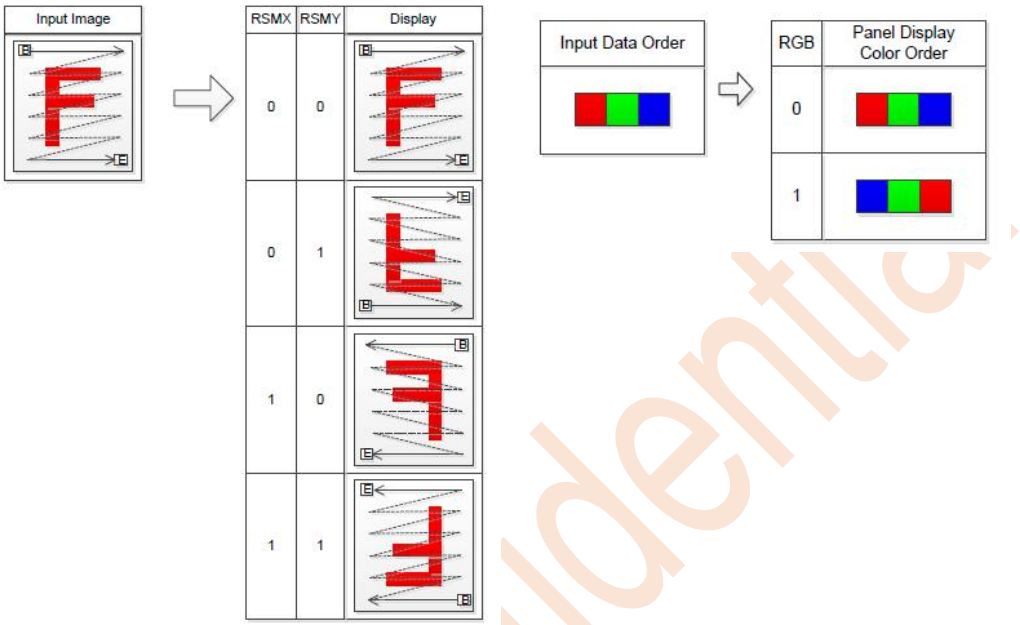
PIXEL_SHIFT_Y_COUNT[3:0]	Pixel Shift of Y-axis
0h	1pixels
1h	2-pixels
2h	3-pixels
Ah	10-pixels
Bh	11-pixels
Ch	12-pixels
Others	Reserved

◆ MADCTL(36h CMD1): Scan direction selection

3600H	WRCTRLD									
Instruction	R/W	Address	Parameter								
		IIC	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
WRCTRLD	W	3600h	--	-	-	-	-	RGB	-	RSMX	RSMY

Description

This command set scan direction of source and gate and data order.



Bit	Symbol	Description	Comment
D3	RGB	Color Order of sub-pixel of true RGB type	1=BGR 0=RGB
D1	RSMX	Horizontal Flip	1=Normal Display 0=Horizontal Flip
D0	RSMY	Vertical Flip	1= Normal Display 0= Vertical Flip

Restriction

Default

Status	Default Value	
Power On Sequence	3600h	00h

11.3 Scaling up

◆ SCACTRL (69h, CMD1): Scaling up control

Instruction	R/W	Address	Parameter								
		IIC	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
DISPCTL	R/W	B800h	--	-	-	-	-	-	-	D[1:0]	

Description

This command sets operation mode of MIPI clock lane during porch time.

Bit	Symbol	Description	Comment
D[1:0]	SC_MOD_SEL	Scaling up ratio selection	0 = off 1 = 1.5x scaling up other = 1.33x scaling up

Default

Status	Default Value	
Power On Sequence	6900h	00h

11.4 Brightness Control (BC) Functions

This function adjusts the gamma parameter according to the register 51h and 53h setting to adjust the luminance.

◆ **BCCTL3 (C2h, CMD2-P1): Brightness CTR_3**

C2H	WRCTRLD									
Instruction	R/W	Address	Parameter							
		I2C	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
BCCTR3	R/W	C200h	--	-	-	-	-	-	-	EM_WD[9:8]	
		C201h	EM_WD[7:0]								
		C202h	--	--	--	--	--	--	--	--	--
		C203h	--	--	--	--	--	--	--	--	--
		C204h	--	EM_CYCLE_NUM[1:0]		--	--	--	--	EM_CYCLE_NUM_IDLE[1:0]	
		C205h	--							EM_WD_TH[9:8]	
		C206h	--	EM_WD_TH[7:0]							

Description

EM_WD[9:0]: The percentage of EM_STV01 for DBV.

EM_WD[9:0]	The percentage of EM_STV01 for DBV
0h	1/1024
1h	2/1024
……	……
3FEh	1023/1024
3FFh	1024/1024

EM_CYCLE_NUM[1:0]: Cycle number of EM_STV01 when emission pulse width more or less than EM_WD_TH[9:0].

EM_CYCLE_NUM[1:0]	Cycle number of EM_STV01
0h	1
1h	2
2h	4
3h	8

EM_CYCLE_NUM_IDLE[1:0]: Cycle number of EM_STV01 when process in idle mode.

EM_CYCLE_NUM_IDLE[1:0]	Cycle number of EM_STV01
0h	1
1h	2
2h	4
3h	8

EM_WD_TH[9:0]: Threshold of percentage of EM_STV01.

CRL	Scan Direction
0h	1/1024
1h	2/1024
.....	.....
3FEh	1023/1024
3FFh	1024/1024

Restriction

Default

Status	Default Value	
Power On Sequence	C200h	03h
	C201h	FFh
	C202h	00h
	C203h	00h
	C204h	00h
	C205h	00h
	C206h	00h

◆ **WRDISBV (51h, CMD1): Write Display Brightness**

C2H	WRCTRLD									
Instruction	R/W	Address	Parameter							
		I2C	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
WRDISBV	W	5100h	--	DBV[7:0]							
		5101h	--							DBV[9:8]	
Description	This command is used to adjust brightness..										
Restriction											
Default	Status	Default Value									
	Power On Sequence	5100h	00								
		5101h	00								

11.5 Read module display status

◆ **RDDPM (0Ah, CMD1): Read Display Power Mode**

0A00H	WRCTRLD									
Instruction	R/W	Address	Parameter							
		I2C	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
RDDPM	R	0A00h	00	D7	D6	-	D4	D3	D2	-	-

Description

This command indicates the status of display driver's power and operation mode:

Bit	Symbol	Description	Comment
D7	BSTON	Boost Status	1=Boost On; 0=Boost Off
D6	IDMON	Idle Mode On/Off	1=Idle Mode On; 0=Idle mode Off
D4	SLPON	Sleep In/Out	1=Sleep Out; 0=Sleep In
D3	NOR	Display Normal Mode On/Off	1= Display Normal On; 0= Display Normal Off
D2	DISPON	Display On/Off	1=Display On; 0=Display Off

Default

Status	Default Value	
Power On Sequence	0A00h	08h

12. Optical Characteristics

12.1 Optical Characteristics

Item			Specification..
White Brightness(255 Level)	LH		200±20% cd/m2
White Uniformity 9 Point	White (255 Level)		>85%
View Angle (White)	Lum. Decay (50%)		±20°
	Color Shift (Δu'v'<0.025)		±20°
Contrast	CR		>50000:1
Color Coordinate	Red	CIE-x	0.63±0.03
		CIE-y	0.36±0.03
	Green	CIE-x	0.24±0.03
		CIE-y	0.69±0.03
	Blue	CIE-x	0.15±0.03
		CIE-y	0.08±0.03
	White	CIE-x	0.29±0.03
		CIE-y	0.31±0.03
Color Gamut(NTSC)			>80%
Color Temperature			>5,000K

Notes: The brightness of the product will be measured after 5 minutes of stabilization for the white screen at room temperature. The formula of the brightness uniformity at 9 points of the white screen is Uniformity=1-(Max. -Min.)/(Ave.), and the Max., Min. and Ave. represent the maximum, minimum and average of the brightness of 9 points,

respectively.

12.2 Measurement System · Measurement Method

The luminance and chromaticity are measured in Measurement System shown below.

Measurement temperature: Tpnl = 30°C

Measurement point: One point on the screen center

All white display: All RGB signal data is set to High.

All black display: All RGB signal data is set to Low.

Luminance and chromaticity: Measure the luminance and chromaticity in all white display in Measurement System.

Contrast: Measure the luminance in all white display (@: 200cd/m^2) and all black display in Measurement System, and substitute them into the formula below.

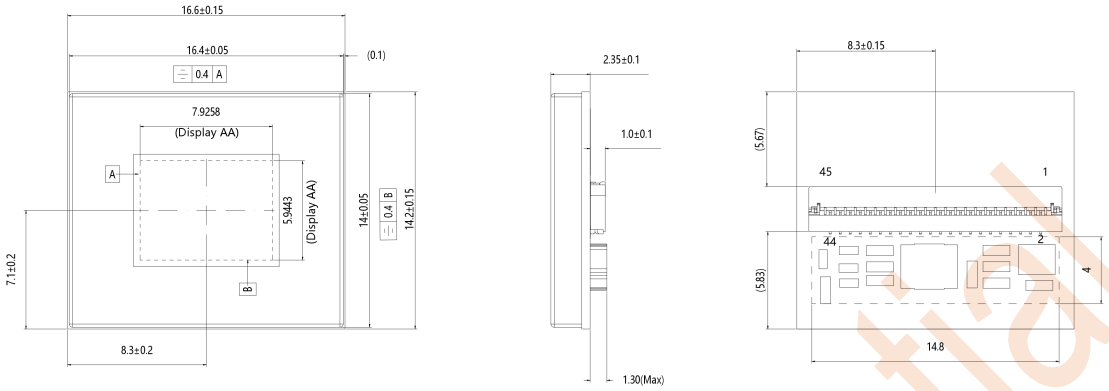
Contrast = Luminance in all white display/Luminance in all black display

13. Reliability test

Item	Test conditions	Specification	Test
High Temperature Storage	Keep 70℃ for 48hrs	The module can be lit up normally after reaching 20℃.	5pcs/lot
Low Temperature Storage	Keep -30℃ for 48hrs	The module can be lit up normally after reaching 20℃.	5pcs/lot
High Temperature Operation	Keep 60℃ for 48hrs Rate of temperature change: 3℃/min;	The module can be lit up normally at 60℃.	5pcs/lot
Low Temperature Operation	Keep -20℃ for 48hrs; Rate of temperature change: 3℃/min	The module can be lit up normally at-20℃.	5pcs/lot
VIB (Vibration)	Vibration frequency: 5HZ~200HZ~5HZ Vibration direction : X/Y/Z Peak acceleration : 3.78Grms Vibration time: 6min/axis	The module can be lit up normally after experiment.	5pcs/lot
Shock	Peak acceleration: 50g Pulse time : 11ms Shock direction : X/Y/Z Shock time: Twice/axis	The module can be lit up normally after experiment.	5pcs/lot
Temperature Shock Test	Temperature cycle interval: -30℃~70℃ Soaking time : 0.5hr Temperature conversion: ≤5℃/min Shock times: 10 Cycles	The module can be lit up normally after reaching 20℃.	5pcs/lot
8585	Keep 85℃ and humidity of 85% for 48hrs, Storage.	The module can be lit up normally after reaching 20℃.	5pcs/lot

14. Package Outline

14.1 PCB Module (Unit： mm)



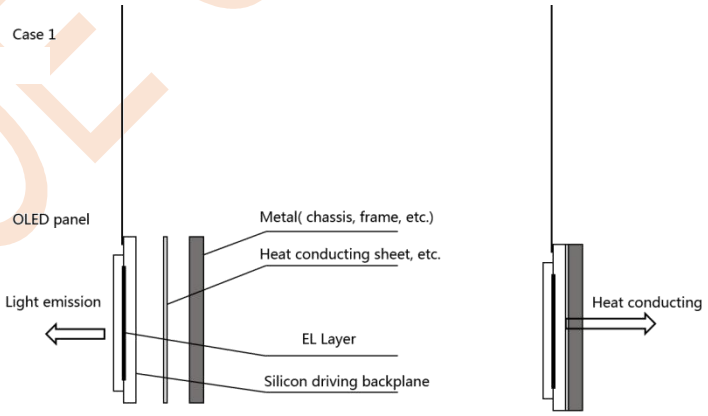
Note: The connector is W03007FA045DAWL, 0.3Pitch 0.9H ZIF connector.

15. Recommended Items

15.1 Suppression of the Panel Temperature

Temperature of organic EL panel tends to rise due to power consumption (heat generation) by the EL emission layer and the integrated silicon drive circuit. The temperature rise may cause luminance rise at initial state, or luminance drop by over time.

The temperature change in panel can be suppressed by establishing a thermal connection between panel rear surface (silicon substrate surface) and metal (chassis, frame, metal structure, etc.) at panel mount area, and the heat conducting sheet size can be changed, So highly recommend the heat conductive sheet between them as show in below.



16. Notes on Handling

16.1 Static charge prevention

Be sure to take the following protective measures. Organic EL panels are easily damaged by static charges.

(1) Use non-chargeable gloves or handle with bare hands.

(2) Use a wrist strap connecting ground when handling.

(3) Do not touch any electrodes on the panel.

(4) Wear non-chargeable clothes and conductive shoes.

(5) Install grounded conductive mats on the working floor and working table.

(6) Keep the panel away from any charged materials.

16.2 Protection from dust and dirt

(7) Operate in a clean environment.

(8) Do not touch the panel surface. The surface is easily scratched.
When cleaning on panel surface, use a clean-room wiper with isopropyl alcohol. Be careful not to leave stains on the surface.

(9) Use ionized air to blow dust off the panel surface.

16.3 Other

(10) Not hold FPC (Flexible Printed Circuit) , not twist the FPC, not bend FPC because connection area between the FPC and panel is easily broken by mechanical stress.

(11) The minimum fold radius of the FPC is 1.0 mm, So, do not fold the FPC less than 1.0mm radius.

(12) Do not drop the module.

(13) Do not twist or bend the module.

(14) Keep the module away from heat sources.

(15) Not be close the module to water or other solvents.

(16) Do not store or use the module at high temperatures or high humidity circumstance, as the circumstance may affect module specifications.

(17) When disposing of this, regard it as industrial waste and please comply with related regulations.

(18) Do not store or use the panel in reactive chemical substance (including alcohol) environments, as these may affect the specifications.