YM2201

IEEE 802.11ax/ac/a/b/g/n Compatible 2T2R WLAN AND INTEGRATED BLUETOOTH 5.2 CONTROLLER WITH PCI EXPRESS /USB MIXED INTERFACE

DATASHEET

(CONFIDENTIAL: Development Partner Only)

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

ELECTROSTATIC DISCHARGE (ESD) WARNING

This product can be damaged by Electrostatic Discharge (ESD). When handling, care must be taken. Damage due to inappropriate handling is not covered by warranty.

Do not open the protective conductive packaging until you have read the following, and are at an approved anti-static workstation.

- Use an approved anti-static mat to cover your work surface.
- Use a conductive wrist strap attached to a good earth ground
- Always discharge yourself by touching a grounded bare metal surface or approved anti-static mat before picking up an ESD-sensitive electronic component
- If working on a prototyping board, use a soldering iron or station that is marked as ESD-safe
- Always disconnect the microcontroller from the prototyping board when it is being worked on

REVISION HISTORY

Revision	Release Date	Summary	Revised by
0.1	2022/03/1	Preliminary release.	Zoro

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1. General Description

The YJT YM2201 is a highly integrated M.2 module that support 2-stream 802.11ax solutions with Multi-user MIMO (Multiple-Input, Multiple-Output) with Wireless LAN (WLAN) PCI Express network interface controller with integrated Bluetooth 5 USB interface controller. It combines a WLAN MAC, a 2T2R capable WLAN baseband, and RF in a single chip. The YM2201 provides a complete solution for a high-performance integrated wireless and Bluetooth device.

2. Features

General

- PCIe interface
- CMOS MAC, Baseband PHY and RF in a single chip for IEEE 802.11a/b/g/n/ac/ax compatible WLAN
- Support 802.11ac 2x2,Wave-2 compliant with RX MU-MIMO
- Support 802.11ax 2x2, with OFDMA and MU-MIMO, by 4 types PPDU format, such as HE-SU-PPDU, HE-ER-SU-PPDU, HE-MU-PPDU, and HE-TB-PPDU
- Complete 802.11n MIMO solution for 2.4GHz and 5Ghz band
- Maximum PHY data rate up to 286.8 Mbps using 20MHz bandwidth, 573.5Mbps using 40MHz bandwidth, and 1201Mbps using 80MHz bandwidth
- Backward compatible with 802.11a/b/g devices while operating at 802.11n data rates
- Backward compatible with 802.11a/n/ac devices while operating at 802.11ax data rates

Host Interface

- Complies with PCI Express Base Specification Revision 1.1
- Complies with USB2.0 FS-mode Specification for Bluetooth.
- PCIe LTR/L1.Off state supported.
- USB Selective Suspend supported.

Standards Supported

- IEEE 802.11a/b/g/n/ac/ax compatible WLAN
- IEEE 802.11e QoS Enhancement (WMM)
- IEEE 802.11i (WPA, WPA2, WPA3). Open, shared key, and pair-wise key authentication services
- IEEE 802.11h DFS, TPC, Spectrum Measurement
- IEEE 802.11k Radio Resource Measurement
- WAPI (Wireless Authentication Privacy Infrastructure) certified.

MAC Features

- Frame aggregation for increased MAC efficiency (A-MSDU, A-MPDU)
- Low latency immediate Block Acknowledgement (BA)
- PHY-level spoofing to enhance legacy compatibility
- MIMO power saving mechanism
- Support TWT function for power saving.
- Channel management and co-existence
- Transmit Opportunity (TXOP) Short Inter-Frame Space (SIFS) bursting for higher multimedia bandwidth
- WiFi Direct supports wireless peer to peer applications.Support BSR and queue size of Qos.
- Support MU EDCA feature.
- Support DFS, Channelinfo, PPDU state by Rx path.

Other Features

- Supports Wake-On-WLAN via Magic Packet and Wake-up frame
- Transmit Beamforming
- Support S3/S4 AES/TKIP group key update
- FTM support distance measurement
- Support Network List Offload
- CCA on secondary through RTS/CTS handshake
- Support TCP/UDP/IP checksum offload
- Compliance with Windows operating system host-implemented FIPS 140-2 security requirements.
- 802.11i (WPA2) compliant
- WPA3 – Enterprise compliant
- WPA3-Enterprise 192-bit Security(based on AES-GCMP-256 & BIP-GMAC-256)

PHY Features

- IEEE 802.11ax MIMO OFDM/OFDMA
- IEEE 802.11ac MIMO OFDM
- IEEE 802.11n MIMO OFDM
- Two Transmit and Two Receive paths
- 20MHz / 40MHz / 80MHz bandwidth transmission
- Support 2.4Ghz and 5Ghz band channels
- Short Guard Interval (0.4us) for non-HE. 1xLTF and 0.8us guard interval for HE SU/ERSU. 4x LTF and 0.8us guard interval for HE MU
- DSSS with DBPSK and DQPSK, CCK modulation with long and short preamble
- OFDM with BPSK, QPSK, 16QAM, 64QAM, 256QAM and 1024QAM modulation. Convolutional Coding Rate: 1/2, 2/3, 3/4, and 5/6
- Maximum data rate 54Mbps in 802.11g, 300Mbps in 802.11n and 866.7Mbps in 802.11ac, 1201Mbps in 802.11ax.
- OFDM/DSSS/CCK receive diversity with MRC using up to 2 receive paths.
- Support STBC
- Support LDPC
- Maximum-Likelihood Detection (MLD)
- Fast receiver Automatic Gain Control (AGC)
- On-chip ADC and DAC
- Build-in both 2.4GHz and 5GHz PA
- Build-in both 2.4GHz and 5GHz LNA

Bluetooth Controller

- Support Bluetooth 5 system (BT 5.2 Logo Compliant)
- Compatible with Bluetooth v2.1+EDR
- Integrated MCU to execute Bluetooth protocol stack
- Supports all packet types in basic rate and enhanced data rate
- Supports Secure Simple Pairing
- Enhanced BT/WIFI Coexistence Control to improve transmission quality in different profiles
- Dual Mode support: Simultaneous LE and BR/EDR
- Supports multiple Low Energy states

Bluetooth Transceiver

- Fast AGC control to improve receiving dynamic range
- Integrated internal Class 1, Class 2, and Class 3 PA
- Supports Enhanced Power Control
- Supports Bluetooth Low Energy
- Integrated 32K oscillator for power management

3. Application Diagrams

3.1. System Block Diagram

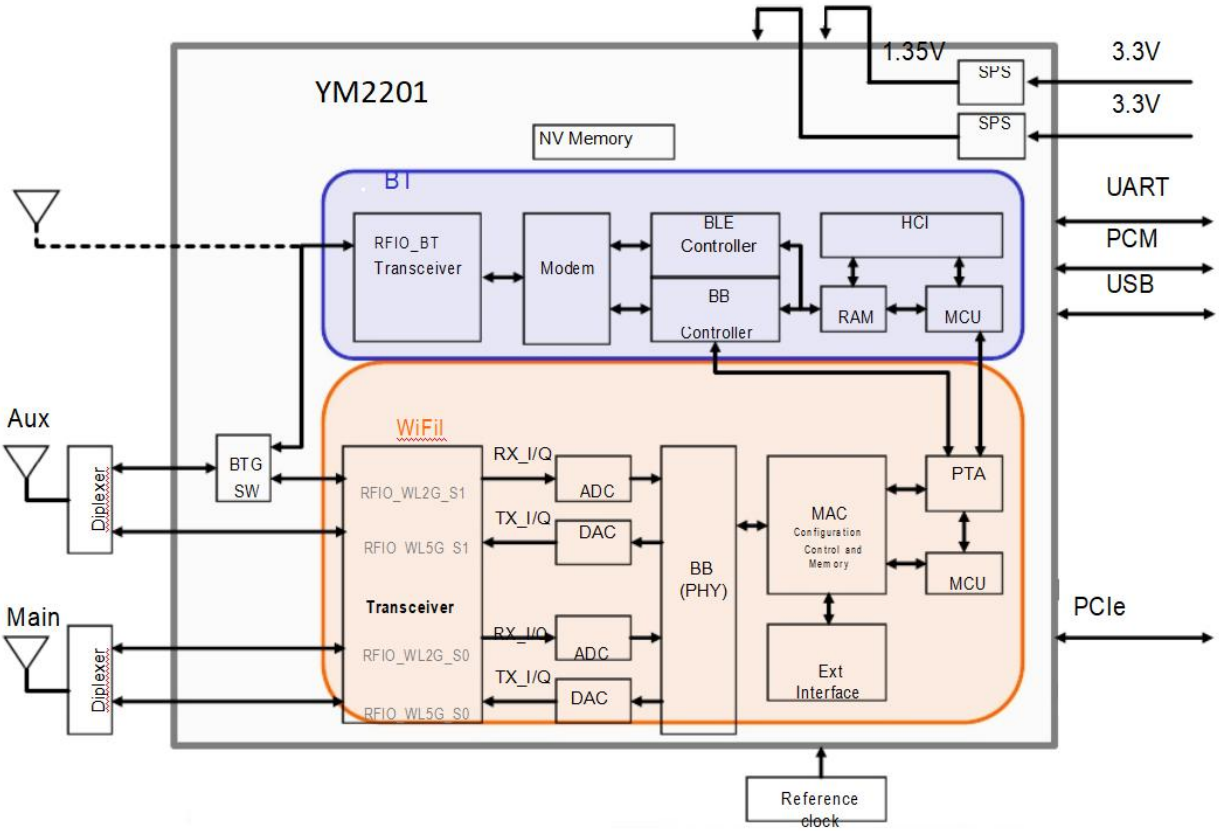


Figure 1, System Block Diagram

4. Pin Assignments

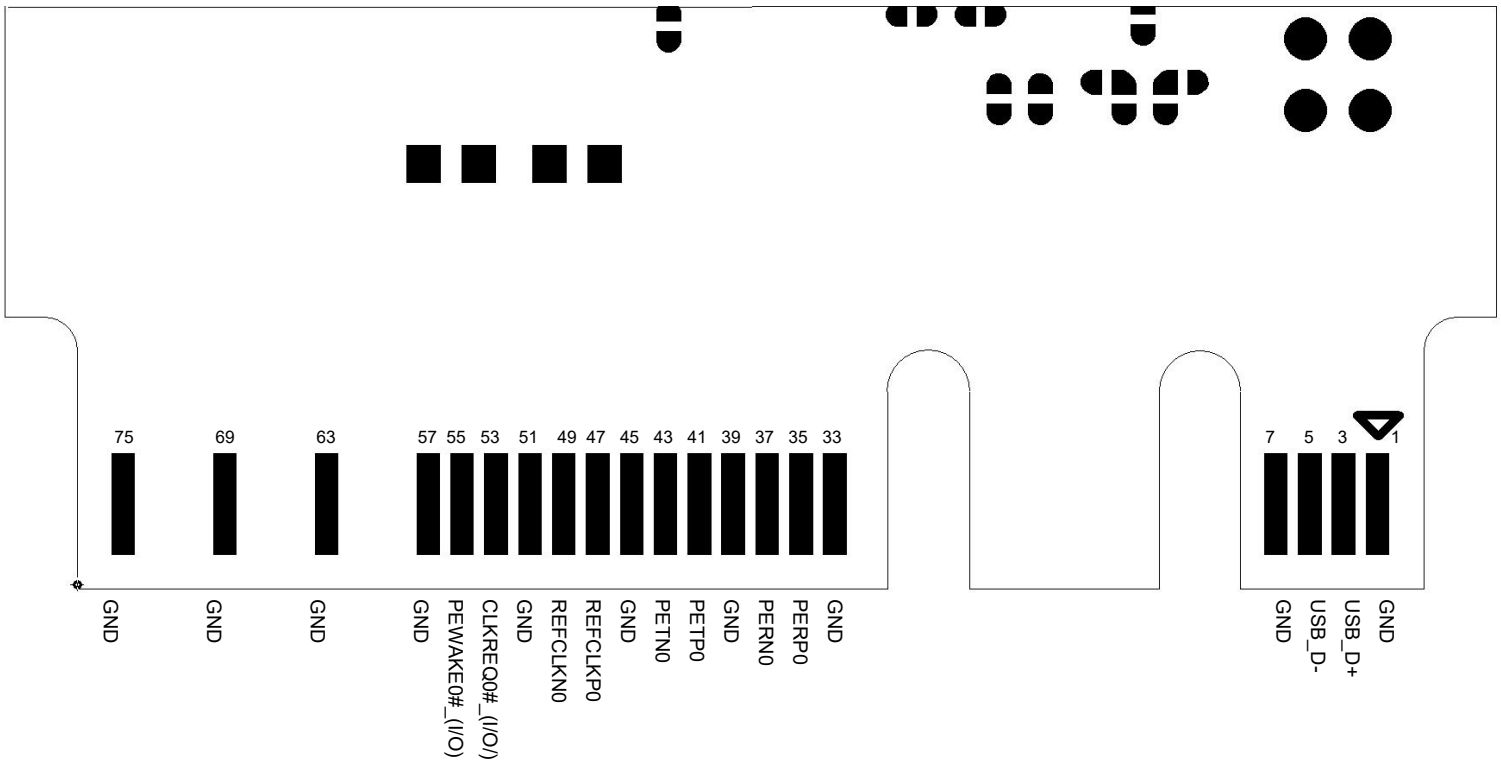


Figure 2.1 Pin AssignmentsTOP

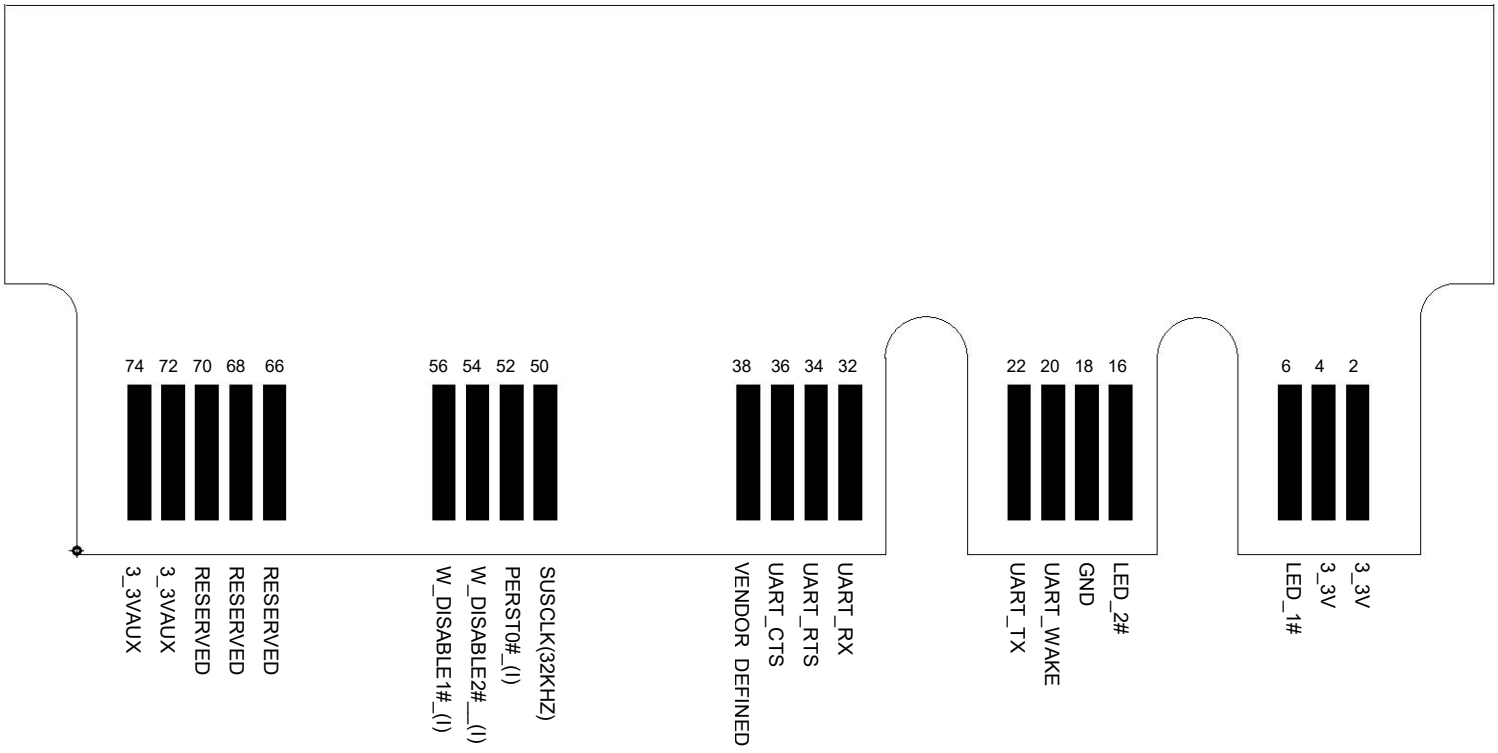


Figure 2.2 Pin Assignments BOTTOM

5. Pin Descriptions

The following signal type codes are used in the tables:

I:	Input	O:	Output
T/S:	Tri-State bi-directional input/output pin	S/T/S:	Sustained Tri-State
O/D:	Open Drain	P:	Power pin
N/A:	No Bonding pin		

5.1. Power Pin

Table 1. Power-On Trap Pins

Symbol	Type	Pin No	Description	Voltage
VD33	P	2,4,72,74	3_3V	3.3V
GND	P	1,7,33,39,45, 51,57,63,69,75	GND	

5.2. PCI Express Transceiver Interface

Table 2. PCI Express Transceiver Interface

Symbol	Type	Pin No	Description	Voltage
HSIN/HSIP	I	35,37	PCI Express Receive Differential Pair	
HSON/HSOP	O	41,43	PCI Express Transmit Differential Pair	
REFCLK_N/REFCLK_P	I	47,49	PCI Express Differential Reference Clock Source: 100MHz ± 300ppm	
CLKREQn	I/O/D	53	Reference Clock Request Signal.Also used by L1 PM substates. This signal is used by the YM2201 to request for the PCI Express reference clock.	3.3V
WAKEN	O/D	55	Power Management Event: Open drain, active low. Used to reactivate the PCI Express slot's main power rails and reference clocks. This WAKE# can be shared with BT wake up host function via sideband signals.	3.3V
PERSTN	I	52	PCI Express Reset Signal: active low. When the PERST# is asserted at power-on state, the YM2201 returns to a pre-defined reset state and is ready for initialization and configuration after the de-assertion of the PERST#.	3.3V

5.3. USB Transceiver Interface

Table 3. USB Transceiver Interface

Symbol	Type	Pin No	Description
HSDP	I/O	3	High-Speed USB D+ Signal
HSDM	I/O	5	High-Speed USB D- Signal

5.4. UART Interface

Table 3. USB Transceiver Interface

Symbol	Type	Pin No	Description
UART_TX	O	22	
UART_RX	I	32	
UART_RTS	I	34	
UART_CTS	O	36	

5.5. LED Interface

Table 5. LED Interface

Symbol	Type	Pin No	Description
BT_LED	O	16	BT LED Pin (Active Low)
WL_LED	O	6	WL LED Pin (Active Low), shared with GPIO8

5.6. Power Management Handshake Interface

Table 6. Power Management Handshake Interface

Symbol	Type	Pin No	Description
WL_DIS_N	I	56	Shared with GPIO9.This pin can be defined as the WLAN Radio-off function with host interface remaining connected. When this pin is pulled low, WLAN function will be Radio-off. When this function is not required, external pull high is not required.
BT_DIS_N	I	54	Shared with GPIO11. This pin can externally shut down the YM2201 BT function when BT_DIS# is pulled Low. When this pin is pulled low, USB interface will be also disabled. When this function is not required, external pull high is not required.

5.7. Clock and Other Pins

Table 7. Clock and Other Pins

Symbol	Type	Pin No	Description
SUSCLK	I	50	Boot from flash select for power on trap and External 32K clock input
PCM_IN	I/O	66	General Purpose Input/ Output Pin
PCM_OUT	I/O	68	General Purpose Input/ Output Pin
PCM_SYNC	I/O	70	General Purpose Input/ Output Pin
HOST_WAKE_BT	I/O	38	General Purpose Input/ Output Pin

6. Electrical and Thermal Characteristics

6.1. Temperature Limit Ratings

Table 12. Temperature Limit Ratings

Parameter	Minimum	Maximum	Units
Storage Temperature	-55	+125	°C
Ambient Operating Temperature	-10	70	°C
Junction Temperature	0	125	°C

Humidity Information

MSL level	3

6.2. DC Characteristics

6.2.1. Power Supply Characteristics

Table 13. DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Peak Current
VD33	3.3V I/O Supply Voltage	3.0V	3.3V	3.6V	2A

6.2.2. Digital IO Pin DC Characteristics

Table 14. 3.3V IO DC Characteristics

Symbol	Parameter	Minimum	Normal	Maximum	Units
V_{IH}	Input high voltage	2.0	3.3	3.6	V
V_{IL}	Input low voltage	--	0	0.9	V
V_{OH}	Output high voltage	2.97	--	3.3	V
V_{OL}	Output low voltage	0	--	0.33	V

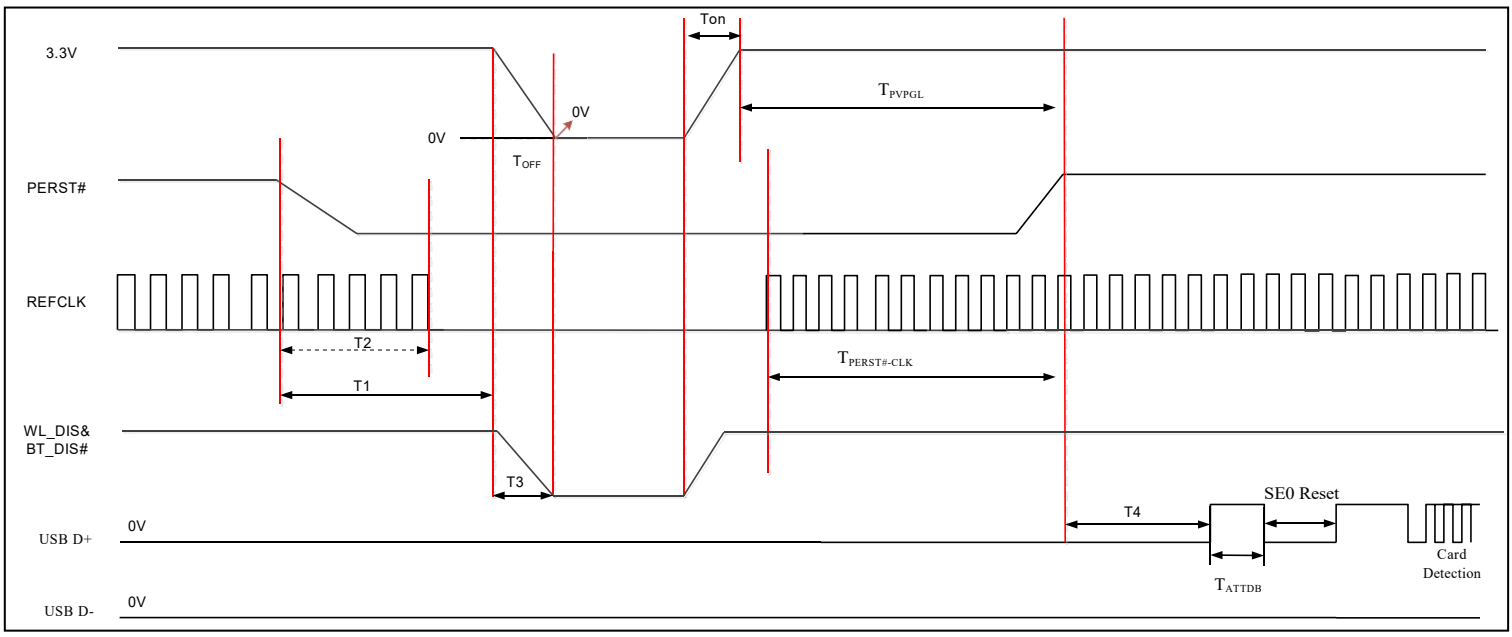
Table 15. 1.8V IO DC Characteristics

Symbol	Parameter	Minimum	Normal	Maximum	Units
V_{IH}	Input high voltage	1.7	1.8	3.6	V
V_{IL}	Input low voltage	--	0	0.8	V
V_{OH}	Output high voltage	1.62	--	1.8	V
V_{OL}	Output low voltage	0	--	0.18	V

7. Interface Timing Specification

7.1. PCIe Bus during Power On Sequence

a. When WLAN is power off



b. When WLAN is NOT power off

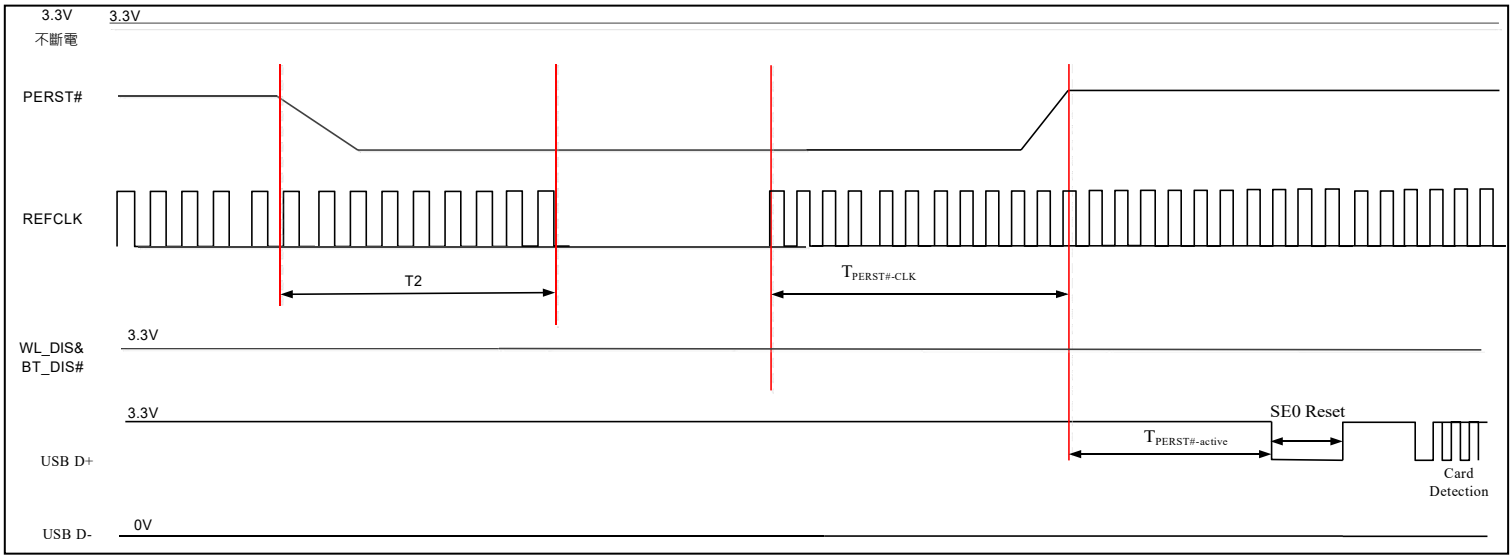


Figure 4. YM2201 PCIe and USB Bus Power On/Off Sequence

T_{on}: The main power ramp up duration

T_{off}: The main power off duration

T_{PVPGL}: Power valid to PERST# input inactive

$T_{PERST\#-CLK}$: Reference clock stable before PERST# inactive

T_{ATTDB}: the debounce interval with a minimal duration of 100ms that provided by the USB system Software

$T_{SE0\ Reset}$: USB host send SE0 Reset duration

$T_{PERST\#-active}$: PCI-e initial duration after PERST# inactive

Note:

1. T1: PERST# goes active before the power on the connector is removed.
2. T2: Clock to inactive after PERST# goes active.
3. T3: WL_DIS# and BT_DIS# goes asserted when the power on the connector is removed.
4. T4: USB D+ go active after PERST# goes inactive.
5. T1/T2/T3/T4 timing value should large than 0.

Symbol	Unit	Min	Typical	Max
T_{on}	ms	0.5	1.5	5
T_{off}	ms	1.5		
T_{PVPGL}	ms	Implementation specific;recommended 50ms	--	--
$T_{PERST\#-CLK}$	us	100	--	--
T_{ATTDB}	ms	100	--	--
$T_{SE0\ Reset}$	ms	10	--	--
$T_{PERST\#-active}$	ms	10	--	--

Table 16. The typical timing range

7.2. PCIe PERST# Timing Sequence (if need at least twice)

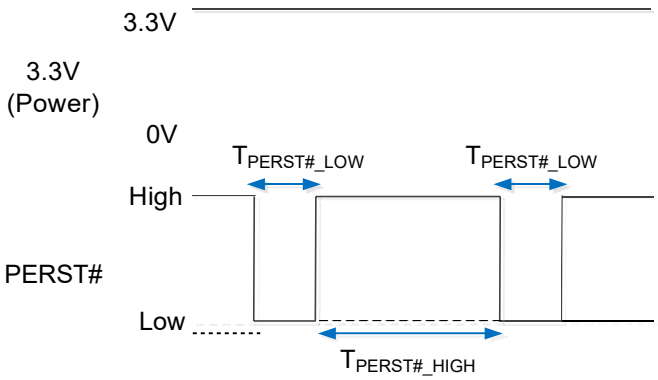


Table 17. YM2201 PCIE PERST# Timing Parameters

	Min	Typical	Max	Unit	Description
TPERST#_LOW	6	10	X	ms	PERST# low duration
TPERST#_HIGH	400	500	X	ms	PERST# high duration

7.3. Power Off Sequence

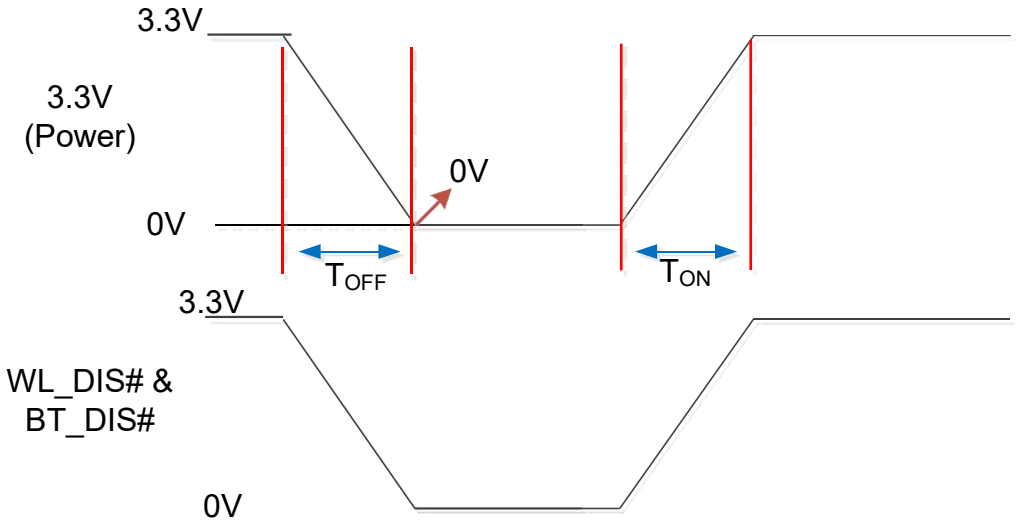


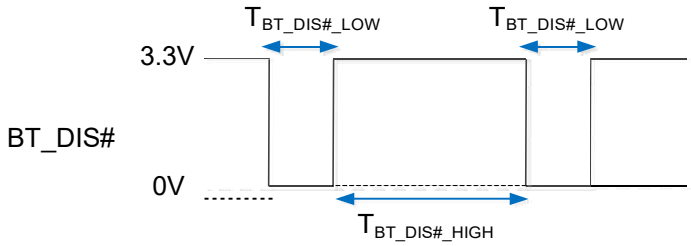
Figure 5. YM2201 Power Off Sequence of 3.3V platform

Table 18. YM2201 Power Off Timing Parameters

Symbol	Min	Typical	Max	Unit	Description
T_{OFF}	1.5	--	--	ms	Measure point start on 100% Measure point end on 0% (must be 0V)
T_{ON}	0.5	1.5	5	ms	Measure point start on 0% (must be 0V) Measure point end on 100%

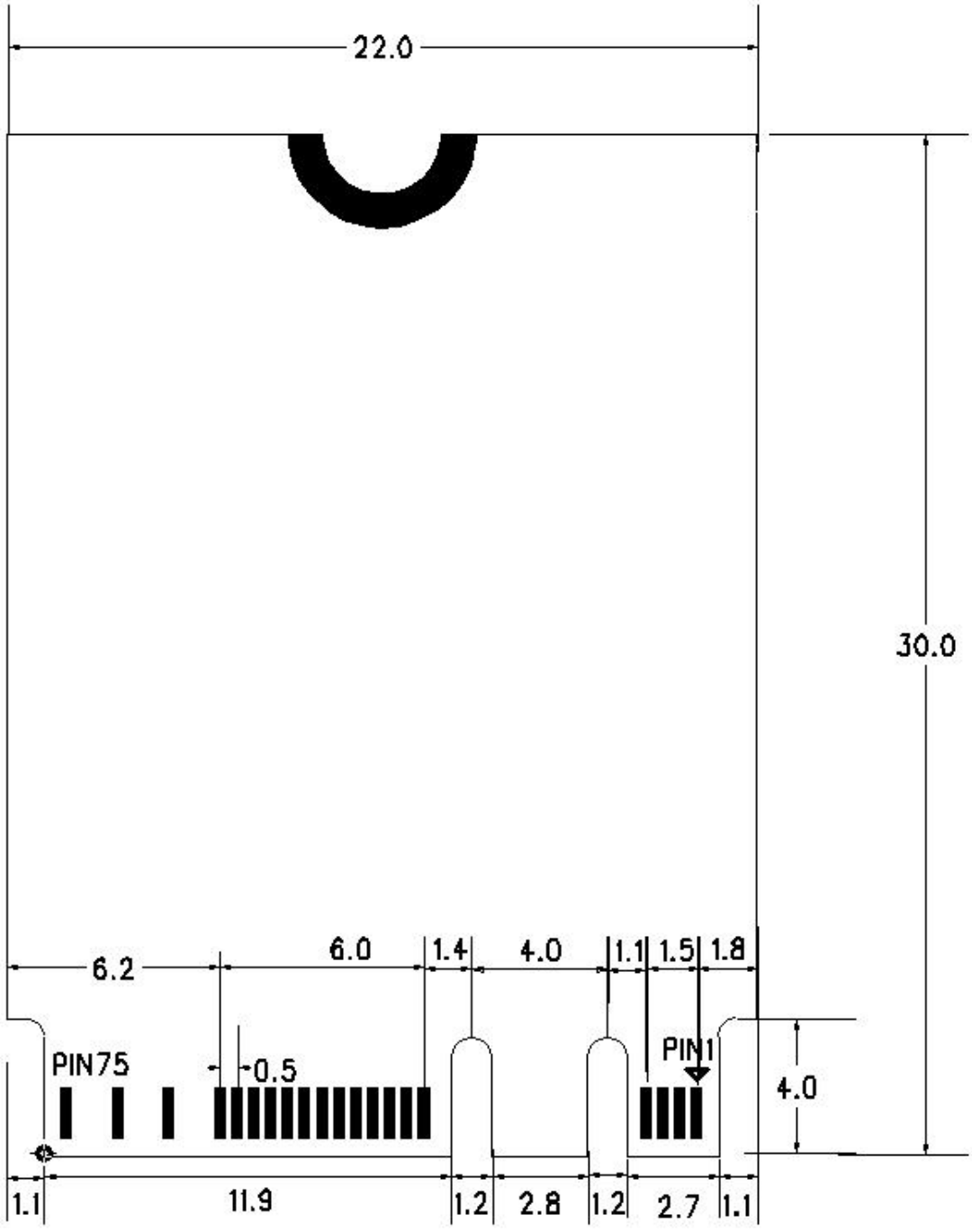
Note: If BT_DIS# can't connect to the same power source with 3.3V, it need to be de-asserted before PERST# with 100ms in power on sequence.

7.4. BT_DIS Timing Sequence

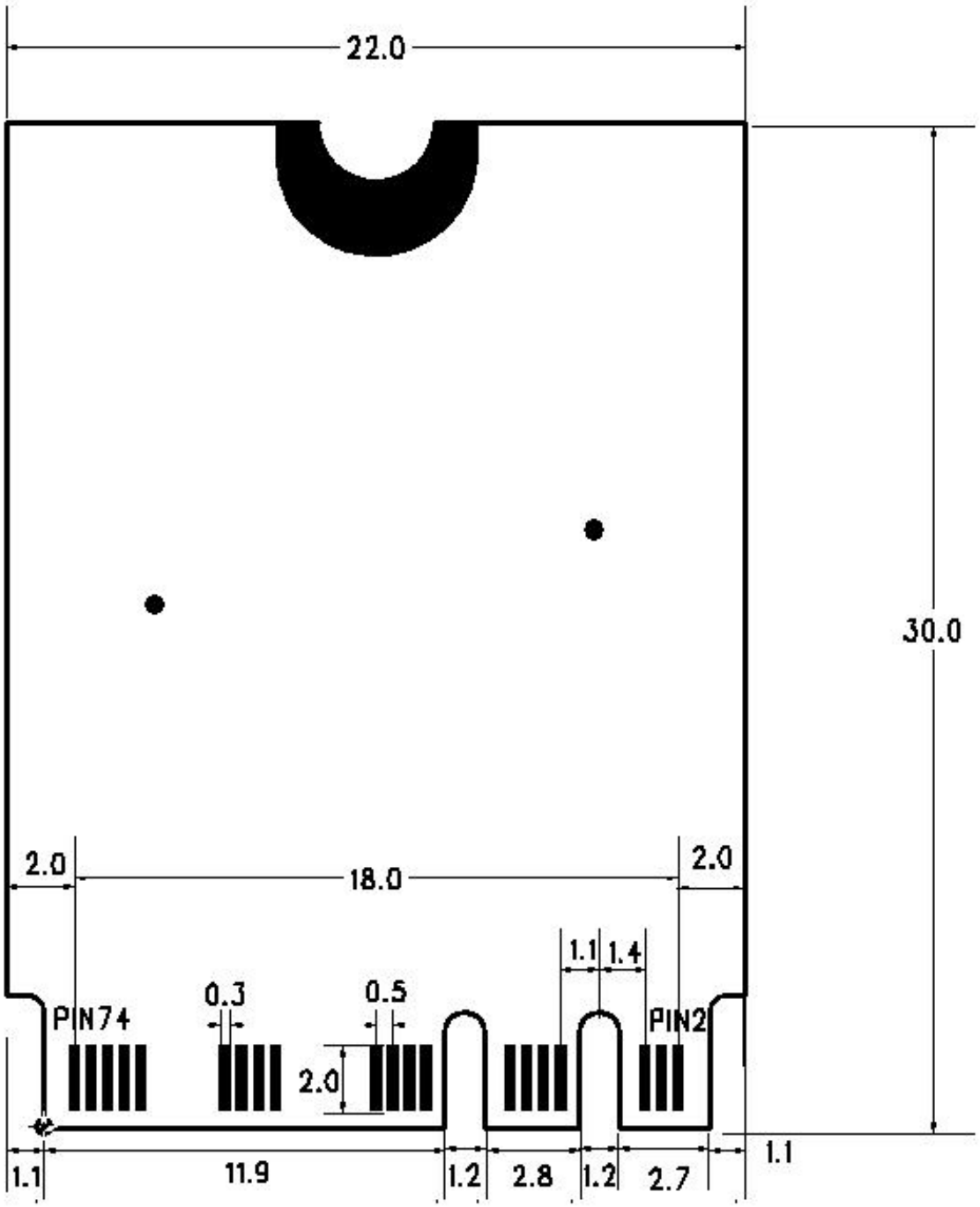


	Min	Typical	Max	Unit	Description
BT_DIS#_LOW	200	--	--	ms	BT_DIS# low duration
BT_DIS#_HIGH	500	--	--	ms	BT_DIS# high duration

8. Mechanical Dimensions



PCB TOP SIDE



PCB BOTTOM SIDE

9. Ordering Information

Table 19. Ordering Information

Part Number	Package	Status
YM2201	PCIe, M.2 , 'Green' Package	Mass Production

10. RF Specification Reference

2G, Tx, internal PA				
Standard	Modulation Scheme and Test Condition	Measurement at Antenna Ports		
		Min	Typ	Max
11b	AVG EVM 8%	18.5	**19.5**	20.5
11g	EVM -28dB, 54M	20.0	**21.0**	22.0
	EVM, -5dB, 6M	19.0	**20.0**	21.0
11n (20M)	EVM -30dB, MCS7	18.5	**19.5**	20.5
	EVM, -5dB, MCS0	18.5	**19.5**	20.5
11n, ax (40M)	EVM -36dB, MCS7	16	**17.0**	18
	EVM -5dB, MCS0	18.5	**19.5**	20.5

5G, Tx, internal PA				
Standard	Modulation Scheme and Test Condition	Measurement at Antenna Ports		
		Min	Typ	Max
11a	EVM -28dB, 54M	19.5	**20.5**	21.5
	EVM -5dB, 6M	18.5	**19.5**	20.5
11n (20M)	EVM -30dB, MCS7	19.0	**20.0**	21.0
	EVM -5dB, MCS0	18.5	**19.5**	20.5
11n (40M)	EVM -30dB, MCS7	19.0	**20.0**	21.0
	EVM -5dB, MCS0	18.5	**19.5**	20.5
11ac, ax (80M)	EVM -36dB, MCS9/11	15.0	**16.0**	17.0
	EVM -5dB, MCS0	16.5	**17.5**	18.5

2G, Rx, internal LNA				
Standard	Modulation Scheme and Test Condition	Measurement at Antenna Ports		
		Max	Typ	Min
11b	11M, BCC	--	-91.5	--
	1M, BCC	--	-99.5	--
11g	54M, BCC	--	-79.0	--
	6M, BCC	--	-95.5	--
11n HT20	MCS7, BCC	--	-76.5	--
	MCS0, BCC	--	-95.5	--
11n HT40	MCS7, BCC	--	-73.5	--
	MCS0, BCC	--	-92.5	--
11ax HE40	MCS11, LDPC	--	-64.0	--
	MCS9, LDPC		-69.5	
	MCS7, LDPC	--	-75.0	--
	MCS0, LDPC	--	-93.5	--

5G, Rx, internal LNA				
Standard	Modulation Scheme and Test Condition	Measurement at Antenna Ports		
		Min	Typ	Max
11a	54M, BCC	--	-78.5	--
	6M, BCC	--	-95.5	--
11n HT20	MCS7, BCC	--	-76.0	--
	MCS0, BCC	--	-95.0	--
11n HT40	MCS7, BCC	--	-73.0	--
	MCS0, BCC	--	-92.0	--
11ac VHT80	MCS9, BCC	--	-64.0	--
	MCS7, BCC	--	-70.0	--
	MCS0, BCC	--	-89.0	--
11ax HE80	MCS11, LDPC	--	-60.5	--
	MCS9, LDPC		-66.5	
	MCS7, LDPC	--	-72.0	--
	MCS0, LDPC	--	-90.0	--

BT, Rx, internal LNA				
Packet Type	Test Condition	Measurement at Antenna Ports		
		Max	Typ	Min
BR	BER < 0.1% (A minimum number of samples, 1600000 returned payload bits)	--	-85	--
EDR2M	BER < 1.00E-04 (A minimum number of samples, 16000000 returned payload bits.)	--	-85	--
EDR3M		--	-80	--
LE1M	PER < 30.8% (A minimum of 1500 packets transmitted by the tester.)	--	-90	--
LE2M		--	-90	--
LR2		--	-90	--
LR8		--	-90	--