8-bit Enhanced USB MCU CH549/CH548

Datasheet

Version: 1G

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1. Overview

CH549 is an enhanced E8051 MCU compatible with MCS51 instruction set, 79% of which are single-byte single-cycle instructions, and the average instruction speed is 8 to 15 times faster than that of the standard MCS51.

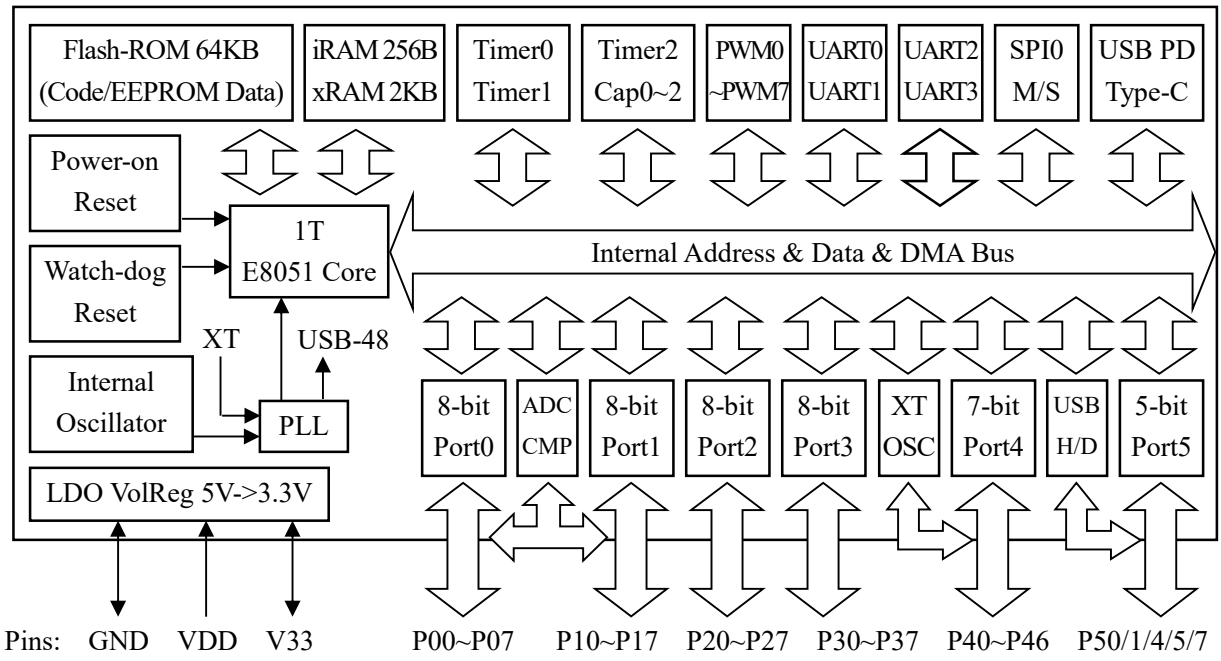
CH549 supports up to 48MHz system clock frequency, ans has built-in 64K program memory Flash-ROM and 256-byte internal iRAM and 2 Kbytes of internal xRAM. And xRAM supports direct memory access (DMA).

CH549 has a built-in 12-bit ADC, capacitive touch key detection module, temperature sensor (TS), built-in clock, 3 timers and 3 channels of signal capture, 8 channels of PWM, 4 UARTs, SPI and other functional modules. It supports full-speed and low-speed USB-Host mode and USB-Device mode as well as USB type-C. CH543 is recommended when complete PD function is required.

CH548 is a simplified version of CH549, the program memory ROM is only 32KB. CH548 only provides UART0 and UART1, others are the same as that of CH549. For details of CH548, directly refer to the datasheet and technical resources of CH549.

Product	Program ROM Boot ROM	xRAM iRAM	Nonvolatile EEPROM	USB host USB device	USB Type-C	Timer	Signal Capture	8-bit PWM	UART	SPI host SPI slave	12-bit ADC	Capacitive touch-key
CH549	60KB+3KB	2048 +256	1KB	Full/low speed	Support	3	3	8	4	2 in 1	16	16
CH548	32KB+3KB								2			

The following is the internal block diagram of CH549, for reference only.



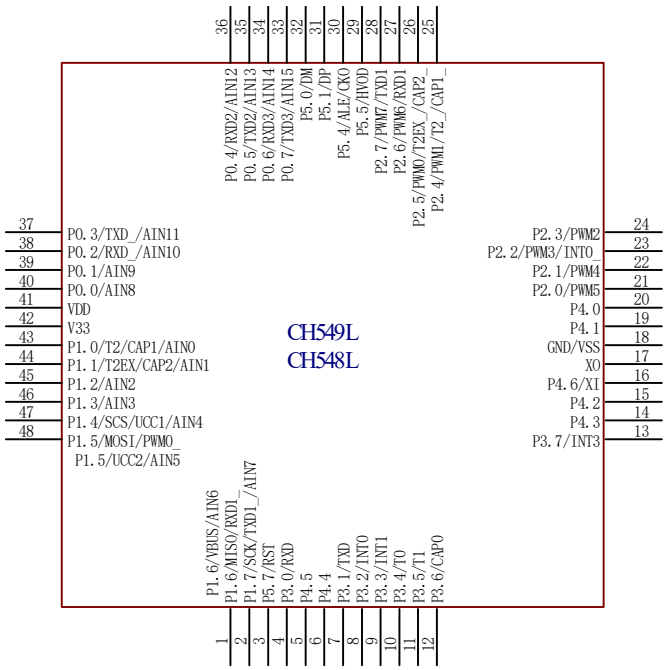
2. Features

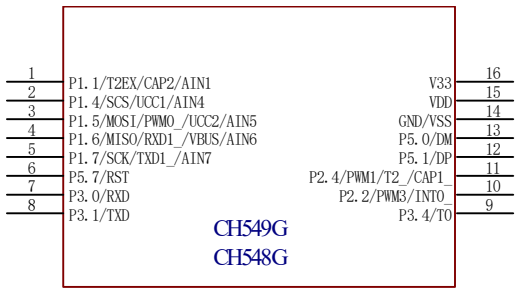
- Core: Enhanced E8051 core compatible with MCS51 command set, 79% of which are single-byte single-cycle commands, and the average command speed is 8 ~ 15 times faster than that of the standard MCS51, with special XRAM data fast copy command, and double DPTR pointers.
- ROM: 64KB nonvolatile memory Flash-ROM, supoorts 10K times of erase and program, and can all be used for the program storage space; or it can be divided into a 60KB program storage area, a 1KB data storage area EEPROM and a 3KB BootLoader/ISP program area.
- EEPROM: 1KB EEPROM, which is divided into 16 independent blocks, supports single-byte read, single-byte write, block write (1 ~ 64 bytes), block erase (64 bytes) operations. In a typical environment, generally it supports 100K times of erase and program (non-guaranteed).
- OTP: One-time programmable data storage area, with a total of 32 bytes, and supports double-word read (4 bytes), single-byte write.
- RAM: 256-byte internal iRAM, which can be used for fast temporary storage of data and stack; 2KB on-chip xRAM, which can be used for large amount of data temporary storage and DMA direct memory access.
- USB: Built-in USB controller and USB transceiver, supports USB-Host mode and USB-Device mode, supports USB 2.0 full speed (12Mbps) and low speed (1.5Mbps) modes, supports data packet of up to 64 bytes, built-in FIFO, and supports DMA.
- USB type-C: Support USB type-C master-slave detection, support USB PD power transmission control and 32-bit CRC calculation.
- Timer: 3 timers, the standard MCS51 timers T0/T1/T2.
- Capture: T2 is extended to support 3-channel signal capture.
- PWM: 8-channel PWM output, supports standard 8-bit data or fast 6-bit data.
- UART: 4 UARTs, UART0 is a standard MCS51 UART; UART1/2/3 has built-in communication baud rate setting register.
- SPI: The SPI controller supports Master/Slave mode, built-in FIFO, clock frequency can be approximate to half of the system clock frequency Fsys. It supports simplex multiplexing of serial data input and output.
- ADC: 16-channel 12-bit A/D converter, it supports voltage comparison of multiple combinations.
- Touch-key: 16-channel capacitive touch key detection. Each ADC channel supports touch key detection.
- TS: Built-in simple temperature sensor.
- GPIO: Up to 44 GPIO pins (including XI and RST and USB pins), support MCS51 compatible quasi-bidirectional mode, newly add high-impedance input, push-pull output, open-drain output mode, one of which supports 12V high-voltage open-drain output.
- Interrupt: 16 interrupt signal sources, including 6 interrupts compatible with the standard MCS51 (INT0, T0, INT1, T1, UART0, T2), and 10 extended interrupts (SPI0, INT3, USB, ADC/UART2, UART1, PWMX/UART3, GPIO, WDOG). GPIO interrupt can be selected from 7 pins.
- Watch-Dog: 8-bit presettable watchdog timer WDOG, supports timing interrupt.
- Reset: 5 reset signal sources, built-in power on reset and multi-stage adjustable power supply low voltage detection reset module, supports software reset and watchdog overflow reset, optional pin external input reset.
- Clock: Built-in 24 MHz clock source, which can support external crystals by multiplexing GPIO pins, and the built-in PLL is used to generate USB clock and system clock frequency Fsys with the required frequency.

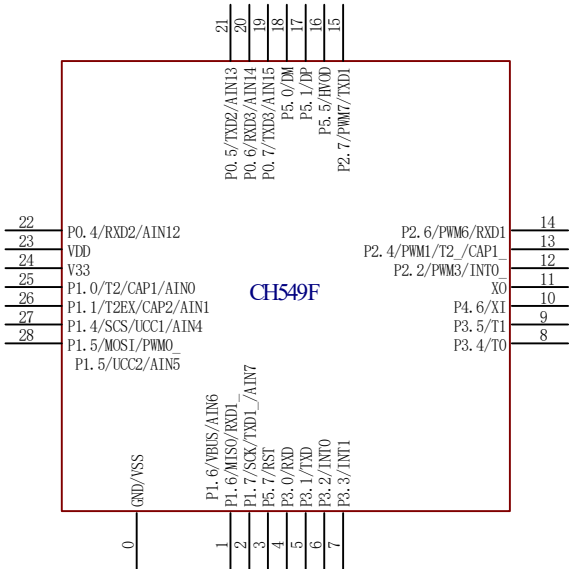
- Power: Built-in 5V to 3.3V low dropout voltage regulator for USB and other modules. It supports 5V or 3.3V or even 6V or 2.8V supply voltage.
- Sleep: Low-power sleep mode, USB, UART0, UART1, SPI0, comparator and part of the GPIO external awake.
- Unique ID for identification.

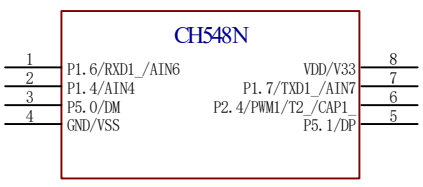
3. Packages

Package	Body size		Lead pitch		Description	Part No.
LQFP48	7*7mm		0.5mm	19.7mil	Standard LQFP 48-pin patch	CH549L
QFN28_4X4	4*4mm		0.4mm	15.7mil	Quad no-lead 28-pin	CH549F
SOP16	3.9mm	150mil	1.27mm	50mil	Standard 16-pin patch	CH549G
LQFP48	7*7mm		0.5mm	19.7mil	Standard LQFP 48-pin patch	CH548L
SOP16	3.9mm	150mil	1.27mm	50mil	Standard 16-pin patch	CH548G
SOP8	3.9mm	150mil	1.27mm	50mil	Standard 8-pin patch	CH548N









4. Pin definitions

Pin No.			Pin	Alternate	Description
SOP16	QFN28	LQFP48	Name	(Left preferential)	
15	23	41	VDD	VCC	I/O power input and external power input of internal USB power regulator, requires an external 0.1UF power decoupling capacitor.
16	24	42	V33	V3	Internal USB power regulator output and internal USB power input, When supply voltage is less than 3.6V, connect VDD to input external power . When supply voltage is greater than 3.6V, an external 0.1uF power decoupling capacitor is required.
14	0	18	GND	VSS	Ground
-	-	40	P0.0	AIN8	AIN8 ~ AIN15: 8-channel ADC analog signal/touch key input. RXD_, TXD_: mapping of RXD and TXD RXD2, TXD2: serial data input and serial data output of UART2. RXD3, TXD3: serial data input and serial data output of UART3
-	-	39	P0.1	AIN9	
-	-	38	P0.2	RXD_/AIN10	
-	-	37	P0.3	TXD_/AIN11	
-	22	36	P0.4	RXD2/AIN12	
-	21	35	P0.5	TXD2/AIN13	
-	20	34	P0.6	RXD3/AIN14	
-	19	33	P0.7	TXD3/AIN15	
-	25	43	P1.0	T2/CAP1/AIN0	AIN0 ~ AIN7: 8-channel ADC analog signal/touch key input. T2: External count input/clock output of timer/counter2. T2EX: Reload/capture input of timer/counter2. CAP1, CAP2: Capture input 1, 2 of timer/counter2. SCS, MOSI, MISO, SCK: SPI0 interface, SCS is chip select input, MOSI is host output/slave input, MISO is host input/slave output, SCK is serial clock. UCC1, UCC2: USB type-C bidirectional configuration channel. VBUS: USB type-C bus voltage detection input. PWM0_, RXD1_, TXD1_: PWM0/RXD1/TXD1 pin mapping.
1	26	44	P1.1	T2EX/CAP2/AIN1	
-	-	45	P1.2	AIN2	
-	-	46	P1.3	AIN3	
2	27	47	P1.4	SCS/UCC1/AIN4	
3	28	48	P1.5	MOSI/PWM0_/UCC2/AIN5	
4	1	1	P1.6	MISO/RXD1_/VBUS/AIN6	
5	2	2	P1.7	SCK/TXD1_/AIN7	
-	-	21	P2.0	PWM5	PWM0~PWM7: 8-channel PWM output. INT0_: INT0 pin mapping. T2_/CAP1_: T2/CAP1 pin mapping. T2EX_/CAP2_: T2EX/CAP2 pin mapping. RXD1, TXD1: UART1 serial data input, serial data output.
-	-	22	P2.1	PWM4	
10	12	23	P2.2	PWM3/INT0_	
-	-	24	P2.3	PWM2	
11	13	25	P2.4	PWM1/T2_/CAP1_	
-	-	26	P2.5	PWM0/T2EX_/CAP2_	
-	14	27	P2.6	PWM6/RXD1	

-	15	28	P2.7	PWM7/TXD1	
7	4	4	P3.0	RXD	RXD, TXD: UART0 serial data input, serial data output. INT0, INT1: external interrupt 0, external interrupt 1 input. T0, T1: timer0, timer1 external input. CAP0: Capture input 0 of timer/counter2. INT3: External interrupt 3.
8	5	7	P3.1	TXD	
-	6	8	P3.2	INT0	
-	7	9	P3.3	INT1	
9	8	10	P3.4	T0	
-	9	11	P3.5	T1	
-	-	12	P3.6	CAP0	
-	-	13	P3.7	INT3	
-	-	20	P4.0		XI, XO: external crystal oscillation input, inverted output
-	-	19	P4.1		
-	-	15	P4.2		
-	-	14	P4.3		
-	-	6	P4.4		
-	-	5	P4.5		
-	10	16	P4.6	XI	
-	11	17	XO		
13	18	32	P5.0	DM/UDM	DM, DP: D- and D+ signal terminals of USB host or USB device. The resistors have been built in, and it is not recommended to connect to external resistors in series.
12	17	31	P5.1	DP/UDP	
-	-	30	P5.4	ALE/CKO	ALE/CKO: Dummy address latch signal output or clock output. HVOD: Suppot 12V high voltage open-drain output.
-	16	29	P5.5	HVOD	
6	3	3	P5.7	RST	External reset input, built-in pull-down resistor.

Note: VDD of CH548N is shorted to V33. The value of VDD should between 3V and 3.6V when USB is used, while between 2.7V and 6.5V when USB is not used.

5. Special function register (SFR)

The following abbreviations are used in this datasheet to describe the registers:

Abbreviation	Description
RO	Software can only read these bits.
WO	Software can only write to this bit. The read value is invalid.
RW	Software can read and write to these bits.
H	End with it to indicate a hexadecimal number
B	End with it to indicate a binary number

5.1 SFR introduction and address distribution

CH549 controls, manages the device, and sets the working mode with the special function registers (SFR and xSFR).

SFR occupies 80H-FFH address range of the internal data storage space and can only be accessed by direct address commands. Registers with the x0h and x8h addresses can be accessed by bits to avoid modifying

the values of other bits when accessing a specific bit. Other registers with the addresses that are not the multiple of 8 can only be accessed by bytes.

Some SFRs can only be written in safe mode, while they can be read-only in non-safe mode , for example: GLOBAL_CFG, CLOCK_CFG, WAKE_CTRL, POWER_CFG.

Some SFRs have one or more names, for example: SPI0_CK_SE/SPI0_S_PRE, UDEV_CTRL/UHOST_CTRL, UEP1_CTRL/UH_SETUP, UEP2_CTRL/UH_RX_CTRL, UEP2_T_LEN/UH_EP_PID, UEP3_CTRL/UH_TX_CTRL, UEP3_T_LEN/UH_TX_LEN, UEP2_3_MOD/UH_EP_MOD, UEP2_DMA_H/UH_RX_DMA_H, UEP2_DMA_L/UH_RX_DMA_L, UEP2_DMA/UH_RX_DMA, UEP3_DMA_H/UH_TX_DMA_H, UEP3_DMA_L/UH_TX_DMA_L, UEP3_DMA/UH_TX_DMA, ROM_ADDR_L/ROM_DATA_LL, ROM_ADDR_H/ROM_DATA_LH, ROM_DATA_HL/ROM_DAT_BUF, ROM_DATA_HH/ROM_BUF_MOD.

Some addresses correspond to several independent SFRs, for example: SAFE_MOD/CHIP_ID, ROM_CTRL/ROM_STATUS.

CH549 contains all registers of 8051 standard SFR, and other device control registers are added. See the table below for SFRs.

Table 5.1 Table of SFRs

SFR	0, 8	1, 9	2, A	3, B	4, C	5, D	6, E	7, F
0xF8	SPI0_STAT	SPI0_DATA	SPI0_CTRL	SPI0_CK_SE SPI0_S_PRE	SPI0_SETUP	A_INV	RESET_KEEP	WDOG_COU NT
0xF0	B	TKEY_CTRL	ADC_CTRL	ADC_CFG	ADC_DAT_L	ADC_DAT_H	ADC_CHAN	ADC_PIN
0xE8	IE_EX	IP_EX	UEP4_1_MOD	UEP2_3_MOD UH_EP_MOD	UEP0_DMA_L	UEP0_DMA_H	UEP1_DMA_L	UEP1_DMA_H
0xE0	ACC	USB_INT_EN	USB_CTRL	USB_DEV_AD	UEP2_DMA_L UH_RX_DMA_L	UEP2_DMA_H UH_RX_DMA_H	UEP3_DMA_L UH_TX_DMA_L	UEP3_DMA_H UH_TX_DMA_H
0xD8	USB_INT_FG	USB_INT_ST	USB_MIS_ST	USB_RX_LEN	UEP0_CTRL	UEP0_T_LEN	UEP4_CTRL	UEP4_T_LEN
0xD0	PSW	UDEV_CTRL UHOST_CTRL	UEP1_CTRL UH_SETUP	UEP1_T_LEN	UEP2_CTRL UH_RX_CTRL	UEP2_T_LEN UH_EP_PID	UEP3_CTRL UH_TX_CTRL	UEP3_T_LEN UH_TX_LEN
0xC8	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2	T2CAP1L	T2CAP1H
0xC0	P4	T2CON2	P4_MOD_OC	P4_DIR_PU	P0_MOD_OC	P0_DIR_PU	T2CAP0L	T2CAP0H
0xB8	IP	CLOCK_CFG	POWER_CFG		SCON1	SBUF1	SBAUD1	SIF1
0xB0	P3	GLOBAL_CFG	GPIO_IE	INTX	SCON2	SBUF2	SBAUD2	SIF2
0xA8	IE	WAKE_CTRL	PIN_FUNC	P5	SCON3	SBUF3	SBAUD3	SIF3
0xA0	P2	SAFE_MOD CHIP_ID	XBUS_AUX	PWM_DATA3	PWM_DATA4	PWM_DATA5	PWM_DATA6	PWM_DATA7
0x98	SCON	SBUF	PWM_DATA2	PWM_DATA1	PWM_DATA0	PWM_CTRL	PWM_CK_SE	PWM_CTRL2
0x90	P1	USB_C_CTRL	P1_MOD_OC	P1_DIR_PU	P2_MOD_OC	P2_DIR_PU	P3_MOD_OC	P3_DIR_PU
0x88	TCON	TMOD	TL0	TL1	TH0	TH1	ROM_DATA_HL ROM_DAT_BUF	ROM_DATA_HH ROM_BUF_MOD
0x80	P0	SP	DPL	DPH	ROM_ADDR_L ROM_DATA_LL	ROM_ADDR_H ROM_DATA_LH	ROM_CTRL ROM_STATUS	PCON

Notes :(1) Those in red text can be accessed by bits;

(2). The following table shows the description of different color boxes

	Register address
	SPI0 register
	ADC register
	USB register
	Timer/counter 2 register
	Port setting register
	PWMX register
	UART1/2/3 registers
	Timer/counter 0 and 1 register
	Flash-ROM register

5.2 SFR classification and reset value

Figure 5.2 Description and reset value of SFRs and xSFRs

Functional Classification	Name	Address	Description	Reset value
System setting registers	B	F0h	B register	0000 0000b
	ACC	E0h	Accumulator	0000 0000b
	A_INV	FDh	Inverted value of accumulator high bit and low bit	0000 0000b
	PSW	D0h	Program status word register	0000 0000b
	GLOBAL_CFG	B1h	Global configuration register (CH549 Bootloader)	1110 0000b
			Global configuration register (CH549 application)	1100 0000b
			Global configuration register (CH548 Bootloader)	1010 0000b
			Global configuration register (CH548 application)	1000 0000b
	CHIP_ID	A1h	CH549 ID (read only)	0100 1001b
			CH548 ID (read only)	0100 1000b
	SAFE_MOD	A1h	Safe mode control register (write only)	0000 0000b
	DPH	83h	Data pointer high	0000 0000b
	DPL	82h	Data pointer low	0000 0000b
	DPTR	82h	16-bit SFR consists of DPL and DPH	0000h
	SP	81h	Stack pointer	0000 0111b
Clock, sleep and power control registers	WDOG_COUNT	FFh	Watchdog count register	0000 0000b
	RESET_KEEP	FEh	Reset keep register (in power on reset state)	0000 0000b
	POWER_CFG	BAh	Power management configuration register	0000 0011b
	CLOCK_CFG	B9h	System clock configuration register	1000 0011b
	WAKE_CTRL	A9h	Sleep wakeup control register	0000 0000b
	PCON	87h	Power supply control register (in power on reset state)	0001 0000b

Interrupt control registers	IP_EX	E9h	Extend interrupt priority control register	0000 0000b
	IE_EX	E8h	Extend interrupt enable register	0000 0000b
	GPIO_IE	C7h	GPIO interrupt enable register	0000 0000b
	IP	B8h	Interrupt priority control register	0000 0000b
	INTX	B3h	Extend external interrupt control register	0000 0000b
	IE	A8h	Interrupt enable register	0000 0000b
Flash-ROM registers	ROM_DATA_HH	8Fh	High byte of flash-ROM data register high word (read only)	xxxx xxxxb
	ROM_DATA_HL	8Eh	Low byte of flash-ROM data register high word (read only)	xxxx xxxxb
	ROM_DATA_HI	8Eh	16-bit SFR consists of ROM_DATA_HL and ROM_DATA_HH	xxxxh
	ROM_BUF_MOD	8Fh	Buffer mode register for flash-ROM erase/program operation	xxxx xxxxb
	ROM_DAT_BUF	8Eh	Data butter register for flash-ROM erase/program operation	xxxx xxxxb
	ROM_STATUS	86h	flash-ROM status register (read only)	0000 0000b
	ROM_CTRL	86h	flash-ROM control register (write only)	0000 0000b
	ROM_ADDR_H	85h	flash-ROM address register high byte	xxxx xxxxb
	ROM_ADDR_L	84h	flash-ROM address register low byte	xxxx xxxxb
	ROM_ADDR	84h	16-bit SFR consists of ROM_ADDR_L and ROM_ADDR_H	xxxxh
	ROM_DATA_LH	85h	High byte of flash-ROM data register low word (read only)	xxxx xxxxb
	ROM_DATA_LL	84h	Low byte of flash-ROM data register low word (read only)	xxxx xxxxb
	ROM_DATA_LO	84h	16-bit SFR consists of ROM_DATA_LL and ROM_DATA_LH	xxxxh
Port setting registers	XBUS_AUX	A2h	External bus auxiliary set register	0000 0000b
	PIN_FUNC	AAh	Pin function select register	0000 0000b
	P0_DIR_PU	C5h	Port0 direction control and pull-up enable register	1111 1111b
	P0_MOD_OC	C4h	Port0 output mode register	1111 1111b
	P4_DIR_PU	C3h	Port4 direction control and pull-up enable register	1111 1111b
	P4_MOD_OC	C2h	Port4 output mode register	1111 1111b
	P3_DIR_PU	97h	Port3 direction control and pull-up enable register	1111 1111b
	P3_MOD_OC	96h	Port3 output mode register	1111 1111b
	P2_DIR_PU	95h	Port2 direction control and pull-up enable register	1111 1111b
	P2_MOD_OC	94h	Port2 output mode register	1111 1111b
	P1_DIR_PU	93h	Port1 direction control and pull-up enable register	1111 1111b

	P1_MOD_OC	92h	Port1 output mode register	1111 1111b
	P5	ABh	Port5 input and output register	0010 0000b
	P4	C0h	Port4 input and output register	1111 1111b
	P3	B0h	Port3 input and output register	1111 1111b
	P2	A0h	Port2 input and output register	1111 1111b
	P1	90h	Port1 input and output register	1111 1111b
	P0	80h	Port0 input and output register	1111 1111b
Timer/counter 0 and 1 registers	TH1	8Dh	Timer1 counter high byte	xxxx xxxxb
	TH0	8Ch	Timer0 counter high byte	xxxx xxxxb
	TL1	8Bh	Timer1 counter low byte	xxxx xxxxb
	TL0	8Ah	Timer0 counter low byte	xxxx xxxxb
	TMOD	89h	Timer0/1 mode register	0000 0000b
	TCON	88h	Timer0/1 control register	0000 0000b
UART0 registers	SBUF	99h	UART0 data register	xxxx xxxxb
	SCON	98h	UART0 control register	0000 0000b
Timer/counter2 registers	T2CAP1H	CFh	Timer2 capture 1 data high byte (read only)	xxxx xxxxb
	T2CAP1L	CEh	Timer2 capture 1 data low byte (read only)	xxxx xxxxb
	T2CAP1	CEh	16-bit SFR consists of T2CAP1L and T2CAP1H	xxxxh
	TH2	CDh	Timer2 counter high byte	0000 0000b
	TL2	CCh	Timer2 counter low byte	0000 0000b
	T2COUNT	CCh	TL2 and TH2 constitute a 16-bit SFR	0000h
	RCAP2H	CBh	Count reload/capature 2 data register high byte	0000 0000b
	RCAP2L	CAh	Count reload/capature 2 data register low byte	0000 0000b
	RCAP2	CAh	16-bit SFR consists of RCAP2L and RCAP2H	0000h
	T2MOD	C9h	Timer2 mode register	0000 0000b
	T2CON	C8h	Timer2 control register	0000 0000b
	T2CAP0H	C7h	Timer2 capture 0 data high byte (read only)	xxxx xxxxb
	T2CAP0L	C6h	Timer2 capture 0 data low byte (read only)	xxxx xxxxb
	T2CAP0	C6h	16-bit SFR consists of T2CAP0L and T2CAP0H	xxxxh
	T2CON2	C1h	Timer2 extension control register	0000 0000b
PWMX registers	PWM_DATA7	A7h	PWM7 data register	xxxx xxxxb
	PWM_DATA6	A6h	PWM6 data register	xxxx xxxxb
	PWM_DATA5	A5h	PWM5 data register	xxxx xxxxb
	PWM_DATA4	A4h	PWM4 data register	xxxx xxxxb
	PWM_DATA3	A3h	PWM3 data register	xxxx xxxxb
	PWM_CTRL2	9Fh	PWM extension control register	0000 0000b
	PWM_CK_SE	9Eh	PWM clock setting register	0000 0000b
	PWM_CTRL	9Dh	PWM control register	0000 0010b

	PWM_DATA0	9Ch	PWM0 data register	xxxx xxxxb
	PWM_DATA1	9Bh	PWM1 data register	xxxx xxxxb
	PWM_DATA2	9Ah	PWM2 data register	xxxx xxxxb
SPI0 registers	SPI0_SETUP	FCh	SPI0 setup register	0000 0000b
	SPI0_S_PRE	FBh	SPI0 slave mode preset data register	0010 0000b
	SPI0_CK_SE	FBh	SPI0 clock setting register	0010 0000b
	SPI0_CTRL	FAh	SPI0 control register	0000 0010b
	SPI0_DATA	F9h	SPI0 data register	xxxx xxxxb
	SPI0_STAT	F8h	SPI0 status register	0000 1000b
UART1 registers	SIF1	BFh	UART1 interrupt status register	0000 0000b
	SBAUD1	BEh	UART1 baud rate set register	xxxx xxxxb
	SBUF1	BDh	UART1 data register	xxxx xxxxb
	SCON1	BCh	UART1 control register	0100 0000b
UART2 registers	SIF2	B7h	UART2 interrupt status register	0000 0000b
	SBAUD2	B6h	UART2 baud rate setting register	xxxx xxxxb
	SBUF2	B5h	UART2 data register	xxxx xxxxb
	SCON2	B4h	UART2 control register	0000 0000b
UART3 registers	SIF3	AFh	UART3 interrupt status register	0000 0000b
	SBAUD3	AEh	UART3 baud rate setting register	xxxx xxxxb
	SBUF3	ADh	UART3 data register	xxxx xxxxb
	SCON3	ACh	UART3 control register	0000 0000b
ADC/TKEY registers	ADC_PIN	F7h	ADC pin digital input control register	0000 0000b
	ADC_CHAN	F6h	ADC analog signal channel select register	0000 0000b
	ADC_DAT_H	F5h	ADC result data high byte (read only)	0000 xxxxb
	ADC_DAT_L	F4h	ADC result data low byte (read only)	xxxx xxxxb
	ADC_DAT	F4h	16-bit SFR consists of ADC_DAT_L and ADC_DAT_H	0xxxh
	ADC_CFG	F3h	ADC configuration register	0000 0000b
	ADC_CTRL	F2h	ADC control and status register	x000 000xb
	TKEY_CTRL	F1h	Touch key charging impulse width control register (write only)	0000 0000b
USB registers	UEP1_DMA_H	EFh	Endpoint1 buffer start address high byte	0000 0xxxb
	UEP1_DMA_L	EEh	Endpoint1 buffer start address low byte	xxxx xxxxb
	UEP1_DMA	EEh	16-bit SFR consists of UEP1_DMA_L and UEP1_DMA_H	0xxxh
	UEP0_DMA_H	EDh	Endpoint0/4 buffer start address high byte	0000 0xxxb
	UEP0_DMA_L	ECh	Endpoint0/4 buffer start address low byte	xxxx xxxxb
	UEP0_DMA	ECh	16-bit SFR consists of UEP0_DMA_L and UEP0_DMA_H	0xxxh
	UEP2_3_MOD	EBh	Endpoint2/3 mode control register	0000 0000b
	UH_EP_MOD	EBh	USB host endpoint mode control register	0000 0000b
	UEP4_1_MOD	EAh	Endpoint1/4 mode control register	0000 0000b
	UEP3_DMA_H	E7h	Endpoint3 buffer start address high byte	0000 0xxxb

	UEP3_DMA_L	E6h	Endpoint3 buffer start address low byte	xxxx xxxxb
	UEP3_DMA	E6h	16-bit SFR consists of UEP3_DMA_L and UEP3_DMA_H	0xxxh
	UH_TX_DMA_H	E7h	USB host transmit buffer start address high byte	0000 0xxxb
	UH_TX_DMA_L	E6h	USB host transmit buffer start address low byte	xxxx xxxxb
	UH_TX_DMA	E6h	16-bit SFR consists of UH_TX_DMA_L and UH_TX_DMA_H	0xxxh
	UEP2_DMA_H	E5h	Endpoint2 buffer start address high byte	0000 0xxxb
	UEP2_DMA_L	E4h	Endpoint2 buffer start address low byte	xxxx xxxxb
	UEP2_DMA	E4h	16-bit SFR consists of UEP2_DMA_L and UEP2_DMA_H	0xxxh
	UH_RX_DMA_H	E5h	USB host receive buffer start address high byte	0000 0xxxb
	UH_RX_DMA_L	E4h	USB host receive buffer start address low byte	xxxx xxxxb
	UH_RX_DMA	E4h	16-bit SFR consists of UH_RX_DMA_L and UH_RX_DMA_H	0xxxh
	USB_DEV_AD	E3h	USB device address register	0000 0000b
	USB_CTRL	E2h	USB control register	0000 0110b
	USB_INT_EN	E1h	USB interrupt enable register	0000 0000b
	UEP4_T_LEN	DFh	Endpoint4 transmission length register	0xxx xxxxb
	UEP4_CTRL	DEh	Endpoint4 control register	0000 0000b
	UEP0_T_LEN	DDh	Endpoint0 transmission length register	0xxx xxxxb
	UEP0_CTRL	DCh	Endpoint0 control register	0000 0000b
	USB_RX_LEN	DBh	USB reception length register (read only)	0xxx xxxxb
	USB_MIS_ST	DAh	USB miscellaneous status register (read only)	xx10 1000b
	USB_INT_ST	D9h	USB interrupt status register (read only)	00xx xxxxb
	USB_INT_FG	D8h	USB interrupt flag register	0010 0000b
	UEP3_T_LEN	D7h	Endpoint3 transmission length register	0xxx xxxxb
	UH_TX_LEN	D7h	USB host transmission length register	0xxx xxxxb
	UEP3_CTRL	D6h	Endpoint3 control register	0000 0000b
	UH_TX_CTRL	D6h	USB host transmit endpoint control register	0000 0000b
	UEP2_T_LEN	D5h	Endpoint2 transmission length register	0000 0000b
	UH_EP_PID	D5h	USB host token set register	0000 0000b
	UEP2_CTRL	D4h	Endpoint2 control register	0000 0000b
	UH_RX_CTRL	D4h	USB host receive endpoint control register	0000 0000b
	UEP1_T_LEN	D3h	Endpoint1 transmission length register	0xxx xxxxb
	UEP1_CTRL	D2h	Endpoint1 control register	0000 0000b
	UH_SETUP	D2h	USB host auxiliary set register	0000 0000b
	UDEV_CTRL	D1h	USB device port control register	00xx 0000b
	UHOST_CTRL	D1h	USB host port control register	00xx 0000b
	USB_C_CTRL	91h	USB type-C configuration channel control	0000 0000b

			register	

5.3 General-purpose 8051 registers

Table 5.3.1 List of general-purpose 8051 registers

Name	Address	Description	Reset value
A_INV	FDh	Inverted value of accumulator high bit and low bit	00h
B	F0h	B register	00h
A, ACC	E0h	Accumulator	00h
PSW	D0h	Program status word register	00h
GLOBAL_CFG	B1h	Global configuration register (CH549 Bootloader)	E0h
		Global configuration register (CH549 application)	C0h
		Global configuration register (CH548 Bootloader)	A0h
		Global configuration register (CH548 application)	80h
CHIP_ID	A1h	CH549 ID number (read only)	49h
		CH548 ID number (read only)	48h
SAFE_MOD	A1h	Safe mode control register (write only)	00h
PCON	87h	Power control register (in power on reset status)	10h
DPH	83h	Data address pointer high 8 bits	00h
DPL	82h	Data address pointer low 8 bits	00h
DPTR	82h	16-bit SFR consists of DPL and DPH	0000h
SP	81h	Stack pointer	07h

B register (B):

Bit	Name	Access	Description	Reset value
[7:0]	B	RW	Arithmetic operation register, mainly used for multiplication and division operations, accessed by bits.	00h

A accumulator (A, ACC):

Bit	Name	Access	Description	Reset value
[7:0]	A/ACC	RW	Arithmetic operation accumulator, accessed by bits.	00h

Program status word register (PSW):

Bit	Name	Access	Description	Reset value
7	CY	RW	Carry flag bit: used to record the carry or borrow of the highest bit when performing arithmetic operations and logical operations. In 8-bit addition operation, this bit is set if the highest bit is carried, otherwise it is cleared. In 8-bit subtraction operation, this bit is set if the highest bit is borrowed, otherwise it is cleared. Logical command can set and reset this bit.	0

6	AC	RW	Auxiliary carry flag bit. In addition and subtraction operations, if there is a carry or borrow from the higher 4 bits to the lower 4 bits, then AC is set, otherwise it is reset.	0
5	F0	RW	General flag bit 0, accessed by bits. User-defined. Set and reset by software.	0
4	RS1	RW	Register bank selection high bit	0
3	RS0	RW	Register bank selection low bit	0
2	OV	RW	Overflow flag bit. In addition and subtraction operations, if the operation result exceeds 8-bit binary number, OV is set to 1 and the flag overflows, otherwise it is reset.	0
1	F1	RW	General flag bit 1, accessed by bits. User-defined. Set and reset by software.	0
0	P	RO	Parity flag bit. This bit records the parity of '1' in accumulator A after the command is executed. If the number of '1' is an odd number, P is set. If the number of '1' is an even number, P is reset.	0

The state of processor is stored in the program status word register (PSW), and PSW can be accessed by bits. The status word includes the carry flag bit, auxiliary carry flag bit for BCD code processing, parity flag bit, overflow flag bit, as well as RS0 and RS1 for working register bank selection.The area where the working register bank is located can be accessed directly or indirectly.

Table 5.3.2 RS1 and RS0 working register bank selection table

RS1	RS0	Working register bank
0	0	Bank 0 (00h-07h)
0	1	Bank 1 (08h-0Fh)
1	0	Bank 2 (10h-17h)
1	1	Bank 3 (18h-1Fh)

Table 5.3.3 Operations that affect flag bits (X means that the flag bit is related to the operation result)

Operation	CY	OV	AC	Operation	CY	OV	AC
ADD	X	X	X	SETB C	1		
ADDC	X	X	X	CLR C	0		
SUBB	X	X	X	CPL C	X		
MUL	0	X		MOV C, bit	X		
DIV	0	X		ANL C, bit	X		
DA A	X			ANL C,/bit	X		
RRC A	X			ORL C, bit	X		
RLC A	X			ORL C,/bit	X		
CJNE	X						

Data address pointer (DPTR):

Bit	Name	Access	Description	Reset value
[7:0]	DPL	RW	Data pointer low byte	00h

[7:0]	DPH	RW	Data pointer high byte	00h

DPL and DPH constitute a 16-bit data pointer (DPTR), which is used to access xSFR, xBUS, xRAM data memory and program memory. The actual DPTR corresponds to 2 sets of physical 16-bit data pointers, DPTR0 and DPTR1, which are dynamically selected by DPS in XBUS_AUX.

Stack pointer (SP):

Bit	Name	Access	Description	Reset value
[7:0]	SP	RW	Stack pointer, mainly used for program calls and interrupt calls as well as data in and out of the stack	07h

Specific function of stack: protect breakpoint and protect site, and carry out management on the principle of first-in last-out. During instack, SP pointer automatically adds 1, saving the data and breakpoint information. During outstack, SP pointer points to the data unit and automatically substracts 1. The initial value of SP is 07h after reset, and the corresponding default stack storage starts from 08h.

5.4 Special registers

Inverted value of accumulator high bit and low bit (A_INV):

Bit	Name	Access	Description	Reset value
[7:0]	A_INV	RO	Inverted value of accumulator high bit and low bit, result of bit 0 ~ bit 7 in bitwise reverse order. Bit 7 and bit 6 ~ bit 0 of A_INV correspond to bit 0 and bit 1 ~ bit 7 of ACC respectively.	00h

Global configuration register (GLOBAL_CFG), only can be written in safe mode:

Bit	Name	Access	Description	Reset value
[7:6]	Reserved	RO	For CH549, it is the fixed value of 11	11b
[7:6]	Reserved	RO	For CH548, it is the fixed value of 10	10b
5	bBOOT_LOAD	RO	Boot loader state bit, used to distinguish ISP boot loader state or application state: set 1 during power on, cleared to 0 during software reset. For the chip with ISP boot loader, if this bit is 1, it has never been reset by software and it is usually in ISP boot loader running after power on state. If this bit is 0, it has been reset by software, and it is usually in application state.	1
4	bSW_RESET	RW	Software reset control bit. If it is set to 1, software reset occurs. Automatically reset by hardware.	0
3	bCODE_WE	RW	Flash-ROM write enable bit Write protection if this bit is 0. Flash-ROM can be written and erased if this bit is 1	0
2	bDATA_WE	RW	Flash-ROM DataFlash area write enable bit Write protection if this bit is 0. DataFlash area can be written and erased if this bit is 1	0

1	Reserved	RO		0
0	bWDOG_EN	RW	Watchdog reset enable bit If this bit is 0, watchdog is only used as a timer. If this bit is 1, watchdog reset enabled when timing overflows.	0

Chip ID (CHIP_ID):

Bit	Name	Access	Description	Reset value
[7:0]	CHIP_ID	RO	For CH549, always 49h, used to identify the chip	49h
[7:0]	CHIP_ID	RO	For CH548, always 48h, used to identify the chip	48h

Safe mode control register (SAFE_MOD):

Bit	Name	Access	Description	Reset value
[7:0]	SAFE_MOD	WO	Used to enter or terminate safe mode	00h

Some SFRs can only be written in safe mode, while they are always read-only in non-safe mode. Steps for entering safe mode:

(1). Write 55h into this register.

(2). And then write AAh into this register.

(3). After that, they are in safe mode for about 13 to 23 system clock cycles, and one or more safe class SFR or ordinary SFR can be rewritten in such validity period.

(4). Automatically terminate the safe mode after the expiration of the above validity period.

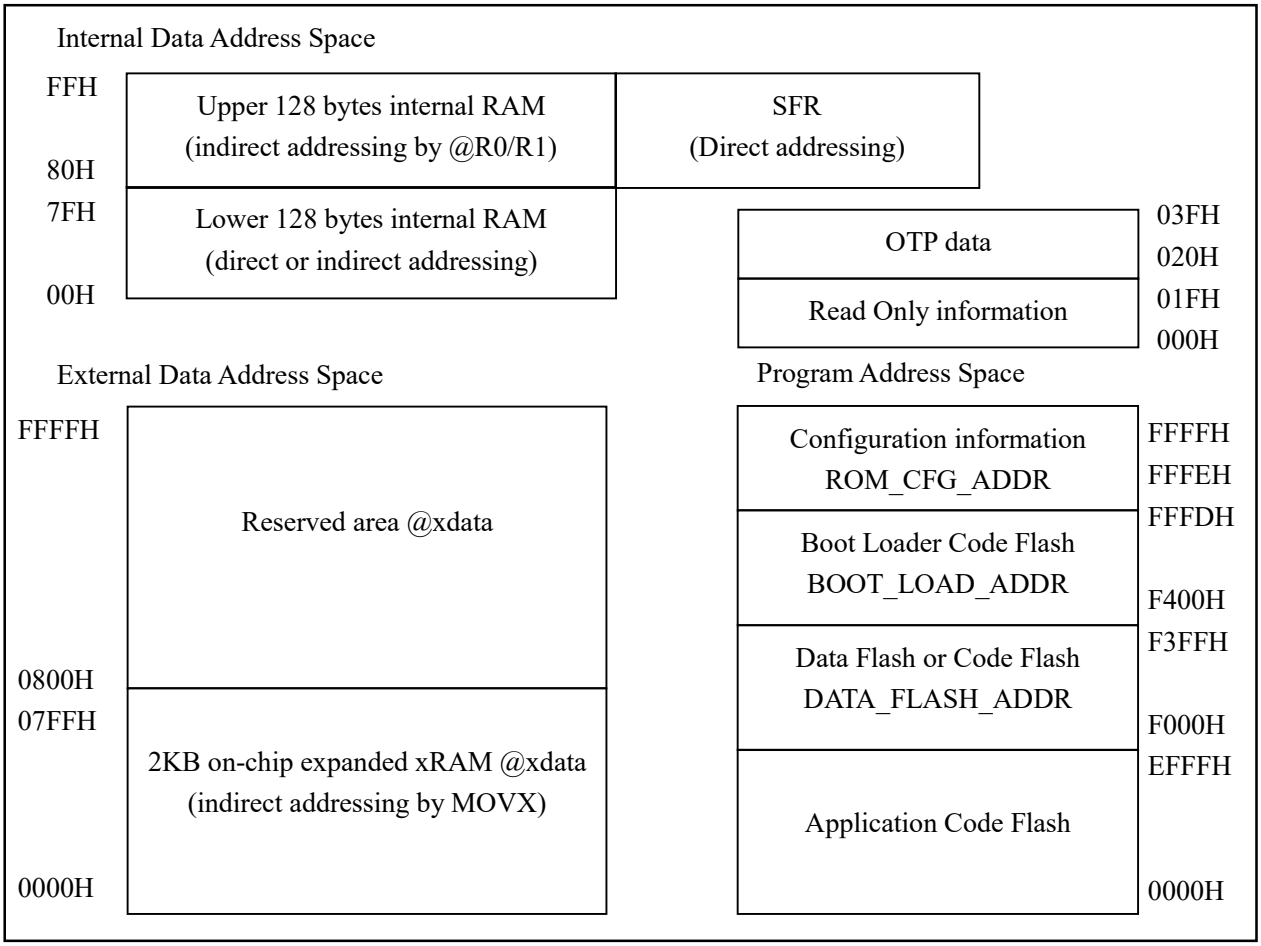
(5). Alternatively, write any value to the register to prematurely terminate safe mode.

6. Register structure

6.1 Register space

CH549 addressing space is divided into program address space, internal data address space and external data address space, read only information and OTP data space.

Figure 6.1 Memory structure



6.2 Program address space

The program address space is 64KB in total, as shown in Figure 6.1, all of which is used for flash-ROM, including the Code Flash area to save the command code, the Data Flash area to save the nonvolatile data, and the Configuration Information area.

Data Flash (EEPROM) address ranges from F000h to F3FFH. It supports single byte read (8 bits), single byte write (8 bits), block write (1 ~ 64 bytes), block erase (64 bytes) operations. The data remains unchanged after power failure of chip, and it can also be used as Code Flash.

Code Flash includes the application code for the low address area and the boot loader code for the high address area, or these two areas and Data Flash may be combined to save a single application code.

For CH548, the application code area of Code Flash is only 32KB.

Configuration Information area has 16 bits of data, which is set by the programmer as required, refer to Table 6.2.

Table 6.2 flash-ROM Configuration Information description

Bit address	Bit name	Description	Recommended value
15	Code_Protect	Code and data protection mode in flash-ROM: 0: Read enabled. 1: Disable the programmer to read, and keep the program secret.	0/1
14	No_Boot_Load	Enable BootLoader start mode: 0: Start from the application from 0000h address; 1: Start from the boot loader from F400h address	1
13	En_Long_Reset	Extra delay reset during enable power on reset: 0: Standard short reset; 1: Wide reset, with extra 44mS reset time added	0
12	En_P5.7_RESET	Enable P5.7 as manual reset input pin: 0: Disabled. 1: RST enabled.	1
11		Reserved	0
10		Reserved	0
9	Must_1	(Automatically set to 1 by the programmer as required)	1
8	Must_0	(Automatically set to 0 by the programmer as required)	0
[7:3]	All_0	(Automatically set to 00000b by the programmer as required)	00000b
[2:0]	LV_RST_VOL (Vpot)	Select the threshold voltage of power supply low voltage detection reset (LVR) module (error 4%): 000/001: Select 2.4V. 010: Select 2.7V. 011: Select 3.0V. 100: Select 3.6V. 101: Select 4.0V. 110: Select 4.3V. 111: Select 4.6V.	000b

6.3 Data address space

The internal data address space, with 256 bytes in total, as shown in Figure 6.1, has been all used for SFR and iRAM, in which iRAM is used for stack and fast temporary data storage, and can be subdivided into the working registers R0-R7, bit variable bdata, byte variable data and idata, etc.

External data storage space is 64KB in total, as shown in Figure 6.1. Except that part of it is used for 2 KB on-chip expanded xRAM, the remaining 0800h to FFFFh addresses are reserved.

Read-only information area and OTP data area each has 32 bytes, as shown in Figure 6.1, and needs to be accessed through a dedicated operation.

6.4 flash-ROM registers

Table 6.4 flash-ROM Operation Register List

Name	Address	Description	Reset value
ROM_DATA_HH	8Fh	High byte of flash-ROM data register high word (read only)	xxh

ROM_DATA_HL	8Eh	Low byte of flash-ROM data register high word (read only)	xxh
ROM_DATA_HI	8Eh	16-bit SFR consists of ROM_DATA_HL and ROM_DATA_HH	xxxxh
ROM_BUF_MOD	8Fh	Buffer mode register for flash-ROM erase/program operation	xxh
ROM_DAT_BUF	8Eh	Data butter register for flash-ROM erase/program operation	xxh
ROM_STATUS	86h	flash-ROM status register (read only)	00h
ROM_CTRL	86h	flash-ROM control register (write only)	00h
ROM_ADDR_H	85h	flash-ROM address register high byte	xxh
ROM_ADDR_L	84h	flash-ROM address register low byte	xxh
ROM_ADDR	84h	16-bit SFR consists of ROM_ADDR_L and ROM_ADDR_H	xxxxh
ROM_DATA_LH	85h	High byte of flash-ROM data register low word (read only)	xxh
ROM_DATA_LL	84h	Low byte of flash-ROM data register low word (read only)	xxh
ROM_DATA_LO	84h	16-bit SFR consists of ROM_DATA_LL and ROM_DATA_LH	xxxxh

flash-ROM address register (ROM_ADDR):

Bit	Name	Access	Description	Reset value
[7:0]	ROM_ADDR_H	RW	flash-ROM address high byte	xxh
[7:0]	ROM_ADDR_L	RW	flash-ROM address low byte	xxh

flash-ROM data register (ROM_DATA_HI, ROM_DATA_LO):

Bit	Name	Access	Description	Reset value
[7:0]	ROM_DATA_HH	RO	High byte of flash-ROM data register high word (16 bits)	xxh
[7:0]	ROM_DATA_HL	RO	Low byte of flash-ROM data register high word (16 bits)	xxh
[7:0]	ROM_DATA_LH	RO	High byte of flash-ROM data register low word (16 bits)	xxh
[7:0]	ROM_DATA_LL	RO	Low byte of flash-ROM data register low word (16 bits)	xxh

Buffer mode register for flash-ROM erase/program operation (ROM_BUF_MOD):

Bit	Name	Access	Description	Reset value
7	bROM_BUF_BYTE	RW	Buffer mode for flash-ROM erase/program operation: 0: Select the data block programming mode, and the data to be written is stored in xRAM pointed to by DPTR. During programming, CH549 will automatically fetch data from xRAM in sequence and temporarily store it in ROM_DAT_BUF and then write	x

			into flash-ROM; support 1-byte to 64-byte data length, and the actual length =MASK_ROM_ADR_END-ROM_ADDR_L[5:0]+1; 1: Select single-byte programming or 64-byte block erase mode, and the data to be written is directly stored in ROM_DAT_BUF	
6	Reserved	RW	Reserved	x
[5:0]	MASK_ROM_ADDR	RW	In flash-ROM data block programming mode, these bits are the lower 6 bits of the end address of the flash-ROM block programming operation (including such address). Reserved in flash-ROM single byte programming or 64-byte erase mode, and recommended to be 00h.	xxh

Data buffer register for flash-ROM erase/program operation (ROM_DAT_BUF):

Bit	Name	Access	Description	Reset value
[7:0]	ROM_DAT_BUF	RW	Data butter register for flash-ROM erase/program operation	xxh

flash-ROM control register (ROM_CTRL):

Bit	Name	Access	Description	Reset value
[7:0]	ROM_CTRL	WO	flash-ROM control register	00h

flash-ROM status register (ROM_STATUS):

Bit	Name	Access	Description	Reset value
7	Reserved	RO	Reserved	1
6	bROM_ADDR_OK	RO	flash-ROM operation address OK status bit: 0: Invalid; 1: Valid	0
[5:2]	Reserved	RO	Reserved	0000b
1	bROM_CMD_ERR	RO	flash-ROM operation command error status bit: 0: The command is valid. 1: Unknown command, or overtime	0
0	Reserved	RO	Reserved	0

6.5 flash-ROM operation steps

1. Erase the flash-ROM, and change all data bits in the target block to 0:
   (1). Enable safe mode: SAFE_MOD = 55h; SAFE_MOD = 0AAh.
   (2). Set GLOBAL_CFG to enable write (bCODE_WE corresponds to code, and bDATA_WE to data).
   (3). Set ROM_ADDR to write a 16-bit target address, actually only the higher 10 bits are valid.

(4). Set ROM_BUF_MOD to 80h, to select 64-byte block erase mode.
(5). Optional, set ROM_DAT_BUF to 00h.
(6). Set ROM_CTRL to 0A6h, to execute block erase operation and the program is automatically suspended during operation.
(7). After the operation is completed, the program resumes running. Read ROM_STATUS to check the status of the operation. If more than one block needs to be erased, repeat steps (3)-(6) and (7). The sequence of step (3), (4), and (5) can be exchanged.
(8). Re-enter the safe mode: SAFE_MOD = 55h; SAFE_MOD = 0AAh.
(9). Set GLOBAL_CFG to start write protection (bCODE_WE=0, bDATA_WE=0).

2. Write flash-ROM in single byte, change some data bits in the target byte from 0 to 1 (the bit data cannot be changed from 1 to 0):
(1). Enable safe mode: SAFE_MOD = 55h; SAFE_MOD = 0AAh.
(2). Set GLOBAL_CFG to enable write (bCODE_WE corresponds to code, and bDATA_WE to data).
(3). Set ROM_ADDR to write a 16-bit target address.
(4). Set ROM_BUF_MOD to 80h, to select byte programming mode.
(5). Set ROM_DAT_BUF to the byte data to be written.
(6). Set ROM_CTRL to 09Ah, to execute write operation, and the program is automatically suspended during operation.
(7). After the operation is completed, the program resumes running. Read ROM_STATUS to check the status of the operation. If more than one block data needs to be written, repeat steps (3)-(6) and (7). The sequence of step (3), (4), and (5) can be exchanged.
(8). Re-enter the safe mode: SAFE_MOD = 55h; SAFE_MOD = 0AAh.
(9). Set GLOBAL_CFG to start write protection (bCODE_WE=0, bDATA_WE=0).

3. Block write flash-ROM, change some data bits in multiple target bytes from 0 to 1 (the bit data cannot be changed from 1 to 0):
(1). Enable safe mode: SAFE_MOD = 55h; SAFE_MOD = 0AAh.
(2). Set GLOBAL_CFG to enable write (bCODE_WE corresponds to code, and bDATA_WE to data).
(3). Set ROM_ADDR to write a 16-bit start target address, for example, 1357h.
(4). Set ROM_BUF_MOD to the lower 6 bits of the end target address (including), and such end address should be greater than or equal to the ROM_ADDR_L[5:0] start target address, select the data block programming mode, for example, if the end address is 1364h, the ROM_BUF_MOD should be set to 24h (64H &3Fh), and the calculated number of bytes of the data block =0Dh.
(5). In the xRAM, allocate a buffer area based on the alignment in 64 bytes, for example 0580h~05BFh, specify the offset address in such buffer area with the lower 6 bits of the starting target address, obtain the xRAM buffer starting address of this data block programming operation, store the data block to be written from the xRAM buffer starting address, and set the xRAM buffer starting address into DPTR, e.g. DPTR=0580h+(57h&3Fh)=0597h, actually only the xRAM of 0597h ~ 05A4h address is used in this programming operation.
(6). Set ROM_CTRL to 09Ah, to execute write operation, and the program is automatically suspended during operation.
(7). After the operation is completed, the program resumes running. Read ROM_STATUS to check the status of the operation. If more than one block data needs to be written, repeat steps (3)-(6) and (7). The sequence of step (3), (4), and (5) can be exchanged.
(8). Re-enter the safe mode: SAFE_MOD = 55h; SAFE_MOD = 0AAh.

(9). Set GLOBAL_CFG to start write protection (bCODE_WE=0, bDATA_WE=0).

4. Read flash-ROM:
   Directly use MOVC command, or read the code or data of the target address through the pointer to the program address space.

5. Write to OTP data area in single byte, change some data bits in the target byte from 0 to 1 (the bit data cannot be changed from 1 to 0):
   (1). Enable safe mode: SAFE_MOD = 55h; SAFE_MOD = 0AAh.
   (2). Set GLOBAL_CFG to enable write (bDATA_WE).
   (3). Set ROM_ADDR to write a target address (20h-3Fh), actually only the higher 4 bits in the lower 6 bits are valid.
   (4). Set ROM_BUF_MOD to 80h, to select byte programming mode;
   (5). Set ROM_DAT_BUF to the byte data to be written;
   (6). Set ROM_CTRL to 099h, to execute write operation, and the program is automatically suspended during operation;
   (7). After the operation is completed, the program resumes running. Read ROM_STATUS to check the status of the operation. If more than one block data needs to be written, repeat steps (3)-(6) and (7). The sequence of step (3), (4), and (5) can be exchanged;
   (8). Re-enter the safe mode: SAFE_MOD = 55h; SAFE_MOD = 0AAh.
   (9). Set GLOBAL_CFG to start write protection (bCODE_WE=0, bDATA_WE=0).

6. Read the ReadOnly information area or OTP data area in 4 bytes:
   (1). Set ROM_ADDR, to write the target address based on the alignment in 4 bytes (00h-3Fh), actually only the lower 6 bits are valid.
   (2). Set ROM_CTRL to 08Dh, to execute read operation, and the program is automatically suspended during operation.
   (3). After the operation is completed, the program resumes running. Read ROM_STATUS to check the status of the operation.
   (4). Obtain 4-byte data from ROM_DATA_HI and ROM_DATA_LO in flash-ROM data register.

7. Notes: it is recommended that flash-ROM/EEPROM is erased/programmed only at the ambient temperature of -20℃ ~ 85℃. If the erase/program operation is performed beyond the above temperature range, it is normal usually, but there may be the possibility of reducing data retention ability TDR and reducing the number of erase/program operations or even affecting the accuracy of data.

6.6 On-board program and ISP download

When Code_Protect=0, the codes and data in CH549 flash-ROM can be read and written by an external programmer through the synchronous serial interface. When Code_Protect=1, the codes and data in the flash-ROM are protected and cannot be read out, but can be erased, and the code protection is removed when the code is erased and powered on again.

When the CH549 is preset with BootLoader program, it supports various ISP downloading types such as USB or UART to load the applications. But in the absence of a boot loader program, the boot loader program or application can only be written to CH549 by an external dedicated programmer. To support on-board programming, 4 connection pins between the CH549 and the programmer should be reserved in

the circuit. The necessary connection pins are P1.4, P1.6 and P1.7.

Table 6.6.1 Connection pins to the programmer

Pin	GPIO	Pin description
RST	P5.7	Reset control pin in programming state (optional). It is allowed to be programmed when at high level.
SCS	P1.4	Chip select input pin in programming state (necessary). It is at high level by default, while active at low level.
SCK	P1.7	Clock input pin in programming state (necessary)
MISO	P1.6	Data output pin in programming state (necessary)

6.7 Unique ID

Each MCU has a unique ID number when it is delivered from the factory, namely the chip identification number. This ID data and its checksum has 8 bytes in total, stored in the read-only information area at 10h offset address, please refer to the C Program Language routines for specific operations.

Table 6.7.1 Chip ID address table

Offset address	ID data description
10h, 11h	ID first word data, correspond to the lowest byte and the second low byte of the ID number in order
12h, 13h	ID secondary word data, correspond to the second high byte and high byte of the ID number in order
14h, 15h	ID last word data, correspond to the second highest byte and the highest byte of the 48-bit ID number in order
16h, 17h	16-bit cumulative sum of ID first word, secondary word, last word data, used for ID check

The ID number can be used with the downloading tools to encrypt the target program. For the general application, only the first 32 bits of the ID number are used.

6.8 Calibration information of temperature sensor (TS)

The calibration information of the temperature sensor is located in the read-only information area at 0Ch offset address. For specific operation, please refer to C Program Language routines.

7. Power control, sleep and reset

7.1 External power input

CH549 has a built-in 5V to 3.3V low dropout voltage regulator (LDO), and the generated 3.3V power supply is used in USB and other modules. CH549 supports external 5V or 3.3V or even 2.8V supply voltage input. Refer to the following table for the two supply voltage input modes.

External supply voltage	VDD voltage: 2.8V to 5V external voltage	V33 voltage: 3.3V internal USB voltage (Notes: V33 is automatically shorted to VDD during sleep)
3.3V or 2.8V including less than 3.6V	Input external 3.3V voltage to I/O and voltage regulator, Must be connected with a decoupling	Short connect VDD input as the internal USB power, Must be connected with a decoupling

	capacitor (not less than 0.1uF) to ground.	capacitor (not less than 0.1uF) to ground.
5V including more than 3.6V	Input external 5V voltage to I/O and voltage regulator, Must be connected with a decoupling capacitor (not less than 0.1uF) to ground.	Internal voltage regulator 3.3V output And 3.3V internal USB power supply input, Must be connected with a decoupling capacitor (not less than 0.1uF) to ground.

After power on or system reset, CH549 is in running state by default. On the premise that the performance meets the requirements, the power consumption can be reduced during operation by appropriately reducing the system clock frequency. When CH549 does not need to be run at all, PD in PCON can be set to enter the sleep state. In the sleep state, external wakeup can be implemented via USB, UART0, UART1, SPI0 and part of GPIO.

7.2 Power supply and sleep control registers

Table 7.2.1 Power supply and sleep control registers

Name	Address	Description	Reset value
WDOG_COUNT	FFh	Watchdog count register	00h
RESET_KEEP	FEh	Reset keep register	00h
POWER_CFG	BAh	Power management configuration register	03h
WAKE_CTRL	A9h	Wakeup control register	00h
PCON	87h	Power control register	10h

Watchdog count register (WDOG_COUNT):

Bit	Name	Access	Description	Reset value
[7:0]	WDOG_COUNT	RW	Current count of watchdog. It overflows when the count is full from 0FFh to 00h, and the bWDOG_IF_TO interrupt flag is automatically set to 1 during overflow.	00h

Reset keep register (RESET_KEEP):

Bit	Name	Access	Description	Reset value
[7:0]	RESET_KEEP	RW	Reset keep register. The value can be modified manually and will not be affected by any other reset except for power on reset	00h

Power management configuration register (POWER_CFG), only can be written in safe mode:

Bit	Name	Access	Description	Reset value
7	bPWR_DN_MODE	RW	Select sleep power down mode: 0: Select the power-down/deep-sleep mode. It can save more power but wake up slowly. 1: Select Standby/normal Sleep mode. It can wake up	0

			quickly.	
6	bUSB_PU_RES	RW	Select the resistance value of the USB pull-up resistor: 0: 1.5KΩ, used when V33 is 3.3V. 1: 7KΩ, used when V33 is 5V	0
5	bLV_RST_OFF	RW	Low voltage reset detection module OFF control 0: Supply voltage detection ON, and reset signal is generated when at low voltage. 1: Low voltage detection OFF.	0
4	bLDO_3V3_OFF	RW	LDO OFF control (auto OFF during sleep): 0: 3.3V voltage is generated by VDD for USB and other modules. 1: LDO OFF, and V33 is internally shorted to VDD.	0
3	bLDO_CORE_VOL	RW	Core voltage mode: 0: Normal voltage mode. 1: Boost voltage mode, which has better performance and support higher clock frequency	0
[2:0]	MASK_ULLDO_VOL	RW	Data retention supply voltage selection in power down/deep sleep mode: 000: 2.0V. 001: 1.9V. 010: 1.8V. 011: 1.7V. 100: 1.6V. 101: 1.5V. 110: 1.4V. 111: 1.3V.	011b

Wakeup control register (WAKE_CTRL), only can be written in safe mode:

Bit	Name	Access	Description	Reset value
7	bWAK_BY_USB	RW	USB event wakeup enable Wakeup is disabled if the bit is 0.	0
6	bWAK_RXD1_LO	RW	UART1 receive input low level wakeup enable Wakeup is disabled if the bit is 0. Select either RXD1 or RXD1_ based on bUART1_PIN_X=0/1	0
5	bWAK_P1_5_LO	RW	P1.5 low level wakeup enable Wakeup is disabled if the bit is 0.	0
4	bWAK_P1_4_LO	RW	P1.4 low level wakeup enable Wakeup is disabled if the bit is 0.	0
3	bWAK_P0_3_LO	RW	P0.3 low level wakeup enable Wakeup is disabled if the bit is 0.	0
2	bWAK_P57H_INT3L	RW	P5.7 high level and INT3 low level wakeup enable Wakeup is disabled if the bit is 0.	0
1	bWAK_INT0E_P33L	RW	INT0 edge change and P3.3 low level wakeup enable Wakeup is disabled if the bit is 0. Select either INT0 or INT0_ pin based on bINT0_PIN_X=0/1	0
0	bWAK_RXD0_LO	RW	UART0 receive input low level wakeup enable	0

			Wakeup is disabled if the bit is 0. Select either RXD0 or RXD0_ pin based on bUART0_PIN_X=0/1	

Voltage comparator wakeup enable is controlled by bCMP_EN. When bCMP_EN is 1, it automatically wakes up if the comparator result changes.

Power control register (PCON):

Bit	Name	Access	Description	Reset value
7	SMOD	RW	When the UART0 baud rate is generated by timer 1, select the communication baud rate of UART0 mode1/2/3: 0-slow mode; 1-fast mode	0
6	Reserved	RO	Reserved	0
5	bRST_FLAG1	RO	Last reset flag high bit	0
4	bRST_FLAG0	RO	Last reset flag low bit	1
3	GF1	RW	General flag bit 1 User-defined. Reset and set by software.	0
2	GF0	RW	General flag bit 0 User-defined. Reset and set by software.	0
1	PD	RW	Sleep mode enable Sleep after set to 1. Automatically reset by hardware after wakeup. It is strongly recommended to disable the global interrupt before sleep (EA=0).	0
0	Reserved	RO	Reserved	0

Table 7.2.2 Last reset flag description

bRST_FLAG1	bRST_FLAG0	Reset flag description
0	0	Software reset Source: bSW_RESET=1 and (bBOOT_LOAD=0 or bWDOG_EN=1)
0	1	Power on reset or low voltage detection reset Source: voltage on VDD pin is lower than detection level.
1	0	Watchdog reset Source: bWDOG_EN=1 and watchdog timeout overflows.
1	1	External pin manual reset Source: En_P5.7_RESET=1 and P5.7 input high level.

7.3 Reset control

CH549 has 5 reset sources: power on reset, power supply low voltage detection reset, external reset, software reset, and watchdog reset. The last three are thermal resets.

7.3.1 Power on reset and power supply low voltage reset

The power on reset (POR) is generated by the on-chip power on detection circuit. Automatically delay Tpor through hardware to keep reset. After the delay, the CH549 will run.

Low voltage reset (LVR) is generated by the on-chip voltage detection circuit. The LVR circuit continuously monitors the supply voltage of VDD pin. When it is lower than the detection level (Vpot), the low voltage reset is generated. Automatically delay Tpor through hardware to keep reset. After the delay, the CH549 will run.

Only power on reset and low voltage reset can enable CH549 to reload the configuration information and reset RESET_KEEP, other thermal resets do not affect it.

7.3.2 External reset

The external reset is generated by the high level applied to the RST pin. The reset process is triggered when En_P5.7_RESET is 1, and the high level duration on the RST pin is greater than Trst. When the external high level signal is canceled, the hardware will automatically delay Trdl to remain the reset state. After the delay, CH549 will be executed from address 0.

7.3.3 Software reset

CH549 supports internal software reset, so that the CPU can be actively reset and re-run without external intervention. Set bSW_RESET in the global configuration register (GLOBAL_CFG) to 1 to reset the software, and automatically delay Trdl to remain the reset state. After the delay, CH549 executes from address 0, and the bSW_RESET bit is reset automatically by hardware.

When bSW_RESET is set to 1, if bBOOT_LOAD=0 or bWDOG_EN=1, then bRST_FLAG1/0 after reset indicates a software reset. When bSW_RESET is set to 1, if bBOOT_LOAD=1 and bWDOG_EN=0, then bRST_FLAG1/0 remains the previous reset flag rather than generate a new one.

For a chip with ISP boot loader, after power on reset, the boot loader runs first, and program will reset the chip via software as needed to switch to the application state. Such software reset only cause bBOOT_LOAD reset, and do not affect bRST_FLAG1/0 state (due to bBOOT_LOAD = 1 before reset), so when switching to the application state, bRST_FLAG1/0 still indicates power on reset state.

7.3.4 Watchdog reset

Watchdog reset is generated when the watchdog timer overflows. The watchdog timer is an 8-bit counter, whose clock frequency of its counts is Fsys/131072, and the overflow signal is generated when the count reaches 0FFh to 00h.

The watchdog timer overflow signal triggers the interrupt flag (bWDOG_IF_TO) to 1, automatically reset when WDOG_COUNT is reloaded or entering the corresponding interrupt service program.

Different timing cycles (Twdc) are achieved by writing different count initial values to WDOG_COUNT. When system clock frequency is 12MHz, the watchdog timing cycle (Twdc) is about 2.8 s when 00h is written, and about 1.4 s when 80h is written.

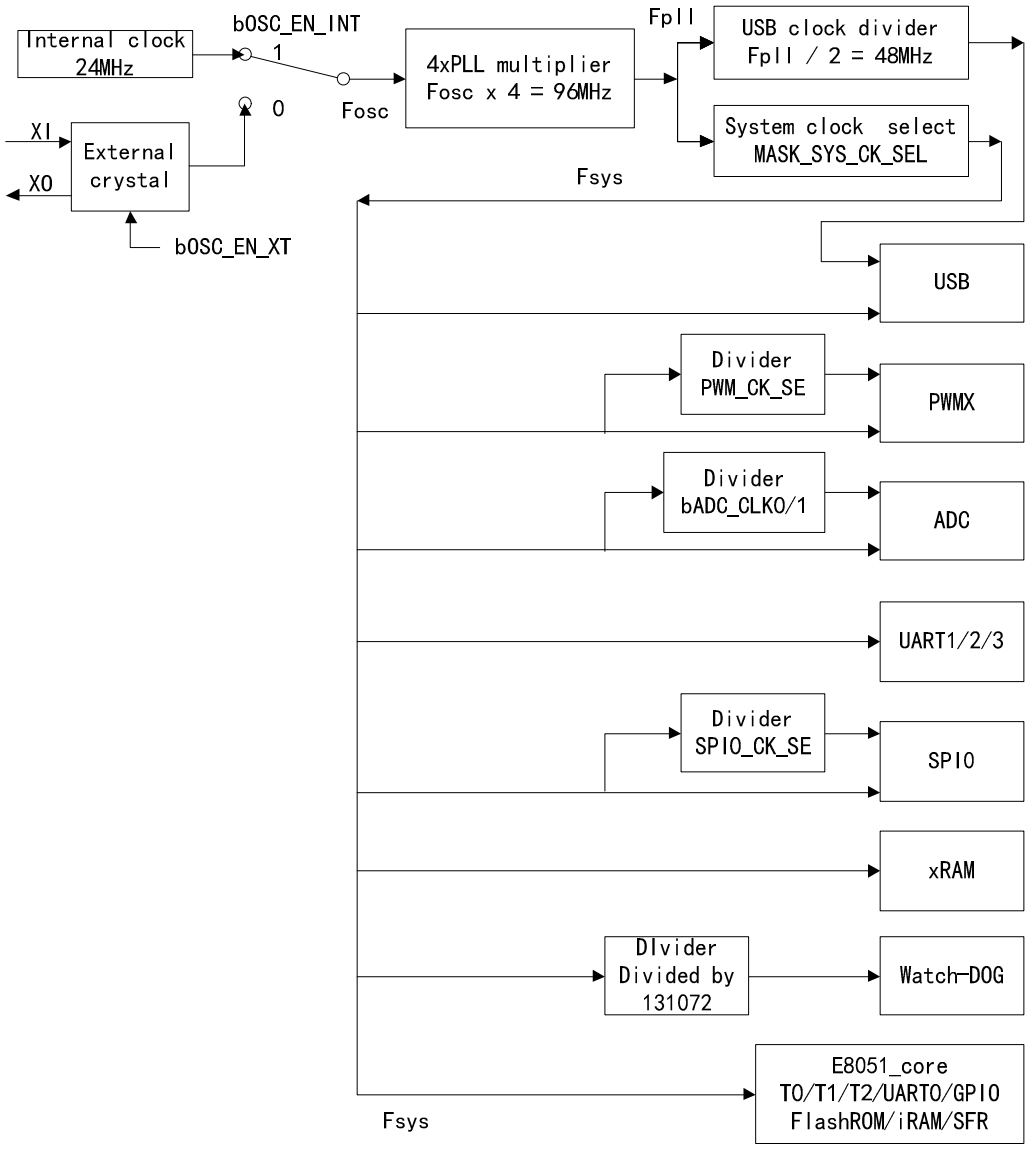
If bWDOG_EN=1 when watchdog timer overflows, watchdog reset is generated and automatically delay Trdl to keep reset. After the delay, CH549 executes from address 0.

When bWDOG_EN=1, to avoid watchdog reset, WDOG_COUNT must be reset timely to avoid its overflow.

8. System clock

8.1 Clock block diagram

Figure 8.1.1 Clock system and structure diagram



After the internal clock or external clock is alternatively selected as the original clock (Fosc), Fpll high frequency clock is generated after PLL multiplier, and finally the system clock (Fsys) and USB module clock (Fusb4x) are respectively obtained via the 2 groups of dividers. The system clock frequency is directly provided for each module of CH549.

8.2 Register description

Table 8.2.1 Clock control register

Name	Address	Description	Reset value
CLOCK_CFG	B9h	System clock configuration register	83h

System clock configuration register (CLOCK_CFG), only can be written in safe mode:

Bit	Name	Access	Description	Reset value
7	bOSC_EN_INT	RW	Internal clock oscillator enable 1: Enable the internal clock oscillator and select the internal clock. 0: Disable the internal clock oscillator and select the external crystal oscillator to provide the clock.	1
6	bOSC_EN_XT	RW	External crystal oscillator enable 1: The P4.6/XO pin is used as XI/XO and the oscillator is enabled. A quartz crystal or ceramic oscillator needs to be externally connected between the XI and XO. 0: Disable the external oscillator.	0
5	bWDOG_IF_TO	RO	Watch dog timer interrupt flag. 1: Interrupt triggered by the timer overflow signal. 0: No interrupt. This bit is automatically reset when the watchdog count register (WDOG_COUNT) is reloaded or after it enters the corresponding interrupt service program.	0
[4:3]	Reserved	RO	Reserved	00b
[2:0]	MASK_SYS_CK_SEL	RW	System clock select. Refer to the Table 8.2.2	011b

Table 8.2.2 System clock frequency selection

MASK_SYS_CK_SEL	System clock frequency (Fsys)	Relation with crystal frequency (Fxt)	Fsys when Fosc=24MHz
000b	Fpll / 512	Fxt / 128	187.5KHz
001b	Fpll / 128	Fxt / 32	750KHz
010b	Fpll / 32	Fxt / 8	3MHz
011b	Fpll / 8	Fxt / 2	12MHz
100b	Fpll / 6	Fxt / 1.5	16MHz
101b	Fpll / 4	Fxt / 1	24MHz
110b	Fpll / 3	Fxt / 0.75	32MHz
111b	Fpll / 2	Fxt / 0.5	48MHz

8.3 Clock configuration

The internal clock is used by default after the CH549 is powered on, and the internal clock frequency is 24MHz. Select either an internal clock or an external crystal oscillator clock through CLOCK_CFG. If the external crystal oscillator is disabled, the XI pins can be selectd as P4.6 general-purpose I/O port. If an external crystal oscillator is used to provide the clock, the crystal should be cross connected between the XI and XO pins, and the oscillating capacitors should be connected to GND with the XI and XO pins respectively. If the clock signal is input directly from the outside, it should be input from the XI pin with the XO pin suspended.

Original clock frequency: Fosc = bOSC_EN_INT ? 24MHz: Fxt

PLL frequency: Fpll = Fosc * 4
USB clock frequency: Fusb4x = Fpll / 2
The system clock frequency is obtained by Fpll division as shown in Table 8.2.2.
In default state after reset, Fosc=24MHz, Fpll=96MHz, Fusb4x=48MHz, and Fsys=12MHz.

Steps for switching to the external crystal oscillator to provide the clock are as follows:
(1). Enter the safe mode: step one SAFE_MOD = 55h; step two SAFE_MOD = AAh.
(2). Set bOSC_EN_XT in CLOCK_CFG to 1 with "OR" operation, other bits remain unchanged, to enable crystal oscillator.
(3). Delay several milliseconds, usually 5mS ~ 10mS, to wait for the crystal oscillator to work steadily.
(4). Re-enter the safe mode: step one SAFE_MOD = 55h; step two SAFE_MOD = AAh.
(5). Reset bOSC_EN_INT in CLOCK_CFG to 0 with "AND" operation, other bits remain unchanged, to switch to external clock.
(6). Terminate safe mode: write any value into SAFE_MOD to prematurely terminate the safe mode.

Steps for modifying the system clock frequency are as follows:
(1). Enter the safe mode: step one SAFE_MOD = 55h; step two SAFE_MOD = AAh.
(2). Write new value to CLOCK_CFG.
(3). Terminate safe mode: write any value into SAFE_MOD to prematurely terminate the safe mode.

Notes:
(1). If the USB module is used, the Fusb4x must be 48MHz. In addition, when the full-speed USB is used, the Fsys is not less than 6 MHz. When the low speed USB is used, the Fsys is not less than 1.5 MHz.
(2). A lower system clock frequency (Fsys) is preferred to be used to reduce the system dynamic power consumption and widen the operating temperature range.

9. Interrupt

CH549 supports 16 interrupt signal sources, including 6 interrupts (INT0, T0, INT1, T1, UART0 and T2) compatible with the standard MCS51, and 10 extended interrupts (SPI0, INT3, USB, ADC/UART2, UART1, PWMX/UART3, GPIO and WDOG). The GPIO interrupt can be selected from 7 I/O pins.

Interrupt service programs are advised to be as compact as possible, to avoid calling functions and subroutines as well as reading and writing xdata variables and code constants.

9.1 Register description

Table 9.1.1 Interrupt vector table

Interrupt source	Entry address	Interrupt No.	Description	Default priority sequence
INT_NO_INT0	0x0003	0	External interrupt 0	High priority
INT_NO_TMR0	0x000B	1	Timer0 interrupt	↓
INT_NO_INT1	0x0013	2	External interrupt 1	↓
INT_NO_TMR1	0x001B	3	Timer1 interrupt	↓
INT_NO_UART0	0x0023	4	UART0 interrupt	↓
INT_NO_TMR2	0x002B	5	Timer2 interrupt	↓

INT_NO_SPI0	0x0033	6	SPI0 interrupt	↓
INT_NO_INT3	0x003B	7	External interrupt 3	↓
INT_NO_USB	0x0043	8	USB interrupt	↓
INT_NO_ADC INT_NO_UART2	0x004B	9	ADC interrupt (when bU2IE=0); UART2 interrupt (when bU2IE=1)	↓
INT_NO_UART1	0x0053	10	UART1 interrupt	↓
INT_NO_PWMX INT_NO_UART3	0x005B	11	PWMX interrupt (when bU3IE=0); UART3 interrupt (when bU3IE=1)	↓
INT_NO_GPIO	0x0063	12	GPIO Interrupt	↓ Low priority
INT_NO_WDOG	0x006B	13	Watchdog timer interrupt	

Table 9.1.2 Interrupt registers

Name	Address	Description	Reset value
IP_EX	E9h	Extend interrupt priority control register	00h
IE_EX	E8h	Extend interrupt enable register	00h
GPIO_IE	CFh	GPIO interrupt enable register	00h
IP	B8h	Interrupt priority control register	00h
INTX	B3h	Extend external interrupt control register	00h
IE	A8h	Interrupt enable register	00h

Interrupt enable register (IE):

Bit	Name	Access	Description	Reset value
7	EA	RW	Global interrupt enable bit 1: Interrupt enabled when E_DIS is 0; 0: All interrupts requests are masked.	0
6	E_DIS	RW	Global interrupt disable bit 1: All interrupts requests are masked. 0: Interrupt enabled when EA is 1. This bit is usually used to disable interrupt temporarily during flash-ROM operation	0
5	ET2	RW	Timer 2 interrupt enable bit 1: T2 interrupt enabled. 0: Interrupt request is masked.	0
4	ES	RW	UART0 interrupt enable bit 1: UART0 interrupt enabled. 0: Interrupt request is masked.	0
3	ET1	RW	Timer 1 interrupt enable bit 1: T1 interrupt enabled. 0: Interrupt request is masked.	0
2	EX1	RW	External interrupt 1 enable bit 1: INT1 interrupt enabled. 0: Interrupt request is masked.	0
1	ET0	RW	Timer 0 interrupt enable bit	0

			1: T0 interrupt enabled. 0: Interrupt request is masked.	
0	EX0	RW	External interrupt 0 enable bit 1: INT0 interrupt enabled. 0: Interrupt request is masked.	0

Extend interrupt enable register (IE_EX):

Bit	Name	Access	Description	Reset value
7	IE_WDOG	RW	Watchdog timer interrupt enable bit 1: WDOG interrupt enabled. 0: Interrupt request is masked.	0
6	IE_GPIO	RW	GPIO interrupt enable bit 1: Interrupt in GPIO_IE enabled. 0: All interrupts in GPIO_IE are masked.	0
5	IE_PWMX IE_UART3	RW	PWMX interrupt enable bit when bU3IE=0 1: PWMX interrupt enabled. 0: PWMX interrupt disabled. UART3 interrupt enable bit when bU3IE=1 1: UART3 interrupt enabled. 0: UART3 interrupt disabled.	0
4	IE_UART1	RW	UART1 interrupt enable bit 1: UART1 interrupt enabled. 0: Interrupt request is masked.	0
3	IE_ADC IE_UART2	RW	ADC interrupt enable bit when bU2IE=0 1: ADC interrupt enabled. 0: ADC interrupt disabled. UART2 interrupt enable bit when bU2IE=1 1: UART2 interrupt enabled. 0: UART2 interrupt disabled.	0
2	IE_USB	RW	USB interrupt enable bit 1: USB interrupt enabled. 0: Interrupt request is masked.	0
1	IE_INT3	RW	External interrupt3 enable bit 1: INT3 interrupt enabled. 0: Interrupt request is masked.	0
0	IE_SPI0	RW	SPI0 interrupt enable bit 1: SPI0 interrupt enabled. 0: Interrupt request is masked.	0

GPIO interrupt enable register (GPIO_IE):

Bit	Name	Access	Description	Reset value
7	bIE_IO_EDGE	RW	GPIO edge interrupt mode enable: 0: Level interrupt mode selected. If the GPIO pin inputs a valid level, bIO_INT_ACT is 1 and always requests interrupt. If GPIO inputs an invalid level, bIO_INT_ACT is 0 and the interrupt request is canceled.	0

			1: Edge interrupt mode selected. When GPIO pin inputs a valid edge, the bIO_INT_ACT interrupt flag is generated and an interrupt is requested. The interrupt flag cannot be cleared by software and can only be cleared automatically when reset or in level interrupt mode or when it enters the corresponding interrupt service program.	
6	bIE_RXD1_LO	RW	1: UART1 receive pin interrupt enabled (active at low level in level mode, while active at falling edge in edge mode). 0: UART1 receive pin interrupt disabled. Select either RXD1 or RXD1_ based on bUART1_PIN_X=0/1	0
5	bIE_P1_5_LO	RW	1: P1.5 interrupt enabled (active at low level in level mode, while active at falling edge in edge mode). 0: P1.5 interrupt disabled.	0
4	bIE_P1_4_LO	RW	1: P1.4 interrupt enabled (active at low level in level mode, while active at falling edge in edge mode). 0: P1.4 interrupt disabled.	0
3	bIE_P0_3_LO	RW	1: P0.3 interrupt enabled (active at low level in level mode, while active at falling edge in edge mode). 0: P0.3 interrupt disabled.	0
2	bIE_P5_7_HI	RW	1: P5.7 interrupt enabled (active at low level in level mode, while active at falling edge in edge mode). 0: P5.7 interrupt disabled.	0
1	bIE_P4_6_LO	RW	1: P4.6 interrupt enabled (active at low level in level mode, while active at falling edge in edge mode). 0: P4.6 interrupt disabled.	0
0	bIE_RXD0_LO	RW	1: UART0 receive pin interrupt enabled (active at low level in level mode, while active at falling edge in edge mode). 0: UART0 receive pin interrupt disabled. Select either RXD0 or RXD0_ pin based on bUART0_PIN_X=0/1	0

Extend external interrupt control register (INTX):

Bit	Name	Access	Description	Reset value
7	Reserved	RO	Reserved	0
6	Reserved	RO	Reserved	0
5	bIX3	RW	Input signal polarity of INT3 0: Select default polarity (low level or falling edge trigger). 1: Select reverse polarity (high level or rising edge trigger)	0
4	Reserved	RO	Reserved	0
3	bIE3	RW	INT3 interrupt request flag bit. Reset automatically after it enters interrupt	0
2	bIT3	RW	Trigger mode control bit of INT3	0

			0: Select low or high level trigger for external interrupt. 1: Select falling or rising edge trigger for external interrupt	
1	Reserved	RO	Reserved	0
0	Reserved	RO	Reserved	0

Interrupt priority control register (IP):

Bit	Name	Access	Description	Reset value
7	PH_FLAG	RO	Flag bit for high-priority interrupt in progress	0
6	PL_FLAG	RO	Flag bit for low-priority interrupt in progress	0
5	PT2	RW	Timer2 interrupt priority control bit	0
4	PS	RW	UART0 interrupt priority control bit	0
3	PT1	RW	Timer1 interrupt priority control bit	0
2	PX1	RW	External interrupt 1 interrupt priority control bit	0
1	PT0	RW	Timer0 interrupt priority control bit	0
0	PX0	RW	External interrupt 0 interrupt priority control bit	0

Extend interrupt priority control register (IP_EX):

Bit	Name	Access	Description	Reset value
7	bIP_LEVEL	RO	Current interrupt nesting level flag bit 0: No interrupt, or 2-level nested interrupt. 1: Current 1-level nested interrupt.	0
6	bIP_GPIO	RW	GPIO interrupt priority control bit	0
5	bIP_PWMX bIP_UART3	RW	PWMX interrupt priority control bit when bU3IE=0. UART3 interrupt priority control bit when bU3IE=1	0
4	bIP_UART1	RW	UART1 interrupt priority control bit	0
3	bIP_ADC bIP_UART2	RW	ADC interrupt priority control bit when bU2IE=0. UART2 interrupt priority control bit when bU2IE=1.	0
2	bIP_USB	RW	USB interrupt priority control bit	0
1	bIP_INT3	RW	External interrupt 3 interrupt priority control bit	0
0	bIP_SPI0	RW	SPI0 interrupt priority control bit	0

IP and IP_EX registers are used to set the interrupt priority. If a bit is set to 1, then the corresponding interrupt source is set to high-priority. If a bit is reset, then the corresponding interrupt source is set to low-priority. For the interrupt sources at the same level, the system has a priority sequence by default, as shown in Table 9.1.1. The combination of PH_FLAG and PL_FLAG represents the priority of interrupts.

Table 9.1.3 Current interrupt priority state

PH_FLAG	PL_FLAG	Interrupt priority state at present
0	0	No interrupt at present
0	1	Low-priority interrupt is executed at present
1	0	High-priority interrupt is executed at present
1	1	Unexpected state, unknown error

10. I/O ports

10.1 GPIO introduction

CH549 provides up to 44 I/O pins, some of which have alternate functions. Among them, the inputs and outputs of P0~P4 ports can be accessed by bits.

If the pin is not configured with alternate functions, it is a general-purpose I/O pin by default. When used as general-purpose digital I/O ports, all of them have a real "read-modify-write" function that allows SETB, CLR and other bit operation commands to independently change the direction and port level of a pin.

10.2 GPIO register

All registers and bits in this section are represented in a generic format: a lowercase "n" represents the serial number of the ports (n=0, 1, 2, 3, 4)), and a lowercase "x" represents the serial number of the bits (x=0, 1, 2, 3, 4, 5, 6, 7).

Table 10.2.1 GPIO registers

Name	Address	Description	Reset value
P0	80h	Port0 input/output register	FFh
P0_DIR_PU	C5h	Port0 direction control and pull-up enable register	FFh
P0_MOD_OC	C4h	Port0 output mode register	FFh
P1	90h	Port1 input/output register	FFh
P1_DIR_PU	93h	Port1 direction control and pull-up enable register	FFh
P1_MOD_OC	92h	Port1 output mode register	FFh
P2	A0h	Port2 input/output register	FFh
P2_DIR_PU	95h	Port2 direction control and pull-up enable register	FFh
P2_MOD_OC	94h	Port2 output mode register	FFh
P3	B0h	Port3 input/output register	FFh
P3_DIR_PU	97h	Port3 direction control and pull-up enable register	FFh
P3_MOD_OC	96h	Port3 output mode register	FFh
P4	C0h	Port4 input/output register	FFh
P4_DIR_PU	C3h	Port4 direction control and pull-up enable register	FFh
P4_MOD_OC	C2h	Port4 output mode register	FFh
P5	ABh	Port5 input/output register	20h
PIN_FUNC	AAh	Pin function select register	00h
XBUS_AUX	A2h	Bus auxiliary set register	00h

Pn port input and output register (Pn):

Bit	Name	Access	Description	Reset value
[7:0]	Pn.0~Pn.7	RW	Pn.x pin state input and data output bits, accessed by bits. Note: P4.7 is the internal bit, must be set to 1 for write operation, and is meaningless for read operation.	FFh

Pn port output mode register (Pn_MOD_OC):

Bit	Name	Access	Description	Reset value
[7:0]	Pn_MOD_OC	RW	Pn.x pin output mode set: 0: Push-pull output. 1: Open-drain output.	FFh

Pn port direction control and pull-up enable register (Pn_DIR_PU):

Bit	Name	Access	Description	Reset value
[7:0]	Pn_DIR_PU	RW	Pn.x pin direction control in push-pull output mode: 0: Input. 1: Output. Pn.x pin pull-up resistor enable control in open-drain output mode: 0: Pull-up resistor disabled. 1: Pull-up resistor enabled.	FFh

Relevant configuration of Pn port is implemented by the combination of Pn_MOD_OC[x] and Pn_DIR_PU[x] as follows.

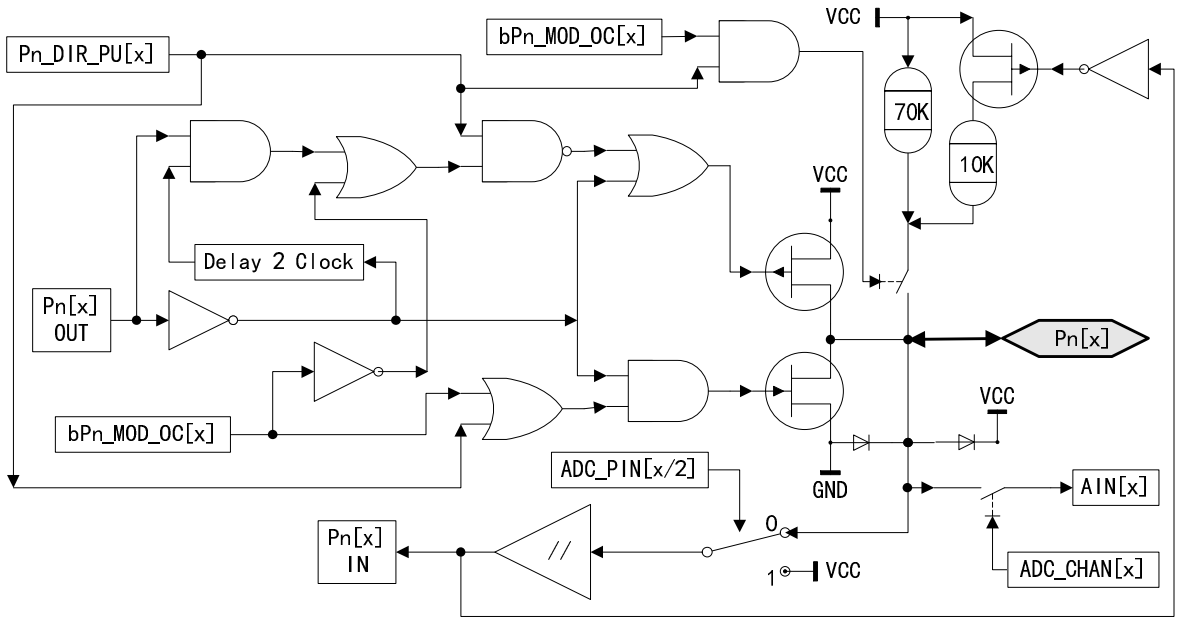
Table 10.2.2 Combination of port configuration registers

Pn_MOD_OC	Pn_DIR_PU	Working mode description
0	0	High impedance input mode, pin has no pull-up resistor
0	1	Push-pull output mode, has symmetrical drive capability which can output or absorb large current
1	0	Open-drain output, support high impedance input, pin has no pull-up resistor
1	1	Quasi-bidirectional mode (standard 8051), open-drain output, support input, pin has pull-up resistor, when the output is changed from low level to high level, it will automatically drive the high level of 2 clock cycles to accelerate the conversion

The P1~P4 ports support pure input, push-pull output and quasi-bidirectional modes, etc.. Each pin has a freely controlled internal pull-up resistor, and a protective diode connected to VDD and GND.

Figure 10.2.1 shows the schematic diagram of the P0.x pin of P0 port and the P1.x pin of P1 port. If AIN, ADC_PIN and ADC_CHAN are removed, it can be applied to P2, P3 and P4 ports.

Figure 10.2.1 I/O pin schematic diagram



P5 port input/output register (P5):

Bit	Name	Access	Description	Reset value
7	P5.7	RO	P5.7 pin state input bit	0
6	Reserved	RO	Reserved	0
5	P5.5	RW	P5.5 pin data output bit (open-drain output, support high voltage): 0: Output low level. 1: No output (high impedance, support external pull-up resistor)	1
4	P5.4	RW	P5.4 pin data output bit: 0: Output low level. 1: Output high level.	0
3	Reserved	RO	Reserved	0
2	Reserved	RO	Reserved	0
1	P5.1	RO	P5.1 pin state input bit, built-in controllable pull-down resistor	0
0	P5.0	RO	P5.0 pin state input bit, built-in controllable pull-down resistor	0

10.3 GPIO alternate functions and map

Some I/O pins of CH549 have alternate functions. After power on, they are all general-purpose I/O pins by default. After different functional modules are enabled, the corresponding pins are configured as corresponding functional pins of each functional module.

Pin function select register (PIN_FUNC):

Bit	Name	Access	Description	Reset value
7	bPWM0_PIN_X	RW	PWM0 pin mapping enable bit 0: P2.5. 1: P1.5.	0

6	bIO_INT_ACT	RO	GPIO interrupt request activation status: When bIE_IO_EDGE=0: 1: GPIO inputs valid level and interrupts the request. 0: Input level invalid. When bIE_IO_EDGE=1, the bit is used as the edge interrupt flag: 1: Effective edge is detected and the bit cannot be cleared by software and can only be cleared automatically in reset or level interrupt mode or when entering the corresponding interrupt service program	0
5	bUART1_PIN_X	RW	UART1 pin mapping enable bit 0: P2.6/P2.7 for RXD1/TXD1. 1: P1.6/P1.7 for RXD1/TXD1.	0
4	bUART0_PIN_X	RW	UART0 pin mapping enable bit 0: P3.0/P3.1 for RXD0/TXD0. 1: P0.2/P0.3 for RXD0/TXD0.	0
3	Reserved	RO	Reserved	0
2	bINT0_PIN_X	RW	INT0 pin mapping enable bit 0: P3.2. 1: P2.2.	0
1	bT2EX_PIN_X	RW	T2EX/CAP2 pin mapping enable bit 0: P1.1. 1: P2.5.	0
0	bT2_PIN_X	RW	T2/CAP1 pin mapping enable bit 0: P1.0. 1: P2.4	0

Table 10.3.1 GPIO alternate functions

GPIO	Other functions: priority sequence from left to right
P0[0]	AIN8, P0.0
P0[1]	AIN9, P0.1
P0[2]	RXD_/bRXD_, AIN10, P0.2
P0[3]	TXD_/bTXD_, AIN11, P0.3
P0[4]	RXD2/bRXD2, AIN12, P0.4
P0[5]	TXD2/bTXD2, AIN13, P0.5
P0[6]	RXD3/bRXD3, AIN14, P0.6
P0[7]	TXD3/bTXD3, AIN15, P0.7
P1[0]	T2/bT2, CAP1/bCAP1, AIN0, P1.0
P1[1]	T2EX/bT2EX, CAP2/bCAP2, AIN1, P1.1
P1[2]	AIN2, P1.2
P1[3]	AIN3, P1.3
P1[4]	SCS/bSCS, UCC1/bUCC1, AIN4, P1.4
P1[5]	MOSI/bMOSI, PWM0_/bPWM0_, UCC2/bUCC2, AIN5, P1.5
P1[6]	MISO/bMISO, RXD1_/bRXD1_, VBUS/bVBUS, AIN6, P1.6
P1[7]	SCK/bSCK, TXD1_/bTXD1_, AIN7, P1.7
P2[0]	PWM5/bPWM5, P2.0
P2[1]	PWM4/bPWM4, P2.1

P2[2]	PWM3/bPWM3, INT0_/bINT0, P2.2
P2[3]	PWM2/bPWM2, P2.3
P2[4]	PWM1/bPWM1, T2_/bT2_, CAP1_/bCAP1_, P2.4
P2[5]	PWM0/bPWM0, T2EX_/bT2EX_, CAP2_/bCAP2_, P2.5
P2[6]	PWM6/bPWM6, RXD1/bRXD1, P2.6
P2[7]	PWM7/bPWM7, TXD1/bTXD1, P2.7
P3[0]	RXD/bRXD, P3.0
P3[1]	TXD/bTXD, P3.1
P3[2]	INT0/bINT0, P3.2
P3[3]	INT1/bINT1, P3.3
P3[4]	T0/bT0, P3.4
P3[5]	T1/bT1, P3.5
P3[6]	CAP0/bCAP0, P3.6
P3[7]	INT3/bINT3, P3.7
P4[0]	P4.0
P4[1]	P4.1
P4[2]	P4.2
P4[3]	P4.3
P4[4]	P4.4
P4[5]	P4.5
P4[6]	XI, P4.6
P5[0]	UDM/bUDM, P5.0
P5[1]	UDP/bUDP, P5.1
P5[4]	bALE/bCKO, P5.4
P5[5]	bHVOD, P5.5
P5[7]	RST/bRST, P5.7

The priority sequence from left to right mentioned in the above table refers to the priority when multiple functional modules compete to use the GPIO. For example, port P2.6/P2.7 is set for UART1, if only RXD1 is needed, then P2.7 can still be used for the functions of PWM7 with higher priority.

11. External bus (xBUS)

CH549 does not provide bus signals for the external, does not support the external bus, but can normally access the on-chip xRAM.

External bus auxiliary set register (XBUS_AUX):

Bit	Name	Access	Description	Reset value
7	bUART0_TX	RO	UART0 transmit status If this bit is 1, the transmission is in progress.	0
6	bUART0_RX	RO	UART0 receive status If this bit is 1, the reception is in progress.	0
5	bSAFE_MOD_ACT	RO	Safe mode activate status	0

			If this bit is 1, it is in safe mode currently.	
4	bALE_CLK_EN	RW	ALE pin clock output enable 1: P5.4 enabled to select the divided clock of the system clock frequency. 0: Output clock signal disabled.	0
3	bALE_CLK_SEL	RW	ALE pin clock selection when bALE_CLK_EN=1; 0: Divided by 12. 1: Divided by 4.	0
3	GF2	RW	Common flag 2 when bALE_CLK_EN=0: User-defined. Cleared and set by software	0
2	bDPTR_AUTO_INC	RW	Enable the DPTR to add 1 automatically after on the completion of movx@dptr command	0
1	Reserved	RO	Reserved	0
0	DPS	RW	Double DPTR data pointer select bit: 0: DPTR0. 1: DPTR1.	0

Table 11.1 Alternate ALE/CKO output state of the P5.4 pin

P5[4]	bALE_CLK_EN	bALE_CLK_SEL	P5.4 pin function description
0	0	0	Output low level (default)
0	1	0	Fsys/12
0	1	1	Fsys/4
1	X	X	Output high level

12. Timer

12.1 Timer0/1

Timer0 and Timer1 are 2 16-bit timers/counters configured by TCON and TMOD. TCON is used for timer/counter T0 and T1 startup control and overflow interrupt as well as external interrupt control. Each timer is a 16-bit timing unit composed of 2 8-bit registers. The high byte counter of timer 0 is TH0 and the low byte counter of timer 0 is TL0. The high byte counter of timer 1 is TH1 and the low byte counter of timer 1 is TL1. Timer 1 can also be used as the baud rate generator of UART0.

Table 12.1.1 Timer0/1 registers

Name	Address	Description	Reset value
TH1	8Dh	Timer1 count high byte	xxh
TH0	8Ch	Timer0 count high byte	xxh
TL1	8Bh	Timer1 count low byte	xxh
TL0	8Ah	Timer0 count low byte	xxh
TMOD	89h	Timer0/1 mode register	00h
TCON	88h	Timer0/1 control register	00h

Timer/counter 0/1 control register (TCON):

Bit	Name	Access	Description	Reset value
7	TF1	RW	Timer1 overflow interrupt flag bit Automatically cleared after it enters Timer1 interrupt.	0
6	TR1	RW	Timer1 startup/stop bit Set to 1 to startup. Set and cleared by software.	0
5	TF0	RW	Timer0 overflow interrupt flag bit Automatically cleared after it enters Timer0 interrupt.	0
4	TR0	RW	Timer0 startup/stop bit Set to 1 to startup. Set and cleared by software.	0
3	IE1	RW	INT1 interrupt request flag bit Automatically cleared after entering INT1 interrupt.	0
2	IT1	RW	INT1 trigger mode control bit 0: INT1 triggered by low level; 1: INT1 triggered by falling edge.	0
1	IE0	RW	INT0 interrupt request flag bit Automatically cleared after it enters INT0 interrupt.	0
0	IT0	RW	INT0 trigger mode control bit 0: INT0 triggered by low level; 1: INT0 triggered by falling edge.	0

Timer/counter 0/1 mode register (TMOD):

Bit	Name	Access	Description	Reset value
7	bT1_GATE	RW	Gate control enable bit. This bit controls whether the Timer1 startup is affected by INT1. 0: Whether the timer/counter 1 is started is independent of INT1. 1: It is started only when the INT1 pin is at high level and TR1 is 1.	0
6	bT1_CT	RW	Timing/counting mode selection bit 0: It works in timing mode. 1: It works in counting mode. Falling edge on T1 pin selected as the clock.	0
5	bT1_M1	RW	Timer/counter 1 mode selection high bit	0
4	bT1_M0	RW	Timer/counter 1 mode selection low bit	0
3	bT0_GATE	RW	Gate control enable bit. This bit controls whether the Timer0 startup is affected by INT0. 0: Whether the timer/counter 0 is started is independent of INT0. 1: It is started only when the INT0 pin is at high level and TR0 is 1	0
2	bT0_CT	RW	Timing/counting mode selection bit 0: It works in timing mode. 1: It works in counting mode. Falling edge on T0 pin selectd as the clock	0
1	bT0_M1	RW	Timer/counter 0 mode selection high bit	0
0	bT0_M0	RW	Timer/counter 0 mode selection low bit	0

Table 12.1.2 Timern working mode selected by bTn_M1 and bTn_M0 (n=0, 1)

bTn_M1	bTn_M0	Timern working mode (n=0, 1)
0	0	Mode0: 13-bit timer/counter n, the count unit is composed of the lower 5 bits of TLn and THn, and the higher 3 bits of TLn is invalid. When the counts of all 13 bits change from 1 to 0, set the overflow flag TFn and reset the initial value
0	1	Mode1: 16-bit timer/counter n, the count unit is composed of TLn and THn. When the counts of all 16 bits change from 1 to 0, set the overflow flag TFn and reset the initial value
1	0	Mode2: 8-bit overload timer/counter n, TLn is used for the count unit, and THn is used as the overload count unit. When the counts of all 8 bits change from 1 to 0, set the overflow flag TFn and automatically load the initial value from THn
1	1	Mode3: For timer/counter 0, it is divided into TL0 and TH0. TL0 is used as an 8-bit timer/counter, which occupies all control bits of Timer0. TH0 is also used as an 8-bit timer, which occupiesg TR1, TF1 and interrupt resources of Timer1. In this case, Timer1 is still available, but the startup control bit (TR1) and the overflow flag bit (TF1) cannot be used. For timer/counter 1, it stops after it enters mode 3.

Timern count low byte (TLn) (n=0, 1):

Bit	Name	Access	Description	Reset value
[7:0]	TLn	RW	Timern count low byte	xxh

Timern count high byte (THn) (n=0, 1):

Bit	Name	Access	Description	Reset value
[7:0]	THn	RW	Timern count high byte	xxh

12.2 Timer2

Timer2 is a 16-bit automatic overload timer/counter configured via T2CON and T2MOD registers, with TH2 as the high byte counter of Timer2 and TL2 as the low byte counter of Timer2. Timer2 can be used as the baud rate generator of UART0, and it also has the function of 3-channel signal level capture. The capture count is stored in RCAP2, T2CAP1 and T2CAP0 registers.

Table 12.2.1 Timer2 registers

Name	Address	Description	Reset value
TH2	CDh	Timer2 counter high	00h
TL2	CCh	Timer2 counter low	00h
T2COUNT	CCh	16-bit SFR consists of TL2 and TH2	0000h
T2CAP1H	CFh	Timer2 capture 1 data high byte (read only)	xxh
T2CAP1L	CEh	Timer2 capture 1 data low byte (read only)	xxh
T2CAP1	CEh	16-bit SFR consists of T2CAP1L and T2CAP1H	xxxxh
T2CAP0H	C7h	Timer2 capture 0 data high byte (read only)	xxh
T2CAP0L	C6h	Timer2 capture 0 data low byte (read only)	xxh

T2CAP0	C6h	16-bit SFR consists of T2CAP0L and T2CAP0H	xxxxh
RCAP2H	CBh	Count reload/capature 2 data register high byte	00h
RCAP2L	CAh	Count reload/capature 2 data register low byte	00h
RCAP2	CAh	16-bit SFR consists of RCAP2L and RCAP2H	0000h
T2MOD	C9h	Timer2 mode register	00h
T2CON	C8h	Timer2 control register	00h
T2CON2	C1h	Timer2 extend control register	00h

Timer/counter2 control register (T2CON):

Bit	Name	Access	Description	Reset value
7	TF2	RW	Timer2 overflow interrupt flag when bT2_CAP1_EN=0 When the Timer2 counts of all 16 bits change from 1 to 0, this overflow flag is set to 1, which requires software to reset. When RCLK=1 or TCLK=1, the bit is not set to 1.	0
7	CAP1F	RW	Timer2 capture 1 interrupt flag when bT2_CAP1_EN=1 It is triggered by the active edge on T2, which requires software to reset.	0
6	EXF2	RW	Timer2 external trigger flag It is triggered by T2EX active edge and set to 1 when EXEN2=1, which requires software to reset.	0
5	RCLK	RW	UART0 receive clock selection 0: Timer1 overflow pulse selected to generate the baud rate. 1: Timer2 overflow pulse selected to generate the baud rate.	0
4	TCLK	RW	UART0 transmit clock selection 0: Timer1 overflow pulse selected to generate the baud rate. 1: Timer2 overflow pulse selected to generate the baud rate.	0
3	EXEN2	RW	T2EX trigger enable bit 0: Ignore T2EX. 1: Reload or capture enabled to be triggered by T2EX active edge	0
2	TR2	RW	Timer2 startup/stop bit Set to 1 to start. Set and cleared by software.	0
1	C_T2	RW	Timer2 clock source selection bit 0: Internal clock selected. 1: Edge count based on falling edge on T2 pin selected.	0
0	CP_RL2	RW	Timer2 function selection bit. This bit should be forced to be 0 if RCLK or TCLK is 1. 0: Timer2 selected as timer/counter to automatically reload the initial value of the count when the counter overflows or T2EX level changes. 1: Timer2 capture 2 function enabled. The active edge on T2EX is captured.	0

Timer/counter2 mode register (T2MOD):

Bit	Name	Access	Description		Reset value
7	bTMR_CLK	RW	Fastest clock mode enable of T0/T1/T2 timer which has selected fast clock. 1: Fsys without division as the count clock. 0: Divided clock selected. This bit has no effect on the timer that selects the standard clock.		0
6	bT2_CLK	RW	Timer2 internal clock frequency selection bit 0: Standard clock selected. Fsys/12 when in timing/counting mode. Fsys/4 when in UART0 clock mode. 1: Fast clock selected. Fsys/4 (bTMR_CLK=0) or Fsys (bTMR_CLK=1) when in timing/counting mode. Fsys/2 (bTMR_CLK=0) or Fsys (bTMR_CLK=1) when in UART0 clock mode.		0
5	bT1_CLK	RW	Timer1 internal clock frequency selection bit 0: Standard clock selected, Fsys/12. 1: Fast clock selected. Fsys/4 (bTMR_CLK=0) or Fsys (bTMR_CLK=1).		0
4	bT0_CLK	RW	Timer0 internal clock frequency selection bit 0: Standard clock selected, Fsys/12. 1: Fast clock selected, Fsys/4 (bTMR_CLK=0) or Fsys (bTMR_CLK=1)		0
3	bT2_CAP_M1	RW	Timer2 capture mode high bit	Capture mode select: X0: From falling ege to falling edge. 01: From any edge to any edge, i.e. level change. 11: From rising edge to rising edge.	0
2	bT2_CAP_M0	RW	Timer2 capture mode low bit		0
1	T2OE	RW	Timer2 clock output enable bit 0: Output disabled. 1: T2 pin enabled to output clock. The frequency is the half of the Timer2 overflow rate.		0
0	bT2_CAP1_EN	RW	Capture 1 mode enable when RCLK=0, TCLK=0, CP_RL2=1, C_T2=0 and T2OE=0 1: Capture 1 function enabled. Active edge on T2 is captured. 0: Capture 1 function disabled.		0

Timer/counter2 extended control register (T2CON2):

Bit	Name	Access	Description	Reset value
[7:4]	Reserved	RO	Reserved	0000b
3	bT2_CAP0F	RW	When bT2_CAP0_EN=1, it is the Timer2 capture 0 interrupt flag, which is triggered by the effective edge of CAP0, which requires software to reset it	0
2	Reserved	RO	Reserved	0

1	Reserved	RO	Reserved	0
0	bT2_CAP0_EN	RW	Capture 0 mode enable when RCLK=0, TCLK=0, CP_RL2=1 1: Enable capture0 function to capture active edge of CAP0. 0: Disable capture0	0

Count reload/capature 2 data register (RCAP2):

Bit	Name	Access	Description	Reset value
[7:0]	RCAP2H	RW	High byte of reload value in timer/counter mode. High byte of timer captured by CAP2 in capture mode	00h
[7:0]	RCAP2L	RW	Low byte of reload value in timer/counter mode. Low byte of timer captured by CAP2 in capture mode	00h

Timer2 counter (T2COUNT):

Bit	Name	Access	Description	Reset value
[7:0]	TH2	RW	Current counter high byte	00h
[7:0]	TL2	RW	Current counter low byte	00h

Timer2 capture 1 data (T2CAP1):

Bit	Name	Access	Description	Reset value
[7:0]	T2CAP1H	RO	High byte of timer captured by CAP1	xxh
[7:0]	T2CAP1L	RO	Low byte of timer captured by CAP1	xxh

Timer2 capture 0 data (T2CAP0):

Bit	Name	Access	Description	Reset value
[7:0]	T2CAP0H	RO	High byte of timer captured by CAP0	xxh
[7:0]	T2CAP0L	RO	Low byte of timer captured by CAP0	xxh

12.3 PWM registers

The PWM_DATA registers in this section are represented in a generic format: a lowercase "n" represents the serial number of the ports (n=0 ~ 7).

Table 12.3.1 PWMX registers

Name	Address	Description	Reset value
PWM_CK_SE	9Eh	PWM clock setting register	00h
PWM_CTRL	9Dh	PWM control register	02h
PWM_CTRL2	9Fh	PWM extension control register	00h
PWM_DATA0	9Ch	PWM0 data register	xxh
PWM_DATA1	9Bh	PWM1 data register	xxh
PWM_DATA2	9Ah	PWM2 data register	xxh

PWM_DATA3	A3h	PWM3 data register	xxh
PWM_DATA4	A4h	PWM4 data register	xxh
PWM_DATA5	A5h	PWM5 data register	xxh
PWM_DATA6	A6h	PWM6 data register	xxh
PWM_DATA7	A7h	PWM7 data register	xxh

PWMn data register (PWM_DATAn):

Bit	Name	Access	Description	Reset value
[7:0]	PWM_DATAn	RW	Store the current PWMn data. Duty cycle of PWMn output active level =PWM_DATAn/PWM_CYCLE	xxh

PWM control register (PWM_CTRL):

Bit	Name	Access	Description	Reset value
7	Reserved	RO	Reserved	0
6	bPWM1_POLAR	RW	Control output polarity of PWM1 0: Low level by default, while active high. 1: High level by default, while active low.	0
5	bPWM0_POLAR	RW	PWM1 output polarity control 0: Low level by default, while active high. 1: High level by default while active low.	0
4	bPWM_IF_END	RW	PWM cycle period end interrupt flag bit 1: A PWM cycle period end interrupt. Write 1 to reset, or reset when the PWM_DATA0 data is reloaded.	0
3	bPWM1_OUT_EN	RW	PWM1 output enable 1: PWM1 output enabled.	0
2	bPWM0_OUT_EN	RW	PWM0 output enable 1: PWM0 output enabled.	0
1	bPWM_CLR_ALL	RW	1: Empty PWM count and FIFO. It requires software to reset.	1
0	bPWM_MOD_6BIT	RW	PWM data width mode: 0: 8-bit data, and PWM cycle is 256; 1: 6-bit data, and PWM cycle is 64.	0

PWM extension control register (PWM_CTRL2):

Bit	Name	Access	Description	Reset value
7	Reserved	RO	Reserved	0
6	Reserved	RO	Reserved	0
5	bPWM7_OUT_EN	RW	PWM7 output enable 1: PWM7 output enabled.	0

4	bPWM6_OUT_EN	RW	PWM6 output enable 1: PWM6 output enabled.	0
3	bPWM5_OUT_EN	RW	PWM5 output enable 1: PWM5 output enabled.	0
2	bPWM4_OUT_EN	RW	PWM4 output enable 1: PWM4 output enabled.	0
1	bPWM3_OUT_EN	RW	PWM3 output enable 1: PWM3 output enabled.	0
0	bPWM2_OUT_EN	RW	PWM2 output enable 1: PWM2 output enabled.	0

PWM clock setting register (PWM_CK_SE):

Bit	Name	Access	Description	Reset value
[7:0]	PWM_CK_SE	RW	Set PWM clock frequency factor	00h

12.4 PWM function

CH549 provides 8-channel PWM, and the output duty cycle of PWM can be dynamically modified. After integrating low-pass filtering via simple Resistor-Capacitor (RC), various output voltages can be obtained, which is equivalent to the low speed Digital-to-Analog Converter (DAC). Among them, PWM0 and PWM1 can also select the reserve polarity output and default output polarity as low level or high level.

PWM_CYCLE = bPWM_MOD_6BIT ? 64 : 256
Duty cycle of PWMn output =PWM_DATAn / PWM_CYCLE

It supports a range of 0% to 99.6% duty cycle in 8-bit data mode and 0% to 100% duty cycle in 6-bit data mode (if PWM_DATAn value is greater than PWM_CYCLE, it is regarded as 100%).

In practical application, it is recommended to enable the PWM pin output and set the PWM output pin to push-pull output.

12.5 Timer function

12.5.1 Timer0/1

(1). Set T2MOD to select Timer internal clock frequency. If bTn_CLK(n=0/1) is 0, the corresponding clock of Timer0/1 is Fsys/12. If bTn_CLK is 1, select either Fsys/4 or Fsys as the clock based on bTMR_CLK=0 or 1.

(2). Set TMOD to configure the working mode of Timer.

Mode0: 13-bit timer/counter

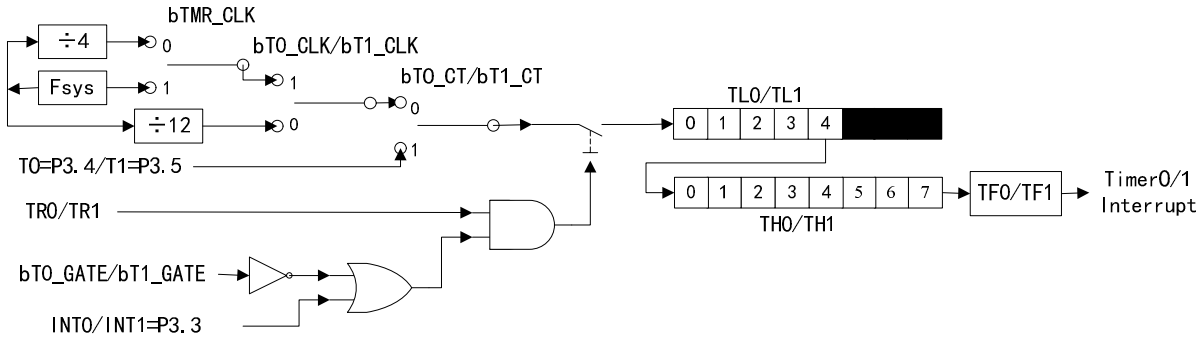


Figure 12.5.1.1 Timer0/1 mode0

Mode1: 16-bit timer/counter

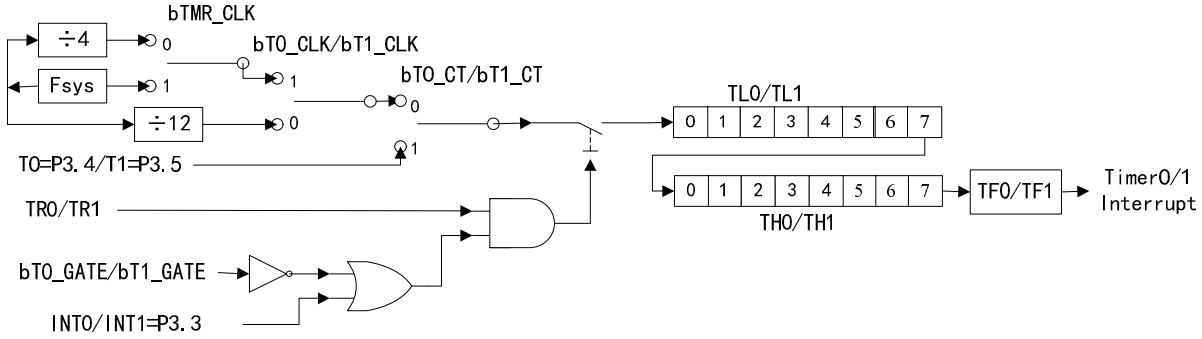


Figure12.5.1.2 Timer0/1 mode1

Mode2: Auto reload 8-bit timer/counter

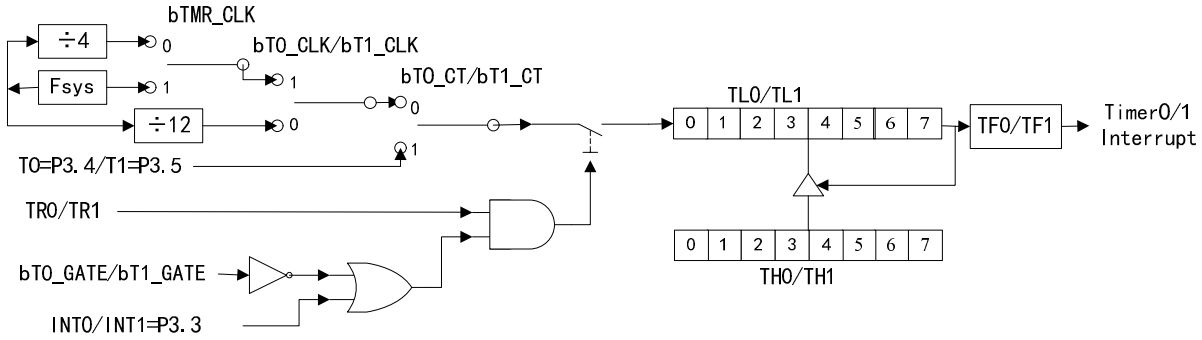


Figure 12.5.1.3 Timer0/1 mode2

Mode3: Timer0 is divided into 2 independent 8-bit timer/counter and borrows the TR1 control bit of Timer1. Timer1 substitutes the borrowed TR1 control bit by whether starting mode 3, and stops running when it enters mode 3.

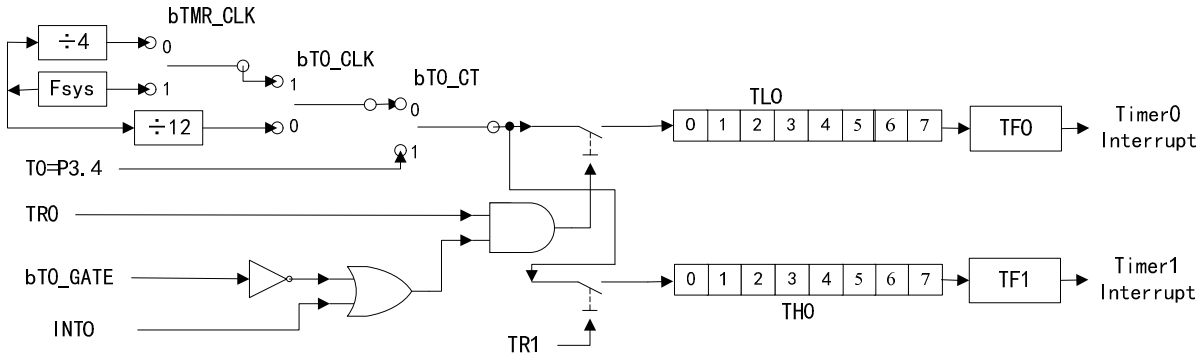


Figure 12.5.1.4 Timer0 mode3

(3). Set initial value TLn and THn(n=0/1) of timer/counter.

(4). Set the TRn bit (n=0/1) in TCON to turn on or stop timer/counter, which can be checked by querying the TFn bit (n=0/1) or by interrupt mode.

12.5.2 Timer2

Timer2 16-bit reload timer/counter mode:

(1). Set the RCLK and TCLK bits in T2CON to 0, to select non-UART baud rate generator mode.

(2). Set the C_T2 bit in T2CON to 0, to select the internal clock, and turn to step (3). Alternatively, set to 1 to select the falling edge on T2 pin as the count clock and skip step (3).

(3). Set T2MOD to select the Timer internal clock frequency. If bT2_CLK is 0, Timer2 clock is Fsys/12. If bT2_CLK is 1, Fsys/4 or Fsys is selected as the clock based on bTMR_CLK=0 or 1.

(4). Set the CP_RL2 bit in T2CON to 0, to select 16-bit reload timer/counter function of Timer2.

(5). Set RCAP2L and RCAP2H as the reload value of timer after overflow. Set TL2 and TH2 as the initial value of the timer (the same as RCAP2L and RCAP2H generally). Set TR2 to 1 to turn on Timer2.

(6). Inquire TF2 or Timer2 interrupt to obtain the current timer/counter state.

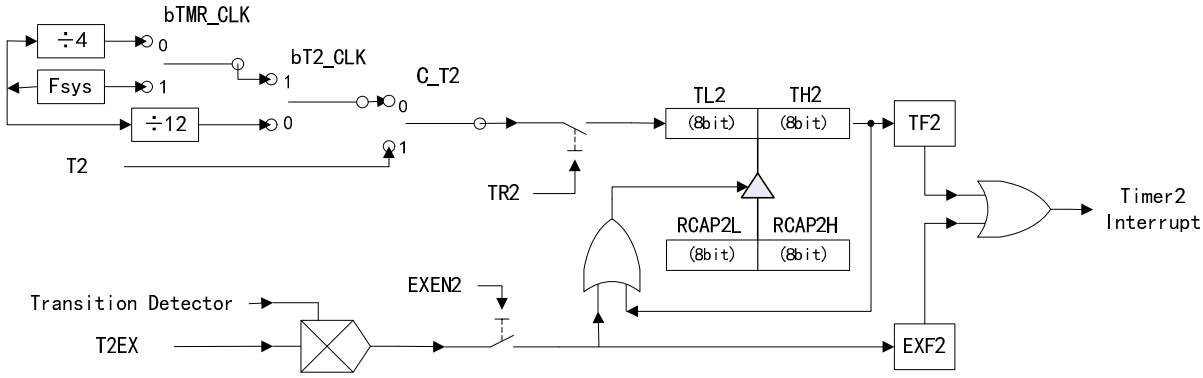


Figure 12.5.2.1 Timer2 16-bit reload Timer/Counter

Timer2 clock output mode:

Refer to the 16-bit reload timer/counter mode and then set the bit T2OE in T2MOD to 1 to enable a two divided-frequency clock of TF2 frequency output from T2 pin.

Timer2 UART0 baud rate generator mode:

(1). Set the C_T2 bit in T2CON to 0, to select the internal clock. Alternatively, set to 1 to select the falling edge on T2 pin as the clock. Set the RCLK and TCLK bits in T2CON to 1, or set one of them to 1 as

required, to select UART baud rate generator mode.

(2). Set T2MOD to select Timer internal clock frequency. If bT2_CLK is 0, the clock of Timer2 is Fsys/4. If bT2_CLK is 1, select either Fsys/2 or Fsys as the clock based on bTMR_CLK=0 or 1.

(3). Set RCAP2L and RCAP2H as the reload value of timer after overflow. Set TR2 to 1 to turn on Timer2.

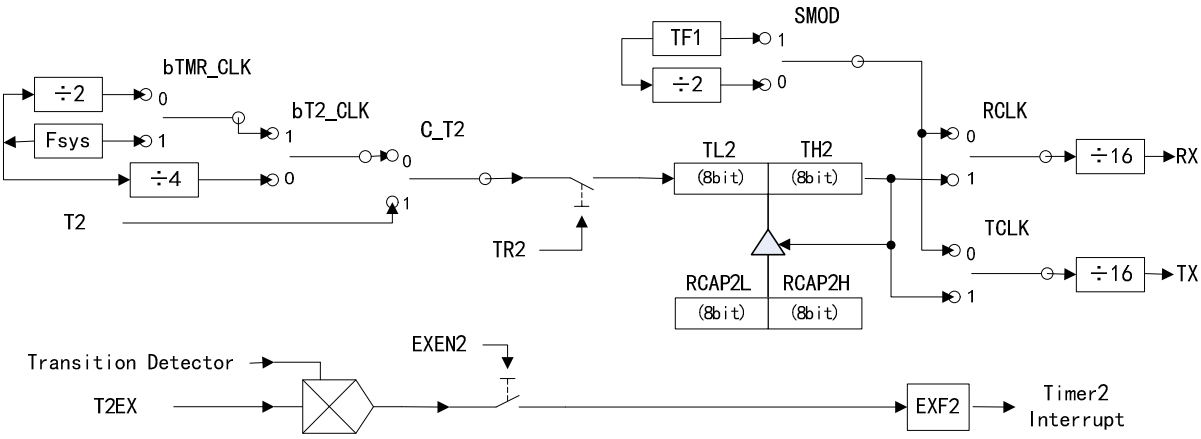


Figure 12.5.2.2 Timer2 UART0 baud rate generator

Timer2 signal channel capture mode:

(1). Set the RCLK and TCLK bits in T2CON to 0, to select non-UART baud rate generator mode.

(2). Set the C_T2 bit in T2CON to 0, to select the internal clock, and turn to step (3). Alternatively, set to 1 to select the falling edge on T2 pin as the count clock and skip step (3).

(3). Set T2MOD to select the Timer internal clock frequency. If bT2_CLK is 0, Timer2 clock is Fsys/12. If bT2_CLK is 1, either Fsys/4 or Fsys is selected as the clock based on bTMR_CLK=0 or 1.

(4). Set the bT2_CAP_M1 and bT2_CAP_M0 bits in T2MOD, to select corresponding edge capture mode.

(5). Set the CP_RL2 bit in T2CON to 1, to select the capture function of Timer2 to T2EX pin.

(6). Set TL2 and TH2 as the initial value of the timer, and set TR2 to 1 to turn on Timer2.

(7). When CAP2 capture is completed, RCAP2L and RCAP2H store the current count values of TL2 and TH2 and set EXF2 to generate an interrupt. The difference between the next captured RCAP2L and RCAP2H and the last captured RCAP2L and RCAP2H is the signal width between the two active edges.

(8). If the C_T2 bit in T2CON is 0, and the bT2_CAP1_EN bit in T2MOD is 1, Timer2 is enabled to capture the T2 pin at the same time. When the CAP1 capture is completed, T2CAP1L and T2CAP1H store the current count values of TL2 and TH2, and set CAP1F to generate an interrupt.

(9). If the bT2_CAP0_EN bit in T2CON2 is 1, Timer2 is enabled to capture the CAP0 pin at the same time. When the CAP0 capture is completed, T2CAP0L and T2CAP0H store the current count values of TL2 and TH2, and set bT2_CAP0F to generate an interrupt.

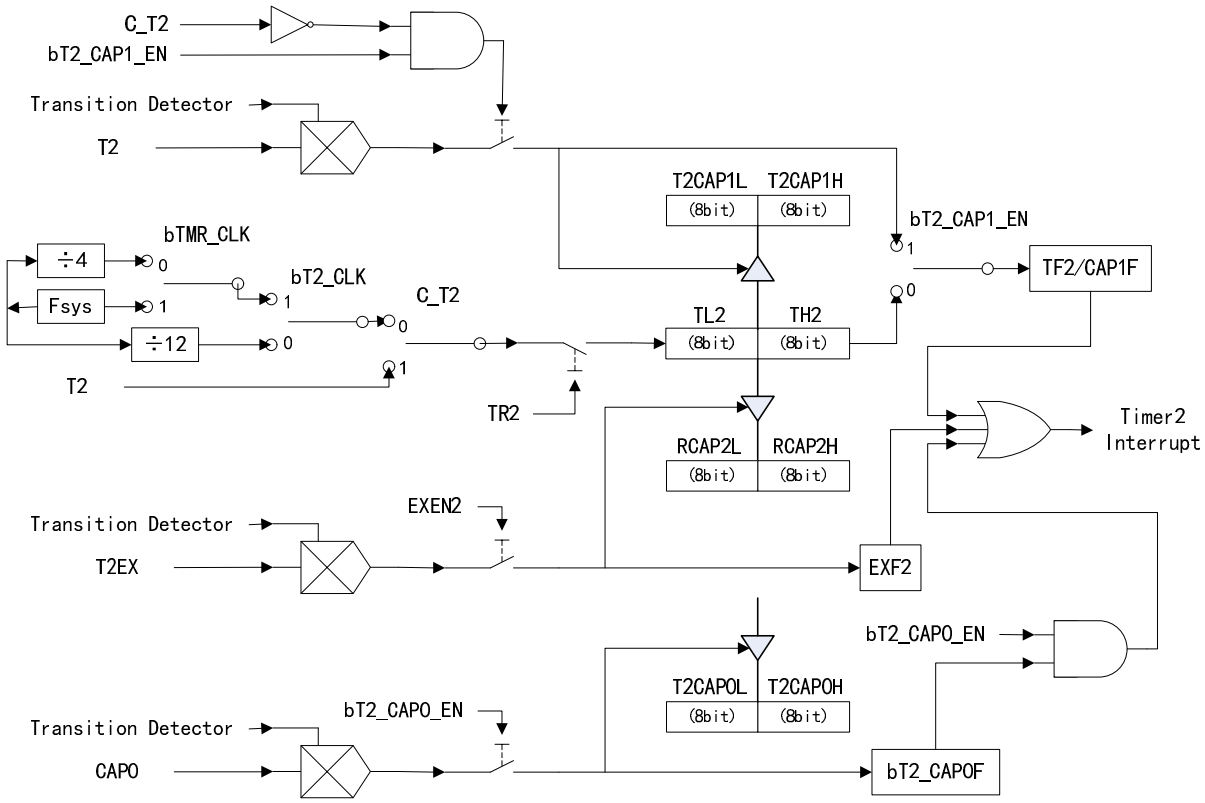


Figure 12.5.2.3 Timer2 capture mode

13. Universal asynchronous receiver/transmitter (UART)

13.1 Introduction of UART

CH549 provides 4 full-duplex UARTs: UART0~UART3. CH548 only provides UART0 and UART1.

UART0 is a standard MCS51 serial port, whose data reception and transmission are realized by physically separated receive/transmit registers via SBUF access. The data written to SBUF is loaded into the transmit register. And the receive buffer register is used for read operation on SBUF.

UART1 is a simplified MCS51 serial port, whose data reception and transmission are realized by physically separated receive/transmit registers via SBUF access. The data written to SBUF1 is loaded into the transmit register. And the receive buffer register is used for read operation on SBUF1. Compared with UART0, UART1 lacks the multi-device communication mode and fixed baud rate, but UART1 has an independent baud rate generator.

UART2 adds an interrupt enable bit on the basis of UART1 to replace ADC interrupt.

The same as UART2, UART3 also adds an interrupt enable bit on the basis of UART1 to replace PWMX interrupt.

13.2 UART register

Table 13.2.1 UART registers

Name	Address	Description	Reset value
SBUF	99h	UART0 data register	xxh
SCON	98h	UART0 control register	00h

SCON1	BCh	UART1 control register	40h
SBUF1	BDh	UART1 data register	xxh
SBAUD1	BEh	UART1 baud rate setting register	xxh
SIF1	BFh	UART1 interrupt status register	00h
SCON2	B4h	UART2 control register	00h
SBUF2	B5h	UART2 data register	xxh
SBAUD2	B6h	UART2 baud rate setting register	xxh
SIF2	B7h	UART2 interrupt status register	00h
SCON3	ACh	UART3 control register	00h
SBUF3	ADh	UART3 data register	xxh
SBAUD3	AEh	UART3 baud rate setting register	xxh
SIF3	AFh	UART3 interrupt status register	00h

13.2.1 UART0 register

UART0 control register (SCON):

Bit	Name	Access	Description	Reset value
7	SM0	RW	UART0 working mode selection bit 0 0: 8-bit data asynchronous communication. 1: 9-bit data asynchronous communication.	0
6	SM1	RW	UART0 working mode selection bit 1 0: Fixed baud rate. 1: Variable baud rate, generated by T1 or T2	0
5	SM2	RW	UART0 multi-device communication control bit: In mode 2 and mode 3, When SM2=1, If RB8 is 0, RI is not set to 1 and the reception is invalid. If RB8 is 1, RI is set to 1 and the reception is valid. When SM2=0, no matter RB8 is 0 or 1, RI is set when receiving data and the reception is valid. In mode 1, if SM2=1, only when the active stop bit is received can the reception be valid; In mode 0, the SM2 bit must be set to 0.	0
4	REN	RW	UART0 receive enable bit 0: UART0 receive disabled. 1: UART0 receive enabled.	0
3	TB8	RW	The 9th bit of the transmitted data In modes 2 and mode 3, TB8 is used to write the 9th bit of the transmitted data, which can be a parity bit. In multi-device communication, it is used to indicate whether the host sends an address byte or a data byte. Data byte when TB8=0, and address byte when TB8=1.	0
2	RB8	RW	The 9th bit of the received data In mode 2 and 3, RB8 is used to store the 9th bit of the received data.	0

			In mode 1, if SM2=0, RB8 is used to store the received stop bit. In mode 0, RB8 is not used.	
1	TI	RW	Transmit interrupt flag bit Set by hardware at the end of a data byte transmission. It requires software to reset.	0
0	RI	RW	Receive interrupt flag bit Set by hardware at the end of a data byte reception. It requires software to reset.	0

Table 13.2.1.1 UART0 working mode selection table

SM0	SM1	Description
0	0	Mode 0, shift register mode. Baud rate is always Fsys/12
0	1	Mode 1, 8-bit asynchronous communication. Variable baud rate, generated by timer T1 or T2
1	0	Mode 2, 9-bit asynchronous communication. Baud rate is Fsys/128(SMOD=0) or Fsys/32(SMOD=1)
1	1	Mode 3, 9-bit asynchronous communication. Variable baud rate, generated by timer T1 or T2

In mode1 and mode3, when RCLK=0 and TCLK=0, UART0 baud rate is generated by timer T1. T1 should be set to mode2 (auto reload 8-bit timer mode). Both bT1_CT and bT1_GATE must be 0. There are the following cases.

Table 13.2.1.2 Formula of UART0 baud rate generated by T1

bTMR_CLK	bT1_CLK	SMOD	Description
1	1	0	TH1 = 256 - Fsys / 32 / baud rate
1	1	1	TH1 = 256 - Fsys / 16 / baud rate
0	1	0	TH1 = 256 - Fsys / 4 / 32 / baud rate
0	1	1	TH1 = 256 - Fsys / 4 / 16 / baud rate
X	0	0	TH1 = 256 - Fsys / 12 / 32 / baud rate
X	0	1	TH1 = 256 - Fsys / 12 / 16 / baud rate

In mode1 and mode3, when RCLK=1 or TCLK=1, UART0 baud rate is generated by timer T2. T2 should be set to 16-bit auto reload baud rate generator mode. Both C_T2 and CP_RL2 must be 0. There are the following cases.

Table 13.2.1.3 Calculation formula of UART0 baud rate generated by T2

bTMR_CLK	bT2_CLK	Description
1	1	RCAP2 = 65536 - Fsys / 16 / baud rate
0	1	RCAP2 = 65536 - Fsys / 2 / 16 / baud rate
X	0	RCAP2 = 65536 - Fsys / 4 / 16 / baud rate

UART0 data register (SBUF):

Bit	Name	Access	Description	Reset value
[7:0]	SBUF	RW	UART0 data register, including the transmit register and the receive register that are physically separated. The transmit register is used to write data to SBUF. The receive register is used to read data from SBUF.	xxh

13.2.2 UART1 register

UART1 control register (SCON1):

Bit	Name	Access	Description	Reset value
7	bU1SM0	RW	UART1 working mode select bit 0: 8-bit data asynchronous communication. 1: 9-bit data asynchronous communication	0
6	Reserved	RO	Reserved	1
5	bU1SMOD	RW	UART1 communication baud rate selection 0: Slow mode. 1: Fast mode.	0
4	bU1REN	RW	UART1 receive enable bit 0: UART1 receive disabled. 1: UART1 receive enabled.	0
3	bU1TB8	RW	The 9th bit of the transmitted data In 9-bit data mode, TB8 is used to write the 9th bit of the transmitted data, which can be a parity bit. In 8-bit data mode, TB8 is ignored	0
2	bU1RB8	RW	The 9th bit of the received data In 9-bit data mode, RB8 is used to store the 9th bit of the received data. In 8-bit data mode, RB8 is used to store the received stop bit	0
1	bU1TIS	WO	Write 1 to preset the transmit interrupt flag bit as 1. For read operation, always return 0.	0
0	bU1RIS	WO	Write 1 to preset the receive interrupt flag bit as 1. For read operation, always return 0.	0

UART1 Baud rate is generated by the SBAUD1 setting and can be divided into two cases according to the selection of bU1SMOD:

When bU1SMOD=0, SBAUD1 = 256 - Fsys / 32 / baud rate;

When bU1SMOD=1, SBAUD1 = 256 - Fsys / 16 / baud rate.

UART1 interrupt state register (SIF1):

Bit	Name	Access	Description	Reset value
[7:2]	Reserved	RO	Reserved	000000b
1	bU1TI	RW	Transmit interrupt flag bit	0

			Set by hardware at the end of a data byte transmission. It requires software to write 1 to reset (writing 0 to this bit is ignored)	
0	bU1RI	RW	Receive interrupt flag bit Set by hardware at the end of a data byte reception. It requires software to write 1 to reset (writing 0 to this bit is ignored)	0

Note: Writing 1 to the interrupt flag bit to reset can ensure that only the specified flag bit is reset, without affecting other interrupt flags in the same register (other interrupt flags may be 1 before the write operation or may have become 1 during write operation). The same below.

UART1 data register (SBUF1):

Bit	Name	Access	Description	Reset value
[7:0]	SBUF1	RW	UART1 data register, including the transmit register and the receive register that are physically separated. The transmit register is used to write data to SBUF1. The receive register is used to read data from SBUF1.	xxh

13.2.3 UART2 registers

UART2 control register (SCON2):

Bit	Name	Access	Description	Reset value
7	bU2SM0	RW	UART2 working mode select bit 0: 8-bit data asynchronous communication; 1: 9-bit data asynchronous communication.	0
6	bU2IE	RW	UART2 interrupt enable bit 0: Disable interrupt, and the interrupt flag can be inquired. 1: Enable interrupt, and the original ADC interrupt is disabled to realize replacement	0
5	bU2SMOD	RW	Select communication baud rate of UART2 0: Slow mode. 1: Fast mode	0
4	bU2REN	RW	UART2 receive control bit 0: Disable. 1: Enable.	0
3	bU2TB8	RW	The 9^{th} bit of the transmitted data In 9-bit data mode, TB8 is used to write the 9^{th} bit of data transmitted, which can be a parity bit. In 8-bit data mode, TB8 is ignored	0
2	bU2RB8	RW	The 9^{th} bit of the received data In 9-bit data mode, RB8 is used to store the 9^{th} bit of data received. In 8-bit data mode, RB8 is used to store the received stop bit	0
1	bU2TIS	WO	Write 1 to preset the transmit interrupt flag bit to 1. For read operation, always return 0.	0

0	bU2RIS	WO	Write 1 to preset the receive interrupt flag bit to 1. For read operation, always return 0.	0

UART2 Baud rate is generated by the SBAUD2 setting and can be divided into two cases according to the selection of bU2SMOD:

When bU2SMOD=0, SBAUD2 = 256 - Fsys / 32 / baud rate;

When bU2SMOD=1, SBAUD2 = 256 - Fsys / 16 / baud rate.

UART2 interrupt status register (SIF2):

Bit	Name	Access	Description	Reset value
[7:2]	Reserved	RO	Reserved	000000b
1	bU2TI	RW	Transmit interrupt flag bit Set by hardware after a data byte is transmitted. It requires software to write 1 to reset (write 0 to this bit is ignored)	0
0	bU2RI	RW	Receive interrupt flag bit Set by hardware after a data byte is received effectively. It requires software to write 1 to reset (write 0 to this bit is ignored)	0

UART2 data register (SBUF2):

Bit	Name	Access	Description	Reset value
[7:0]	SBUF2	RW	UART2 data register, including the transmit register and the receive register that are physically separated. The transmit register is used to write data to SBUF2. The receive register is used to read data from SBUF2.	xxh

13.2.4 UART3 register

UART3 control register (SCON3):

Bit	Name	Access	Description	Reset value
7	bU3SM0	RW	UART3 working mode select bit 0: 8-bit data asynchronous communication. 1: 9-bit data asynchronous communication	0
6	bU3IE	RW	UART3 interrupt enable bit 0: Disable interrupt, and the interrupt flag can be inquired. 1: Enable interrupt, and the original PWMX interrupt is disabled to realize replacement	0
5	bU3SMOD	RW	Select communication baud rate of UART3 0: Slow mode. 1: Fast mode	0
4	bU3REN	RW	UART3 receive control bit 0: Disable. 1: Enable.	0
3	bU3TB8	RW	The 9th bit of transmitted data	0

			In 9-bit data mode, TB8 is used to write the 9th bit of data transmitted, which can be a parity bit. In 8-bit data mode, TB8 is ignored.	
2	bU3RB8	RW	The 9th bit of received data In 9-bit data mode, RB8 is used to store the 9th bit of data received. In 8-bit data mode, RB8 is used to store the received stop bit	0
1	bU3TIS	WO	Write 1 to preset the transmit interrupt flag bit to 1. For read operation, always return 0.	0
0	bU3RIS	WO	Write 1 to preset the receive interrupt flag bit to 1. For read operation, always return 0.	0

UART3 baud rate is generated by the SBAUD3 setting and can be divided into two cases according to the selection of bU3SMOD:

When bU3SMOD=0, SBAUD3 = 256 - Fsys / 32 / baud rate;

When bU3SMOD=1, SBAUD3 = 256 - Fsys / 16 / baud rate.

UART3 interrupt status register (SIF3):

Bit	Name	Access	Description	Reset value
[7:2]	Reserved	RO	Reserved	000000b
1	bU3TI	RW	Transmit interrupt flag bit Set by hardware after a data byte is transmitted. It requires software to write 1 to clear (writing 0 to this bit is ignored)	0
0	bU3RI	RW	Receive interrupt flag bit Set by hardware after a data byte is received effectively. It requires software to write 1 to clear (writing 0 to this bit is ignored)	0

UART3 data register (SBUF3):

Bit	Name	Access	Description	Reset value
[7:0]	SBUF3	RW	UART3 data register, including the transmit register and the receive register that are physically separated. The transmit register is used to write data to SBUF3. The receive register is used to read data from SBUF3.	xxh

13.3 UART applications

UART0 application:

(1). Select the baud rate generator for UART0, either from T1 or T2, and configure corresponding counter.

(2). Enable T1 or T2.

(3). Set SM0, SM1 and SM2 in SCON to select the working mode of UART0. Set REN as 1 and enable UART0 receiving.

(4). UART interrupt can be set or R1 and T1 interrupt state can be inquired.

(5). Read and write SBUF to implement data reception and transmission of UART, and the allowable baud

rate error of UART receive signal is not more than 2%.

UART1 application:

(1). Select bU1SMOD and set SBAUD1 based on the baud rate.

(2). Set bU1SM0 in SCON1 to select the working mode of UART1. Set bU1REN to 1 to enable UART1 receiving.

(3). UART1 interrupt can be set or bU1RI and bU1TI interrupt state can be inquired (only writing 1 to the specified bit can reset it).

(4). Read and write SBUF1 to realize data reception and transmission of UART1, and the allowable baud rate error of UART receive signal is not more than 2%.

UART2 application (or UART3 application):

(1). Select bU2SMOD and set SBAUD2 based on the baud rate.

(2). Set bU2SM0 in SCON2 to select the working mode of UART2. Set bU2REN to 1 to enable UART2 receiving.

(3). Query the interrupt status of bU2RI and bU2TI (write 1 to the specified bit to reset), or enable UART2 interrupt and set bU2IE to 1 to replace ADC (PWMX for UART3) interrupt.

(4). Read and write SBUF2 to implement data reception and transmission of UART2, and the allowable baud rate error of the UART receive signal is not more than 2%.

14. Synchronous serial peripheral interface (SPI)

14.1 SPI introduction

CH549 provides an SPI interface for high-speed synchronous data transfer with peripherals.

(1). Supports Master mode and slave mode.

(2). Clock mode: mode0 and mode3.

(3). Optional 3-wire full duplex or 2-wire half-duplex mode.

(4). Optional MSB-first or LSB-first.

(5). Clock frequency is adjustable, up to half of the system clock frequency.

(6). Built-in 1-byte receive FIFO and 1-byte transmit FIFO.

(7). Supports the first byte pre-load data in slave mode to facilitate the host to obtain the returned data immediately in the first byte.

14.2 SPI register

Table 14.2.1 SPI registers

Name	Address	Description	Reset value
SPI0_SETUP	FCh	SPI0 setup register	00h
SPI0_S_PRE	FBh	SPI0 slave mode preset data register	20h
SPI0_CK_SE	FBh	SPI0 clock setting register	20h
SPI0_CTRL	FAh	SPI0 control register	02h
SPI0_DATA	F9h	SPI0 data register	xxh
SPI0_STAT	F8h	SPI0 status register	08h

SPI0 setup register (SPI0_SETUP):

Bit	Name	Access	Description	Reset value
7	bS0_MODE_SLV	RW	SPI0 master/slave mode selection bit 0: Master mode. 1: Slave mode/device mode.	0
6	bS0_IE_FIFO_OV	RW	FIFO overflow interrupt enable bit in slave mode 1: FIFO overflow interrupt enabled. 0: FIFO overflow does not generate interrupt.	0
5	bS0_IE_FIRST	RW	Receive first byte completed interrupt enable bit in slave mode 1: Interrupt triggered when the first data byte is received in slave mode. 0: Interrupt is not generated when the first byte is received.	0
4	bS0_IE_BYTE	RW	Data byte transmit completed interrupt enable bit 1: Data byte transmit completed interrupt enabled. 0: Interrupt is not generated when the byte transmission is completed.	0
3	bS0_BIT_ORDER	RW	Order control bit of data byte 0: MSB first. 1: LSB first.	0
2	Reserved	RO	Reserved	0
1	bS0_SLV_SELT	RO	Chip select activate status bit in slave mode 0: Not selected currently. 1: Being selected currently	0
0	bS0_SLV_PRELOAD	RO	Pre-load data status bit in slave mode 1: Current pre-load state after valid chip select and before the data is not transmitted	0

SPI0 clock setting register (SPI0_CK_SE):

Bit	Name	Access	Description	Reset value
[7:0]	SPI0_CK_SE	RW	Set SPI0 clock frequency division factor in master mode	20h

SPI0 preset data register in slave mode (SPI0_S_PRE)

Bit	Name	Access	Description	Reset value
[7:0]	SPI0_S_PRE	RW	Preload first transmission data in slave mode	20h

SPI0 control register (SPI0_CTRL):

Bit	Name	Access	Description	Reset value
7	bS0_MISO_OE	RW	SPI0 MISO output enable 1: SPI0 MISO output enabled.	0

			0: SPI0 MISO output disabled.	
6	bS0_MOSI_OE	RW	SPI0 MOSI output enable 1 SPI0 MOSI output enabled. 0: SPI0 MOSI output disabled.	0
5	bS0_SCK_OE	RW	SPI0 SCK output enable 1: SPI0 SCK output enabled. 0: SPI0 SCK output disabled.	0
4	bS0_DATA_DIR	RW	SPI0 data direction control bit 0: Output. Only writing to FIFO is regarded as an effective operation, and an SPI transmission is started. 1: Input. Reading/writing to FIFO is regarded as an effective operation, and an SPI transmission is started.	0
3	bS0_MST_CLK	RW	SPI0 master clock mode control bit 0: Mode 0. SCK defaults to low level when free. 1: Mode 3. SCK defaults to high level.	0
2	bS0_2_WIRE	RW	2-wire half-duplex mode enable bit of SPI0 0: 3-wire full-duplex mode (SCK, MOSI and MISO). 1: 2-wire half-duplex mode (SCK, MISO).	0
1	bS0_CLR_ALL	RW	1: Empty SPI0 interrupt flag and FIFO. It requires software to reset.	1
0	bS0_AUTO_IF	RW	Enable bit that allows automatic clear of byte receive completed interrupt flag through FIFO effective operation 1: Auto clear the byte receive completed interrupt flag (S0_IF_BYTE) during the effective read and write operation of FIFO	0

SPI0 data register (SPI0_DATA):

Bit	Name	Access	Description	Reset value
[7:0]	SPI0_DATA	RW	Including the transmit FIFO and the receive FIFO which are physically separated. The receive FIFO is used for read operation. And the transmit FIFO is used for write operation. Effective read/write operation can initiate an SPI transfer.	xxh

SPI0 status register (SPI0_STAT):

Bit	Name	Access	Description	Reset value
7	S0_FST_ACT	RO	1: Currently, reception of the first byte is completed in slave mode.	0
6	S0_IF_OV	RW	FIFO overflow flag bit in slave mode 1: FIFO overflow interrupt. 0: No interrupt. Directly write 0 to reset, or write 1 to the corresponding bit	0

			in the register to reset. When bS0_DATA_DIR=0, transmit FIFO empty triggers interrupt. When bS0_DATA_DIR=1, receive FIFO full triggers interrupt,	
5	S0_IF_FIRST	RW	First byte receive completed interrupt flag bit in slave mode 1: The first byte is received. Directly write 0 to reset, or write 1 to the corresponding bit in the register to reset.	0
4	S0_IF_BYTE	RW	Data byte transmit completed interrupt flag bit 1: One byte transmission is completed. Directly write 0 to reset, or write 1 to the corresponding bit in the register to reset, or reset by FIFO effective operation when bS0_AUTO_IF=1.	0
3	S0_FREE	RO	SPI0 free flag bit 1: No SPI shift at present, usually it is in the free period between the data bytes.	1
2	S0_T_FIFO	RO	SPI0 transmit FIFO count. 0 and 1 both are valid.	0
1	Reserved	RO	Reserved	0
0	S0_R_FIFO	RO	SPI0 receive FIFO count. 0 and 1 both are valid.	0

14.3 SPI transfer formats

SPI master mode supports two transfer formats, i.e. mode0 and mode3, which can be selected by setting the bSn_MST_CLK bit in the SPIn_CTRL register. CH549 always samples MISO data on the rising edge of CLK. The data transfer formats are shown in the figures below.

Mode0: bSn_MST_CLK = 0

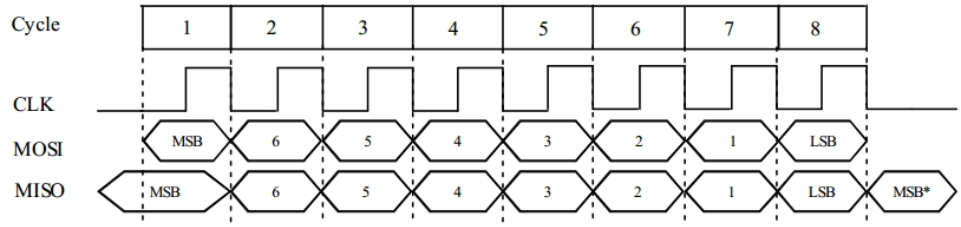


Figure 14.3.1 SPI mode0 timing diagram

Mode3: bSn_MST_CLK = 1

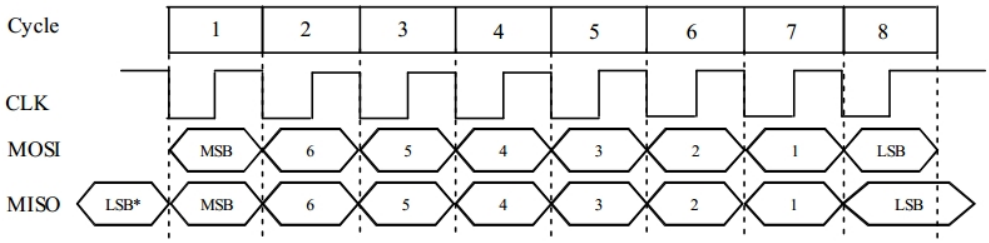


Figure 14.3.2 SPI mode3 timing diagram

14.4 SPI configuration

14.4.1 Master mode

In SPI master mode, SCK pin output serial clock, and chip select output pin can be specified as any I/O

pin.

SPI0 configuration prodecure:

(1). Set SPI0_CK_SE to configure SPI clock frequency.

(2). Set the bS0_MODE_SLV bit in the SPI0_SETUP register to 0, to select Master mode.

(3). Set the bS0_MST_CLK bit in the SPI0_CTRL register, to select mode0 or mode3 as required.

(4). Set the bS0_SCK_OE bit and bS0_MOSI_OE bit in the SPI0_CTRL register to 1, and set the bS0_MISO_OE bit to 0, to set the P1 port direction bSCK and bMOSI to output, bMISO to input, and chip select pin to output.

Data transmission:

(1). Write to the SPI0_DATA register, write the to be sent data to FIFO to automatically initiate an SPI transfer.

(2). Wait for S0_FREE to be 1, it indicates that the transmission is completed and the transmission of the next byte can be proceeded.

Data reception:

(1). Write to the SPI0_DATA register, write any data to FIFO, e.g. 0FFh, to initiate an SPI transfer.

(2). Wait for S0_FREE to be 1, it indicates that the reception is completed and SPI0_DATA can be read to obtain the received data.

(3). If bS0_DATA_DIR is set to 1 previously, the above read operation still can initiate the next SPI transfer, otherwise it will not start.

14.4.2 Slave mode

Only SPI0 supports Slave mode. In Slave mode, SCK pin is used to receive the serial clock of the connected SPI host.

(1). Set the bS0_MODE_SLV bit in the SPI0 setup register (SPI0_SETUP) to 1, to select Slave mode.

(2). Set the bS0_SCK_OE bit and bS0_MOSI_OE bit in the SPI0 control register (SPI0_CTRL) to 0, and set the bS0_MISO_OE bit to 1, to set the P1 port direction bSCK, bMOSI, bMISO and chip select pin to input. When SCS is active (low level), MISO output is automatically enabled. In this case, it is recommended to set MISO pin to high impedance input (P1_MOD_OC[6]=0, P1_DIR_PU[6]=0), so that MISO will not output during invalid chip select, which is convenient for sharing SPI bus.

(3). Optionally, set the preset data register in SPI slave mode (SPI0_S_PRE), to be automatically loaded into the buffer for the first time after chip select for external output. After 8 serial clocks, that is, the first byte of data transmission and exchange is completed, CH549 obtains the first byte of data (possibly command code) sent by the external SPI host, and the external SPI host obtains the preset data (possibly the status value) in SPI0_S_PRE through exchange. The bit 7 in the SPI0_S_PRE register is automatically loaded into the MISO pin during the low level period of SCK after the SPI chip select is active. For SPI mode 0, if the bit 7 in SPI0_S_PRE is preset by CH549, the external SPI host obtains the preset value of bit 7 in SPI0_S_PRE by inquiring the MISO pins when the SPI chip select is active but there is no data transfer, thereby the value of bit 7 in SPI0_S_PRE can be obtained only by the effective SPI chip select.

Data transmission:

Inquire S0_IF_BYTE or wait for interrupt. After each SPI data byte transfer, write to the SPI0_DATA register, and write the data to be sent to FIFO. Or wait for S0_FREE to be changed from 0 to 1, and the transmission of the next byte can be proceeded.

Data reception:
Inquire S0_IF_BYTE or wait for interrupt. After each SPI data byte transfer, read the SPI0_DATA register to obtain the received data from FIFO. Inquire S0_R_FIFO to know whether there are remaining bytes in FIFO.

15. Analog-to-digital converter (ADC）and Touch key (TKEY)

15.1 Introduction of ADC and CMP

CH549 provides an 12-bit analog digital converter, including Analog-Digital Converter (ADC) and voltage comparator CMP module.

This ADC has 16 external analog signal input channels and 4 internal input channels (reference voltage), which supports time-sharing acquisition and supports analog input voltage that ranges from 0 to VDD.

The positive phase input of the CMP multiplexes the above ADC input. The inverse phase input has 2 external analog signal input channels and 2 internal reference voltage input channels, which allows time-sharing comparison. There are more than 68 kinds of cross combinations, supporting analog input voltage that ranges from 0 to VDD.

15.2 ADC and CMP registers

Table 15.2.1 ADC registers

Name	Address	Description	Reset value
ADC_CTRL	F2h	ADC control and state register	xxh
ADC_CFG	F3H	ADC configuration register	00h
ADC_DAT_H	F5h	ADC result data high byte (read only)	0xh
ADC_DAT_L	F4h	ADC result data low byte (read only)	xxh
ADC_DAT	F4h	16-bit SFR consists of ADC_DAT_L and ADC_DAT_H	0xxxh
ADC_CHAN	F6h	ADC analog signal channel select register	00h
ADC_PIN	F7h	ADC pin digital input control register	00h

ADC control and state register (ADC_CTRL):

Bit	Name	Access	Description	Reset value
7	bCMPDO	RO	The output bit of voltage comparator results after synchronous delay, which is the status of bCMPO after synchronous delay with bCMP_IF	x
6	bCMP_IF	RW	Voltage comparator result change interrupt flag 1: The voltage comparator results have changed, and write 1 to clear	0
5	bADC_IF	RW	ADC conversion completion interrupt flag 1: An ADC conversion is completed, and write 1 to clear or clear when writing TKEY_CTRL data	0
4	bADC_START	RW	ADC start control bit, set 1 to start an ADC conversion, the bit will be cleared automatically after the ADC conversion is completed	0

3	bTKEY_ACT	RO	Indicate the touch key detection running state 1: Capacitor is being charged and the ADC is being measured	0
[2:1]	Reserved	RO	Reserved	00b
0	bCMPO	RO	The result real-time output bit of the voltage comparator 0: Voltage of the positive phase input terminal is lower than that of the inverting input terminal. 1: Voltage of the positive phase input terminal is higher than that of the inverting input terminal	x

ADC configuration register (ADC_CFG):

Bit	Name	Access	Description	Reset value
[7:6]	Reserved	RO	Reserved	00b
5	bADC_AIN_EN	RW	CMP positive phase input terminal and ADC input channel external AIN enable bit 1: One is selected by MASK_ADC_CHAN from 16 AIN. 0: Disable external AIN	0
4	bVDD_REF_EN	RW	Internal reference voltage enable bit 1: Internal reference voltage is generated by multiple series resistors to the supply voltage. 0: Disable divider resistor	0
3	bADC_EN	RW	Power control bit of ADC module 0: Disable power supply of the ADC module and enter the sleep state. 1: Enable.	0
2	bCMP_EN	RW	Power control bit of voltage comparator 0: Disable power supply of the voltage comparator and enter the sleep state. 1: Enable. At the same time, it will automatically enable the waking function of voltage comparator, and it will automatically wake up if the comparator result changes during sleep	0
1	bADC_CLK1	RW	ADC reference clock frequency select high bit	0
0	bADC_CLK0	RW	ADC reference clock frequency select low bit	0

Table 15.2.2 ADC reference clock frequency selection table

bADC_CLK1	bADC_CLK0	ADC reference clock frequency	Time required to complete an ADC	Applicable scope
0	0	750KHz	512 Fosc cycles	Rs<=16KΩ or Cs>=0.08uF
0	1	1.5MHz	256 Fosc cycles	Rs<=8KΩ or Cs>=0.08uF
1	0	3MHz	128 Fosc cycles	VDD>=3V and (Rs<=4KΩ or Cs>=0.08uF)
1	1	6MHz	64 Fosc cycles	VDD>=4.5V and

				(Rs<=2KΩ or Cs>=0.08uF)

Notes: VDD refers to supply voltage. Cs refers to shunt capacitance of signal source. Rs refers to internal resistance in series of signal source (the sampling time is only 3 reference clocks).
The resistance of the internal reference voltage channel is large, so a slower reference clock is recommended, or discard the first few data after multiple samples.

ADC analog signal channel select register (ADC_CHAN):

Bit	Name	Access	Description	Reset value
[7:6]	MASK_CMP_CHAN	RW	CMP inverted input signal channel selection	00b
[5:4]	MASK_ADC_I_CH	RW	CMP positive input and ADC input internal signal channel selection	00b
[3:0]	MASK_ADC_CHAN	RW	When bADC_AIN_EN=1, the CMP positive input and ADC input external signal channel are selected. When bADC_AIN_EN=0, the external signal channel is closed	0000b

Table 15.2.1 Voltage comparator (CMP) inverted input signal channel selection table

bCMP_EN	bVDD_REF_EN	MASK_CMP_CHAN	Select CMP inverted input terminal signal channel
0	x	xxb	Disconnect signal channel, suspending
1	0	00b	Disconnect signal channel, suspending
1	1	00b	Connect to internal reference voltage: 12.5% of VDD voltage
1	0	01b	Connect to internal reference voltage: 100% of VDD voltage
1	1	01b	Connect to internal reference voltage: 25% of VDD voltage
1	x	10b	Connect to external signal AIN1 (P1.1)
1	x	11b	Connect to external signal AIN12 (P1.2)

Table 15.2.2 Voltage comparator (CMP) positive input and ADC input internal signal channel selection table

bADC_EN	bADC_AIN_EN	bVDD_REF_EN	MASK_ADC_I_CH	Select CMP positive phase input terminal and ADC input internal signal channel
x	x	0	00b	Disconnect internal signal channel, suspending
x	x	1	00b	Connect to internal reference voltage: 50% of VDD voltage
x	x	x	01b	Connect to internal reference voltage: V33 voltage
x	x	x	10b	Connect to internal voltage/with noise: 54.5% of V33 voltage

1	0	x	11b	Connect to internal signal: temperature sensor (TS), For specific operation, please refer to C Language Example Program
0	x	x	11b	Disconnect internal signal channel, suspended
x	1	x	11b	Disconnect internal signal channel, suspended

Table 15.2.3 Voltage comparator (CMP) positive inputl and ADC input external signal channel selection table

bADC_AIN_EN	MASK_ADC_CHAN	Select CMP positive phase input terminal and ADC input external signal channel
0	xxxxb	Disconnect the external signal channel (AIN0 ~ AIN15), suspended
1	0000b	Connect to external signal AIN0 (P1.0)
1	0001b	Connect to external signal AIN1 (P1.1)
1	0010b	Connect to external signal AIN12 (P1.2)
1	0011b	Connect to external signal AIN13 (P1.3)
1	0100b	Connect to external signal AIN4 (P1.4)
1	0101b	Connect to external signal AIN5 (P1.5)
1	0110b	Connect to external signal AIN6 (P1.6)
1	0111b	Connect to external signal AIN7 (P1.7)
1	1000b	Connect to external signal AIN8 (P0.0)
1	1001b	Connect to external signal AIN9 (P0.1)
1	1010b	Connect to external signal AIN10 (P0.2)
1	1011b	Connect to external signal AIN11 (P0.3)
1	1100b	Connect to external signal AIN12 (P0.4)
1	1101b	Connect to external signal AIN13 (P0.5)
1	1110b	Connect to external signal AIN14 (P0.6)
1	1111b	Connect to external signal AIN15 (P0.7)

The voltage comparator CMP positive phase input terminal and ADC input can be connected only to the internal signal, or only to the external signal, or both the internal and external signals. In the case of simultaneous connection of internal and external signals, intercommunication will be realized between the internal signals and external signals. The on resistance is a series connection of 2 Rsw, and the internal reference voltage (there is also its internal resistance) will be connected to the external signal pins AIN0 ~ AIN15 via the above two Rsw resistors, which is equivalent to the pull-up resistor providing a specific voltage for the signal pins.

Ca is a sampling capacitor with a capacitance of about 15pF. The R2/R1 resistance ratio is 54.5:45.5. The 4R/2R/R resistance ratio is 4:2:1.

ADC data register (ADC_DAT):

Bit	Name	Access	Description	Reset value
[7:0]	ADC_DAT_H	RO	High byte of ADC sampling result data	0xh
[7:0]	ADC_DAT_L	RO	Low byte of ADC sampling result data	xxh

ADC pin digital input control register (ADC_PIN):

Bit	Name	Access	Description	Reset value
7	bAIN14_15_DI_DIS	RW	Disable digital input on AIN14 and AIN15 0: Enable	0
6	bAIN12_13_DI_DIS	RW	Disable digital input on AIN12 and AIN13 0: Enable	0
5	bAIN10_11_DI_DIS	RW	Disable digital input on AIN10 and AIN11 0: Enable	0
4	bAIN8_9_DI_DIS	RW	Disable digital input on AIN8 and AIN9 0: Enable	0
3	bAIN6_7_DI_DIS	RW	Disable digital input on AIN6 and AIN7 0: Enable	0
2	bAIN4_5_DI_DIS	RW	Disable digital input on AIN4 and AIN5 0: Enable	0
1	bAIN2_3_DI_DIS	RW	Disable digital input on AIN2 and AIN3 0: Enable	0
0	bAIN0_1_DI_DIS	RW	Disable digital input on AIN0 and AIN1 0: Enable	0

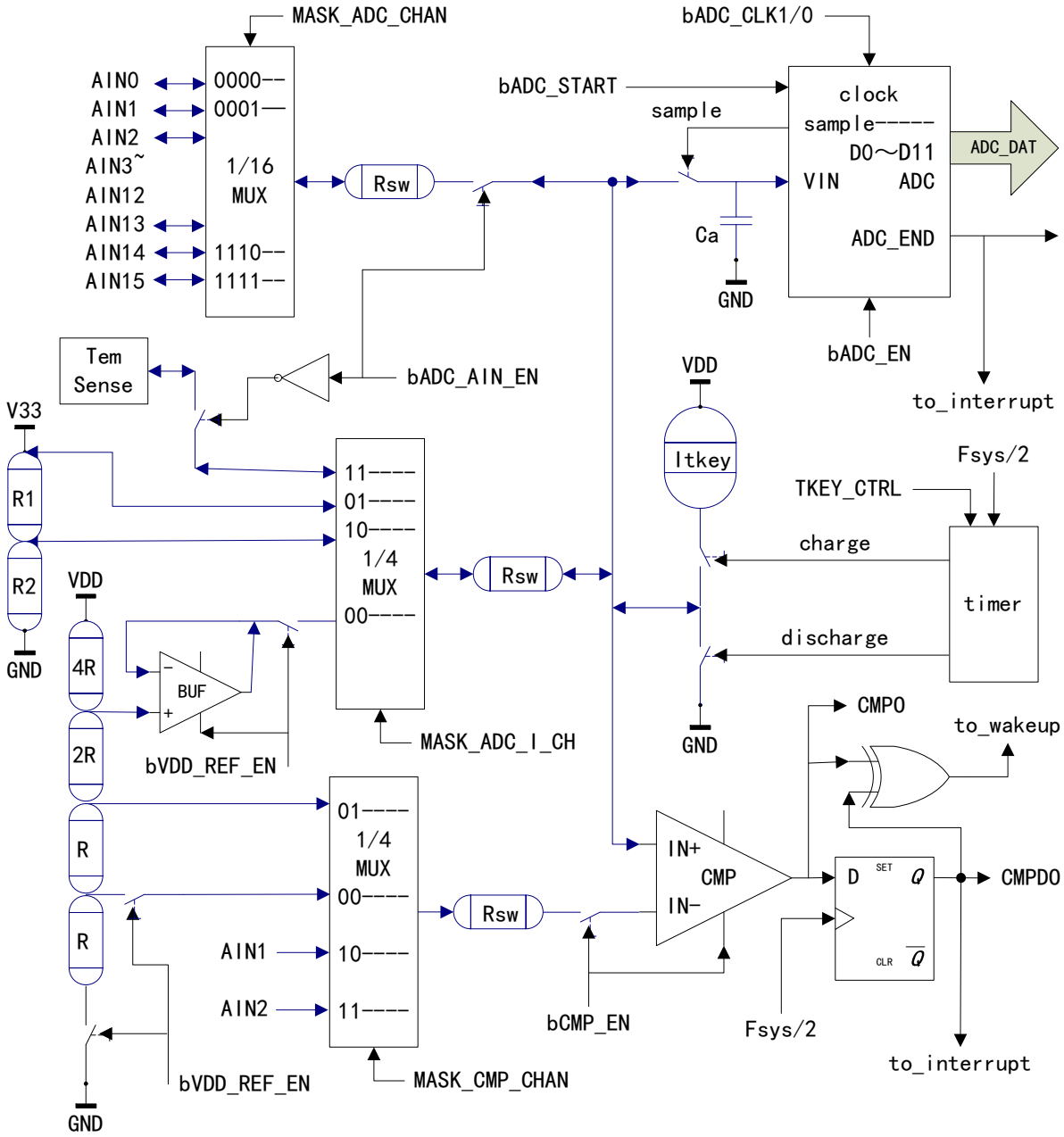


Figure 15.2.1 ADC/CMP/TKEY structure diagram (Blue lines represents analog signals)

15.3 Touch Key (TKEY) registers

Table 15.3.1 TKEY registers

Name	Address	Description	Reset value
TKEY_CTRL	F1h	Touch key charging impulse width control register	00h

Touch key charging impulse width control register (TKEY_CTRL):

Bit	Name	Access	Description	Reset value
[7:0]	TKEY_CTRL	WO	Touch key charging impulse width value, only the lower 7 bits are effective, count in the unit (2/Fsys) of twice the system period, and it will automatically	00h

			initate the voltage on the ADC measuring capacitor when the timing is up	

15.4 ADC and Touch-Key functions

ADC sampling mode configuration steps:

(1). Set the bADC_EN bit in ADC_CFG register as 1, turn on ADC module, and set the bADC_CLK0/1 selection frequency.

(2). Set MASK_ADC_CHAN or MASK_ADC_I_CH in ADC_CHAN register, select external or internal signal channel.

(3). Optional, reset interrupt flag bADC_IF. Optional, if the interrupt mode is used, the interrupt needs to be enabled here.

(4). Set bADC_START in ADC_CTRL register, and start an ADC conversion.

(5). Wait for bADC_START to be changed into 0, or bADC_IF to be set to 1 (if reset to zero before), it indicates that the result data can be read through ADC_DAT after ADC conversion. This data is the value of the input voltage relative to 4095 equal parts of the VDD supply voltage, for example, if the result data is 475, it indicates that the input voltage is approximate to 475/4095 of the VDD voltage. If the VDD supply voltage is also uncertain, another determined reference voltage value can be measured, and the measured input voltage value and the VDD supply voltage value can be calculated proportionally.

(6). If bADC_START is set again, start the next ADC conversion.

(7). If the ADC reference clock frequency is high, resulting in a short sampling time, or high internal resistance of signal source in series, or large Rsw internal resistance due to the low supply voltage, then it is possible that Ca could not sample enough signal voltage and affect the ADC result. The solution is to discard the first ADC data, immediately start the second ADC and use its ADC result data, namely sampling twice.

(8). In case of high accuracy requirement, it is recommended to calibrate before use and eliminate the inherent deviation with software.

Voltage comparrator mode configuration steps:

(1). Set the bCMP_EN bit in ADC_CFG register as 1, turn on the voltage comparator module.
Set MASK_ADC_CHAN, MASK_CMP_CHAN and MASK_ADC_I_CH in ADC_CHAN register, and select the positive and reverse input terminals signals respectively. Multiple combinations can be selected, such as comparison between AIN0~AIN15 and AIN1/AIN2, comparison between AIN0~AIN15 and internal reference voltage, and comparison between AIN1/AIN2 and internal reference voltage, etc.

(3). Optional, reset interrupt flag bCMP_IF. Optional, if the interrupt mode is used, the interrupt needs to be enabled here.

(4). You can inquire the status of the bCMPO bit at any time to obtain the results of the current comparator.

(5). If the bCMP_IF is changed into 1, it indicates that the result of the comparator has changed.

Touch-Key detection steps:

(1). Set the bADC_EN bit in ADC_CFG register as 1, turn on ADC module, and set the bADC_CLK0/1 selection frequency.

(2). Set MASK_ADC_CHAN in ADC_CHAN register, select touch key signal channel.

(3). Select the appropriate charging impulse width according to the actual capacitance of the touch key, and

write into the TKEY_CTRL register. The simple calculation formula is as follows (assume that the external capacitance of the touch key Ckey=25pF, assume VDD=5V, Fsys=12MHz, rough calculation):

count=(Ckey+Cint)*0.7VDD/ITKEY/(2/Fsys)=(25p+15p)*0.35*5*12M/50u=17

TKEY_CTRL=count > 127 ? 127 : count

(4). Optional, if the interrupt mode is used, the interrupt needs to be enabled here.

(5). When the capacitor charge timing of the touch key is reached, CH549 will automatically set bADC_START to start the ADC and measure the voltage on the capacitor

(6). Wait for bTKEY_ACT to be changed into 0, or bADC_IF to be set to 1, it indicates that the result data can be read through ADC_DAT after the charging and ADC conversion. The software then compares this value with that without any key, and determines whether the touch key is pressed or not according to the change in capacitance.

(7). Shift to step (2) as required and select another touch key signal channel for detection.

(8). If the actual capacitance of the touch key is greater than 40pF or the clock frequency is one of 48MHz and 6MHz, then the internal automatic discharge time may be insufficient, and it may be necessary to output the low level of the GPIO at about 1uS to realize full discharge of the above capacitance.

For the above selected external analog signal channel, the GPIO pin where it's located must be set in either high-impedance input mode or open-drain output mode and in output 1 state (equivalent to high-impedance input), Pn_DIR_PU[x]=0, and turn off the pull-up resistor and pull-down resistor.

16. USB controller

16.1 USB controller introduction

CH549 is built-in with USB controller and USB transceiver, with the features as follows:

(1). USB Host functions and USB Device functions;

(2). USB 2.0 full speed 12Mbps and low speed 1.5Mbps;

(3). USB control transmission, batch transmission, interrupt transmission, synchronous/real-time transmission;

(4). Data packet of up to 64 bytes, built-in FIFO, interrupts and DMA.

The USB registers of CH549 are divided into 3 parts, some of which are reused in the host and device modes.

(1). USB global registers;

(2). USB device controller registers;

(3). USB host controller registers;

16.2 Global registers

Table 16.2.1 USB global registers (those marked in grey are controlled by bUC_RESET_SIE reset)

Name	Address	Description	Reset value
USB_C_CTRL	91h	USB type-C configuration channel control register	0000 0000b
USB_INT_FG	D8h	USB interrupt flag register	0010 0000b
USB_INT_ST	D9h	USB interrupt state register (read only)	00xx xxxxb
USB_MIS_ST	DAh	USB miscellaneous state register (read only)	xx10 1000b
USB_RX_LEN	DBh	USB receive length register (read only)	0xxx xxxxb

USB_INT_EN	E1h	USB interrupt enable register	0000 0000b
USB_CTRL	E2h	USB control register	0000 0110b
USB_DEV_AD	E3h	USB device address register	0000 0000b

USB type-C configuration channel control register (USB_C_CTRL):

Bit	Name	Access	Description	Reset value
7	bUCC_PD_MOD	RW	1: Enable USB PD BMC protocol output mode of UCC1 and UCC2 pins. 0: Disable.	0
6	bUCC2_PD_EN	RW	1: Enable the internal 5.1K pull-down resistor of UCC2 pin. 0: Disable.	0
5	bUCC2_PU1_EN	RW	Internal pull-up resistor of UCC2 pin control select high bit	0
4	bUCC2_PU0_EN	RW	Internal pull-up resistor of UCC2 pin control select low bit	0
3	bVBUS_PD_EN	RW	1: Enable the internal 10K pull-down resistor of VBUS pin. 0: Disable.	0
2	bUCC1_PD_EN	RW	1: Enable the internal 5.1K pull-down resistor of UCC1 pin. 0: Disable.	0
1	bUCC1_PU1_EN	RW	Internal pull-up resistor of UCC1 pin control select high bit	0
0	bUCC1_PU0_EN	RW	Internal pull-up resistor of UCC1 pin control select low bit	0

The pull-up resistor inside the UCCn pin is selected by bUCCn_PU1_EN and bUCCn_PU0_EN.

bUCCn_PU1_EN	bUCCn_PU0_EN	Select the pull-up resistor inside the UCCn pin
0	0	Disable the internal pull-up resistor
0	1	Enable internal 56KΩ pull-up resistor, it indicates providing default USB current
1	0	Enable internal 22KΩ pull-up resistor, it indicates providing 1.5A current
1	1	Enable internal 10KΩ pull-up resistor, it indicates providing 3A current

The above mentioned USB type-C pull-up resistor and pull-down resistor are independent from the Pn_DIR_PU port direction control and the port pull-up resistor controlled by the pull-up enable register, when a pin is used for USB type-C, the corresponding port pull-up resistor of the pin should be forbidden. It's recommended to enable the high impedance input mode of the pin (to avoid low level or high level output by the pin).

For detailed control and input detection of USB type-C configuration channels, please refer to USB type-C application commands and routines. For USB PD power transmission control and CRC processing, please refer to USB PD subprograms, application specifications and routines. The CH543 is recommended.

USB interrupt flag register (USB_INT_FG):

Bit	Name	Access	Description	Reset value
7	U_IS_NAK	RO	In USB device mode: 1: NAK busy response is received during current USB	0

			transmission. 0: No NAK response is received	
6	U_TOG_OK	RO	Current USB transmission DATA0/1 synchronous flag matching state 1: Synchronous, and the data is valid. 0: Asynchronous, and the data may be invalid	0
5	U_SIE_FREE	RO	Idle status bit of USB protocol processor 0: Busy, and USB transmission is in progress. 1: USB in idle	1
4	UIF_FIFO_OV	RW	USB FIFO overflow interrupt flag bit 1: FIFO overflow interrupt. 0: No interrupt. Directly write 0 to clear or write 1 to the corresponding bit in the register	0
3	UIF_HST_SOF	RW	SOF timing interrupt flag bit in USB host mode 1: SOF timing interrupt, triggered by SOF packet transmission completion. 0: No interrupt. Directly write 0 to clear or write 1 to the corresponding bit in the register.	0
2	UIF_SUSPEND	RW	USB bus suspending or waking event interrupt flag bit 1: There is an interrupt, triggered by USB suspending event or waking event. 0: No interrupt. Directly write 0 to clear or write 1 to the corresponding bit in the register.	0
1	UIF_TRANSFER	RW	USB transmission completion interrupt flag bit 1: There is an interrupt, triggered by a USB transmission completion. 0: No interrupt. Directly write 0 to clear or write 1 to the corresponding bit in the register.	0
0	UIF_DETECT	RW	USB device connection or disconnection event interrupt flag bit in USB host mode 1: There is an interrupt, triggered by detecting a USB device connection or disconnection. 0: No interrupt. Directly write 0 to clear or write 1 to the corresponding bit in the register.	0
0	UIF_BUS_RST	RW	USB bus reset event interrupt flag bit in USB device mode 1: There is an interrupt, triggered by the USB bus reset event. 0: No interrupt. Directly write 0 to clear or write 1 to the corresponding bit in the register.	0

USB interrupt state register (USB_INT_ST):

Bit	Name	Access	Description	Reset value
7	bUIS_IS_NAK	RO	In USB device mode, if the bit is 1, it indicates that NAK busy response is received during current USB transmission. The same as U_IS_NAK	0

6	bUIS_TOG_OK	RO	Current USB transmission DatA0/1 synchronization flag matching state 1: Synchronous; 0: Asynchronous. The same as U_TOG_OK	0
5	bUIS_TOKEN1	RO	The token PID of the current USB transmission service identifies the high bit in device mode	x
4	bUIS_TOKEN0	RO	The token PID of the current USB transmission service identifies the low bit in device mode	x
[3:0]	MASK_UIS_ENDP	RO	The endpoint number of the current USB transmission service in USB device mode 0000: Endpoint 0; ...; 1111: Endpoint15.	xxxxb
[3:0]	MASK_UIS_H_RES	RO	The response PID identification of the current USB transmission service in USB host mode 0000: The device has no response or time out. Other values: Response PID	xxxxb

BUIS_TOKEN1 and bUIS_TOKEN0 constitutes MASK_UIS_TOKEN, which is used to identify the token PID of the current USB transmission transaction in USB device mode: 00 represents OUT packet; 01 represents SOF packet; 10 represents IN packet; 11 represents SETUP packet.

USB miscellaneous state register (USB_MIS_ST):

Bit	Name	Access	Description	Reset value
7	bUMS_SOF_PRES	RO	SOF packet predictive state bit in USB host mode 1: SOF packet will be sent, and it will be automatically delayed if there are other USB data packet	x
6	bUMS_SOF_ACT	RO	SOF packet transmission state in USB host mode 1: SOF packet is being sent; 0: The transmission is completed, or idle	x
5	bUMS_SIE_FREE	RO	Idle status bit of USB protocol processor 0: Busy, and USB transmission is in progress. 1: Idle. The same as U_SIE_FREE	1
4	bUMS_R_FIFO_RDY	RO	USB receive FIFO data ready status bit 0: The receive FIFO is empty. 1: The receive FIFO is not empty.	0
3	bUMS_BUS_RESET	RO	USB bus reset status bit 0: No USB bus reset at present. 1: USB bus reset is in progress	1
2	bUMS_SUSPEND	RO	USB suspending status bit 0: USB activity at present. 1: There has been no USB activity for some time, and request to be suspended.	0
1	bUMS_DM_LEVEL	RO	In USB host mode, record the state of DM pin when the	0

			USB device is just connected to the USB port 0: Low level. 1: Hhigh level. This bit is used to judge full speed or low speed	
0	bUMS_DEV_ATTACH	RO	USB device connection state bit in USB host mode 1: The port has been connected to the USB device. 0: Not connected.	0

USB reception length register (USB_RX_LEN):

Bit	Name	Access	Description	Reset value
[7:0]	bUSB_RX_LEN	RO	The number of bytes of the data received by the current USB endpoint	xxh

USB interrupt enable register (USB_INT_EN):

Bit	Name	Access	Description	Reset value
7	bUIE_DEV_SOF	RW	1: Enable USB device mode receive SOF packet interrupt. 0: Disable.	0
6	bUIE_DEV_NAK	RW	1: Enable USB device mode receive NAK interrupt. 0: Disable.	0
5	Reserved	RO	Reserved	0
4	bUIE_FIFO_OV	RW	1: Enable FIFO overflow interrupt. 0: Disable.	0
3	bUIE_HST_SOF	RW	1: Enable USB host mode SOF timing interrupt. 0: Disable.	0
2	bUIE_SUSPEND	RW	1: Enable USB bus suspend or wakeup event interrupt. 0: Disable.	0
1	bUIE_TRANSFER	RW	1: Enable USB transmission completion interrupt. 0: Disable.	0
0	bUIE_DETECT	RW	1: Enable USB device connection or disconnection event interrupt in USB host mode. 0: Disable.	0
0	bUIE_BUS_RST	RW	1: Enable USB bus reset event interrupt in USB device mode. 0: Disable.	0

USB control register (USB_CTRL)

Bit	Name	Access	Description	Reset value
7	bUC_HOST_MODE	RW	USB working mode selection bit 0: Select USB device mode (DEVICE). 1: Select USB host mode (HOST)	0
6	bUC_LOW_SPEED	RW	USB bus signal transmission rate selection bit	0

			0: Select full speed 12Mbps. 1: Select low speed 1.5Mbps	
5	bUC_DEV_PU_EN	RW	In USB device mode, USB device enable and internal pull-up resistor control bit. 1: Enable USB device transmission and enable internal pull-up resistor	0
5	bUC_SYS_CTRL1	RW	USB system control high bit	0
4	bUC_SYS_CTRL0	RW	USB system control low bit	0
3	bUC_INT_BUSY	RW	Auto pause enable bit before the USB transmission completion interrupt flag is reset 1: It automatically pauses before the interrupt flag UIF_TRANSFER is reset, and replies to the busy NAK for the device mode . 0: Not pause.	0
2	bUC_RESET_SIE	RW	USB protocol processor software reset control bit 1: It is forced to reset the USB protocol processor and most of the USB control registers, which requires software to clear	1
1	bUC_CLR_ALL	RW	1: Empty USB interrupt flag and FIFO, which requires software to clear	1
0	bUC_DMA_EN	RW	1: Enable USB DMA and DMA interrupt. 0: Disable	0

bUC_HOST_MODE, bUC_SYS_CTRL1 and bUC_SYS_CTRL0 constitutes the USB system control combination:

bUC_HOST_MODE	bUC_SYS_CTRL1	bUC_SYS_CTRL0	USB system control description
0	0	0	Disable USB device function, turn off internal pull-up resistor
0	0	1	Enable USB device function, turn off internal pull-up, and external pull-up needs to be added
0	1	X	Enable USB device function, turn on internal 1.5KΩ pull-up resistor This pull-up resistor is prior to the pull-down resistor, which also can be used in GPIO mode
1	0	0	Select USB host mode, normal working state
1	0	1	Select USB host mode, compulsory DP/DM output SE0 state
1	1	0	Select USB host mode, compulsory DP/DM output J state
1	1	1	Select USB host mode, compulsory DP/DM output K state/wake up

USB device address register (USB_DEV_AD):

Bit	Name	Access	Description	Reset value
7	bUDA_GP_BIT	RW	USB common flag bit, user-defined, and cleared or set by	0

			software	
[6:0]	MASK_USB_ADDR	RW	In host mode, it is the address of the USB device being operated. In device mode, it is the address of the USB device	00h

16.3 Device registers

In USB device mode, CH549 provides 5 sets of bidirectional endpoints, including endpoint0, endpoint1, endpoint2, endpoint3, and endpoint4. The maximum data packet length of all endpoints is 64 bytes.

Endpoint0 is the default endpoint and supports control transfer. Transmission and reception share a 64-byte data buffer area.

Endpoint1, endpoint2, endpoint3 each includes a transmission endpoint IN and a reception endpoint OUT. The transmission and the reception each has a separate 64-byte buffer or double 64-byte data buffer respectively, and they support control transmission, batch transmission, interrupt transmission, and real-time/synchronous transmission.

Endpoint4 includes a transmission endpoint IN and a reception endpoint OUT. The transmission and the reception each has a separate 64-byte data buffer respectively, supporting control transmission, batch transmission, interrupt transmission, and real-time/synchronous transmission.

Each group of endpoints has a control register (UEPn_CTRL) and a length transmission register UEPn_T_LEN(n=0/1/2/3/4), which are used to set the synchronization trigger bit of endpoint, the response to OUT transactions and IN transactions and the length of data to be sent.

As the necessary USB bus pull-up resistor of USB device, it can be set whether to be enabled by the software at any time. When bUC_DEV_PU_EN in the USB control register (USB_CTRL) is set to 1, CH549 will internally connect the pull-up resistor with the DP pin or DM pin of the USB bus based on bUD_LOW_SPEED and enable the USB device function.

When a USB bus reset, USB bus suspend or wakeup event is detected, or when the USB successfully processes either data transmission or reception, the USB protocol processor will set corresponding interrupt flag and generate an interrupt request. The application program can directly query or query and analyze the interrupt flag register USB_INT_FG in the USB interrupt service program, and perform corresponding processing according to UIF_BUS_RST and UIF_SUSPEND. In addition, if UIF_TRANSFER is valid, it is required to continue to analyze the USB interrupt state register USB_INT_ST, and perform the corresponding processing according to the current endpoint number MASK_UIS_ENDP and the current transaction token PID identifier MASK_UIS_TOKEN. If the synchronization trigger bit bUEP_R_TOG of OUT transaction of each endpoint is set in advance, you can judge whether the synchronization trigger bit of the data packet received matches the synchronization trigger bit of the endpoint through U_TOG_OK or bUIS_TOG_OK. If the data is synchronized, the data is valid. If the data is not synchronized, the data should be discarded. After the USB transmit or receive interrupt is processed each time, the synchronization trigger bit of corresponding endpoint should be modified correctly to synchronize the data packet sent next time and detect whether the data packet received next time is synchronized. In addition, bUEP_AUTO_TOG can be set to automatically flip the corresponding synchronization trigger bit after successful transmission or reception.

The data to be sent by each endpoint is in their own buffer, and the length of the data to be sent is independently set in UEPn_T_LEN. The data received by each endpoint is in their own buffer, but the

length of the data received is in the USB reception length register USB_RX_LEN, and it can be distinguished according to the current endpoint number when the USB is receiving an interrupt.

Table 16.3.1 USB device registers (those marked in grey are controlled by RB_UC_RESET_SIE reset)

Name	Address	Description	Reset value
UDEV_CTRL	D1h	USB device physical port control register	00xx 0000b
UEP1_CTRL	D2h	Endpoint1 control register	0000 0000b
UEP1_T_LEN	D3h	Endpoint1 transmission length register	0xxx xxxxb
UEP2_CTRL	D4h	Endpoint2 control register	0000 0000b
UEP2_T_LEN	D5h	Endpoint2 transmission length register	0000 0000b
UEP3_CTRL	D6h	Endpoint3 control register	0000 0000b
UEP3_T_LEN	D7h	Endpoint3 transmission length register	0xxx xxxxb
UEP0_CTRL	DCh	Endpoint0 control register	0000 0000b
UEP0_T_LEN	DDh	Endpoint0 transmission length register	0xxx xxxxb
UEP4_CTRL	DEh	Endpoint4 control register	0000 0000b
UEP4_T_LEN	DFh	Endpoint4 transmission length register	0xxx xxxxb
UEP4_1_MOD	EAh	Endpoint1/4 mode control register	0000 0000b
UEP2_3_MOD	EBh	Endpoint2/3 mode control register	0000 0000b
UEP0_DMA_H	EDh	Endpoint0&4 buffer start address high byte	0000 0xxxb
UEP0_DMA_L	ECh	Endpoint0&4 buffer start address low byte	xxxx xxxxb
UEP0_DMA	ECh	16-bit SFR consists of UEP0_DMA_L and UEP0_DMA_H	0xxxh
UEP1_DMA_H	EFh	Endpoint1 buffer start address high byte	0000 0xxxb
UEP1_DMA_L	EEh	Endpoint1 buffer start address low byte	xxxx xxxxb
UEP1_DMA	EEh	16-bit SFR consists of UEP1_DMA_L and UEP1_DMA_H	0xxxh
UEP2_DMA_H	E5h	Endpoint2 buffer start address high byte	0000 0xxxb
UEP2_DMA_L	E4h	Endpoint2 buffer start address low byte	xxxx xxxxb
UEP2_DMA	E4h	16-bit SFR consists of UEP2_DMA_L and UEP2_DMA_H	0xxxh
UEP3_DMA_H	E7h	Endpoint3 buffer start address high byte	0000 0xxxb
UEP3_DMA_L	E6h	Endpoint3 buffer start address low byte	xxxx xxxxb
UEP3_DMA	E6h	16-bit SFR consists of UEP3_DMA_L and UEP3_DMA_H	0xxxh

USB device physical port control register (UDEV_CTRL), controlled by bUC_RESET_SIE reset:

Bit	Name	Access	Description	Reset value
7	bUD_PD_DIS	RW	USB device port UDP/UDM pin internal pull-down resistor disable bit 1: Disable the internal pull-down resistor. 0: Enable the internal pull-down resistor. This bit also can be used in GPIO mode to provide pull-down resistor	0

6	Reserved	RO	Reserved	0
5	bUD_DP_PIN	RO	Current UDP pin status 0: Low level; 1: High level.	x
4	bUD_DM_PIN	RO	Current UDM pin status 0: Low level; 1: High level.	x
3	Reserved	RO	Reserved	0
2	bUD_LOW_SPEED	RW	USB device physical port low speed mode enable bit 1: Select 1.5Mbps low speed mode. 0: Select 12Mbps full speed mode.	0
1	bUD_GP_BIT	RW	USB device mode common flag bit, user-defined. Cleared or set by software	0
0	bUD_PORT_EN	RW	USB device physical port enable bit 1: Enable the physical port. 0: Disable the physical port.	0

Endpoint n control register (UEPn_CTRL):

Bit	Name	Access	Description	Reset value
7	bUEP_R_TOG	RW	The synchronization trigger bit expected by the receiver of USB endpoint n (handle SETUP/OUT services). 0: Expected DATA0. 1: Expected DATA1.	0
6	bUEP_T_TOG	RW	The synchronization trigger bit prepared by the transmitter of USB endpoint n (handle IN services). 0: Transmit DATA0. 1: Transmit DATA1.	0
5	Reserved	RO	Reserved	0
4	bUEP_AUTO_TOG	RW	Synchronization trigger bit automatic toggle enable 1: Automatic turnonver of the corresponding synchronization trigger bit after sucessful transmission or reception. 0: No automatic turnover, but manual switch is allowed. Only support single-receiving or single-sending modes with endpoint1/2/3. It is not supported if RX EN and TX EN are both 1 for the same endpoint	0
3	bUEP_R_RES1	RW	Response control high bit by the receiver of endpoint n to SETUP/OUT services	0
2	bUEP_R_RES0	RW	Response control low bit by the receiver of endpoint n to SETUP/OUT services	0
1	bUEP_T_RES1	RW	Response control high bit by the transmitter of endpoint n to IN services	0
0	bUEP_T_RES0	RW	Response control low bit by the transmitter of endpoint n to IN services	0

MASK_UEP_R_RES, consisting of bUEP_R_RES1 and bUEP_R_RES0, is used to control the response of the receiver of endpoint n to the SETUP/OUT services: 00 represents reply ACK or ready. 01 represents timeout/no response, which is used to realize real-time/synchronous transmission of non-endpoint 0. 10 represents reply NAK or busy. 11 represents reply STALL or error.

MASK_UEP_T_RES, consisting of bUEP_T_RES1 and bUEP_T_RES0, is used to control the response of the transmitter of endpoint n to the IN services: 00 represents reply DATA0/DATA1 or data ready or expected ACK. 01 represents reply DATA0/DATA1 and expected no response, which is used to realize real-time/synchronous transmission of non-endpoint 0. 10 represents reply NAK or busy. 11 represents reply STALL or error.

Endpoint n transmission length register (UEPn_T_LEN):

Bit	Name	Access	Description	Reset value
[7:0]	bUEPn_T_LEN	RW	Set the number of data bytes that USB endpoint n is ready to send (n=0/1/3/4)	xxh
	bUEP2_T_LEN		Set the number of data bytes that USB endpoint 2 is ready to send	00h

USB endpoint1/4 mode control register (UEP4_1_MOD):

Bit	Name	Access	Description	Reset value
7	bUEP1_RX_EN	RW	0: Disable endpoint1 reception. 1: Enable endpoint1 reception (OUT).	0
6	bUEP1_TX_EN	RW	0: Disable endpoint1 transmission. 1: Enable endpoint1 transmission (IN).	0
5	Reserved	RO	Reserved	0
4	bUEP1_BUF_MOD	RW	Endpoint1 data buffer mode control bit	0
3	bUEP4_RX_EN	RO	0: Disable endpoint4 reception. 1: Enable endpoint4 reception (OUT).	0
2	bUEP4_TX_EN	RW	0: Disable endpoint4 transmission. 1: Enable endpoint4 transmission (IN).	0
[1:0]	Reserved	RO	Reserved	00b

The data buffer modes of USB endpoint0/4 are controlled by a combination of bUEP4_RX_EN and bUEP4_TX_EN, refer to the following table.

Table 16.3.2 Endpoint0/4 buffer mode

bUEP4_RX_EN	bUEP4_TX_EN	Structure description: arrange from low to high with UEP0 DMA as the start address
0	0	Endpoint0 single 64-byte transmit/receive shared buffer (IN and OUT)
1	0	Endpoint0 single 64-byte transmit/receive shared buffer. Endpoint4 single 64-byte receive buffer (OUT)
0	1	Endpoint0 single 64-byte transmit/receive shared buffer. Endpoint4 single 64-byte transmit buffer (IN)

1	1	Endpoint0 single 64-byte transmit/receive shared buffer. Endpoint4 single 64-byte receive buffer (OUT). Endpoint4 single 64-byte transmit buffer (IN). All 192 bytes are arranged as follows: UEP0_DMA+0 address: endpoint0 transceiver; UEP0_DMA+64 address: endpoint4 receiver; UEP0_DMA+128: endpoint4 transmitter.

USB endpoint2/3 mode control register (UEP2_3_MOD):

Bit	Name	Access	Description	Reset value
7	bUEP3_RX_EN	RW	0: Disable endpoint3 reception. 1: Enable endpoint3 reception (OUT).	0
6	bUEP3_TX_EN	RW	0: Disable endpoint3 transmission. 1: Enable endpoint 3 transmission (IN).	0
5	Reserved	RO	Reserved	0
4	bUEP3_BUF_MOD	RW	Endpoint3 data buffer mode control bit	0
3	bUEP2_RX_EN	RO	0: Disable endpoint2 reception. 1: Enable endpoint2 reception (OUT).	0
2	bUEP2_TX_EN	RW	0: Disable endpoint2 transmission. 1: Enable endpoint2 transmission (IN).	0
1	Reserved	RO	Reserved	0
0	bUEP2_BUF_MOD	RW	Endpoint2 data buffer mode control bit	0

The data buffer modes of USB endpoint1/2/3 are controlled by a combination of bUEPn_RX_EN, bUEPn_TX_EN and bUEPn_BUF_MOD(n=1/2/3) respectively, refer to the following table. In the double-64 byte buffer mode, the first 64 bytes buffer will be selected based on bUEP_*_TOG=0 and the last 64 bytes buffer will be selected based on bUEP_*_TOG=1 during USB data transmission to realize automatic switch.

Table 16.3.3 Endpoint n buffer mode (n=1/2/3)

bUEPn_RX_EN	bUEPn_TX_EN	bUEPn_BUF_MOD	Structure description: arrange from low to high with UEPn_DMA as the start address
0	0	x	Endpoint is disabled, and the UEPn_DMA buffer is not used
1	0	0	Single 64-byte receive buffer (OUT)
1	0	1	Double 64-byte receive buffers, selected by bUEP_R_TOG.
0	1	0	Single 64-byte transmit buffer (IN)
0	1	1	Double 64-byte transmit buffers, selected by bUEP_T_TOG.
1	1	0	Single 64-byte receive buffer (OUT). Single 64-byte transmit buffer (IN)
1	1	1	Double 64-byte receive buffers, selected by bUEP_R_TOG. Double 64-byte transmit buffers, selected by bUEP_T_TOG.

			All 256 bytes are arranged as follows: UEPn_DMA+0 address: endpoint receiver when bUEP_R_TOG=0; UEPn_DMA+64 address: endpoint receiver when bUEP_R_TOG=1; UEPn_DMA+128 address: endpoint transmitter when bUEP_T_TOG=0; UEPn_DMA+192 address: endpoint transmitter when bUEP_T_TOG=1

USB endpoint n buffer start address (UEPn_DMA)(n=0/1/2/3):

Bit	Name	Access	Description	Reset value
[7:0]	UEPn_DMA_H	RW	Endpoint n buffer start address high byte, only the lower 3 bits are valid, and the higher 5 bits are fixed to be 0	0xh
[7:0]	UEPn_DMA_L	RW	Endpoint n buffer area start address low byte	xxh

Note: the length of the buffer that receives data >= min (maximum data packet length possibly received + 2 bytes, 64 bytes)

16.4 Host registers

In USB host mode, CH549 provides 1 set of bidirectional host endpoints, including a transmission endpoint (OUT) and a reception endpoint (IN). The maximum data packet length is 64 bytes, supporting control transmission, batch transmission, interrupt transmission, and real-time/synchronous transmission.

Each USB transaction initiated by host endpoint, and it will automatically set the interrupt flag UIF_TRANSFER after processing. The application program can directly query or query and analyze the interrupt flag register USB_INT_FG in the USB interrupt service program, and perform corresponding processing according to each interrupt flag. In addition, if UIF_TRANSFER is valid, it is required to continue to analyze the USB interrupt state register (USB_INT_ST), and perform the corresponding processing according to the response PID identification (MASK_UIS_H_RES) of the current USB transmission transaction.

If the synchronization trigger bit (bUH_R_TOG) of IN transaction of host reception endpoint is set in advance, you can judge whether the synchronization trigger bit of the data packet received matches the synchronization trigger bit of the endpoint through U_TOG_OK or bUIS_TOG_OK. If the data is synchronized, the data is valid. If the data is not synchronized, the data should be discarded. After the USB transmit or receive interrupt is processed each time, the synchronization trigger bit of corresponding host endpoint should be modified correctly to synchronize the data packet sent next time and detect whether the data packet received next time is synchronized. In addition, bUEP_AUTO_TOG can be set to automatically flip the corresponding synchronization trigger bit after successful transmission or reception.

USB host token setting register (UH_EP_PID) is the reuse of the USB endpoint 2 control register in USB device mode, which is used to set the endpoint number of the target device being operated and the token PID packet identification of the USB transmission transaction. The data corresponding to the SETUP token and OUT token is provided by the host transmission endpoint. The data to be sent is in the UH_TX_DMA buffer, and the length of the data to be sent is set in UH_TX_LEN. The data corresponding to the IN token is returned by the target device to the host reception endpoint, the received data is stored in the

UH_RX_DMA buffer, and the length of the received data is stored in USB_RX_LEN.

Table 16.4.1 USB host registers (those marked in grey are controlled by RB_UC_RESET_SIE reset)

Name	Address	Description	Reset value
UHOST_CTRL	D1h	Physical port control register of USB host	00xx 0000b
UH_SETUP	D2h	USB host auxiliary setting register	0000 0000b
UH_RX_CTRL	D4h	USB host reception endpoint control register	0000 0000b
UH_EP_PID	D5h	USB host token setting register	0000 0000b
UH_TX_CTRL	D6h	USB host transmission endpoint control register	0000 0000b
UH_TX_LEN	D7h	USB host transmission length register	0xxx xxxxb
UH_EP_MOD	EBh	USB host endpoint mode control register	0000 0000b
UH_RX_DMA_H	E5h	USB host receive buffer start address high byte	0000 0xxxb
UH_RX_DMA_L	E4h	USB host receive buffer start address low byte	xxxx xxxxb
UH_RX_DMA	E4h	UH_RX_DMA_L and UH_RX_DMA_H constitute a 16-bit SFR	0xxxh
UH_TX_DMA_H	E7h	USB host transmit buffer start address high byte	0000 0xxxb
UH_TX_DMA_L	E6h	USB host transmit buffer start address low byte	xxxx xxxxb
UH_TX_DMA	E6h	UH_TX_DMA_L and UH_TX_DMA_H constitute a 16-bit SFR	0xxxh

USB host physical port control register (UHOST_CTRL), controlled by bUC_RESET_SIE reset:

Bit	Name	Access	Description	Reset value
7	bUH_PD_DIS	RW	USB host port UDP/UDM pin internal pull-down resistor disable bit 1: Disable the internal pull-down resistor. 0: Enable the internal pull-down resistor. It also can be used in GPIO mode to provide pull-down resistor	0
6	Reserved	RO	Reserved	0
5	bUH_DP_PIN	RO	Current UDP pin status 0: Low level; 1: High level.	x
4	bUH_DM_PIN	RO	Current UDM pin status 0: Low level; 1: High level.	x
3	Reserved	RO	Reserved	0
2	bUH_LOW_SPEED	RW	USB host port low speed mode enable bit 1: Select 1.5Mbps low speed mode. 0: Select 12Mbps full speed mode.	0
1	bUH_BUS_RESET	RW	USB host port bus reset control bit 1: Force the host port to output USB bus reset. 0: End output.	0
0	bUH_PORT_EN	RW	USB host port enable bit 0: Disable the host port.	0

			1: Enable the host port. The bit is reset automatically when the USB device is disconnected	

USB host auxiliary setting register (UH_SETUP):

Bit	Name	Access	Description	Reset value
7	bUH_PRE_PID_EN	RW	Low speed preamble packet PRE PID enable bit 1: Enable the USB host to communicate with the low speed USB device via external HUB. 0: Disable the low speed preamble packet, and there should be no HUB between the USB host and low speed USB device	0
6	bUH_SOF_EN	RW	Automatic generation of SOF packet enable bit 1: USB host automatically generates the SOF packet. 0: No SOF packet generated automatically, but it can be generated manually	0
[5:0]	Reserved	RO	Reserved	00h

USB host reception endpoint control register (UH_RX_CTRL):

Bit	Name	Access	Description	Reset value
7	bUH_R_TOG	RW	Synchronization trigger bit expected by the receiver of USB host (handle IN services). 0: Expected DATA0. 1: Expected DATA1.	0
[6:5]	Reserved	RO	Reserved	00b
4	bUH_R_AUTO_TOG	RW	Auto toggle bUH_R_TOG enable control bit 1: Auto turnover of the bUH_R_TOG flag after successfully received by USB host. 0: No auto turnover, but manual switch is allowed	0
3	Reserved	RO	Reserved	0
2	bUH_R_RES	RW	Response control bit of USB host receiver for IN transaction 0: Reply ACK or ready. 1: No reponse, which is used for real-time/synchronous transmission with non-endpoint 0 of the target device	0
[1:0]	Reserved	RO	Reserved	00b

USB host token setting register (UH_EP_PID):

Bit	Name	Access	Description	Reset value
[7:4]	MASK_UH_TOKEN	RW	Set the token PID packet identification of this USB transmission transaction	0000b

[3:0]	MASK_UH_ENDP	RW	Set the endpoint number of the target device being operated this time	0000b

USB host transmission endpoint control register (UH_TX_CTRL):

Bit	Name	Access	Description	Reset value
7	Reserved	RO	Reserved	0
6	bUH_T_TOG	RW	Synchronization trigger bit prepared by the transmitter of USB host (handle SETUP/OUT services). 0: Transmit DATA0. 1: Transmit DATA1.	0
5	Reserved	RO	Reserved	0
4	bUH_T_AUTO_TOG	RW	Auto toggle bUH_T_TOG enable control bit 1: Auto turnover of the bUH_T_TOG flag after successfully transmitted by the USB host. 0: No auto turnover, but manual switch is allowed	0
[3:1]	Reserved	RO	Reserved	000b
0	bUH_T_RES	RW	Response control bit of USB host transmitter for SETUP/OUT transaction 0: Expect reply ACK or ready. 1: Expect no reponse, which is used for real-time/synchronous transmission with non-endpoint0 of the target device	0

USB host length transmission register (UH_TX_LEN):

Bit	Name	Access	Description	Reset value
[7:0]	UH_TX_LEN	RW	Set the number of data bytes that USB host transmission endpoint is ready to send	xxh

USB host endpoint mode control register (UH_EP_MOD):

Bit	Name	Access	Description	Reset value
7	Reserved	RO	Reserved	0
6	bUH_EP_TX_EN	RW	0: Disable the USB host transmission endpoint to transmit data. 1: Enable the USB host transmission endpoint to transmit data (SETUP/OUT)	0
5	Reserved	RO	Reserved	0
4	bUH_EP_TBUF_MOD	RW	USB host transmission endpoint data buffer mode control bit	0
3	bUH_EP_RX_EN	RO	0: Disable the USB host reception endpoint to receive data. 1: Enable the USB host reception endpoint to receive	0

			data (IN)	
[2:1]	Reserved	RO	Reserved	00b
0	bUH_EP_RBUF_MOD	RW	USB host reception endpoint data buffer mode control bit	0

The data buffer modes of USB host transmission endpoint are controlled by a combination of bUH_EP_TX_EN and bUH_EP_TBUF_MOD, refer to the following table.

Table 16.4.2 Host transmit buffer mode

bUH_EP_TX_EN	bUH_EP_TBUF_MOD	Structure description: Take UH_TX_DMA as the start address
0	x	Endpoint is disabled, and UH_TX_DMA buffer is not used
1	0	Single 64-byte transmit buffer (SETUP/OUT)
1	1	Double 64-byte transmit buffers, selected by bUH_T_TOG: When bUH_T_TOG=0, select the first 64 bytes of the buffer. When bUH_T_TOG=1, select the last 64 bytes of the buffer

The data buffer modes of USB host reception endpoint are controlled by a combination of bUH_EP_RX_EN and bUH_EP_RBUF_MOD, refer to the following table.

Table 16.4.3 Host receive buffer mode

bUH_EP_RX_EN	bUH_EP_RBUF_MOD	Structure description: Take UH_RX_DMA as the start address
0	x	Endpoint is disabled, and UH_RX_DMA buffer is not used
1	0	Single 64-byte receive buffer (IN)
1	1	Double 64-byte receive buffers, selected by bUH_R_TOG: When bUH_R_TOG=0 select the first 64 bytes of the buffer. When bUH_R_TOG=1, select the last 64 bytes of the buffer

USB host receive buffer start address (UH_RX_DMA)

Bit	Name	Access	Description	Reset value
[7:0]	UH_RX_DMA_H	RW	USB host receive buffer start address high byte, only the lower 3 bits are valid, and the higher 5 bits are fixed to be 0	0xh
[7:0]	UH_RX_DMA_L	RW	USB host receive buffer start address low byte	xxh

USB host transmit buffer start address (UH_TX_DMA):

Bit	Name	Access	Description	Reset value
[7:0]	UH_TX_DMA_H	RW	USB host transmit buffer start address high byte, only the lower 3 bits are valid, and the higher 5 bits are fixed to 0	0xh
[7:0]	UH_TX_DMA_L	RW	USB host transmit buffer start address low byte	xxh

17. Parameters

17.1 Absolute maximum ratings

Stresses at or above the absolute maximum ratings listed in the table below may cause permanent damage to the device.

Symbol	Parameter description		Min.	Max.	Unit
TA	Operating ambient temperature	Fsys<40MHz	-40	85	℃
		Fsys=48MHz and bLDO_CORE_VOL=1 (if necessary)	-40	70	℃
		Fsys=48MHz and bLDO_CORE_VOL=0	-20	70	℃
TAROM	Ambient temperature for Flash-ROM/EEPROM write operation (recommended)		-20	85	℃
TS	Ambient temperature during storage		-55	125	℃
VDD	Supply voltage (VDD is connected to power, GND to ground)		-0.4	7.0	V
V33	Internal USB supply voltage		-0.4	VDD+0.4	V
VIO	Voltage on input/output pins		-0.4	VDD+0.4	V
VIOU	Voltage on UDP/UDM pin		-0.4	V33+0.4	V
VIOHV	Voltage on P5.5/HVOD pin		-0.4	13	V

17.2 Electrical characteristics (5V)

Test conditions: TA=25℃, VDD=5V, Fsys=12MHz

Symbol	Parameter description		Min.	Typ.	Max.	Unit
VDD5	VDD pin supply voltage	V33 is only connects to a capacitor externally	3.7	5	6.5	V
V33	Internal power regulator output voltage (Automatically short connected to VDD during sleep)	TA=-15~65℃	3.23	3.3	3.37	V
		TA=-40~85℃	3.2	3.3	3.4	V
ICC48M5	Total supply current when Fsys=48MHz		6.3	7.4		mA
ICC12M5	Total supply current when Fsys=12MHz		2.5	3.0		mA
ICC750K5	Total supply current when Fsys=750KHz		1.4	1.6		mA
ISLP5	Total supply current after standby/normal sleep			1.1	1.4	mA
ISLP5L	Total supply current after power off/deep sleep bLDO_3V3_OFF=1, LDO disabled			4	13	uA
IADC5	ADC operating current			200	800	uA
ICMP5	CMP operating current			100	500	uA
ITKEY5	Touch key capacitance charging current		35	50	70	uA
VIL5	Input low level voltage		0		1.2	V
VIH5	Input high level voltage		2.4		VDD	V
VOL5	Output low level voltage (I_{IL}=15mA)				0.4	V
VOH5	Output high level voltage (I_{OH}=6mA)		VDD-0.4			V

VOH5U	UDP/UDM high level output voltage (I_{OH}=8mA)	V33-0.4			V
VHVOD	Voltage on P5.5/HVOD pin (not output/high impedance)	0		12.6	V
IIN	Input current without pull-up resistor	-5	0	5	uA
IDN5	Input current with pull-down resistor	-35	-70	-140	uA
IUP5	Input current with pull-up resistor	35	70	140	uA
IUP5X	Input current with pull-up resistor from low to high	250	400	600	uA
Rsw5	ON resistance of the analog switch of ADC and other modules	500	700	1350	Ω
Vpot	Power on reset threshold	2.3	4.0	4.6	V

17.3 Electrical characteristics (3.3V)

Test conditions: TA=25℃, VDD=V33=3.3V, Fsys=12MHz

Symbol	Parameter description		Min.	Typ.	Max.	Unit
VDD3	VDD pin Power supply voltage	V33 connected to VDD, and turn on USB	3.0	3.3	3.6	V
		V33 connected to VDD, and turn off USB	2.7	3.3	3.6	V
ICC48M3	Total supply current when Fsys=48MHz		6.3	7.4		mA
ICC12M3	Total supply current when Fsys=12MHz		2.5	3.0		mA
ICC750K3	Total supply current when Fsys=750KHz		1.4	1.6		mA
ISLP3	Total supply current after standby/normal sleep			1.1	1.3	mA
ISLP3L	bLDO_3V3_OFF=1, turn off LDO, Total supply current after power off/deep sleep			2	9	uA
IADC3	ADC operating current			180	700	uA
ICMP3	CMP operating current			70	300	uA
ITKEY3	Touch key capacitance charging current		35	50	70	uA
VIL3	Input low level voltage		0		0.8	V
VIH3	Input high level voltage		1.9		VDD	V
VOL3	Output low level voltage (I_{IL}=10mA)				0.4	V
VOH3	Output high level voltage (I_{OH}=4mA)		VDD-0.4			V
VOH3U	UDP/UDM output high level voltage (I_{OH}=8mA)		V33-0.4			V
VHVOD	Voltage on P5.5/HVOD pin (not output/high impedance)		0		12.6	V
IIN	Input current without pull-up resistor		-5	0	5	uA
IDN3	Input current with pull-down resistor		-15	-30	-60	uA
IUP3	Input current with pull-up resistor		15	30	60	uA
IUP3X	Input current with pull-up resistor from low to high		100	170	250	uA
Rsw3	ONresistance of the analog switch of ADC and other modules		600	1000	2500	Ω
Vpot	Power on reset threshold		2.3	2.7	3.0	V

17.4 Timing parameters

Test conditions: TA=25℃, VDD=5V or VDD=V33=3.3V, Fsys=12MHz

Symbol	Parameter description		Min.	Typ.	Max.	Unit
Fxt	External crystal frequency or XI input clock frequency		6	24	24	MHz
Fosc	Internal clock frequency after calibration when VDD>=3V	TA=-15~65℃	23.64	24	24.36	MHz
		TA=-40~85℃	23.5	24	24.5	MHz
Fosc3	Internal clock frequency after calibration when VDD<3V		23.28	24	24.72	MHz
Fpll	Frequency after PLL		24	96	96	MHz
Fusb4x	USB sampling clock frequency for the USB host		47.98	48	48.02	MHz
	USB sampling clock frequency for the USB device		47.04	48	48.96	MHz
Fsys	System clock frequency (VDD>=3V)		0.1	12	48	MHz
	System clock frequency (VDD<3V)		0.1	12	24	MHz
Tpor	Power on reset delay		8	11	15	mS
Trst	External input valid reset signal width		70			nS
Trdl	Thermal reset delay		20	30	50	uS
Twdc	Watchdog overflow/Timer calculation formula		131072 * (0x100 - WDOG_COUNT) / Fsys			
Tusp	Automatically suspend time in USB host mode		2	3	4	mS
	Automatically suspend time in USB device mode		4	5	6	mS
Twaksb	Wake-up completion time after chip standby/normal sleep		0.5	0.8	3	uS
Twakdp	Wake-up completion time after chip power off/deep sleep		120	200	1000	uS

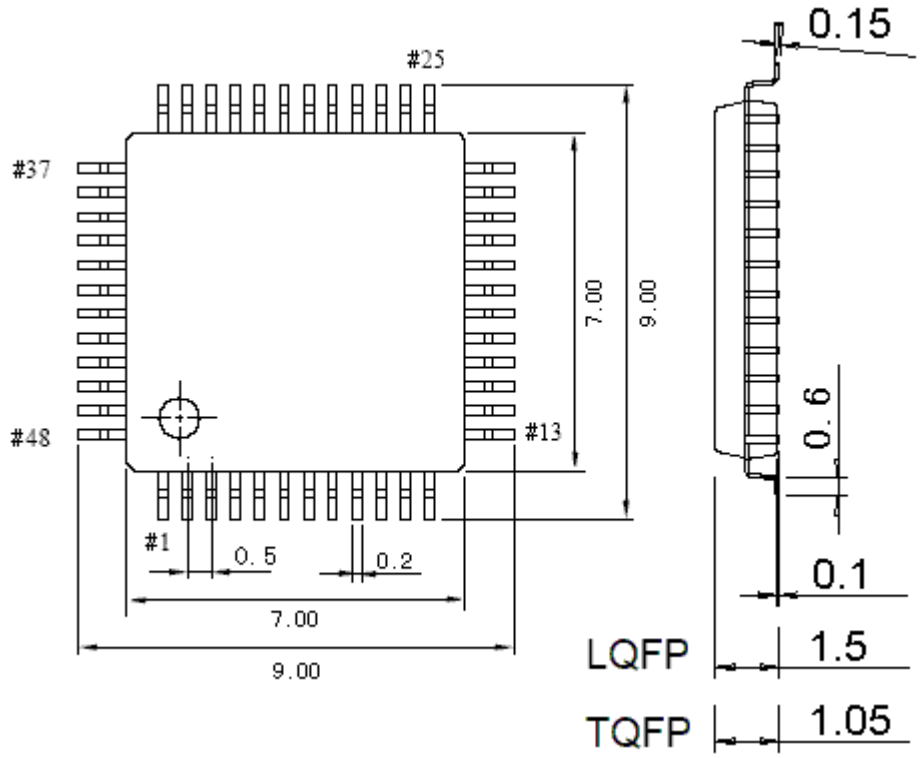
17.5 Other parameters

Test conditions: TA=25℃, VDD=4.5V~5.5V or VDD=V33=3.0V~3.6V

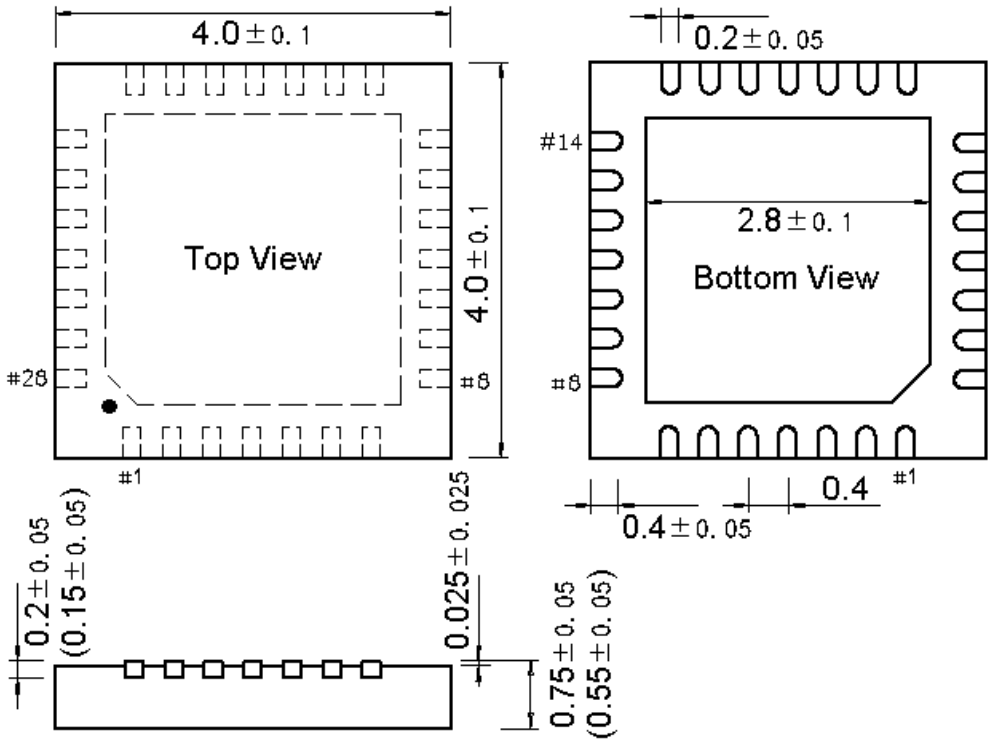
Symbol	Parameter description	Min.	Typ.	Max.	Unit
RTS	Measurement range of TS temperature sensor	-40		90	℃
ATSC	Measurement error of temperature sensor calibrated by software		±7		℃
CTSV	Sensitivity of temperature sensor (voltage/temperature coefficient)	4	5	6	mV/℃
TERPG	Time to perform single erase/program operation on Flash-ROM/EEPROM	2	5	8	mS
NEPCE	Erase/program cycle endurance	10K	Not guaranteed 100K		times
TDR	Data hold capability of Flash-ROM/EEPROM	10			years
VESD	ESD voltage on I/O pins	4K	Not guaranteed 8K		V

18. Package information

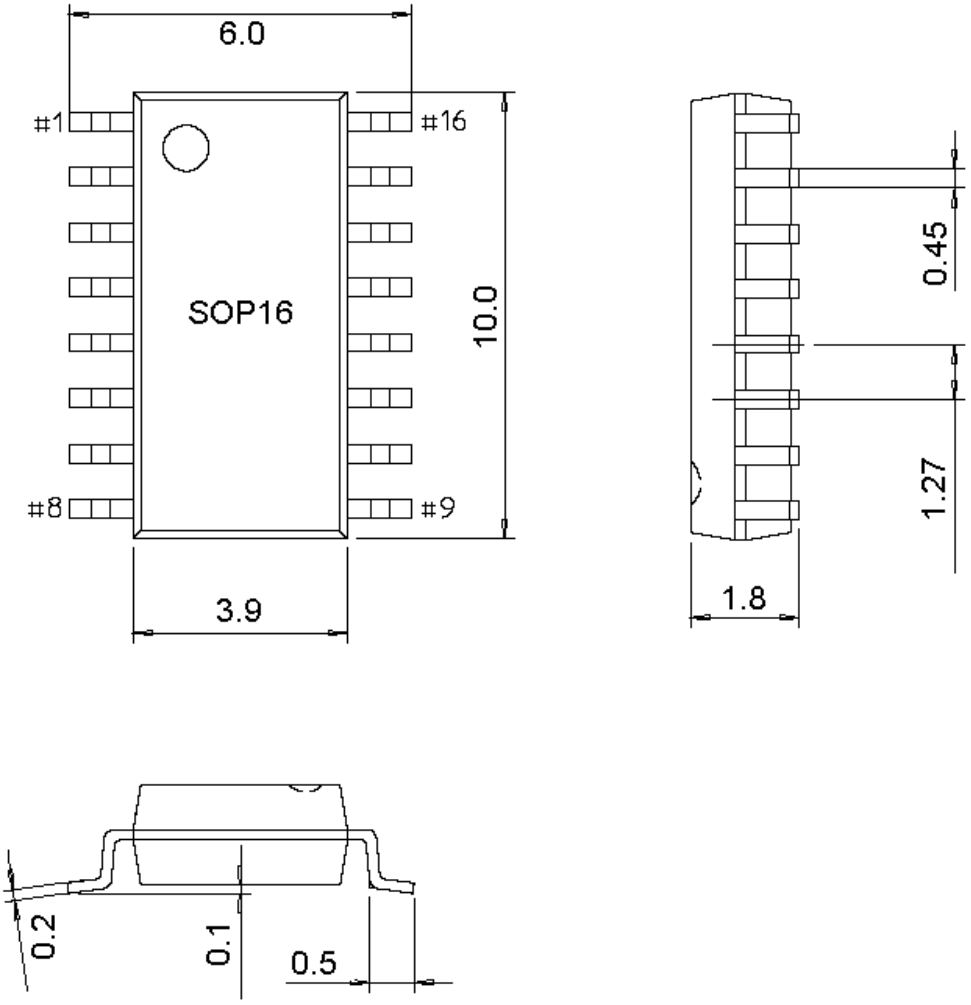
18.1 LQFP48-7*7



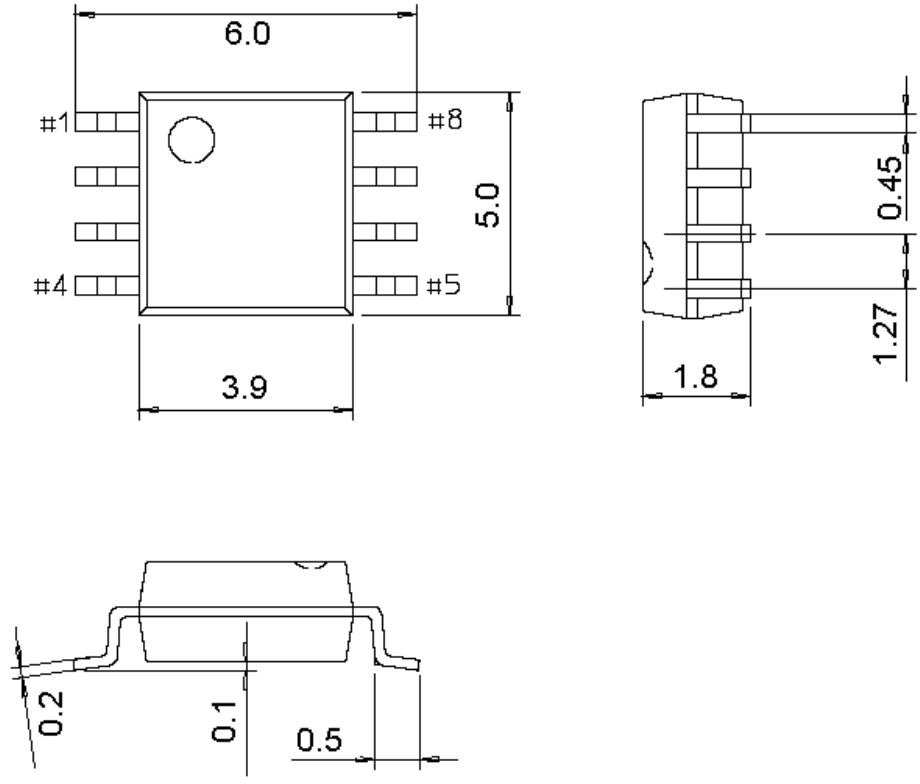
18.2 QFN28-4*4



18.3 SOP16-150mil



18.4 SOP8-150mil



19. Revision history

Revision	Date	Description
V0.99	September 27, 2017	Initial release
V1.0	March 7, 2018	Official release
V1.1	November 13, 2018	A_INV introduction modified. Routine file name deleted. VDD3 modified. INTX added.
V1.2	May 29, 2019	The register is renamed POWER CFG, it is recommended to disable global interrupt during sleep, Note that V33 is automatically short circuited to VDD during sleep. Size marked in package figures.
V1.3	December 20, 2019	Clerical error modified in Section 15.4 (5). Clerical error modified in Section 16.4 (UH_TX_DMA).
V1.4	June 26, 2020	Section 16.3 modified. Some parameters in Section 17.2 and Section 17.3 are slightly adjusted.
V1.5	November 12, 2020	Package of CH548N added.
V1.6	October 15, 2021	The system clock frequency is limited to not exceed 48MHz. Note that USB pins are not connected to external resistors in series.
V1.7	January 28, 2022	Optimize the expression about bit reset: Directly write 0 to clear or write 1 to the corresponding bit in the register.