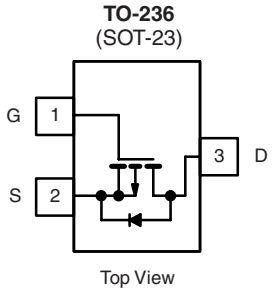
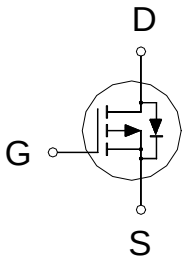
P-Channel Logic Level Enhancement Mode Field Effect Transistor

Product Summary:

BV_{DSS}	-30V
$R_{DSON\ (MAX.)}$	52mΩ
I_D	-4.3A





Pb-Free Lead Plating & Halogen Free

MARKING
5103S23

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_A = 25 °C	I_D	-4.3	A
Pulsed Drain Current[1]		I_{DM}	-20	
Power Dissipation	T_A = 25 °C	P_D	1.5	W
Operating Junction & Storage Temperature Range		T_j, T_{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Ambient	$R_{\theta JA}$		84	°C / W

ELECTRICAL CHARACTERISTICS (T_A = 25 °C, Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250μA	-30			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250μA	-1		-3	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0V, V_{GS} = ±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -24V, V_{GS} = 0V			-1	μA
On-State Drain Current[1]	$I_{D(ON)}$	V_{DS} = -5V, V_{GS} = -10V	-4.3			A
Drain-Source On-State Resistance[1]	$R_{DS(ON)}$	V_{GS} = -10V, I_D = -4A		40	52	mΩ
		V_{GS} = -4.5V, I_D = -3A		48	90	
Forward Transconductance[1]	g_{fs}	V_{DS} = -5V, I_D = -1A		10		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = -15V, f = 1MHz		700		pF
Output Capacitance	C_{oss}			120		
Reverse Transfer Capacitance	C_{rss}			75		
Total Gate Charge[1,2]	Q_g	V_{DS} = -15V, V_{GS} = -10V, I_D = -4A		14		nC
Gate-Source Charge[1,2]	Q_{gs}			3.1		
Gate-Drain Charge[1,2]	Q_{gd}			3		
Turn-On Delay Time[1,2]	$t_{d(on)}$	V_{DS} = -15V, V_{GS} = -10V, R_{GS} = 3Ω		9		nS
Rise Time[1,2]	t_r			5		
Turn-Off Delay Time[1,2]	$t_{d(off)}$			28		
Fall Time[1,2]	t_f			13.5		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS (T_C = 25 °C)						
Continuous Current	I_S				4.3	A
Pulsed Current[3]	I_{SM}				-12	
Forward Voltage[1]	V_{SD}	I_F = I_S, V_{GS} = 0V			-1.2	V

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production

TYPICAL CHARACTERISTICS

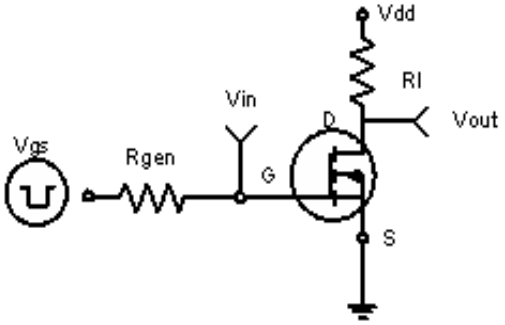


Figure 1:Switching Test Circuit

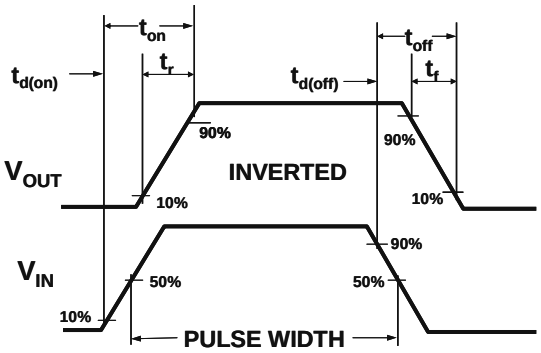
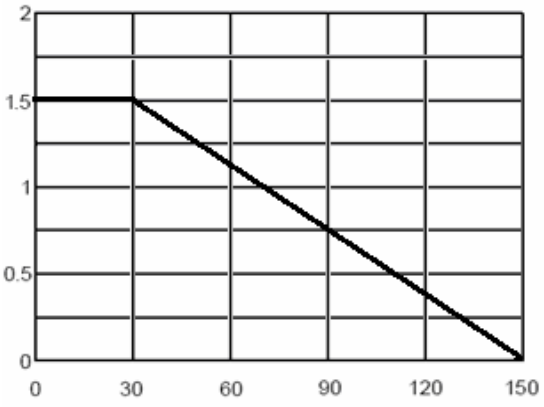
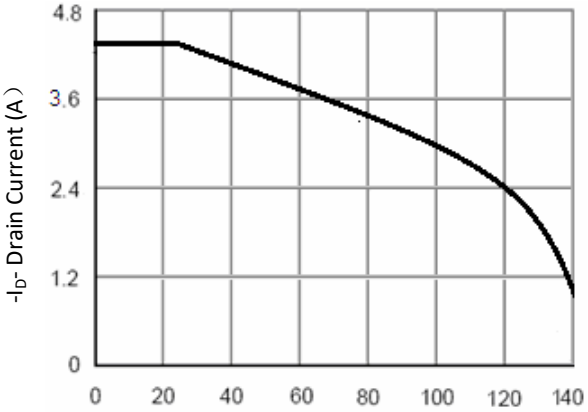


Figure 2:Switching Waveforms



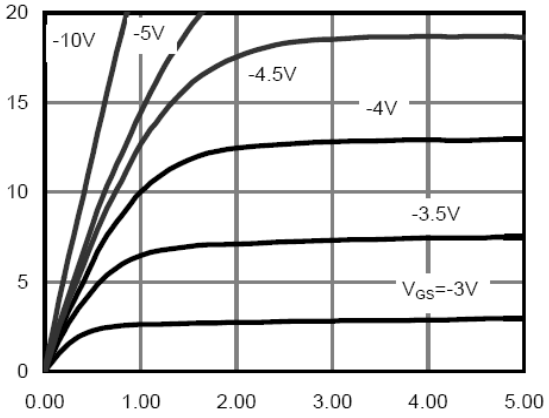
T_J-Junction Temperature(℃)

Figure 3 Power Dissipation



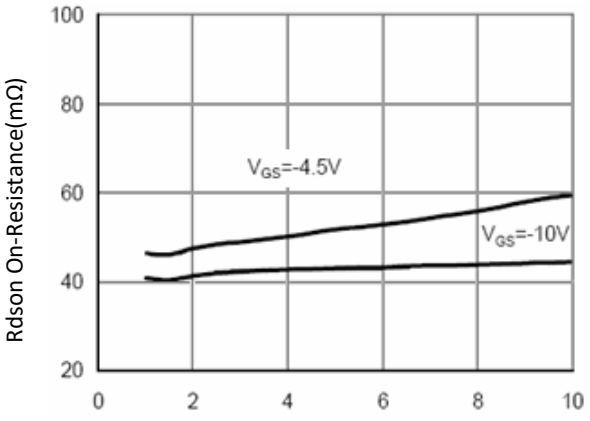
T_J-Junction Temperature(℃)

Figure 4 Drain Current



-Vds Drain-Source Voltage (V)

Figure 5 Output Characteristics



$-I_D$- Drain Current (A)

Figure 6 Drain-Source On-Resistance

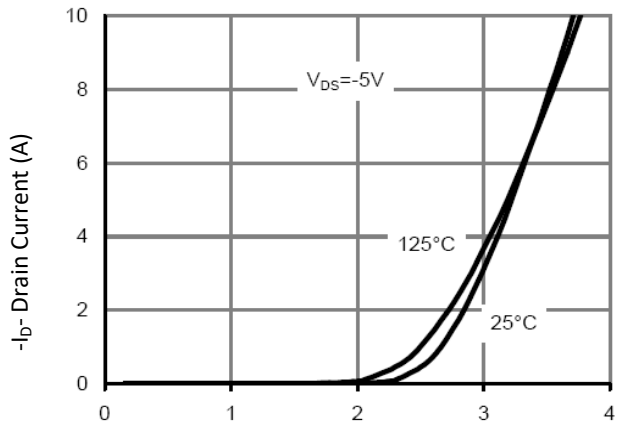


Figure 7 Transfer Characteristics

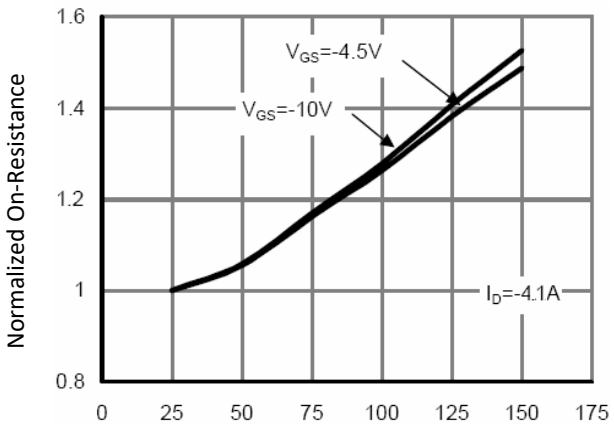


Figure 8 Drain-Source On-Resistance

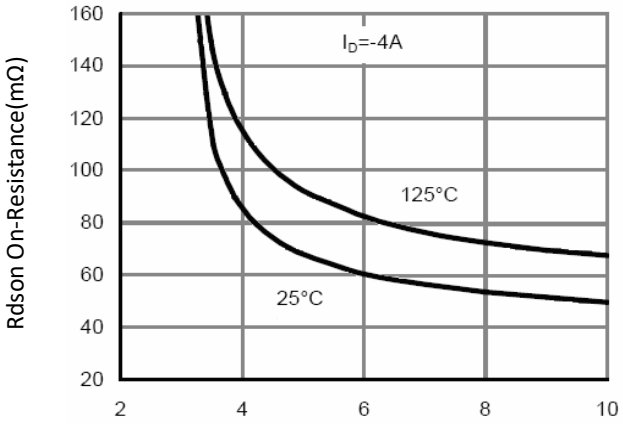


Figure 9 Rdson vs Vgs

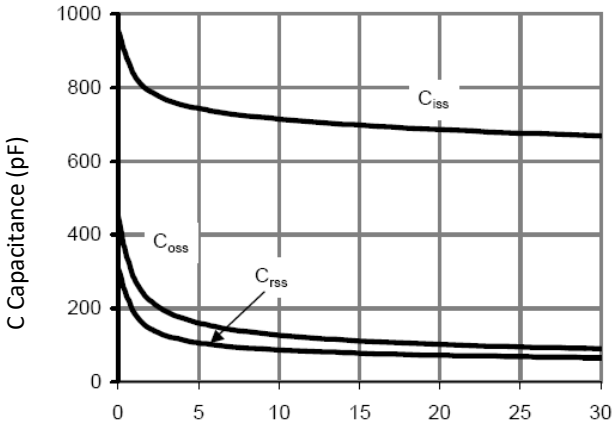


Figure 10 Capacitance vs Vds

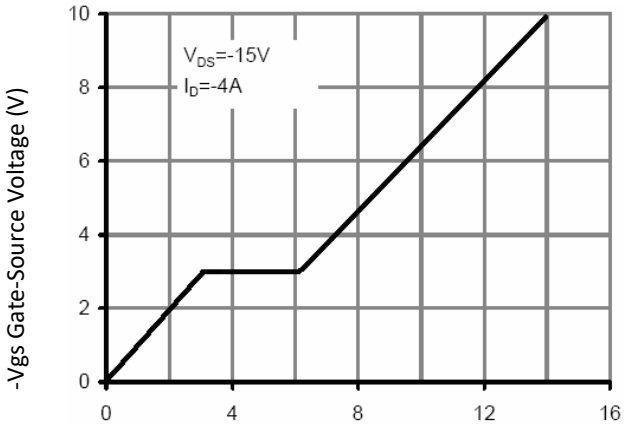


Figure 11 Gate Charge

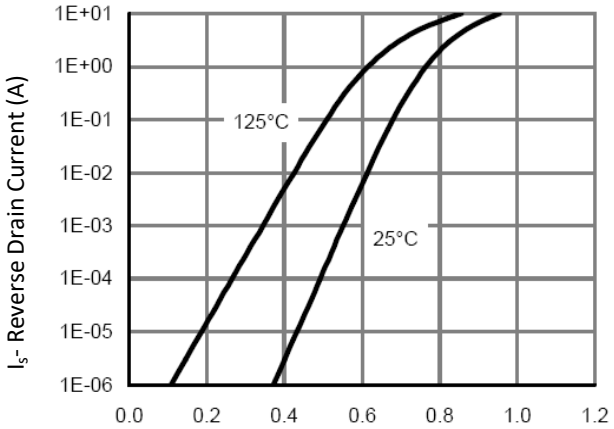


Figure 12 Source- Drain Diode Forward

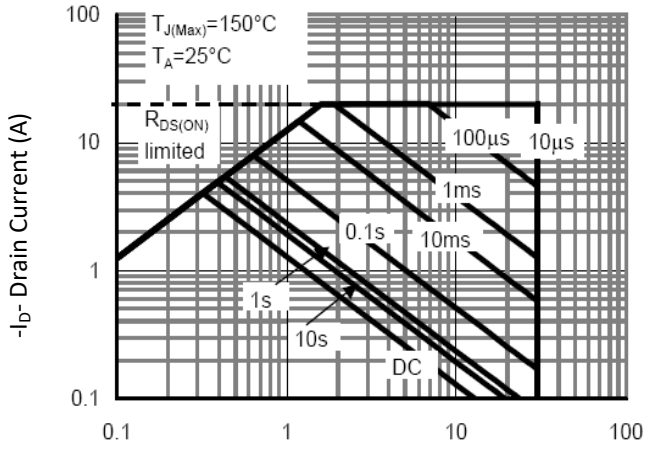


Figure 13 Safe Operation Area

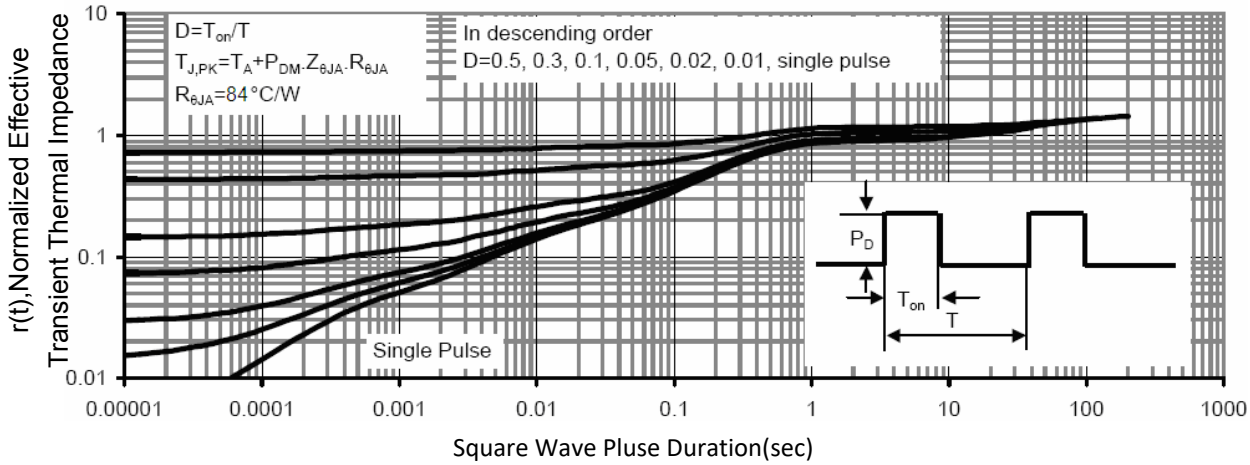


Figure 14 Normalized Maximum Transient Thermal Impedance