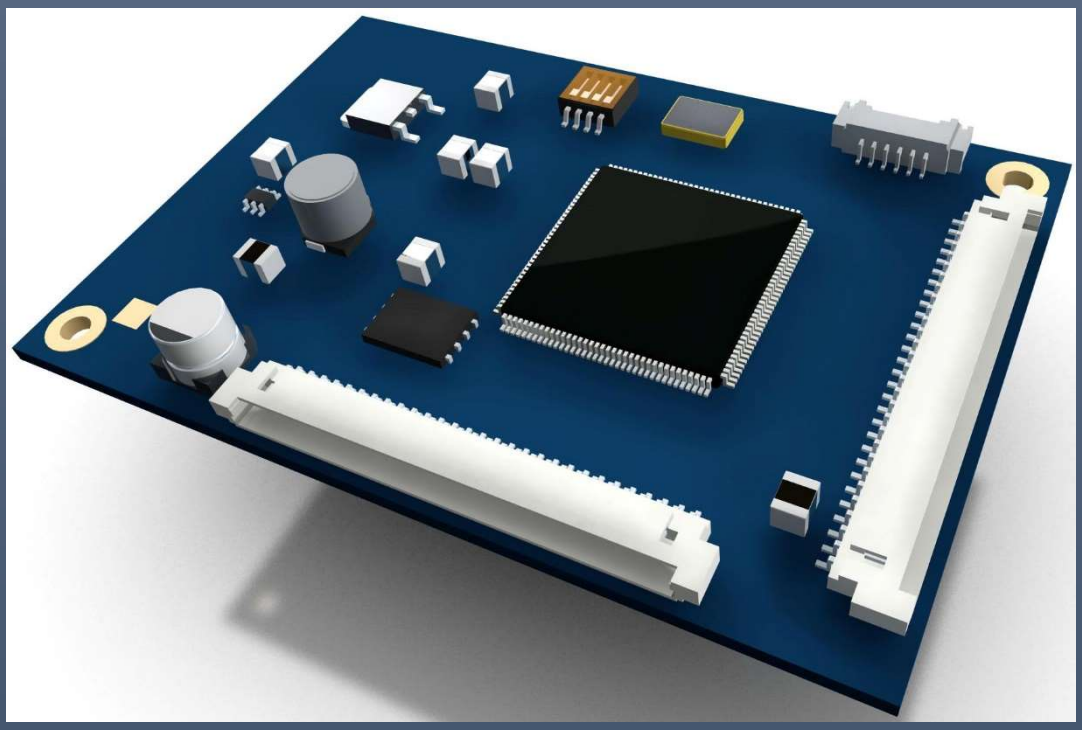
2019

Data Sheet



LVDS Converter

Model Name :

LFC-NLT9	**for NL192108AC10-01D / NLT 9"**
LFC-KOE7	**for TX18D200VM0EAA / KOE(JDI) 7"**
	for TX18D204VM0BAA / KOE(JDI) 7"
LFC-LG123	**for LA123WF1-SL01 or -SL02 / LG 12.3”**

Revision History

PCB Version	Rev. date	Revision Details
0.0	March 2014	Initial Version issue
1.0	April. 2014	Mass production version start
1.1	May, 2014	Firmware revision for AEON SBC GENE-CV05
-	June, 2014	Typo correction. Changed power requirements from 3.3V to 5.0V
-	April, 2016	Addition the support for KOE(JDI) 7" model / TX18D204VM0BAA
-	June, 2016	Addition the support for LG 12.3” model / LA123WF1-SL01 or – SL02
-	Jul 2017	Amend the LVDS Pin map table and relevant drawing
2.0	Dec . 2019	-. Changed the layer of PCB (2Layer ----> 4Layer) -. Changing the Shunt Switch for target LCD model selection : from Pin Header type Shunt Switch (J1) at 10 mm height to Selectable button type logical Switch (SW1) at 2.3 mm height -. Addition a connector on the bottom surface of PCB : for board to board connection by CN5 (FX8C-60S-SV5 / Hirose) -. Addition of an optional Q1 (RQ6E060AT / ROHM) : for the settlement of Signal timing

Contents

The information presented in this document may form a part of quotation or contract under the agreement of both parties. Otherwise, this datasheet is subject to change without notice.

1. Background of Design Concept

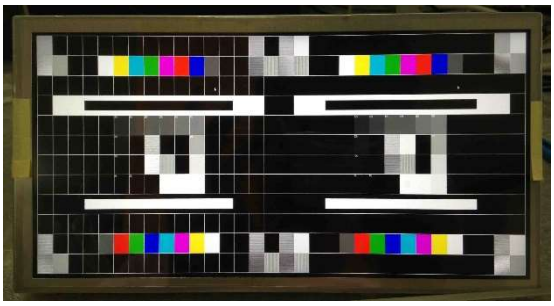
This LVDS Converter provides an easiest device for the supporting following TFT LCD Displays.

-. **NLT 9", NL192108AC10-01D, Full HD model**
-. **KOE (JDI) 7", TX18D200VM0EAA10, Full HD model**
-. **all kinds of LVDS based 10 bit Displays from 8 bit source (JEIDA-to-VESA conversion)**

This converter board takes a role of intermediate device in between ordinary AD board, SBC (single board computer) or Embedded PC and TFT LCD Display (NLT 9" or KOE(JDI) 7").
Because in general the ordinary type driving board cannot support to make a correct video image on the screen on the NLT 9" or KOE(JDI) 7" without having been adopted the FPGA circuit function on the driving boards.

1.1 in case of NLT 9" and LG 12.3”

The NLT 9” was designed by (960 x 1080) + (960 x 1080) resolution basis in order to make the FHD (1920 x 1080), therefore any normal driving board supports this display, the screen shows just (960 x 1080) + (960 x 1080) as dual pictures as below.



Therefore, when the user fits up the LVDS Converter in between NLT 9" and users' existing Driving board, the above dual video images will be an unified picture as one video image on the full screen NLT 9".

Please note that the input source of this converter MUST meet requirement of LCD panel driving condition.
All driving parameters(such as VTotal,HTotal,DE,VActive,HActive) will be passed thru the converter to the LCD panel itself as it is.

The converter works on both Venus board and SBC(Single Board Computer) with DE Only Mode.
These panel must be driven with DE enabled signal. The source must generate DE signal properly in order to work correctly. The converter does NOT generate DE on its own.
Version 1.1 or higher is required to work with DE only mode.

For troubleshooting, please confirm that the input source(or device) should be able to display like above screenshot WITHOUT this converter. After confirmation of above image, apply this converter between the source and the panel. All the same as the above, but the LG 12.3” is 1920 x 720 type.

1.2 in case of KOE (JDI) 7"

-. the status of ordinary board design

Almost ordinary driving boards are designed to work with single and dual LVDS interface by configuration.
However, even if A/D boards support dual link interface, it does not support enough bandwidth for the full HD on single channel, in this case 148.5MHz.

-. the implementation of problems with KOE(JDI) 7" display

the ordinary boards are manufactured on double-sided PCB to minimize manufacturing cost.
While KOE recommends Thine’s THC63LVDM87(http://www.thine.co.jp/files/topics/167_ext_12_0.pdf),

it is impossible to implement this IC for existing solution or double-sided PCB since it only comes with BGA chip which requires multi-layer PCB architecture.
Also, it is required to implement the dual link LVDS receiver in order to pass signal thru THC63LVDM87 as single link LVDS. It will costs you two expensive ICs for just converting dual to single link.

-. How could this LVDS converter resolve the problem

This LVDS converter receives dual-link LVDS, then an integrated FPGA combines into single link LVDS at doubled clock rate.
Thanks to this integrated high-performance FPGA for receiving, processing and transmitting of LVDS stream, it eliminates custom design cost and work burden for KOE FHD panel.
The converter can be used to work with existing solution with very small form factor.

Please note that the input source of this converter MUST meet requirement of LCD panel driving condition.
All driving parameters(such as **V**total, **H**total, DE, **V**active, **H**active) will be passed thru the converter to the LCD panel itself as it is.

However, since it is impossible to match these parameters as it is, devide all parameters by 2 (two).
For example, **H**total is typically 2200 clock, but the input source should be programmed as 1100 clock just like dual-link application.

1.3 JEIDA-to-VESA conversion

There are two major LVDS format in this industry. One is VESA, and the other is JEIDA.
These standards are quite similar however there is significant difference in how they align MSB and LSB.
VESA aligns MSB and LSB in simple sequential order, while JEIDA combines all LSBs into the last channel of LVDS stream.
Because JEIDA format combines all LSBs into single channel, it is easy to abandon LSBs by disconnecting the last channel.
For example, typical LVDS format for 24bits requires 4 channels of LVDS channel, but 30bits requires 5 channels for LSBs. Without 5th channel, JEIDA format panel works without 10bit LSBs.

Unfortunately, the newest panels with 10 bit capability comes with VESA format which is not possible to display with 8 bit sources under 4 channels LVDS.
This converter converts JEIDA format to VESA format, so thus, all 8bit and 10bits format can be fitted into 10 bit panel. However, this converter does NOT enhance quality of 8 bits source.

Please note that the input source of this converter MUST meet requirement of LCD panel driving condition.
All driving parameters(such as **V**total, **H**total, DE, **V**active, **H**active) will be passed thru the converter to the LCD panel itself as it is. However, output LVDS format should be JEIDA in this case.

2. Features

- LVDS Input
- LVDS Output
- LVDS Line Buffer
- LVDS Pixel Formatter

3. General Description

- Installation for the open customers who adopt this board with their own driving board

All components are placed on the top layer. Bottom layer is free from all obstacles. It can be attached to the panel directly with adhesive tape, or it can be mounted to chassis using two holes for mounting.

Please, note that bottom layer is not insulated. Proper insulation is required when attaching to the LCD panel directly.

- Installation for the customers who adopt this board with Venus board (branded Disteck solution)

There is a board to board connector for the purpose of additional wire connection separately between this board (input port) and mating driving board (LVDS output port)

- Caution

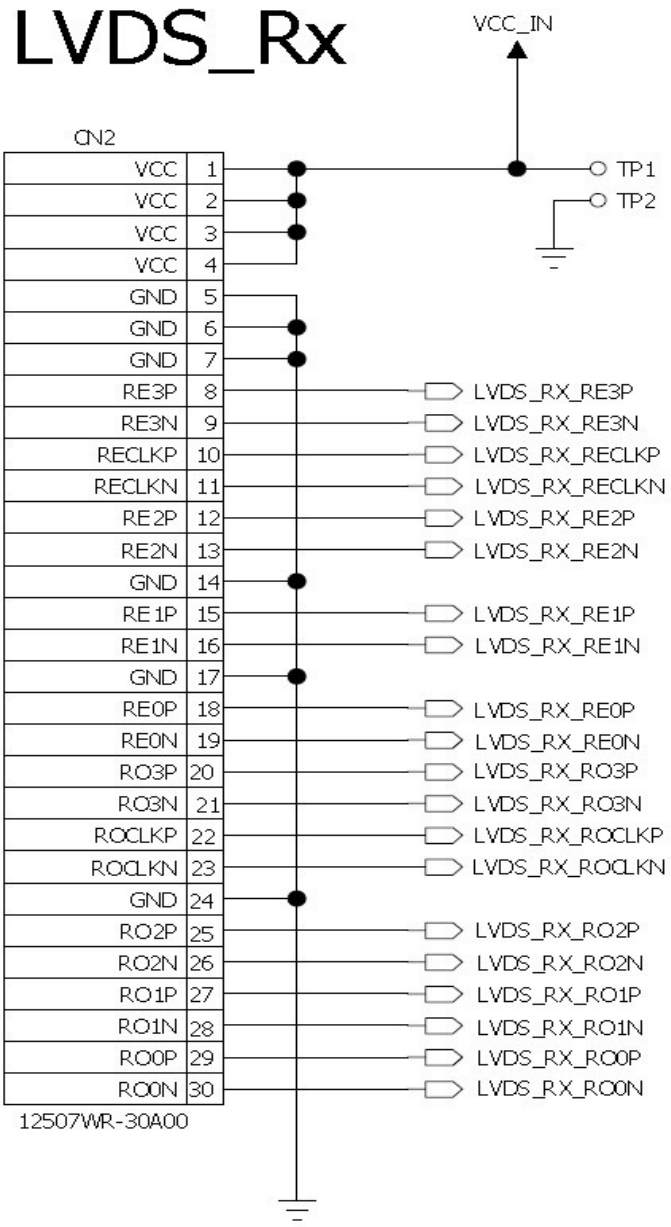
Be sure that LVDS wiring should be thick enough to deliver 5.0V to the Converter itself.

4. LVDS Pin Map

4.1 LVDS input : LVDS 30Pin (12507WR-30P) / CN2

Pin No.	Function	Pin No	Function	Pin No.	Function	Pin No.	Function	Pin No.	Function
1	Vcc	7	GND	13	RE2-	19	RE0-	25	RO2+
2	Vcc	8	RE3+	14	GND	20	RO3+	26	RO2-
3	Vcc	9	RE3-	15	RE1+	21	RO3-	27	RO1+
4	Vcc	10	REC+	16	RE1-	22	ROC+	28	RO1-
5	GND	11	REC-	17	GND	23	ROC-	29	RO0+
6	GND	12	RE2+	18	RE0+	24	GND	30	RO0-

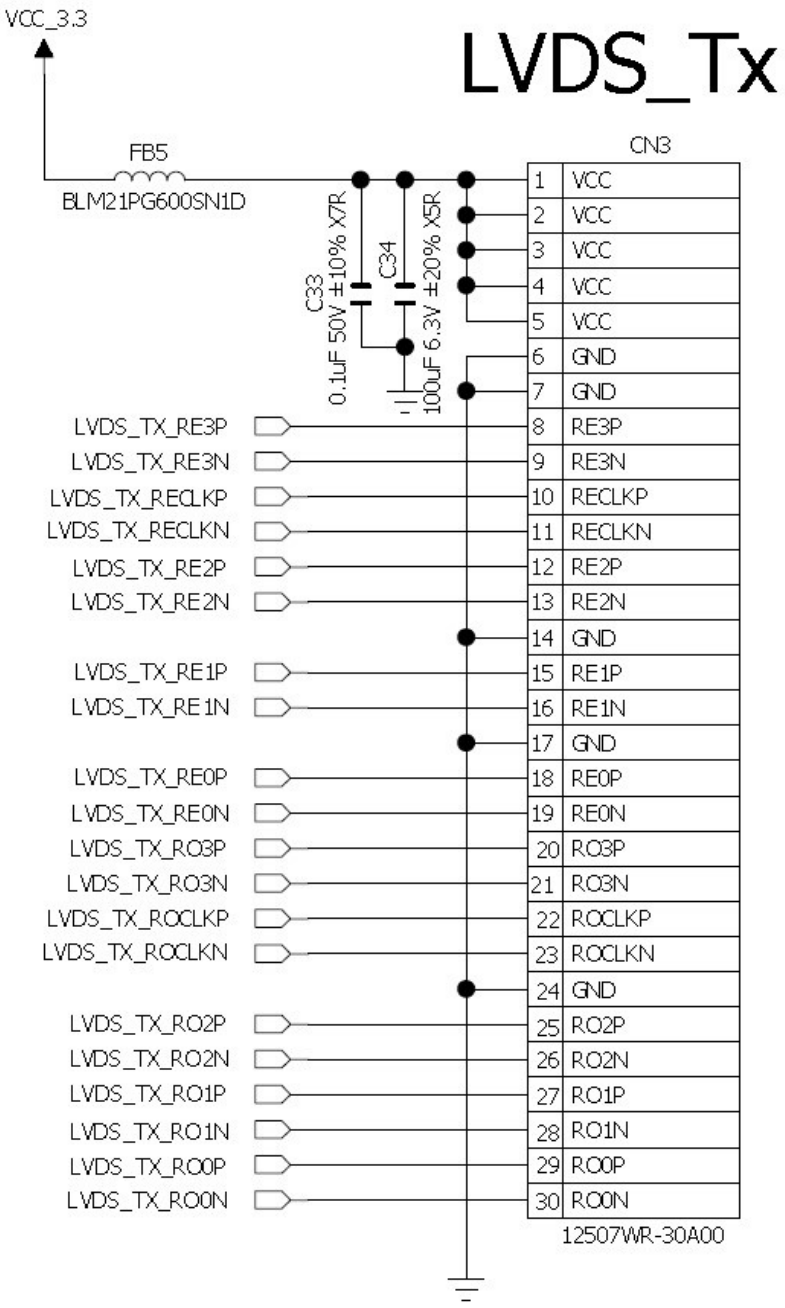
Equivalent Circuit Diagram



4.2 LVDS output : LVDS 30Pin (12507WR-30P) / CN3

Pin No.	Function	Pin No	Function	Pin No.	Function	Pin No.	Function	Pin No.	Function
1	Vcc	7	GND	13	RE2-	19	RE0-	25	RO2+
2	Vcc	8	RE3+	14	GND	20	RO3+	26	RO2-
3	Vcc	9	RE3-	15	RE1+	21	RO3-	27	RO1+
4	Vcc	10	REC+	16	RE1-	22	ROC+	28	RO1-
5	Vcc	11	REC-	17	GND	23	ROC-	29	RO0+
6	GND	12	RE2+	18	RE0+	24	GND	30	RO0-

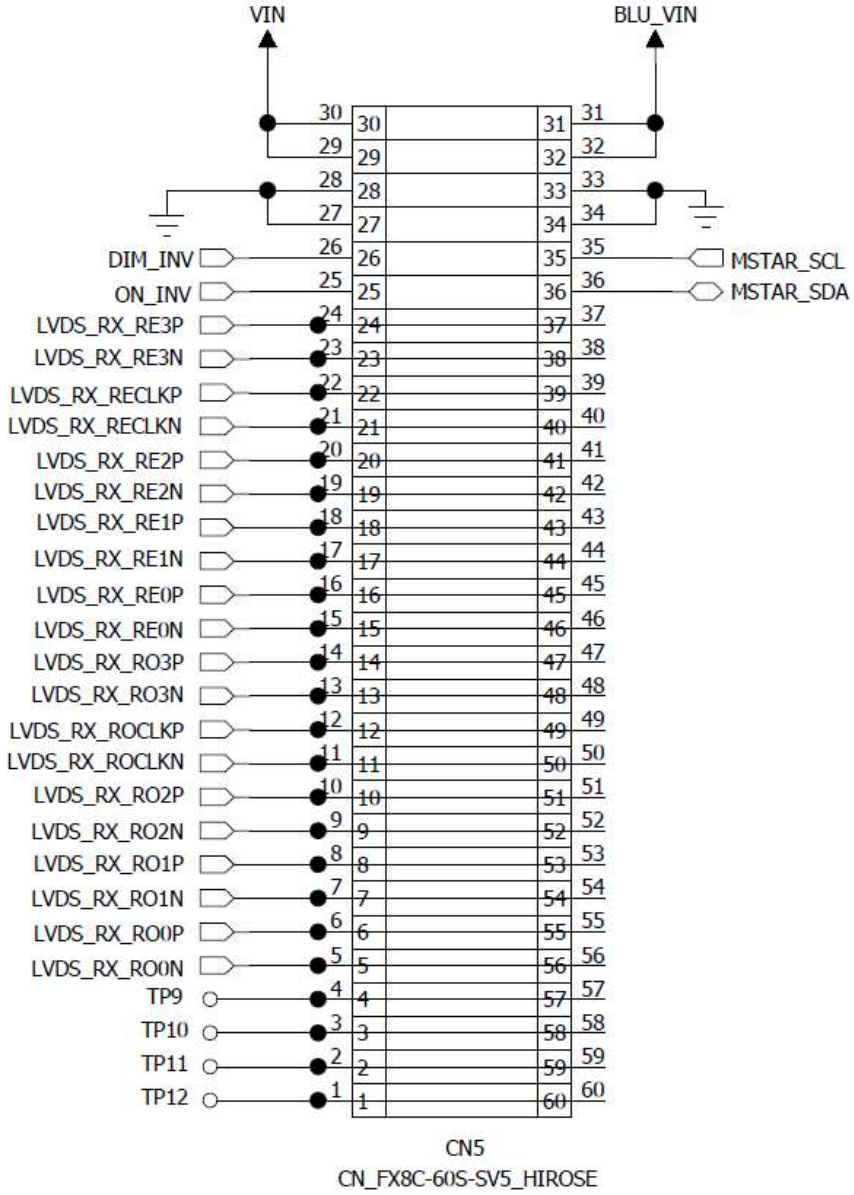
Equivalent Circuit Diagram



4.2 LVDS Input (Optional Connector) : LVDS 60 pin (FX8C-60S-SV5 / CN5)

Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	TXO4-	13	TXO3-	25	ON_INV	37	TXE3+	49	TXOC+
2	TXO4+	14	TXO3+	26	DIM_INV	38	TXE3-	50	TXOC-
3	TXE4-	15	TXE0-	27	GND	39	TXEC+	51	TXO2+
4	TXE4+	16	TXE0+	28	GND	40	TXEC-	52	TXO2-
5	TXO0-	17	TXE1-	29	VPANEL	41	TXE2+	53	TXO1+
6	TXO0+	18	TXE1+	30	VPANEL	42	TXE2-	54	TXO1-
7	TXO1-	19	TXE2-	31	BLU_VIN	43	TXE1+	55	TXO0+
8	TXO1+	20	TXE2+	32	BLU_VIN	44	TXE1-	56	TXO0-
9	TXO2-	21	TXEC-	33	GND	45	TXE0+	57	TXE4+
10	TXO2+	22	TXEC+	34	GND	46	TXE0-	58	TXE4-
11	TXOC-	23	TXE3-	35	MCU_SCL	47	TXO3+	59	TXO4+
12	TXOC+	24	TXE3+	36	MCU_SDA	48	TXO3-	60	TXO4-

Equivalent Circuit Diagram



4.3 Connectors Summary

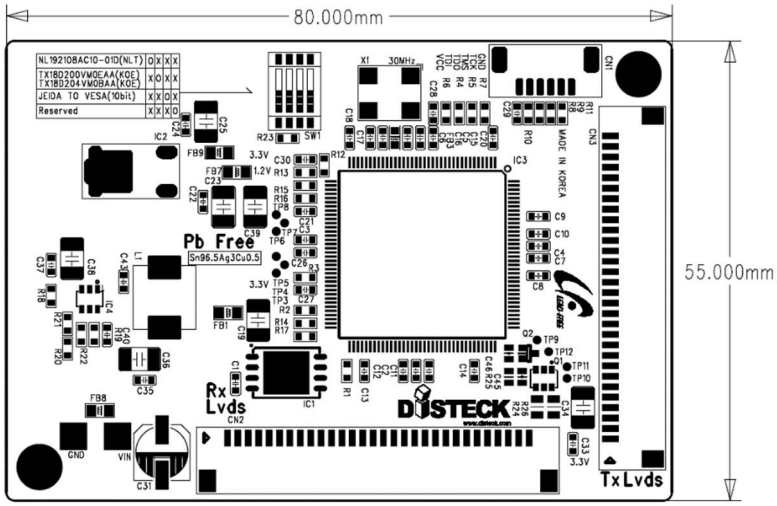
Service	Maker	Part number	Description	Point / Mating Housing
LVDS Input	Yeon-Ho	12507WR-30A00	1.25mm, 30p SMD	CN2 / 12507HS-30
LVDS Output	Yeon-Ho	12507WR-30A00	1.25mm, 30p SMD	CN3 / 12507HS-30
Factory use	Yeon-Ho	12505WR-06P	Firmware Download	CN1 / 12505HS-06
LVDS Input (Option)	Hirose	FX8C-60S-SV5	Board to Board Connection	CN5 / FX8C-60P-SV2

4.4 Dimension and others

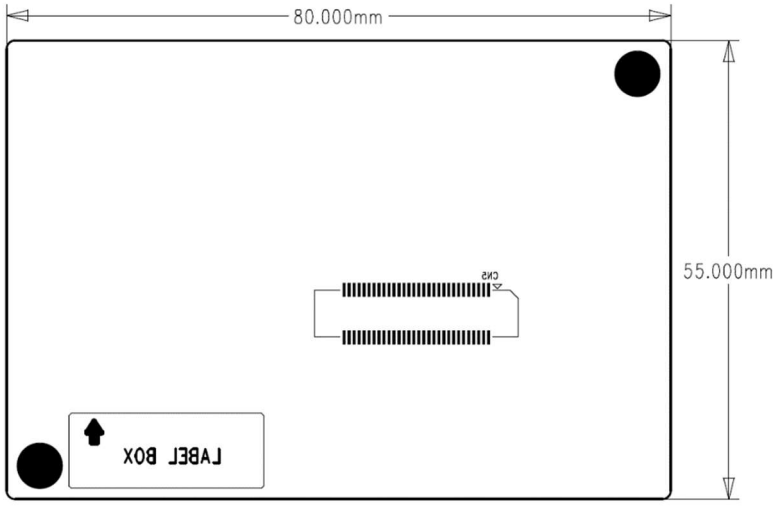
-. form factor : 55.00 mm (W) x 80.00 mm (V) x 7.3 mm (H)
-. Vcc in : Min 4.8V / Typ 5.0V / Max 5.2V

5. Printed Wiring Board

Top Layer



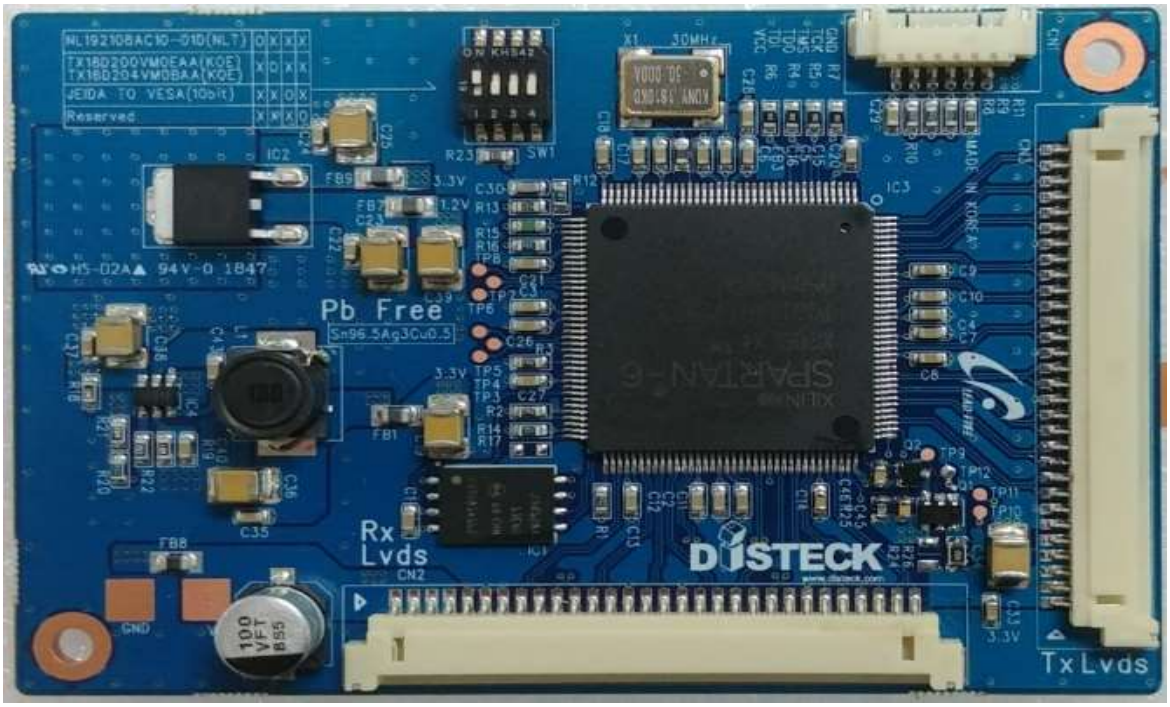
Bottom Layer



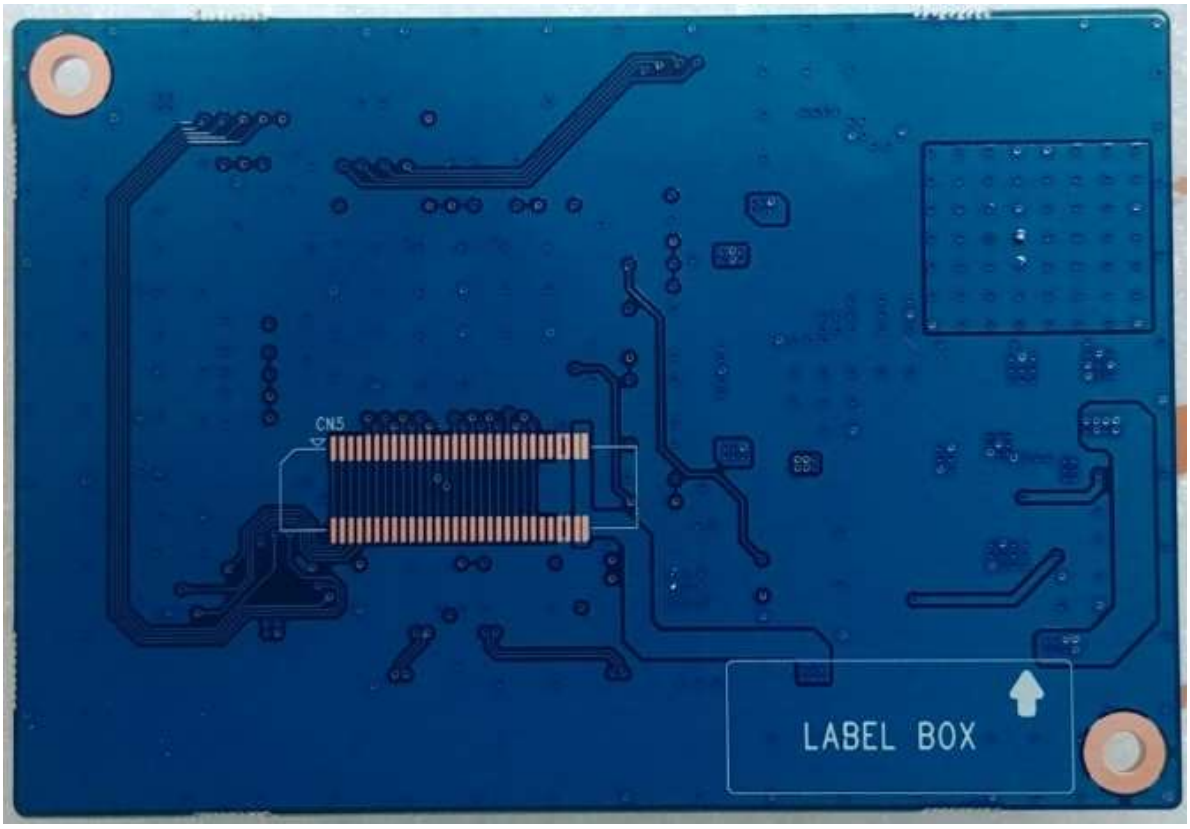
6. Product Pictures

6.1 Standard Product Case

Front View



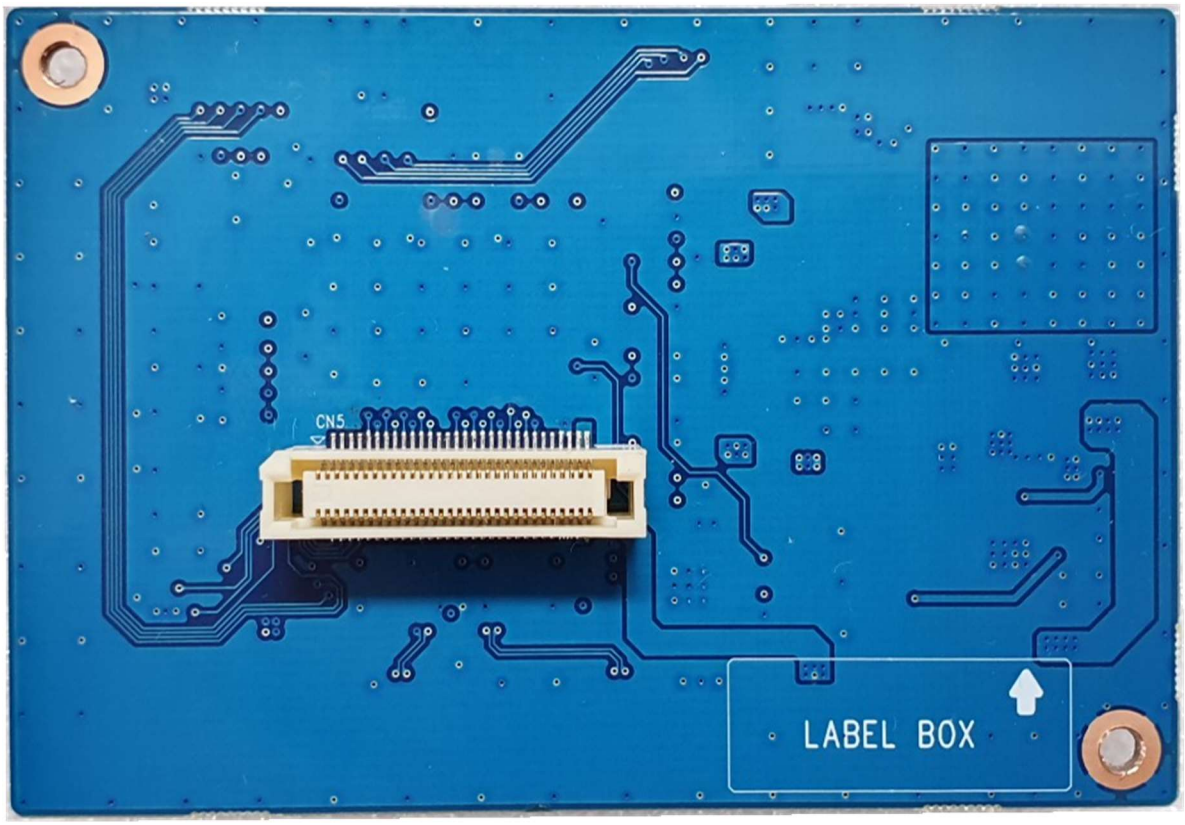
Rear View



6.2 Optional Product Case

Front View

Rear View



7. Connection Cables

7.1 Shape of LVDS Connectors on NLT 9”

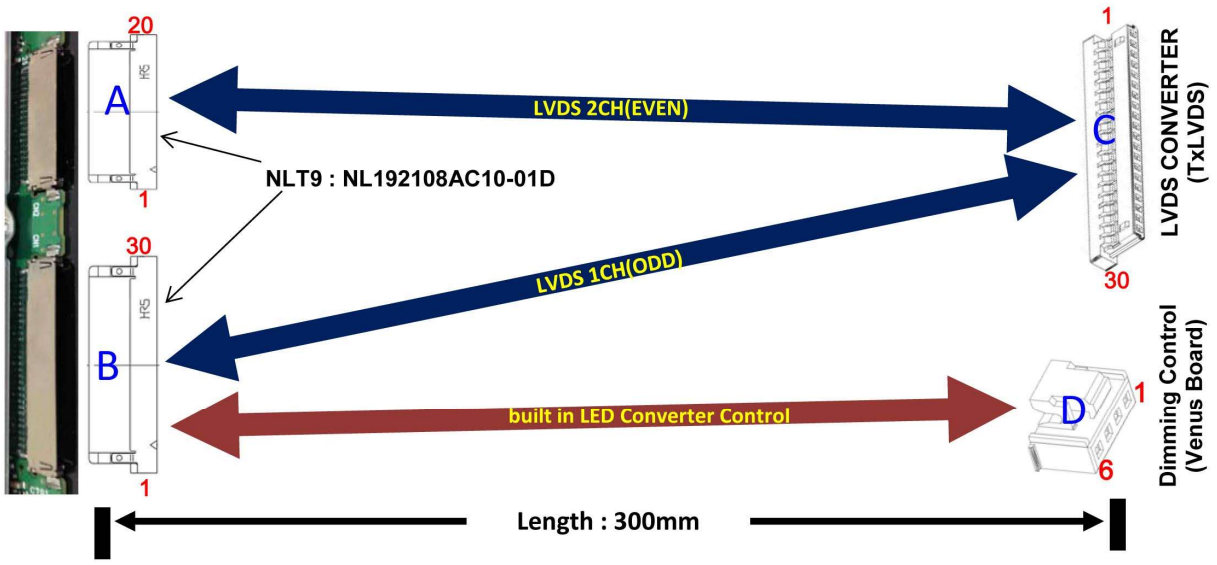
The mating LVDS Cable refer to the chapter 7.3 (see page 10)

7.2 Shape of LVDS Connectors on KOE(JDI) 7”

The mating LVDS Cable refer to the chapter 7.4 (see page 11)

7.3 Connection Cable between NLT 9" and LVDS Converter

LVDS Cable for NLT 9(LVDS Converter to NLT 9)



A

PANEL : NLT 9" (NL192108AC10-02D)	
SPEC	PIN
LVDS DR0-	2
LVDS DR0+	3
LVDS DR1-	5
LVDS DR1+	6
LVDS DR2-	8
LVDS DR2+	9
LVDS CLKR-	11
LVDS CLKR+	12
LVDS DR3-	14
LVDS DR3+	15
PANEL VCC	18
PANEL VCC	19
PANEL VCC	20

Connection

19
18
16
15
13
12
11
10
9
8
3
2
1

Connection Detail

C

LVDS CONVERTER (Tx LVDS)	
PIN	SPEC
19	LVDS DR0-
18	LVDS DR0+
16	LVDS DR1-
15	LVDS DR1+
13	LVDS DR2-
12	LVDS DR2+
11	LVDS CLKR-
10	LVDS CLKR+
9	LVDS DR3-
8	LVDS DR3+
3	PANEL VCC
2	PANEL VCC
1	PANEL VCC
30	LVDS DL0-
29	LVDS DL0+
7	GND
28	LVDS DL1-
27	LVDS DL1+
14	GND
26	LVDS DL2-
25	LVDS DL2+
17	GND
23	LVDS CLKL-
22	LVDS CLKL+
24	GND
21	LVDS DL3-
20	LVDS DL3+
4	LVDS FRC

B

PANEL : NLT 9" (NL192108AC10-02D)	
SPEC	PIN
LVDS DL0-	13
LVDS DL0+	14
GND	15
LVDS DL1-	16
LVDS DL1+	17
GND	18
LVDS DL2-	19
LVDS DL2+	20
GND	21
LVDS CLKL-	22
LVDS CLKL+	23
GND	24
LVDS DL3-	25
LVDS DL3+	26
LVDS FRC	28
VLED 12V	2
VLED 12V	3
GND	5
GND	6
PWM	7
ON OFF	8

Connection

30
29
7
28
27
14
26
25
17
23
22
24
21
20
4
1
2
3
4
5
6

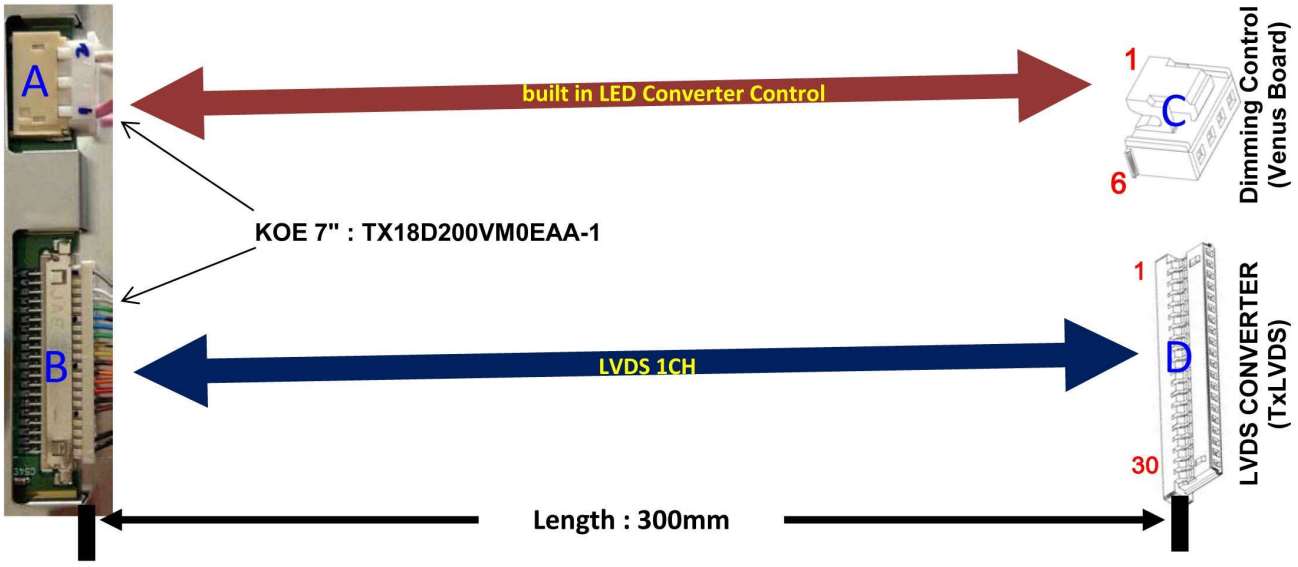
Connection Detail

D

Dimming Control (Venus Board)	
PIN	SPEC
1	VLED 12V
2	VLED 12V
3	GND
4	GND
5	PWM
6	ON OFF

7.4 Connection Cable between KOE(JDI) 7” and LVDS Converter

LVDS Cable for KOE 7(LVDS Converter to KOE 7)



A	
PANEL : KOE 7" (TX18D200VM0EAA-1)	
SPEC	PIN
VLED 12V	1
GND	2

Connection

1 & 2
3 & 4

Connection Detail

C	
Dimming Control (VENUS Board)	
PIN	SPEC
1	VLED 12V
2	VLED 12V
3	GND
4	GND
5	PWM

B	
PANEL : KOE 7" (TX18D200VM0EAA-1)	
SPEC	PIN
PANEL VCC	1
PANEL VCC	2
LVDS IN0-	5
LVDS IN0+	6
GND	7
LVDS IN1-	8
LVDS IN1+	9
GND	10
LVDS IN2-	11
LVDS IN2+	12
GND	13
LVDS CLKIN-	14
LVDS CLKIN+	15
GND	16
LVDS IN3-	17
LVDS IN3+	18
DIM	20

Connection

1
2
30
29
24
28
27
17
26
25
14
23
22
7
21
20
5

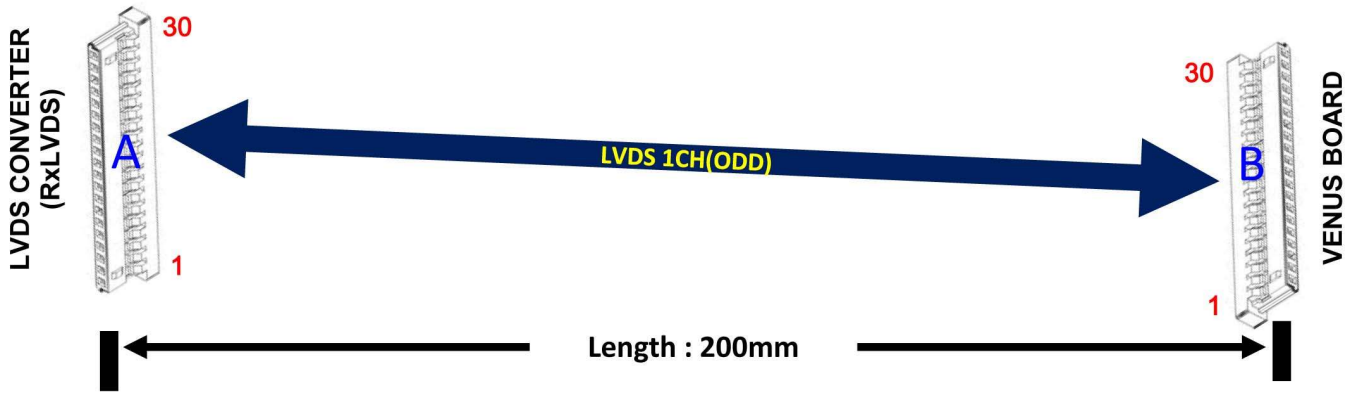
Connection Detail

Connection Detail

D	
LVDS CONVERTER (Tx LVDS)	
PIN	SPEC
1	PANEL VCC
2	PANEL VCC
30	RO0N
29	RO0P
24	GND
28	RO1N
27	RO1P
17	GND
26	RO2N
25	RO2P
14	GND
23	ROCLKN
22	ROCLKP
7	GND
21	RO3N
20	RO3P

7.5 Connection Cable between LVDS Converter and AD board (below drawing is based on the Venus model as an AD board)

LVDS Cable for Converter(Venus to Converter)



A				B	
LVDS CONVERTER (Rx LVDS : Input)				VENUS BOARD	
SPEC	PIN			PIN	SPEC
VCC 5V	1		30	30	VCC 5V
VCC 5V	2		29	29	VCC 5V
VCC 5V	3		28	28	VCC 5V
GND	7		24	24	GND
RE3P	8		23	23	RE3P
RE3N	9		22	22	RE3N
RECLKP	10		21	21	RECLKP
RECLKN	11		20	20	RECLKN
RE2P	12		19	19	RE2P
RE2N	13		18	18	RE2N
GND	14		17	17	GND
RE1P	15		16	16	RE1P
RE1N	16	Connection	15	15	RE1N
GND	17		14	14	GND
RE0P	18		13	13	RE0P
RE0N	19		12	12	RE0N
RO3P	20		11	11	RO3P
RO3N	21		10	10	RO3N
ROCLKP	22		9	9	ROCLKP
ROCLKN	23		8	8	ROCLKN
GND	24		7	7	GND
RO2P	25		6	6	RO2P
RO2N	26		5	5	RO2N
RO1P	27		4	4	RO1P
RO1N	28		3	3	RO1N
RO0P	29		2	2	RO0P
RO0N	30		1	1	RO0N

Connection Detail