



Product Specification

M270DTR01.0

AU OPTRONICS CORPORATION

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() Preliminary Specification
(V) Final Specification

Module	27" Color TFT-LCD
Model Name	M270DTR01.0

Customer	Date
_____	_____
Approved by	Date
_____	_____
Note: This Specification is subject to change without notice.	

Approved by	Date
<u>Howard Lee</u>	<u>May 17, 2017</u>
Prepared by	Date
<u>Bruce TL Yu</u>	<u>May 17, 2017</u>
AU Optronics corporation	

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Record of Revision

Version	Date	Page	Old description	New Description	Remark																																																																																																																
0.0	2016/10/21	All	First version release																																																																																																																		
1.0	2017/02/17	All	Final version release																																																																																																																		
1.1	2017/04/17	4		Add item 13 & item 14																																																																																																																	
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1 Handling Precautions

- 1) Since polarizer is easily damaged, do not touch or press the surface of polarizer with hand.
- 2) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 3) When the cell surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 4) Since the cell is made of glass, it may break or crack if dropped or bumped on hard surface.
- 5) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 6) Do not press or pat the panel surface by fingers, hand or tooling.
- 7) Please handle TFT cell with care. The FPCs can only sustain for quite limited stress.
- 8) The cell package tray is packed in clean room. Please do pack & unpack it in clean room.
- 9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT cell.
- 10) Pls avoid touching COF position while you are doing mechanical design.
- 11) When storing modules as spares for a long time, the following precaution is necessary: Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5°C and 35°C at normal humidity.
- 12) Do not apply the same pattern for a long time, it will enhance relevant defect.
- 13) If the product will be used under extreme conditions such as under high temperature, humidity, display patterns or the operation time etc., it is strongly recommended to contact AUO for the advice about the application of engineering. Otherwise, its reliability and the function may not be guaranteed. Extreme conditions are commonly found at airports, transit stations, banks, stock markets, and controlling systems.
- 14) Module designer should apply adequate thermal solutions to keep the electrical components surface temperature under control limit (ex: Source Driver IC 100°C , Components on T-con PCB 85°C) Operations over the temperature can cause damages or decrease of lifetime.



2 General Description

This specification applies to the 27 inch wide Color a-Si TFT-LCD Module M270DTR01.0. The display supports the QHD - 2560(H) x 1440(V) screen format and 16.7M colors (RGB 8-bits data). The input interface is 8-lanes eDP.

2.1 Display Characteristics

The following items are characteristics summary on the table under 25°C condition:

ITEMS	Unit	SPECIFICATIONS	
Screen Diagonal	[mm]	684.67 (27")	
Active Area	[mm]	596.74 (H) x 335.66 (V)	
Pixels H x V	-	2560(x3) x 1440	
Pixel Pitch	[um]	233.1 (per one triad) x233.1	
Pixel Arrangement	-	R.G.B. Vertical Stripe	
Display Mode	-	TN Mode (Twisted Nematic), Normally White	
Response Time	[msec]	~3 (Typ., on/off)	
Power Consumption	[Watt]	LCD module : PDD (Typ.)=7.2W @ Black pattern,Fv=165Hz	
Weight	[Grams]	630	
Electrical Interface	-	8-lanes eDP	
Support Color	-	16.7M colors (RGB 8-bit)	
Surface Treatment	-	Anti-Glare, 3H	
Temperature Range Operating Storage (Shipping)	[°C]	0 to +50 -20 to +60	
Cell transmittance	[%]	2.8 (Typ.)	Base on AUO LED Backlight
		2.5 (Min.)	
Cell thickness	[mm]	1.44 (Thickness of polarizer film: 0.22 mm each side)	

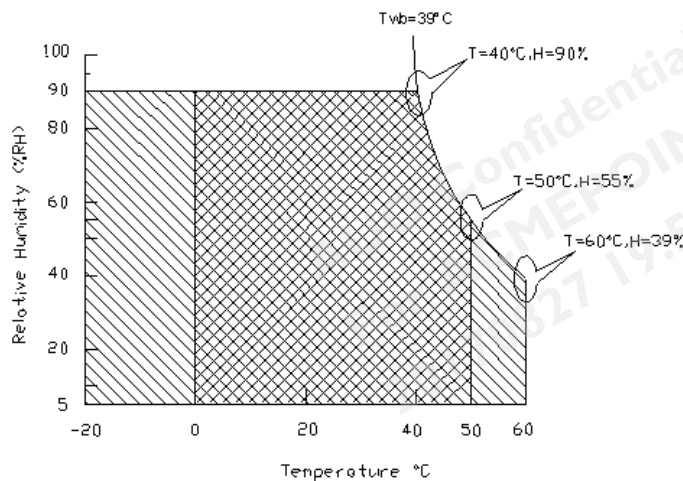
2.2 Absolute Maximum Rating of Environment

Permanent damage may occur if exceeding the following maximum rating.

Symbol	Description	Min.	Max.	Unit	Remark
TOP	Operating Temperature	0	+50	[°C]	Note 2-1
TGS	Glass surface temperature (operation)	0	+65	[°C]	Note 2-1 Function judged only
HOP	Operation Humidity	5	90	[%RH]	Note 2-1
TST	Storage Temperature	-20	+60	[°C]	
HST	Storage Humidity	5	90	[%RH]	

Note 2-1: Temperature and relative humidity range are shown as the below figure.

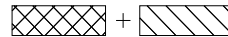
1. 90% RH Max ($T_a \leq 39^\circ\text{C}$)
2. Max wet-bulb temperature at 39°C or less. ($T_a \leq 39^\circ\text{C}$)
3. No condensation



Operating Range



Storage Range



2.3 Optical Characteristics

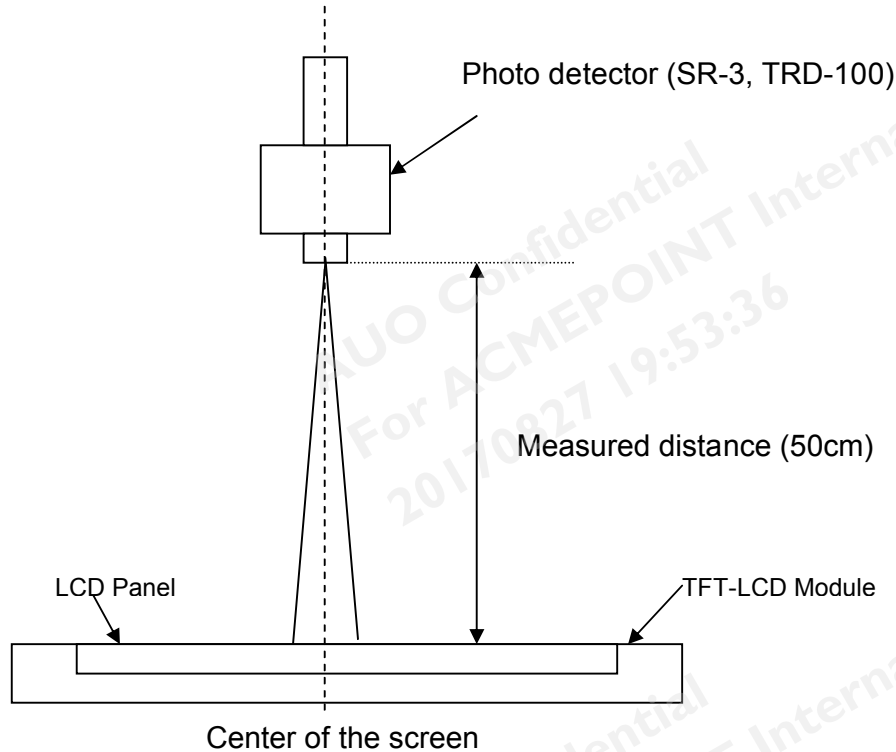
The optical characteristics are measured on the following test condition.

Test Condition:

1. Equipment setup: Please refer to **Note 2-2**.
2. Panel Lighting time: 30 minutes
3. VDD=12V, Fv=120 Hz ,Is=50mA,Ta=25°C

Symbol	Description		Min	Typ.	Max	Unit	Remark
CR	Contrast Ratio (Center of screen)		600	1000	-	[cd/m ²]	Note 2-3 Base on AUO LED Backlight
θ_R	Horizontal Viewing Angle (CR=10)	Right	75	85	-	[degree]	Note 2-4 By Eldim (Base on AUO backlight design)
θ_L		Left	75	85	-		
Φ_H	Vertical Viewing Angle (CR=10)	Up	70	80	-		
Φ_L		Down	70	80	-		
θ_R	Horizontal Viewing Angle (CR=5)	Right	75	88	-		
θ_L		Left	75	88	-		
Φ_H	Vertical Viewing Angle (CR=5)	Up	70	85	-		
Φ_L		Down	70	85	-		
T_R	Response Time	Rising Time	-	2.4	4.4	[msec]	Note 2-5 By TRD-100
T_F		Falling Time	-	1.1	2.1		
-		Rising + Falling	-	3.5	6.5		
R_x	Color Coordinates (CIE 1931)	Red x	0.631	0.661	0.691	-	Base on C light
R_y		Red y	0.301	0.331	0.361		
G_x		Green x	0.254	0.284	0.314		
G_y		Green y	0.576	0.606	0.636		
B_x		Blue x	0.108	0.138	0.168		
B_y		Blue y	0.061	0.091	0.121		
W_x		White x	0.289	0.319	0.349		
W_y		White y	0.327	0.357	0.387		
CT	Crosstalk				1.5	[%]	Note 2-6 By SR-3
F_{dB}	Flicker (Center of screen)				-20	[dB]	Note 2-7 By SR-3

Note 2-2: Equipment setup :



Note 2-3: Contrast Ratio Measurement

Definition:

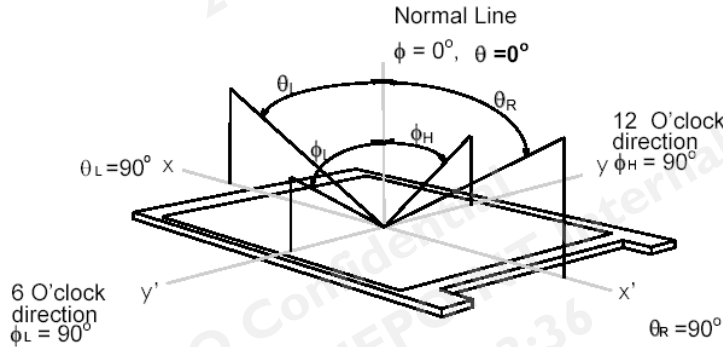
$$\text{Contrast Ratio} = \frac{\text{Luminance of White pattern}}{\text{Luminance of Black pattern}}$$

a. Measured position: Center of screen (P5) & perpendicular to the screen
($\theta = \Phi = 0^\circ$)

Note 2-4: Viewing angle measurement

Definition: The angle at which the contrast ratio is greater than 10 & 5 .

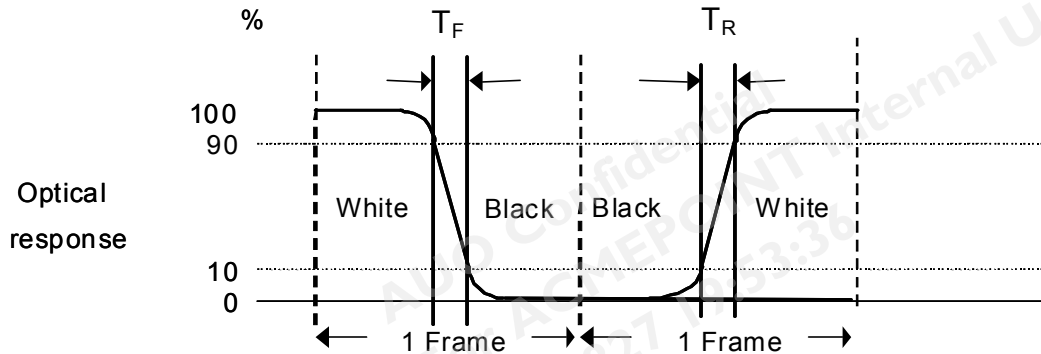
a. Horizontal view angle: Divide to left & right (θ_L & θ_R)
Vertical view angle: Divide to up & down (Φ_H & Φ_L)



Note 2-5: Response measurement

time

The output signals of photo detector are measured when the input signals are changed from “Black” to “White” (rising time, T_R), and from “White” to “Black” (falling time, T_F), respectively. The response time is interval between the 10% and 90% of optical response. (Black & White color definition: Please refer section 3.4.3)



Note 2-6: Crosstalk measurement

Definition:

$$CT = \text{Max. } (CT_H, CT_V);$$

Where

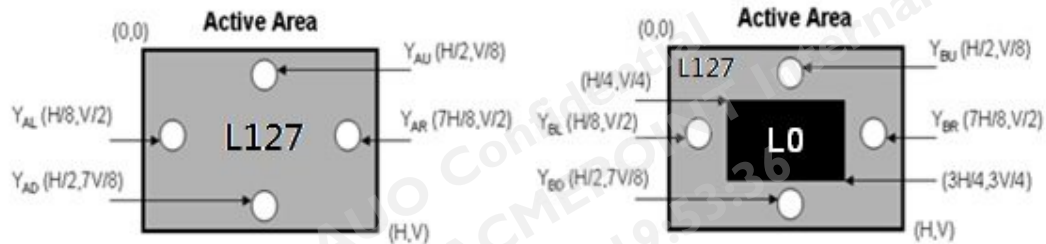
a. Maximum Horizontal Crosstalk :

$$CT_H = \text{Max. } (| Y_{BL} - Y_{AL} | / Y_{AL} \times 100 \%, | Y_{BR} - Y_{AR} | / Y_{AR} \times 100 \%);$$

Maximum Vertical Crosstalk:

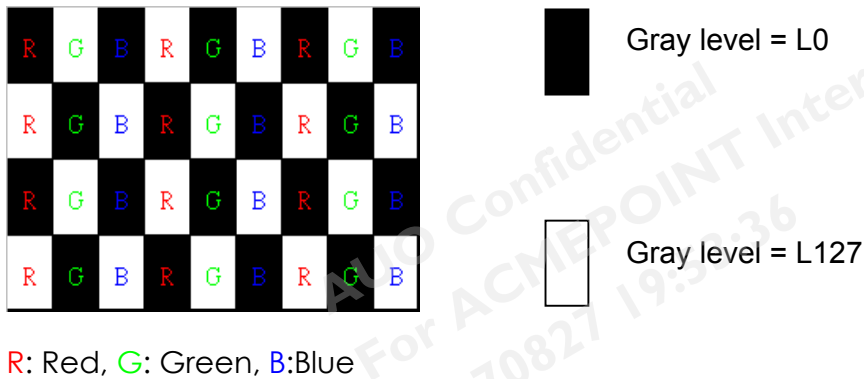
$$CT_V = \text{Max. } (| Y_{BU} - Y_{AU} | / Y_{AU} \times 100 \%, | Y_{BD} - Y_{AD} | / Y_{AD} \times 100 \%);$$

- b. $Y_{AU}, Y_{AD}, Y_{AL}, Y_{AR}$ = Luminance of measured location without Black pattern
- $Y_{BU}, Y_{BD}, Y_{BL}, Y_{BR}$ = Luminance of measured location with Black pattern



Note 2-7: Flicker measurement

- a. Test pattern: It is listed as following.

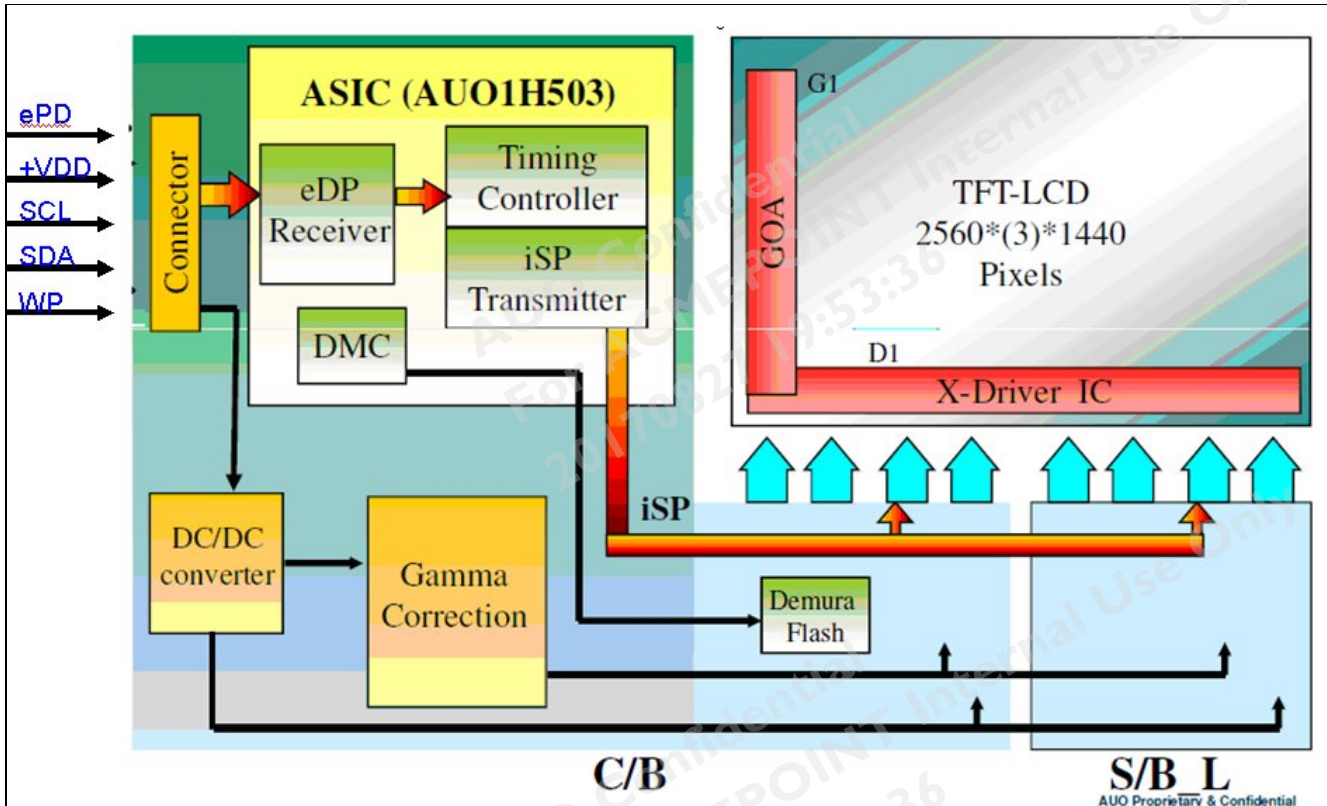


- b. Measured position: Center of screen & perpendicular to the screen

3 TFT-LCD Module

3.1 Block Diagram

The following shows the block diagram of the 27.0 inch Color TFT-LCD Module.





3.2 Interface Connection

3.2.1 Connector Type

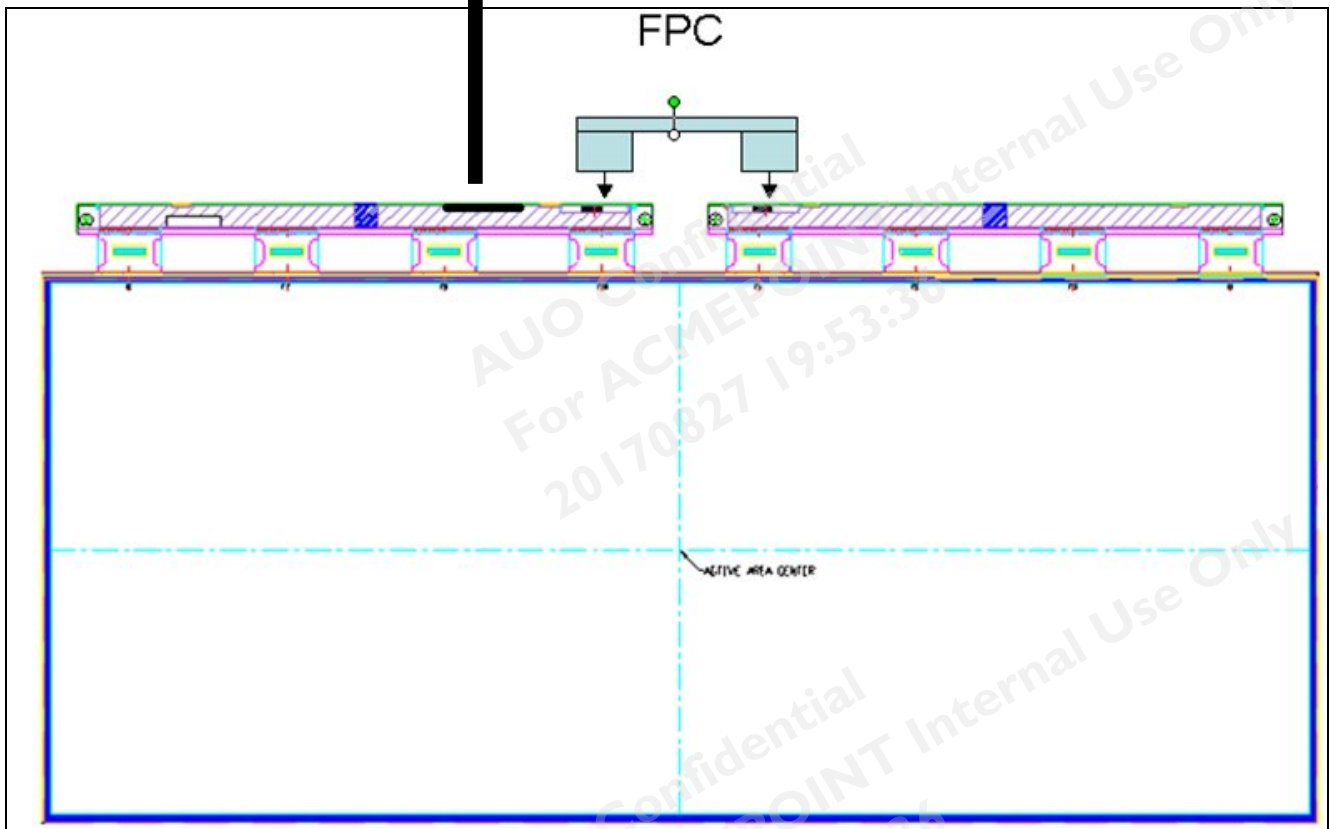
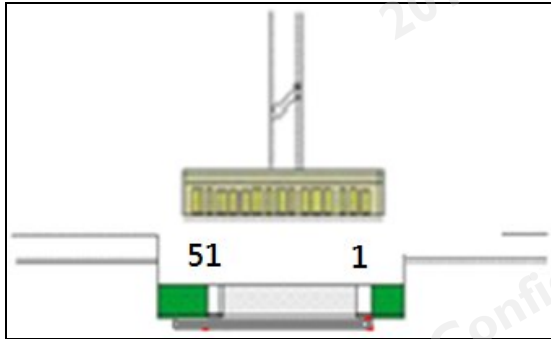
TFT-LCD Connector	Manufacturer	JAE	P-TWO	STARCONN
	Part Number	FI-RTE51SZ-HF	187059-5122	115E51-0000RA-M3-R
Mating Connector	Manufacturer	JAE or compatible		
	Part Number	FI-RE51CL		

3.2.2 Connector Pin Assignment

PIN #	Symbol	Description	Remark
1	VDD	Power +12V	
2	VDD	Power +12V	
3	VDD	Power +12V	
4	VDD	Power +12V	
5	VDD	Power +12V	
6	GND	Ground	
7	GND	Ground	
8	GND	Ground	
9	WP	Digital-Vcom write protection	
10	SDA	I2C-Compatible Serial-Data Input / Output for Vcom	
11	SCL	I2C-Compatible Serial-Clock Input for Vcom adjust	
12	N.C.	No connection (for AUO test only. Do not connect)	
13	N.C.	No connection (for AUO test only. Do not connect)	
14	N.C.	No connection (for AUO test only. Do not connect)	
15	IMS	Interlace Mode Selection	
16	IMS POL	Interlace Mode Selection Polarity	
17	GND	Ground	
18	D1 3N	Negative lane 3 input(display port 1)	
19	D1 3P	Positive lane 3 input(display port 1)	
20	GND	Ground	
21	D1 2N	Negative lane 2 input(display port 1)	
22	D1 2P	Positive lane 2 input(display port 1)	
23	GND	Ground	
24	D1 1N	Negative lane 1 input(display port 1)	
25	D1 1P	Positive lane 1 input(display port 1)	
26	GND	Ground	



27	D1_0N	Negative lane 0 input(display port 1)	
28	D1_0N	Positive lane 0 input(display port 1)	
29	GND	Ground	
30	AUX1P	Positive AUX input(display port 1)	
31	AUX1N	Negative AUX input(display port 1)	
32	GND	Ground	
33	N.C.	No connection (for AUO test only. Do not connect)	
34	GND	Ground	
35	D2_3N	Negative lane 3 input(display port 2)	
36	D2_3P	Positive lane 3 input(display port 2)	
37	GND	Ground	
38	D2_2N	Negative lane 2 input(display port 2)	
39	D2_2P	Positive lane 2 input(display port 2)	
40	GND	Ground	
41	D2_1N	Negative lane 1 input(display port 2)	
42	D2_1P	Positive lane 1 input(display port 2)	
43	GND	Ground	
44	D2_0N	Negative lane 0 input(display port 2)	
45	D2_0P	Positive lane 0 input(display port 2)	
46	GND	Ground	
47	AUX2P	Positive AUX input(display port 2)	
48	AUX2P	Negative AUX input(display port 2)	
49	GND	Ground	
50	HPD	Hot plug detection	
51	GND	Ground	



3.3 Electrical Characteristics

3.3.1 Absolute Maximum Rating

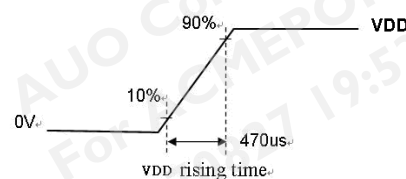
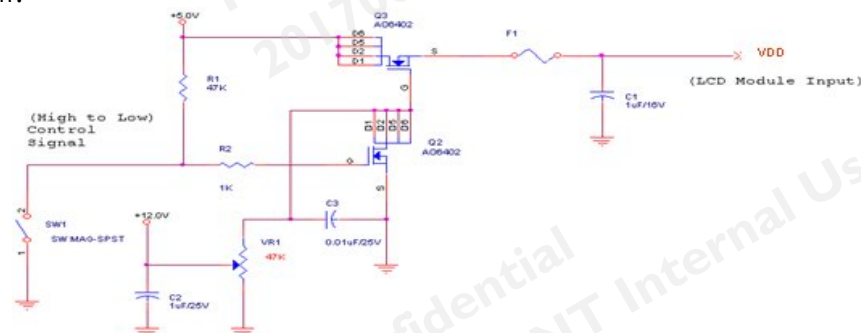
Permanent damage may occur if exceeding the following maximum rating.

Symbol	Description	Min	Max	Unit	Remark
VDD	Power Supply Input Voltage	GND-0.3	14.0	[Volt]	Ta=25°C
SCL,SDA,WP	I2C input Voltage	GND-0.3	4.0	[Volt]	Ta=25°C

3.3.2 Recommended Operating Condition

Symbol	Description	Min	Typ	Max	Unit	Remark
VDD	Power supply Input voltage	10.8	12.0	13.2	[Volt]	
IDD	Power supply Input Current (RMS)	-	0.5	1.1	[A]	VDD= 12.0V, Black Pattern, Fv=120Hz
		-	0.6	1.2	[A]	VDD= 12.0V, Black Pattern, Fv=165Hz
PDD	VDD Power Consumption	-	6.0	13.2	[Watt]	VDD= 12.0V, Black Pattern, Fv=120Hz
		-	7.2	14.4	[Watt]	VDD= 12.0V, Black Pattern, Fv=165Hz
IRush	Inrush Current	-	-	3	[A]	Note 3-1
VDDrp	Allowable VDD Ripple Voltage	-	-	1200	[mV]	VDD= 12.0V, Black Pattern, Fv=120Hz

Note 3-1: Inrush Current measurement:
Test circuit:



The duration of VDD rising time: 470us.

3.3.3 Input control signal threshold voltage definition

Item	Symbol	Min.	Typ.	Max.	Unit
Input High Threshold Voltage	V _{IH}	2.7	-	3.6	V
Input Low Threshold Voltage	V _{IL}	0	-	0.6	V

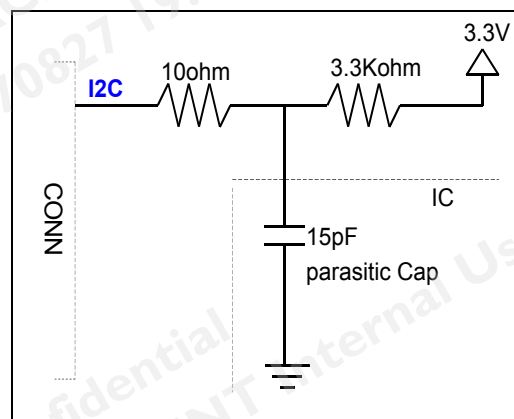
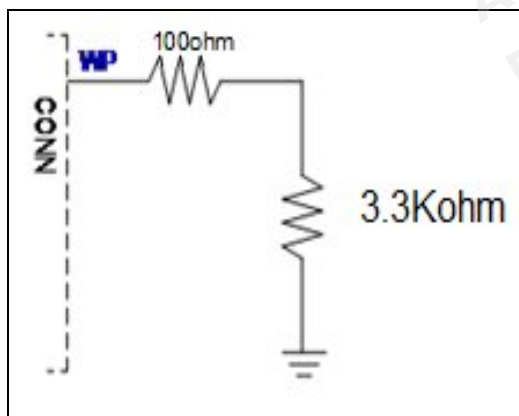
3.3.4 Write Protection mode selection

WP	Note
L or OPEN	Protection
H	Writable

3.3.5 Input equivalent impedance

1. Input equivalent impedance of WP pin SDA/SCL pin

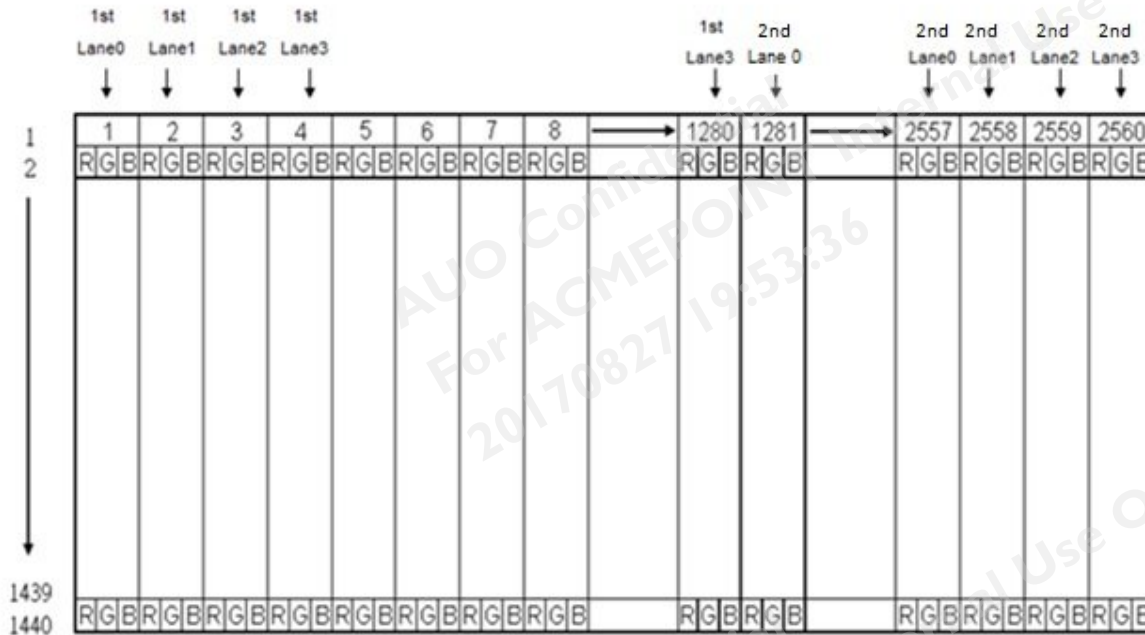
2. Input equivalent impedance of



3.4 Signal Characteristics

3.4.1 LCD Pixel Format

Following figure shows the relationship between the input signals and LCD pixel format.



Note 3-2: The module use 8-Lanes eDP interface.

- 1st Lane0 : 1, 5.....→1277pixel → $4N+1$ $N=0, \sim 319$ (1,5.. 1277pixel)
- 1st Lane1 : 2, 6.....→1278pixel → $4N+2$ $N=0, \sim 319$ (2,6.. 1278pixel)
- 1st Lane2 : 3, 7.....→1279 pixel → $4N+3$ $N=0, \sim 319$ (3,7.. 1279pixel)
- 1st Lane3 : 4, 8.....→1280 pixel → $4N+4$ $N=0, \sim 319$ (4,8.. 1280pixel)
- 2nd Lane0 : 1281, 1285.....→2557pixel → $4N+1281$ $N=0, \sim 319$ (1281, .. 2557pixel)
- 2nd Lane1 : 1282, 1286.....→2558pixel → $4N+1282$ $N=0, \sim 319$ (1282, .. 2558pixel)
- 2nd Lane2 : 1283, 1287.....→2559 pixel → $4N+1283$ $N=0, \sim 319$ (1283, .. 2559pixel)
- 2nd Lane3 : 1284, 1188.....→2560 pixel → $4N+1284$ $N=0, \sim 319$ (1284, .. 2560pixel)



3.4.2 eDP Data Format

1st Lane0	1st Lane1	1st Lane2	1st Lane3
R1-7:0	R2-7:0	R3-7:0	R4-7:0
G1-7:0	G2-7:0	G3-7:0	G4-7:0
B1-7:0	B2-7:0	B3-7:0	B4-7:0
R5-7:0	R6-7:0	R7-7:0	R8-7:0
G5-7:0	G6-7:0	G7-7:0	G8-7:0
B5-7:0	B6-7:0	B7-7:0	B8-7:0
R9-7:0	R10-7:0	R11-7:0	R12-7:0
G9-7:0	G10-7:0	G11-7:0	G12-7:0
B9-7:0	B10-7:0	B11-7:0	B12-7:0
.	.	.	.
.	.	.	.
.	.	.	.

2nd Lane0	2nd Lane1	2nd Lane2	2nd Lane3
R1281-7:0	R1282-7:0	R1283-7:0	R1284-7:0
G1281-7:0	G1282-7:0	G1283-7:0	G1284-7:0
B1281-7:0	B1282-7:0	B1283-7:0	B1284-7:0
R1285-7:0	R1286-7:0	R1287-7:0	R1288-7:0
G1285-7:0	G1286-7:0	G1287-7:0	G1288-7:0
B1285-7:0	B1286-7:0	B1287-7:0	B1288-7:0
R1289-7:0	R1290-7:0	R1291-7:0	R1292-7:0
G1289-7:0	G1290-7:0	G1291-7:0	G1292-7:0
B1289-7:0	B1290-7:0	B1291-7:0	B1292-7:0
.	.	.	.
.	.	.	.
.	.	.	.



3.4.3 Color versus Input Data

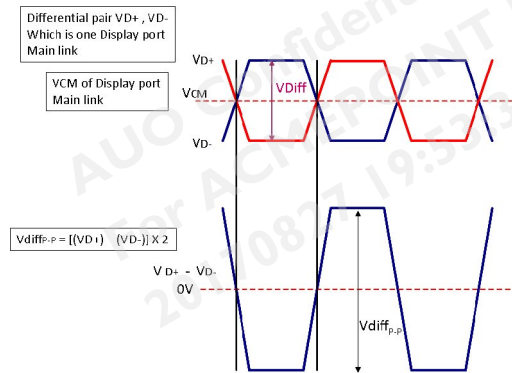
The following table is for color versus input data (8bit). The higher the gray level, the brighter the color.

Color	Gray Level	Color Input Data																								Remark
		RED data (MSB:R7, LSB:R0)								GREEN data (MSB:G7, LSB:G0)								BLUE data (MSB:B7, LSB:B0)								
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0	
Black	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
White	-	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
Gray 127	-	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	
Red	L0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Black
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	L255	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Green	L0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Black
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	L255	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	
Blue	L0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Black
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
	L255	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	

3.4.4 eDP Specification (Follow as VESA DisplayPort Standard Version 1.2)

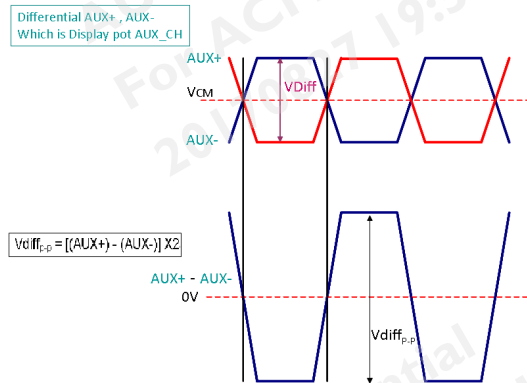
a. DisplayPort main link signal:

DisplayPort main link					
		Min	Typ	Max	unit
VCM	RX input DC Common Mode Voltage	-	0	-	v
VDiff _{P-P}	Peak-to-peak Voltage at a receiving Device	150	-	-	mV



b. DisplayPort AUX_CH signal:

DisplayPort AUX_CH					
		Min	Typ	Max	unit
VCM	AUX DC Common Mode Voltage	0		2.0	v
V Diff _{P-P}	AUX Peak-to-peak voltage at a receiving device	0.27		1.36	v



c. DisplayPort VHPD signal:

DisplayPort VHPD					
		Min	Typ	Max	unit
VHPD	HPD Voltage	2.25	-	3.6	v

d. Intra-Pair skew:



Product Specification

M270DTR01.0

AU OPTRONICS CORPORATION

LRX-SKEW-INTRA_PAIR		Min	Typ	Max	unit
LRX-SKEW-INTRA_PAIR	Lane Intra-pair Skew Tolerance	-	-	60	ps

e. Inter-Pair Skew:

LRX-SKEW-INTER_PAIR		Min	Typ	Max	unit
LRX-SKEW-INTER_PAIR	Lane-to-Lane Skew at RX package pins	-	-	5200	ps

3.4.5 Input Timing Specification

It only support DE mode, and the input timing are shown as the following table.

Symbol	Description		Min.	Typ.	Max.	Unit	Remark
Tv	Vertical Section	Period	1460	1480	8194	Th	
Tdisp (v)		Active	1440	1440	1440	Th	
Tblk (v)		Blanking	20	40	6754	Th	
Fv		Frequency	30	120	165	Hz	Note 3-5
Th	Horizontal Section	Period	1392	1400	1480	Tclk	
Tdisp (h)		Active	1280	1280	1280	Tclk	
Tblk (h)		Blanking	112	120	200	Tclk	
Fh		Frequency	94.8	177.6	245.8	KHz	Note 3-3
Tclk	Pixel Clock	Period	2.9	4.0	7.6	ns	1/Fclk
Fclk		Frequency	132	248.6	342.2	MHz	Note 3-4
Link Rate Per Lane			2.7			Gbps	

Note 3-3: The equation is listed as following. Please don't exceed the above recommended value.

$$Fh (Typ.) = Fclk (Typ.) / Th (Typ.)$$

$$Fh (Min.) \leq Fclk / Th \leq Fh (Max.)$$

Note 3-4: The equation is listed as following. Please don't exceed the above recommended value.

$$Fclk (Typ.) = Fv (Typ.) \times Th (Typ.) \times Tv (Typ.)$$

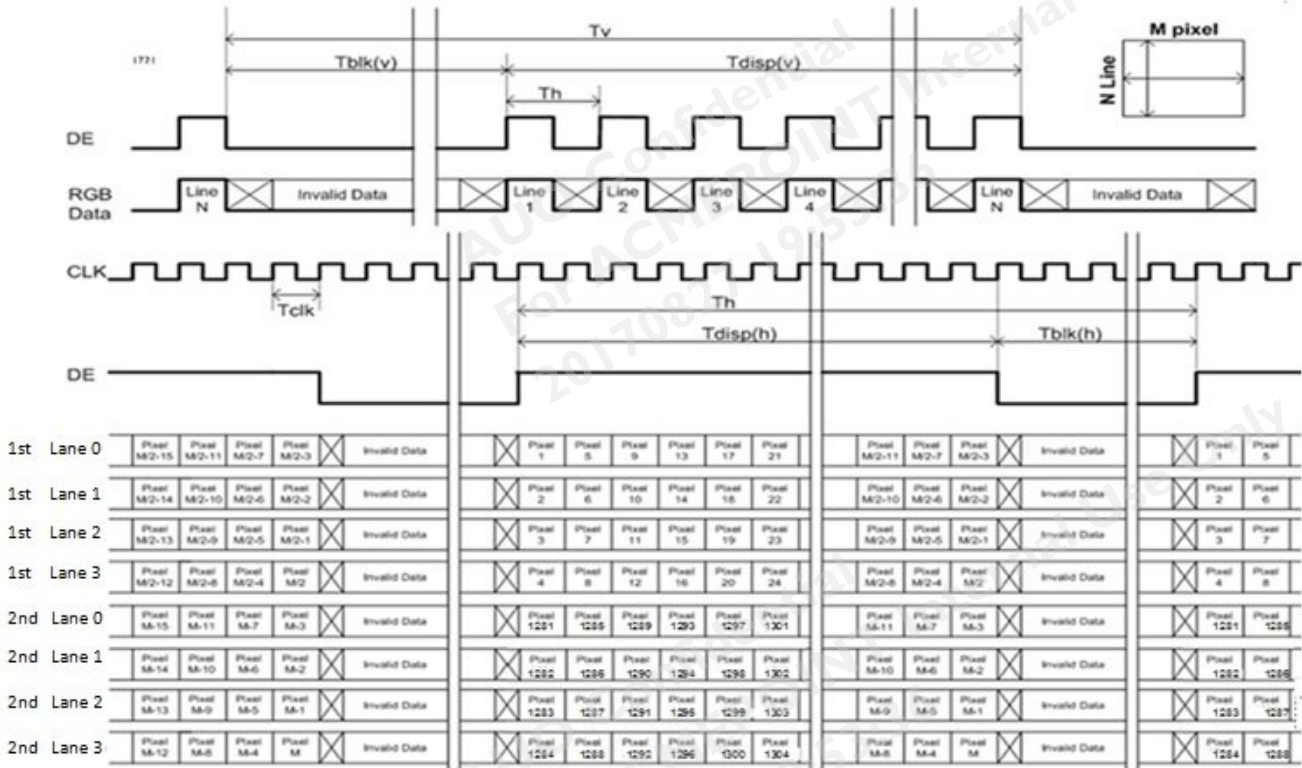
$$Fclk (Min.) \leq Fv \times Th \times Tv \leq Fclk (Max.)$$

Note 3-5: The optimal Vertical Frequency is 119~165 Hz for best picture quality.

3.4.6 Input Timing Diagram

(1st Lane0~3 eDP data:1, 2, 3, 4)

(2nd Lane0~3 eDP data:1281, 1282, 1283,1284)



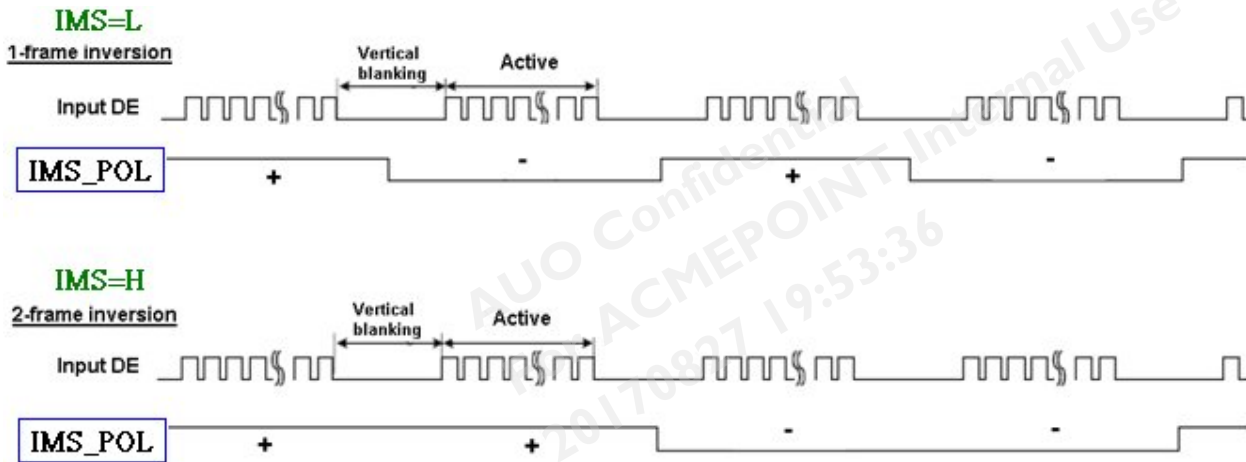
3.4.7 IMS Control

3.4.7.1. IMS control I/O Characteristics

Pin #	Symbol	I/O	Buffer	Description	Remark
pin 16	IMS_POL	O	4mA	Frame Inversion polarity Index IMS=L :1-frame inversion IMS=H :2-frame inversion	Note 3-7
pin 15	IMS	I	IPL*	Interlace Mode Selection	

* IPL : internal pull low

Note 3-7





3.4.7.2. Absolute Maximum Rating

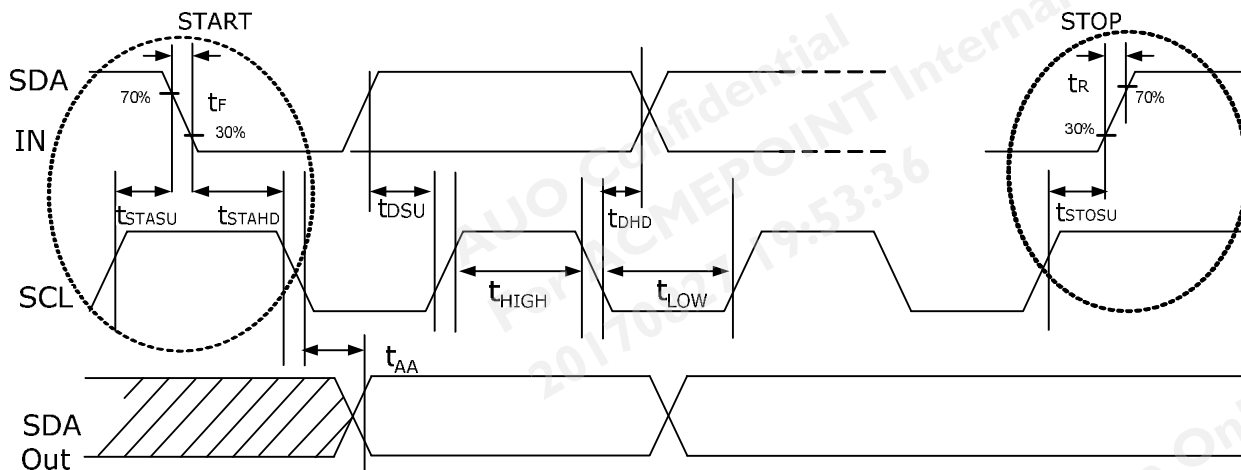
Symbol	Description	Min	Max	Unit	Remark
IMS	Interlace Mode	GND-0.3	5.0	[Volt]	Ta=25°C

3.4.7.3. Recommended Operating Condition

Symbol	Parameter	Condition	Rating			Unit
			Min	Typ	Max	
V _{IH}	Input High Voltage	-	2.0	-	3.6	V
V _{IL}	Input Low Voltage	-	0	-	0.8	V
V _{OH}	Output High Voltage	I _{OH} = 4mA	2.4	-	3.4	V
V _{OL}	Output Low Voltage	I _{OL} = -4mA	0	-	0.4	V

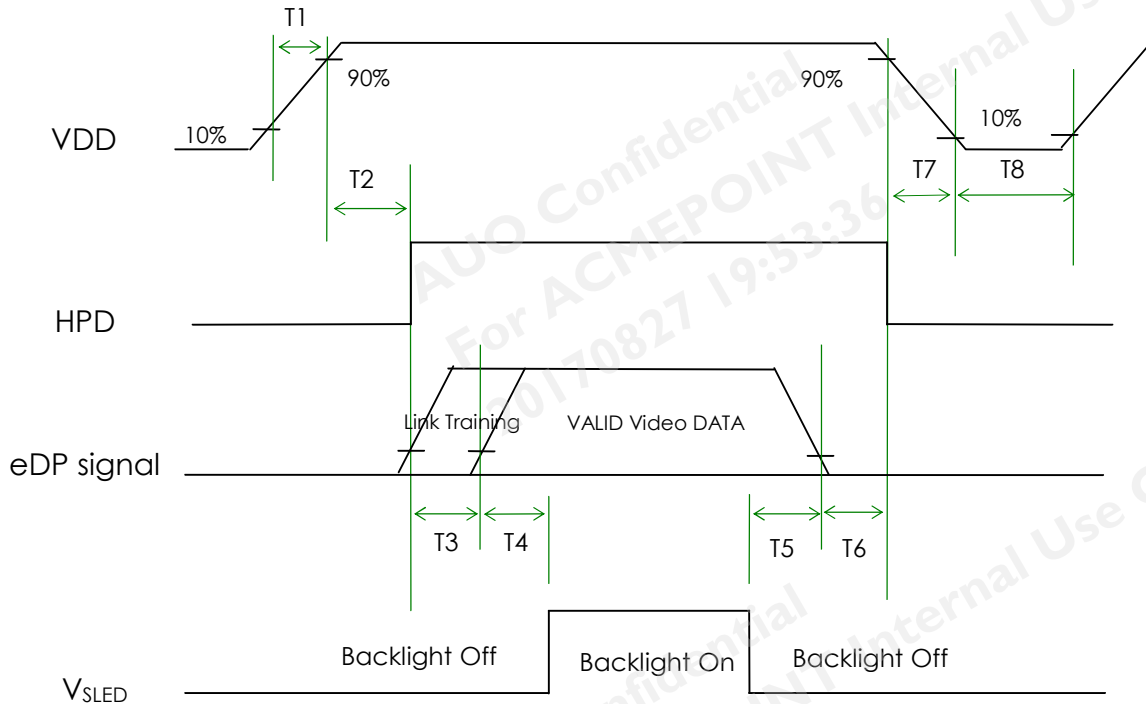
3.4.8 I2C Electrical Characteristics (VDD=12V, VSDA/VSCL=3.3V, TA=25°C)

Parameter		Symbol	Min.	Typ.	Max	Unit
I2C	SCL clock frequency	fSCL	-	-	350	kHz
	Clock Pulse Width Low	tLOW	1.85	-	-	µs
	Clock Pulse Width High	tHIGH	0.4	-	-	µs
	Clock Low to Data Output Valid	tAA	1.76	-	-	µs
	Start Setup Time	tSTASU	0.6	-	-	µs
	Start Hold Time	tSTAHD	0.6	-	-	µs
	Stop Setup Time	tSTOSU	0.6	-	-	µs
	Data In Setup Time	tDSU	0.1	-	-	µs
	Data In Hold Time	tDHD	0	-	-	µs
	SCL/SDA Rise Time	tR	-	-	0.3	µs
	SCL/SDA Fall Time	tF	-	-	0.3	µs



3.5 Power ON/OFF Sequence

VDD power, eDP signal and backlight on/off sequence are as following. eDP signals from any system shall be Hi-Z state when VDD is off.



Power Sequence Timing

Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
T1	0.5	-	10	[ms]	
T2	0	-	200	[ms]	
T3	0	-	-	[ms]	Note 3-7
T4	500	-	-	[ms]	
T5	100	-	-	[ms]	
T6	0	-	50	[ms]	Note 3-8 Note 3-9
T7	0	-	200	[ms]	Note 3-9 Note 3-10
T8	1000	-	-	[ms]	

Note 3-7: During T3 period , eDP link training time by customer's system.

Note 3-8: Recommend setting T6 = 0ms to avoid electronic noise when VDD is off.

Note 3-9: During T6 and T7 period , please keep the level of input eDP signals with Hi-Z state.

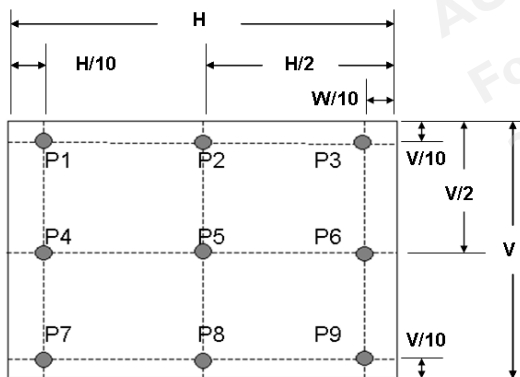
Note 3-10: Voltage of VDD must decay smoothly after power-off.(customer system decide this value)

3.6 Vcom adjustment flow

A. Flicker Pattern
 Column (1V) L127

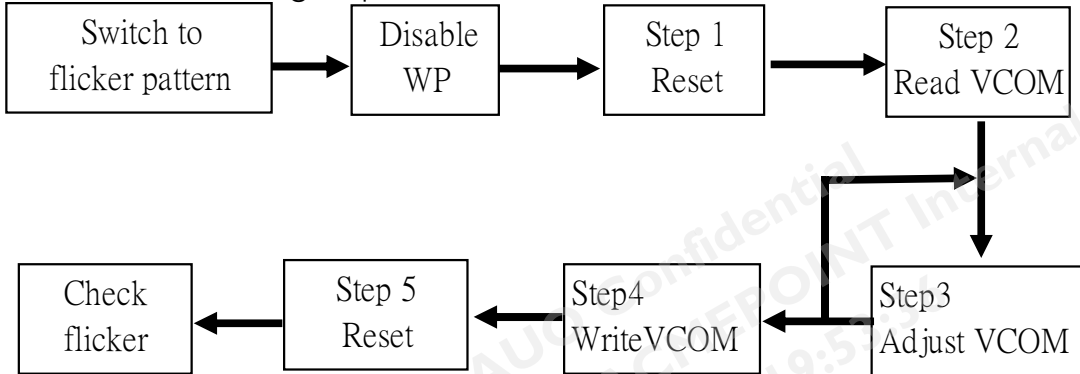


B. Vcom is optimization when minimized flicker phenomenon of location P5 (as below figure)



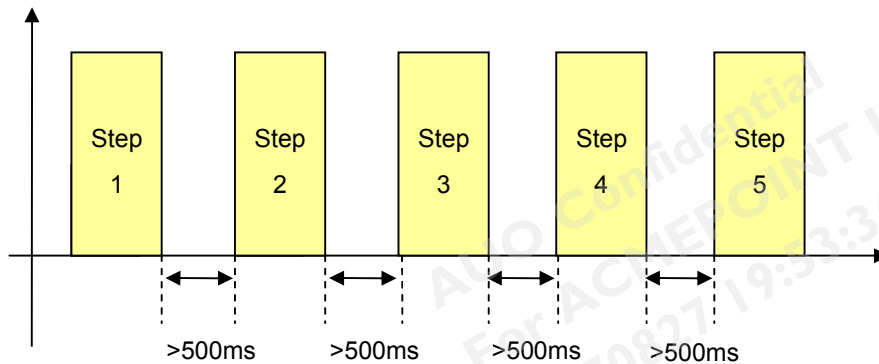
C. Tuning Step

VCOM I2C Tuning Step



D. Interval of Step to Step

VCOM I2C Tuning Step



E. I2C Protocol Define

DVCOM IC address (slave) : 1110100 (0x74)

Step1 Reset Command

Start	Slave Address							W	ACK	Index Address 0							ACK	Control Byte							ACK	Stop				
	1	1	1	0	1	0	0	0		0	0	0	0	0	0	0		0	0	0	0	0	0	1			0	0	1	0
	0xE8									0x00									0x12											
	Device Address + W									Control Address									Reset + OUT_EN											

Step2 Read Vcom Command

Start	Slave Address							W	ACK	Index Address 0							ACK	Start	Slave Address							W	ACK	VCOM data							ACK	Stop			
	1	1	1	0	1	0	0	0		0	0	0	0	0	0	0			1	1	1	1	0	1	0	0		1	X	X	X	X	X	X			X	X	NA
	0xE8									0x01										0xE9									0~127										
	Device Address + W									VCOM Address										Device Address + R									DATA										

Step3 Adjust Vcom Command

Start	Slave Address							W	ACK	Index Address 1							ACK	VCOM data							ACK	Stop			
	1	1	1	0	1	0	0	0		0	0	0	0	0	0	0		1	X	X	X	X	X	X			X	X	NA
	0xE8									0x01									0~127										
	Device Address + W									VCOM Address									VCOM Value										

Step4 Write Vcom Command

Start	Slave Address							W	ACK	Index Address 0							ACK	Control Byte							ACK	Stop		
	1	1	1	0	1	0	0	0		0	0	0	0	0	0	0		0	0	0	0	0	1	0			1	0
	0xE8									0x00									0x0A									
	Device Address + W									Control Address									Write DAC to NVM									

Step5 Reset Command

Start	Slave Address							W	ACK	Index Address 0							ACK	Control Byte							ACK	Stop		
	1	1	1	0	1	0	0	0		0	0	0	0	0	0	0		0	0	0	0	1	0	0			1	0
	0xE8									0x00									0x12									
	Device Address + W									Control Address									Reset + OUT_EN									



4 Reliability Test

AUO reliability test items are listed as following table. *(Bare Panel only)*

Items	Condition	Remark
Temperature Humidity Bias (THB)	Ta= 50°C , 80%RH, 300hours	
High Temperature Operation (HTO)	Ta= 50°C , 50%RH, 300hours	
Low Temperature Operation	Ta= 0°C , 300hours	
High Temperature Storage (HTS)	Ta= 60°C , 300hours	
Low Temperature Storage (LTS)	Ta= -20°C , 300hours	
Thermal Shock Test (TST)	-20°C/30min, 60°C/30min, 100 cycles	Note 4-1

- Note 4-1:**
- a. A cycle of rapid temperature change consists of varying the temperature from -20°C to 60°C, and back again. Power is not applied during the test.
 - b. After finish temperature cycling, the unit is placed in normal room ambient for at least 4 hours before power on.

5 Shipping Label

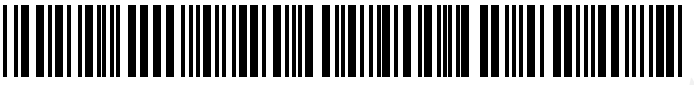
5.1 Small Shipping Label

The label is on the PCBA as shown below :

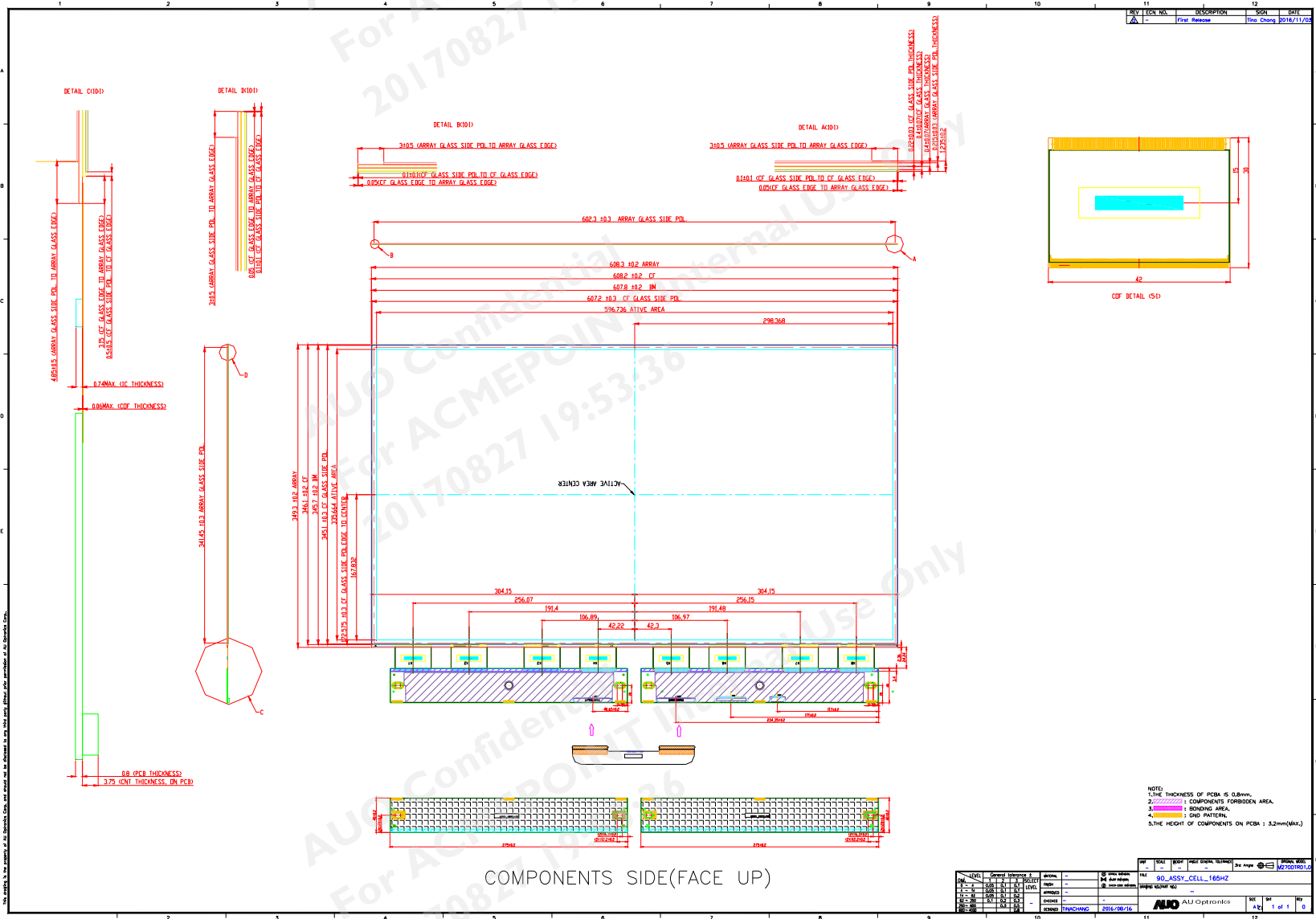


5.2 Run Card Label

The label is on the panel as shown below :

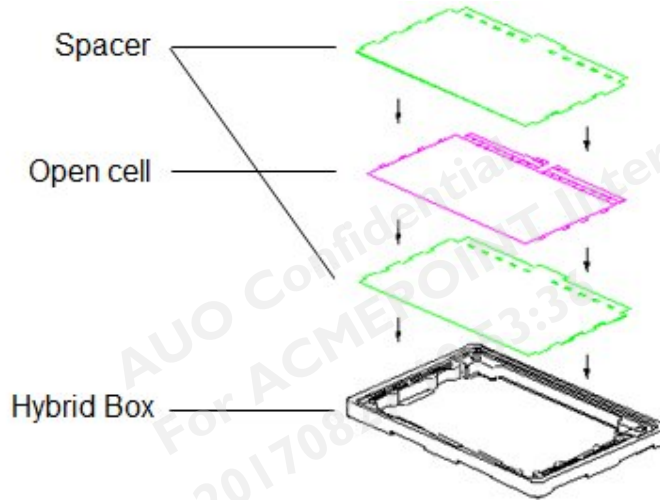
M270DTN01-x/xx		xx:xxxxxxxxxx	Remark : X	
0				SKD
S/N	xxxxxxxxxxxx (xxxxx)	Z	P	N V
xxxxx	xxxxx	xxxxx		
xxxxx	xxxxx	xxxxx		
xxxxx	xxxxx	xxxxx		
xxxxx	xxxxx	xxxxx		

6 Mechanical Characteristics

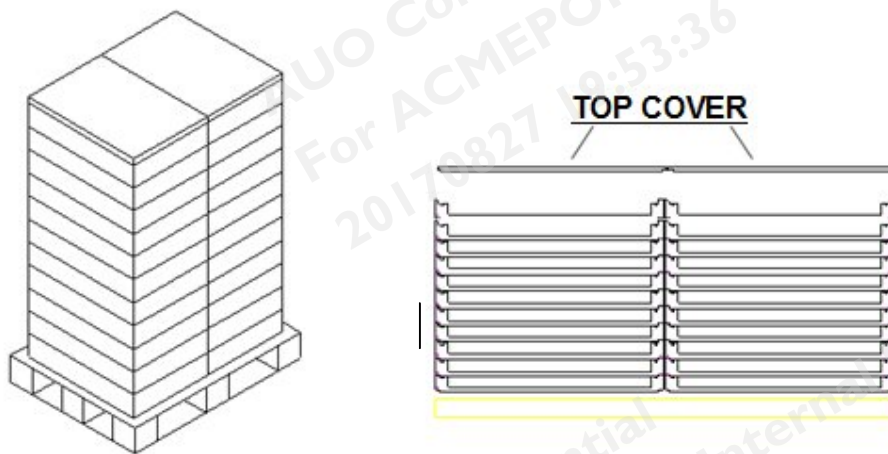


7 Packing Specification

7.1 Packing Flow



- Open cell : 16 (pcs/Box)
- Spacer : 17 (pcs/Box)



- 2 (Box/Layer)
- 10 (Layer/Pallet)

7.2 Pallet and shipment information

Item	Specification			Remark
	Q'ty	Dimension	Weight(kg)	
Box	1	780(L)mm x 545(W)mm x 161(H)mm	2.26	without cell & spacer
Packing Box	20pcs/Box	780(L)mm x 545(W)mm x 161(H)mm	13.76	with cell & Box & spacer
Pallet	1	1150(L)mm x 840(W)mm x 132(H)mm	13.6	
Pallet after Packing	20 boxes/pallet	1150(L)mm x 840(W)mm x 1330(H)mm	288.8	