

Model Name: P430QVN01.3

Issue Date: 2021/05/20

() Preliminary Specifications
(*) Final Specifications

Customer Signature	Date	AUO	Date
Approved By		Approval By PM Director CT Wu <i>CT Wu</i>	
Note		Reviewed By RD Director Lamy Chen <i>Lamy Chen</i>	
		Reviewed By Project Leader Chia Hsuan Lin <i>Chia Hsuan Lin</i>	
		Prepared By PM Phoebe Chen <i>Phoebe Chen</i>	

CONTENTS

1. GENERAL DESCRIPTION	4
2. ABSOLUTE MAXIMUM RATINGS	5
3. OPTICAL SPECIFICATION	6
4. INTERFACE SPECIFICATION	9
4.1 INPUT POWER	9
4.2 INPUT CONNECTION	10
4.3 INPUT DATA FORMAT	13
4.3.1 V by one color data mapping	13
4.3.2 Color Input Data Reference	14
5. SIGNAL TIMING SPECIFICATION	15
5.1 INPUT TIMING	15
5.2 V BY ONE SPEC	17
5.3 POWER SEQUENCE FOR LCD	20
6. MECHANICAL CHARACTERISTICS	21
6.1 OPEN CELL AND T-CON MECHANICAL DRAWING	21
6.2 FFC SHAPE AND DIMENSION RECOMMENDATION	23
6.2.1 Connector Type	23
6.2.2 FFC Drawing	23
7. PACKING	24
8. PRECAUTIONS	27
8.1 STORAGE	27
8.2 MODULE ASSEMBLY	27
8.2.1 Protection film peeling	27
8.2.2 Assembly Precautions	27
8.2.3 FFC & PCB Precautions	28
8.2.4 Flicker adjust	28
8.3 AGING	28
8.4 OPERATING PRECAUTIONS	28
8.5 OTHERS	29
APPENDIX I – VCOM ADJUSTMENT	30

1. General Description

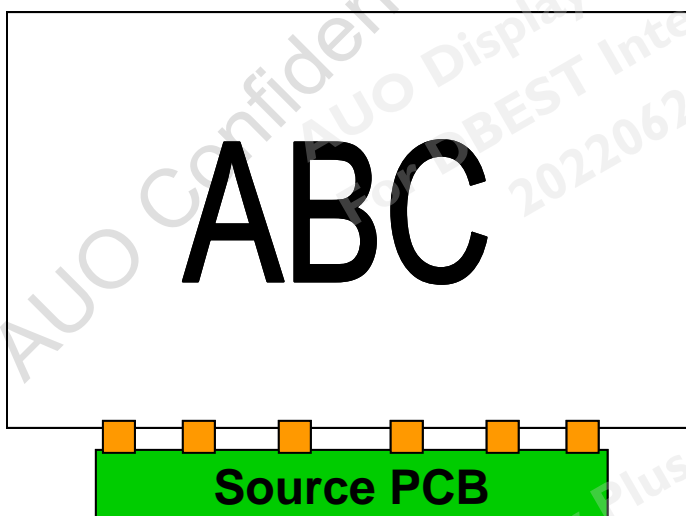
This specification applies to the 43 inch Color TFT-LCD SKD model P430QVN01.3. This Open Cell Unit has a TFT active matrix type liquid crystal panel with 3840 x 2160 pixels and V by one interface; which can display up to 1.07 billion colors.

* General Information

Items	Specification	Unit	Note
Active Screen Size	43	inch	
Display Area	941.184 (H) x 529.416 (V)	mm	
Outline Dimension	953 (H) x 577.99 (V)	mm	
Cell Dimension	953 (H) x 543 (V) x 1.4(D)	mm	D: cell thickness
Driver Element	a-Si TFT active matrix		
Display Colors	10 bit (8bit+FRC)	Colors	
Number of Pixels	3,840 x 2,160	Pixel	
Pixel Pitch	0.2451 (H) x 0.2451(W)	mm	
Pixel Arrangement	RGB vertical stripe		
Display Operation Mode	Normally Black		
Surface Treatment	Anti-Glare, 3H		Haze=25%
Transmittance (with Polarizer)	4.1%		Typical value
Weight	1530	g	Typical value
Display Orientation	Signal input with "ABC"		Note 1

Note 1: LCD display as below illustrated when signal input with "ABC".

Front side



2. Absolute Maximum Ratings

The followings are maximum values which, if exceeded, may cause faulty operation or damage to the unit or the unrecoverable damage on the device.

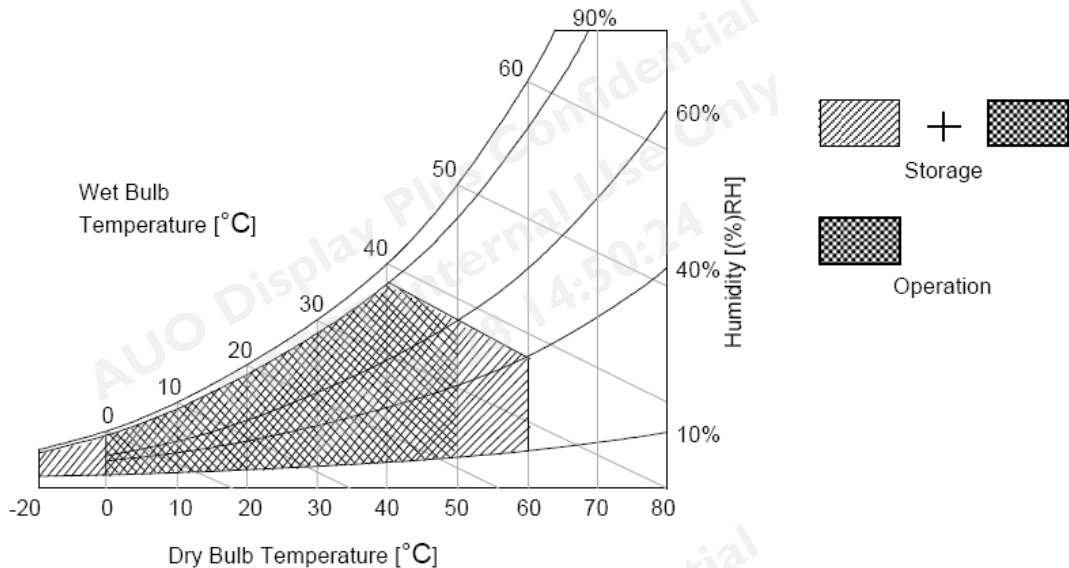
Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	V _{DD}	-0.3	14	[Volt] _{DC}	Note 1
Input Voltage of Signal	V _{in}	-0.3	4	[Volt] _{DC}	Note 1
Operating Temperature	TOP	0	+50	[°C]	Note 2
Operating Humidity	HOP	10	90	[%RH]	Note 2
Storage Temperature	TST	-20	+60	[°C]	Note 2
Storage Humidity	HST	10	90	[%RH]	Note 2
Panel Surface Temperature	PST		65	[°C]	Note 3

Note 1: Duration:50 msec.

Note 2 : Maximum Wet-Bulb should be 39°C and No condensation.

The relative humidity must not exceed 90% non-condensing at temperatures of 40°C or less. At temperatures greater than 40°C, the wet bulb temperature must not exceed 39°C

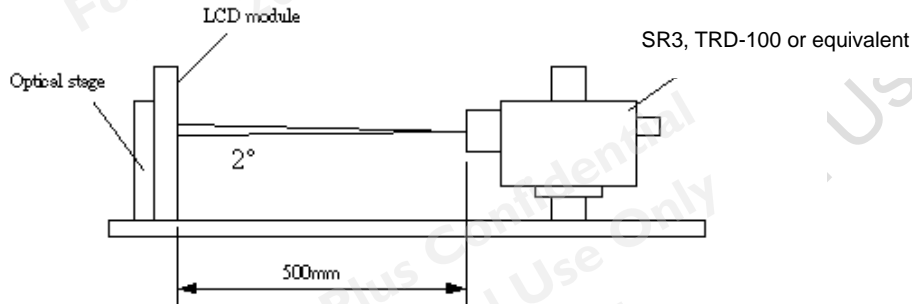
Note 3: Surface temperature is measured at 50°C Dry condition



3. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable for approximately 45 minutes in a dark environment at 25°C. The values specified are measured on the center of active area and at an approximate distance 500 mm from the LCD surface at a viewing angle of ϕ and θ equal to 0°.

Fig.1 presents additional information concerning the measurement equipment and method.



Parameter	Symbol	Condition	Values			Unit	Notes
			Min.	Typ.	Max		
Contrast Ratio	CR	SR3, TRD-100	3200	4000	--		1, 2
Response Time (G to G)	T_{γ}		--	8	16	ms	3
Color Chromaticity		With SR3 Standard light source "C"	Typ.-0.03		Typ.+0.03		4
Red	R_x			0.664			
	R_y			0.324			
Green	G_x			0.273			
	G_y			0.593			
Blue	B_x			0.137			
	B_y			0.116			
White	W_x			0.291			
	W_y	0.346					
Viewing Angle		SR3					1, 5
x axis, right($\phi=0^\circ$)	θ_r		85	89	--	degree	
x axis, left($\phi=180^\circ$)	θ_l		85	89	--	degree	
y axis, up($\phi=90^\circ$)	θ_u		85	89	--	degree	
y axis, down ($\phi=270^\circ$)	θ_d		85	89	--	degree	

1. Light source here is the BLU of AUO module (film structure: two diffuser sheets).
2. Contrast Ratio (CR) is defined mathematically as:

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance at center location of all white pixels}}{\text{Surface Luminance at center location of all black pixels}}$$

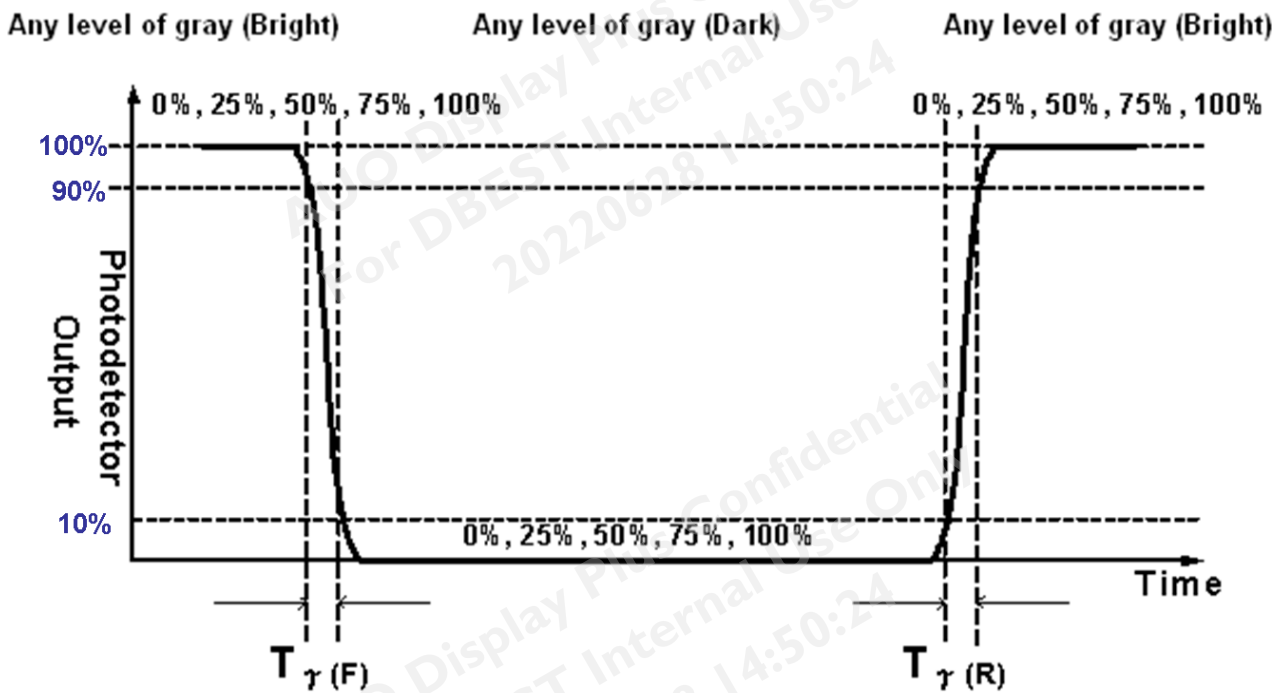
3. Response time T_{γ} is the average time required for display transition by switching the input signal for five luminance ratio (0%,25%,50%,75%,100% brightness matrix) and is based on Frame rate = 60Hz to optimize.

Measured Response Time		Target				
		0%	25%	50%	75%	100%
Start	0%		0% to 25%	0% to 50%	0% to 75%	0% to 100%
	25%	25% to 0%		25% to 50%	25% to 75%	25% to 100%
	50%	50% to 0%	50% to 25%		50% to 75%	50% to 100%
	75%	75% to 0%	75% to 25%	75% to 50%		75% to 100%
	100%	100% to 0%	100% to 25%	100% to 50%	100% to 75%	

T_{γ} is determined by 10% to 90% brightness difference of rising or falling period. (As illustrated)

The response time is defined as the following figure and shall be measured by switching the input signal for “any level of gray(bright)” and “any level of gray(dark)”.

FIG.3 Response Time

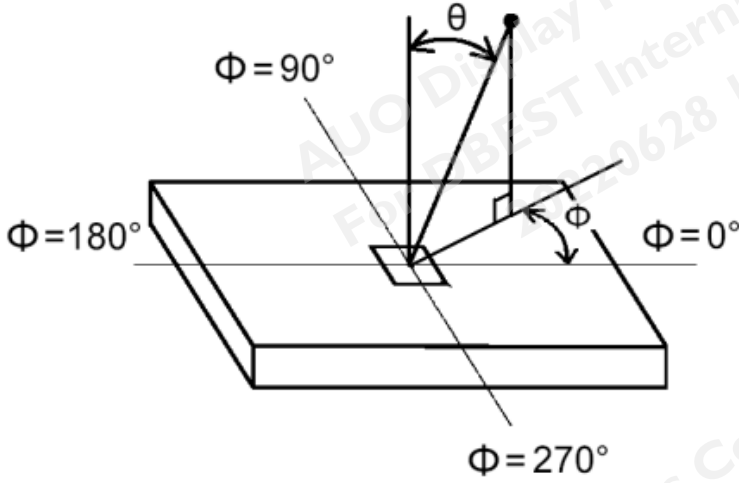


4. Light source here is the standard light source “C” which is defined by CIE and driving voltages are based on suitable gamma voltages. The calculating method is as following :

- A. Measure the “Module” and “BLU” optical spectrums (W, R, G, B).
- B. Calculate cell spectrum from “Module” and “BLU” spectrums.
- C. Calculate color chromaticity by using cell spectrum and the spectrum of standard light source “C”.

5. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see FIG4.

FIG.4 Viewing Angle



4. Interface Specification

4.1 Input power

The P430QVN01.3 Open Cell Unit requires power input which is employed to power the LCD electronics and to drive the TFT array and liquid crystal.

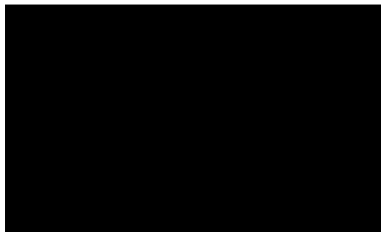
Item	Symbol	Min.	Typ.	Max	Unit	Note
Power Supply Input Voltage	V _{DD}	10.8	12	13.2	V	1
Power Supply Input Current	Black pattern	-	0.73	0.88	A	2
	White pattern	-	0.75	0.9	A	
	H-strip pattern	-	1.42	1.71	A	
Power Consumption	Black pattern	-	8.76	10.56	Watt	2
	White pattern	-	9	10.8	Watt	
	H-strip pattern	-	17.04	20.52	Watt	
Inrush Current	I _{RUSH}	--	--	5	A	3

Note1. The ripple voltage should be fewer than 5% of V_{DD}.

Note2. Test Condition:

- (1) V_{DD} = 12.0V, (2) F_v = 60Hz, (3) F_{clk} = 74.25MHz, (4) Temperature = 25 °C
- (5) Power dissipation check pattern. (Only for power design)

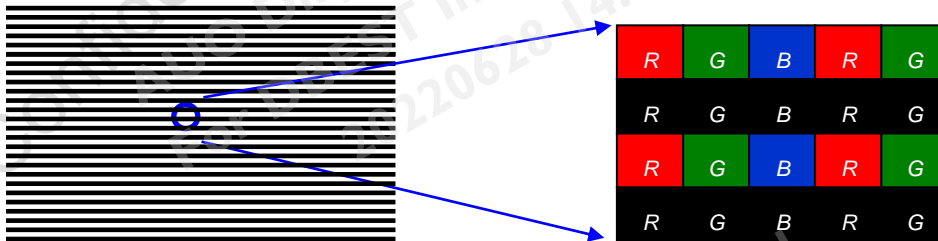
a. Black pattern



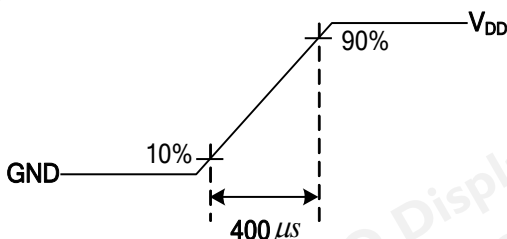
b. White pattern



c. H-Strip pattern



Note3. Measurement condition : Rising time = 400us



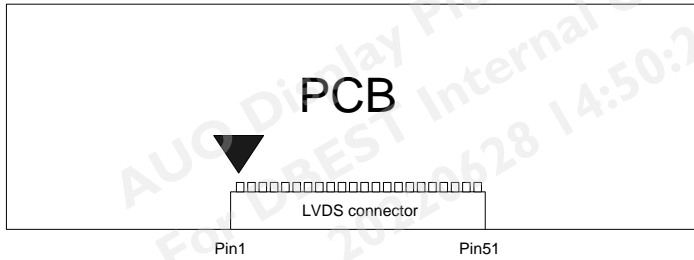
4.2 Input Connection

- LCD connector: JAE FI-RTE51SZ-HF

PIN	Symbol	Description	PIN	Symbol	Description
1	V _{DD}	Power Supply Input Voltage	26	LOCKN	Vx1 LOCK
2	V _{DD}	Power Supply Input Voltage	27	GND	Ground
3	V _{DD}	Power Supply Input Voltage	28	RX0N	Vx1 lane 0
4	V _{DD}	Power Supply Input Voltage	29	RX0P	Vx1 lane 0
5	V _{DD}	Power Supply Input Voltage	30	GND	Ground
6	V _{DD}	Power Supply Input Voltage	31	RX1N	Vx1 lane 1
7	V _{DD}	Power Supply Input Voltage	32	Rx1P	Vx1 lane 1
8	V _{DD}	Power Supply Input Voltage	33	GND	Ground
9	N.C.	No connection (for AUO test only. Do not connect)	34	RX2N	Vx1 lane 2
10	GND	Ground	35	RX2P	Vx1 lane2
11	GND	Ground	36	GND	Ground
12	GND	Ground	37	RX3N	Vx1 lane 3
13	GND	Ground	38	RX3P	Vx1 lane 3
14	GND or N.C.	Ground or No connection (for AUO test only. Do not connect)	39	GND	Ground
15	N.C.	No connection (for AUO test only. Do not connect)	40	RX4N	Vx1 lane 4
16	N.C.	No connection (for AUO test only. Do not connect)	41	RX4P	Vx1 lane 4
17	N.C.	No connection (for AUO test only. Do not connect)	42	GND	Ground
18	SDA	SDA - I2C Serial Data Open : High (3.3V)	43	RX5N	Vx1 lane 5
19	SCL	SCL - I2C Serial Clock Open : High (3.3V)	44	RX5P	Vx1 lane 5
20	WP	EEPROM Write Protection High (3.3V) for Writable, Open/Low (GND) for Protection	45	GND	Ground
21	N.C.	No connection (for AUO test only. Do not connect)	46	RX6N	Vx1 lane 6
22	GND or N.C.	Ground or No connection (for AUO test only. Do not connect)	47	RX6P	Vx1 lane 6
23	N.C.	No connection (for AUO test only. Do not connect)	48	GND	Ground
24	GND	Ground	49	RX7N	Vx1 lane 7

25	HTPDN	Vx1 HTPDN	50	RX7P	Vx1 lane 7
			51	GND	Ground

Note1. Pin number start from the left side as the following figure.



Note2. Please leave this pin unoccupied. It can not be connected by any signal (Low/GND/High).

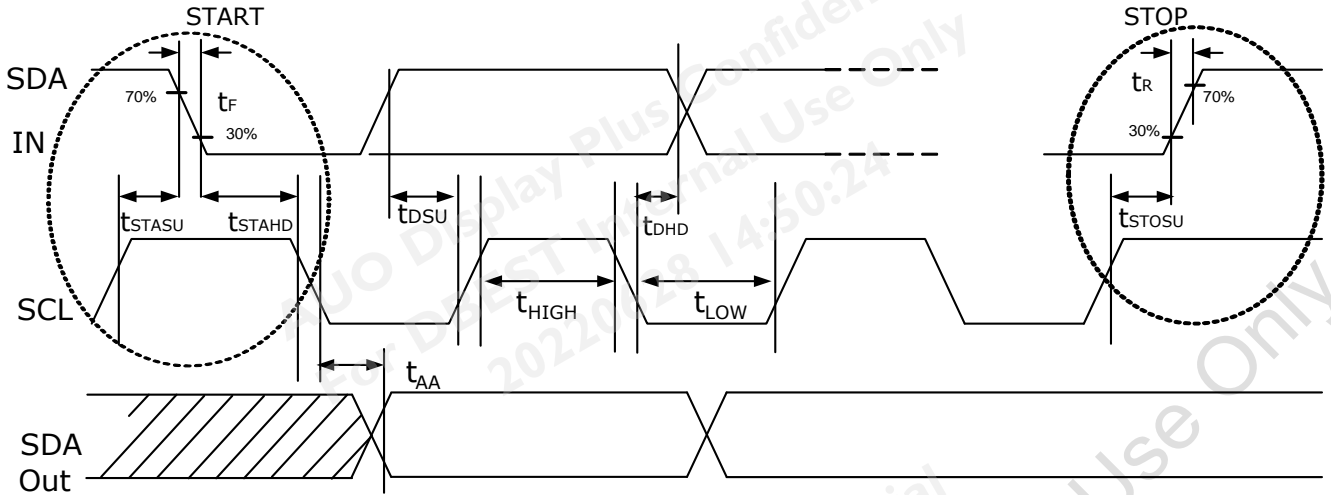
Note3. Input control signal threshold voltage definition

Item	Symbol	Min.	Typ.	Max.	Unit
Input High Threshold Voltage	VIH	2.7	-	3.6	V
Input Low Threshold Voltage	VIL	0	-	0.6	V

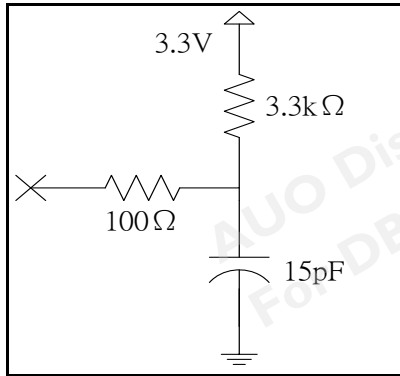
Note4. I2C Data and Clock

I2C Data and Clock timing

Parameter		Symbol	Min.	Typ.	Max	Unit
I2C	SCL clock frequency	fSCL	-	-	350	MHz
	Clock Pulse Width Low	tLOW	1.85	-	-	us
	Clock Pulse Width High	tHIGH	0.4	-	-	us
	Clock Low to Data Output Valid	tAA	1.76	-	-	us
	Start Setup Time	tSTASU	0.6	-	-	us
	Start Hold Time	tSTAHD	0.6	-	-	us
	Stop Setup Time	tSTOSU	0.6	-	-	us
	Data In Setup Time	tDSU	0.1	-	-	us
	Data In Hold Time	tDHD	0	-	-	us
	SCL/SDA Rise Time	tR	-	-	0.3	us
	SCL/SDA Fall Time	tF	-	-	0.3	us



Input equivalent impedance of SDA/SCL pin

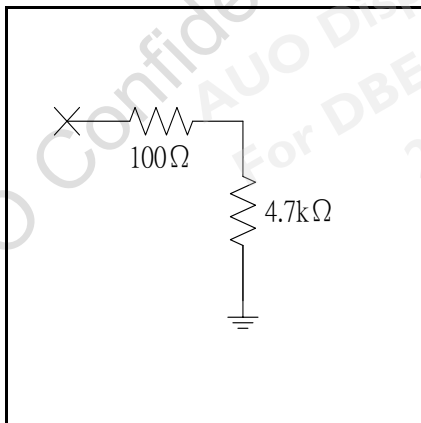


Note5. Write Protection

Mode selection

WP	Note
L or OPEN	Protection
H	Writable

Input equivalent impedance of WP pin



4.3 Input Data Format

4.3.1 V by one color data mapping

Mode	Packer input & Unpacker output	30bpp RGB /YCbCr444 (10bit)	
4byte mode	Byte0	D[0]	R/Cr[2]
		D[1]	R/Cr[3]
		D[2]	R/Cr[4]
		D[3]	R/Cr[5]
		D[4]	R/Cr[6]
		D[5]	R/Cr[7]
		D[6]	R/Cr[8]
		D[7]	R/Cr[9]
	Byte1	D[8]	G/Y[2]
		D[9]	G/Y[3]
		D[10]	G/Y[4]
		D[11]	G/Y[5]
		D[12]	G/Y[6]
		D[13]	G/Y[7]
		D[14]	G/Y[8]
		D[15]	G/Y[9]
	Byte2	D[16]	B/Cb[2]
		D[17]	B/Cb[3]
		D[18]	B/Cb[4]
		D[19]	B/Cb[5]
		D[20]	B/Cb[6]
		D[21]	B/Cb[7]
		D[22]	B/Cb[8]
		D[23]	B/Cb[9]
	Byte3	D[24]	--
		D[25]	--
		D[26]	B/Cb[0]
		D[27]	B/Cb[1]
		D[28]	G/Y[0]
		D[29]	G/Y[1]
		D[30]	R/Cr[0]
		D[31]	R/Cr[1]

4.3.2 Color Input Data Reference

The brightness of each primary color (red, green and blue) is based on the 10 bit (8 bit+FRC)gray scale data input for the color; the higher the binary input, the brighter the color. The table below provides a reference for color versus data input.

COLOR DATA REFERENCE

Color		Input Color Data																													
		RED										GREEN										BLUE									
		MSB					LSB					MSB					LSB					MSB			LSB						
		R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Blue(1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R	RED(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	RED(001)	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

	RED(1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
G	GREEN(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	GREEN(001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	

	GREEN(1022)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	GREEN(1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
B	BLUE(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	BLUE(001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	

	BLUE(1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0
	BLUE(1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

5. Signal Timing Specification

5.1 Input Timing

This is the signal timing required at the input of the user connector. All of the interface signal timing should be satisfied with the following specifications for its proper operation.

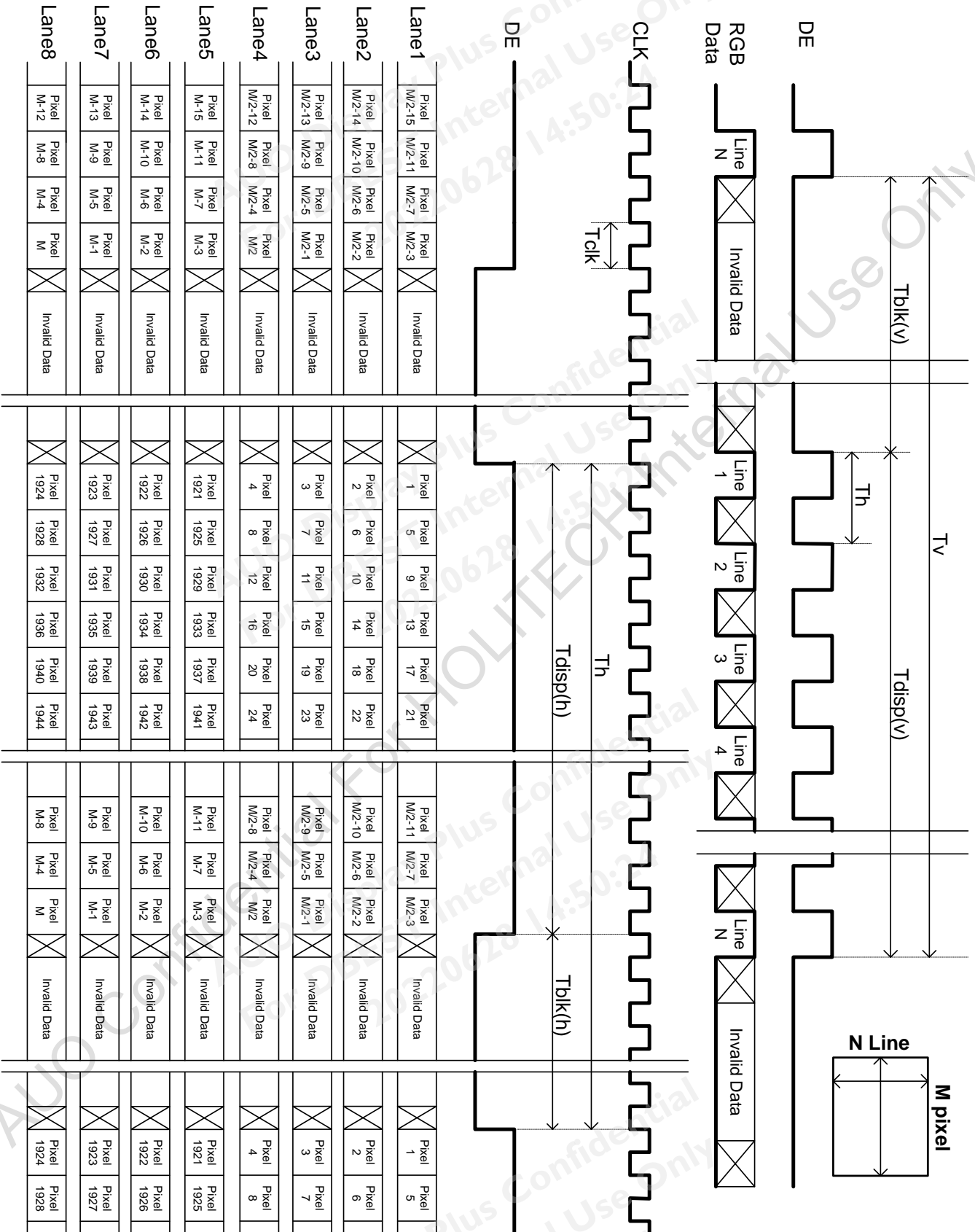
Timing Table (DE only Mode)

For 2D application

Signal	Item	Symbol	Min.	Typ.	Max	Unit
Vertical Section	Period	Tv	2200	2250	2715	Th
	Active	Tdisp (v)	2160			
	Blanking	Tblk (v)	40	90	555	Th
Horizontal Section	Period	Th	530	550	600	Tclk
	Active	Tdisp (h)	480			
	Blanking	Tblk (h)	50	70	120	Tclk
Clock	Frequency	Fclk=1/Tclk	66	74.25	77	MHz
Vertical Frequency	Frequency	Fv	47	60	63	Hz
Horizontal Frequency	Frequency	Fh	120	135	139.2	KHz

The timing diagrams of the input timing

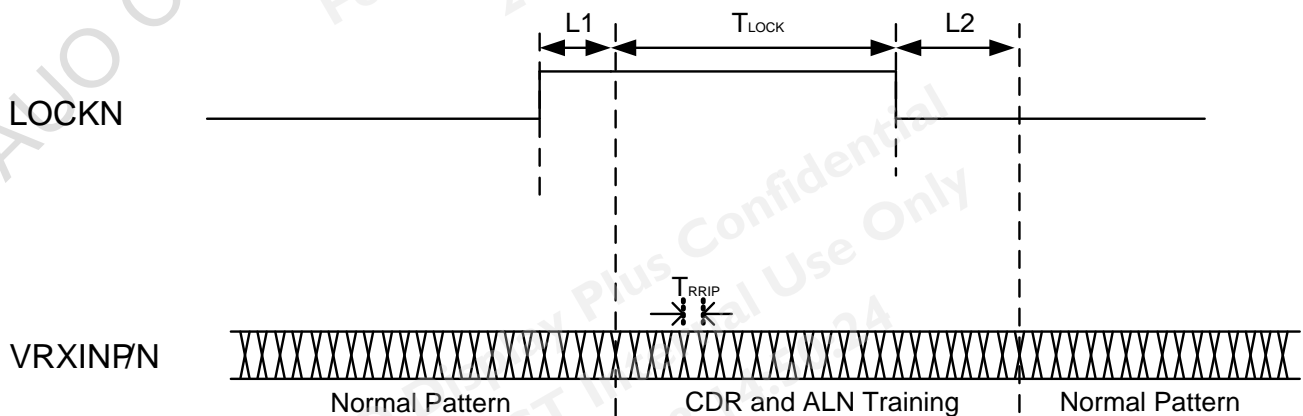
(Lane1~8 V-by one data: 1, 2, 3, 4, 1921, 1922, 1923, 1924)



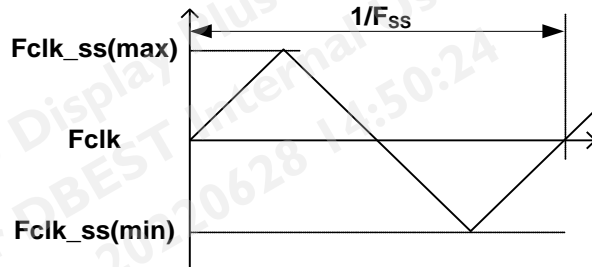
5.2 V by one spec

Item	Symbol	Min.	Typ.	Max	Unit	Note	
V-by-one Interface	VRXINP/N input each bit Period	T_{RRIP} (UI)	310	--	379	ps	10bit 1
	Receiver Clock : Spread Spectrum Modulation range	Fclk_ss	Fclk -0.5%	--	Fclk +0.5%	MHz	2
	Receiver Clock : Spread Spectrum Modulation frequency	Fss	--	--	30	KHz	2
	CDR training pattern time	T_{LOCK}	--	500	--	us	1
	Latency from LOCKN 'HIGH' to clock training pattern	L1	0	--	--	us	1
	Latency from LOCKN 'LOW' to normal 8b10b data	L2	--	--	70	us	1
	CML Differential Input High Threshold	V_{RTH}	+50	--	--	mV _{DC}	
	CML Differential Input Low Threshold	V_{RTL}	--	--	-50	mV _{DC}	
	CML Common mode Bias Voltage	V_{RCT}	0.8	0.9	1.0	V _{DC}	
	Intra-pair skew	T_{INTRA}	--	--	0.3	UI	3
	Inter-pair skew	T_{INTER}	--	--	5	UI	4
	Eye diagram at receiver	A_X	--	0.25	--	UI	5
		A_Y	--	0	--	mV	
		B_X	--	0.3	--	UI	
B_Y		--	50	--	mV		
C_X		--	0.7	--	UI		
C_Y		--	50	--	mV		
D_X		--	0.75	--	UI		
D_Y		--	0	--	mV		
E_X		--	0.7	--	UI		
E_Y		--	-50	--	mV		
F_X	--	0.3	--	UI			
F_Y	--	-50	--	mV			

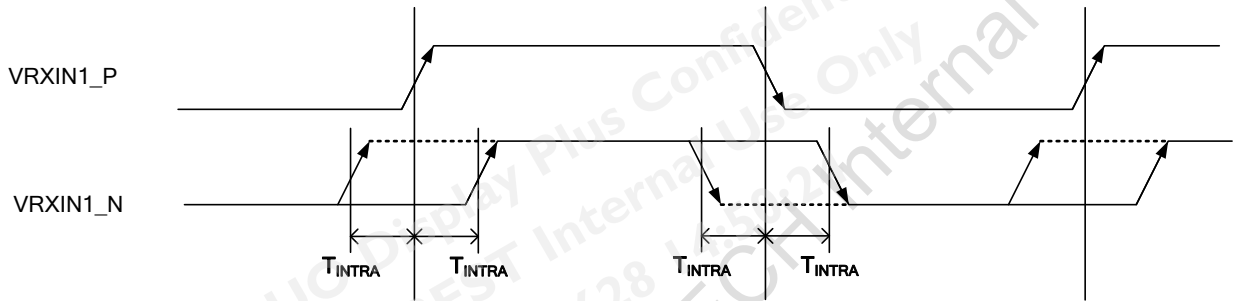
1. V-by-one Signal diagram



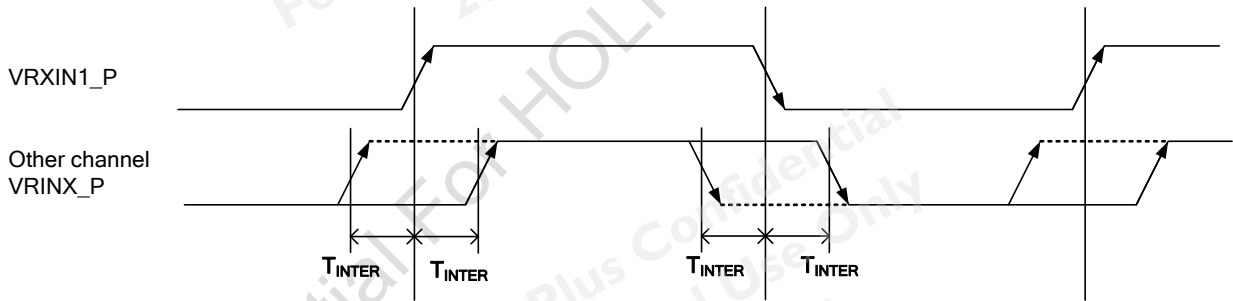
2. Receiver Clock SSCG (Spread spectrum clock generator) is defined as below figures.



3. V-by-one Intra-pair Skew

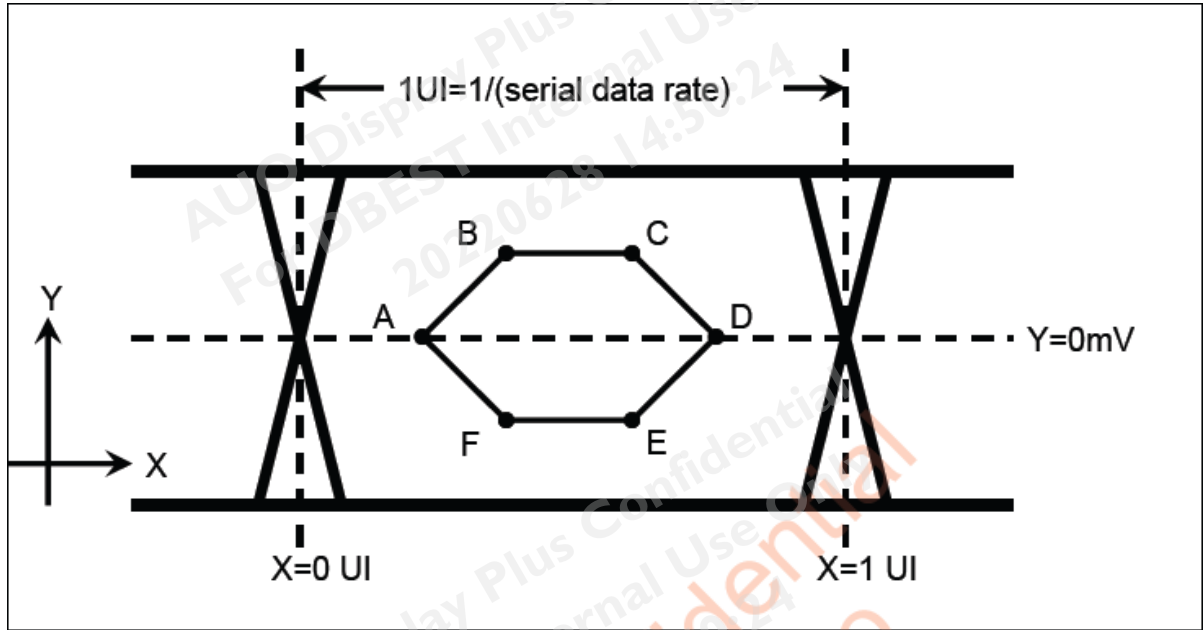


4. V-by-one Inter-pair Skew



5. Eye diagram at receiver

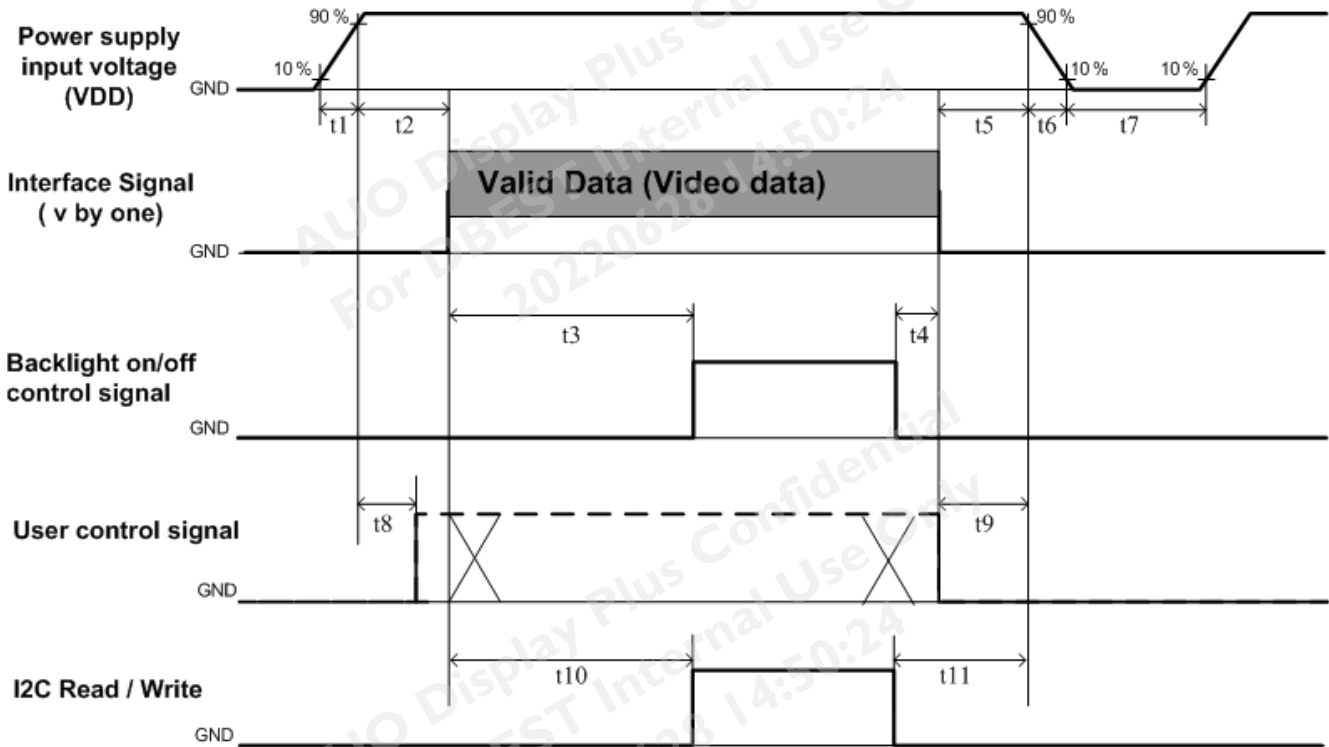
Eye Mask



Example of Eye diagram



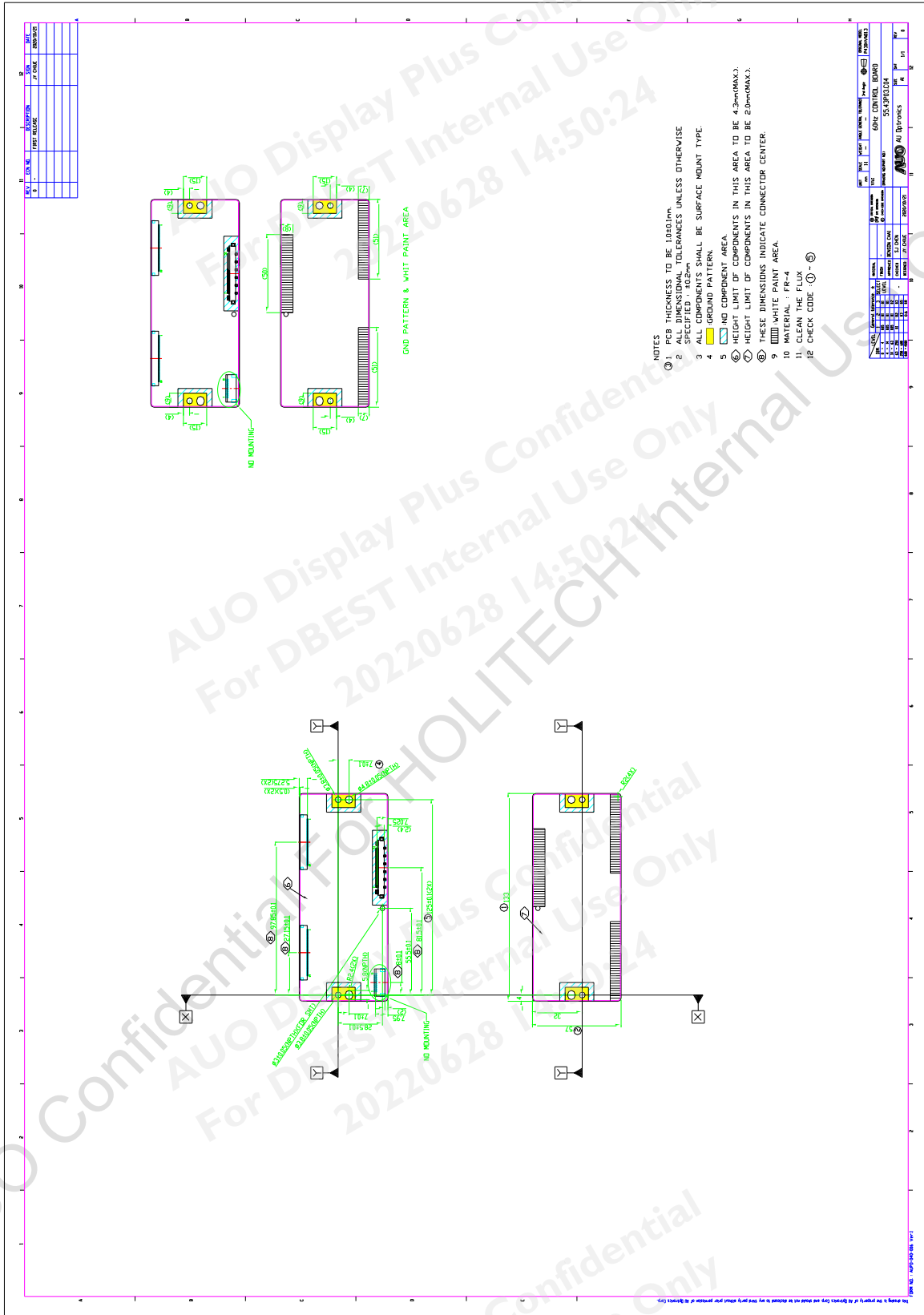
5.3 Power Sequence for LCD



Parameter	Values			Unit
	Min.	Type.	Max.	
t1	0.4	---	30	ms
t2	40	---	---	ms
t3	640	---	---	ms
t4	0*1	---	---	ms
t5	0	---	---	ms
t6	---	---	---*2	ms
t7	1000	---	---	ms
t8	20*3	---	50	ms
t9	0	---	---	ms
t10	640	---	---	ms
t11	150	---	---	ms

Note:

- (1) t4=0 : concern for residual pattern before BLU turn off.
- (2) t6 : voltage of VDD must decay smoothly after power-off. (customer system decide this value)
- (3) When user control signal is N.C. (no connection), opened in Transmitted end, t8 timing spec can be negligible.

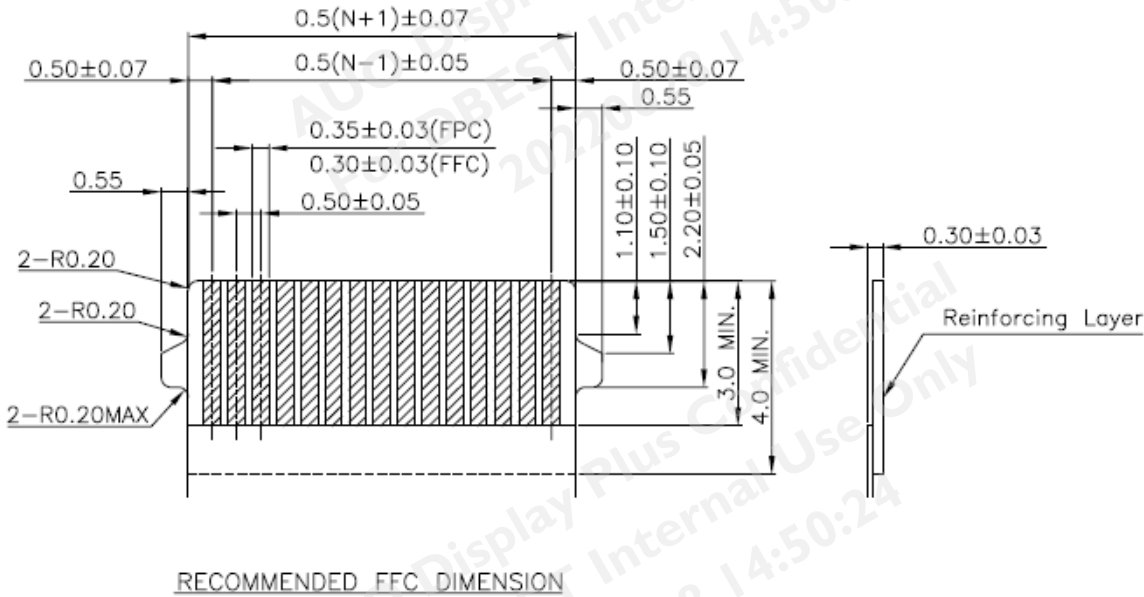


6.2 FFC Shape and Dimension Recommendation

6.2.1 Connector Type

- FFC connector: P-TWO 196395-60041 SB to CB_0.5 pitch_60Pin or compatible

6.2.2 FFC Drawing



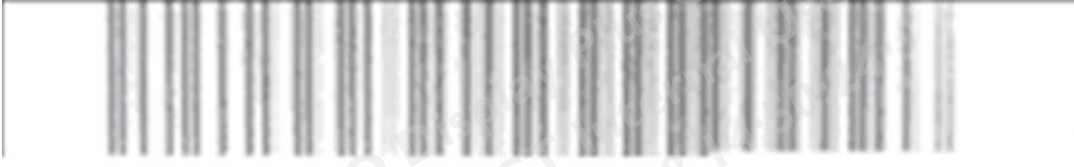
Note1: FFC drawing is provided by connector vendor.

Note2: AUO recommend FFC length ≤ 90 mm, with Aluminum foil shield to secure signal integrity.

Note3: Impedance Spec: $100 \pm 10 \Omega$

7. Packing

Open cell shipping label (35*7mm)



XXXXXXXXXXXX - XXXXXX - XXXX - XXXXXXXXXXXX

- ①
- ②
- ③
- ④

1. S/N Number
2. AUO internal use
3. Manufactured week
4. Model name


Carton Label:

AU Optronics RoHS Pb

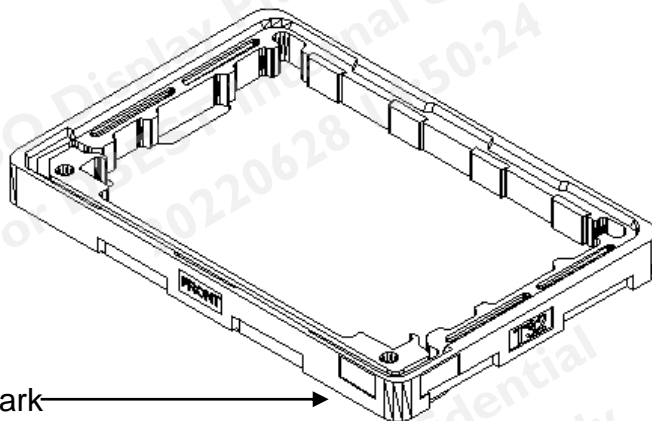
MODEL NO: P430QVN01.3

PART NO: 91.43PXX.3XX

CUSTOMER NO: XXXXX-XXXXX-XXXXX

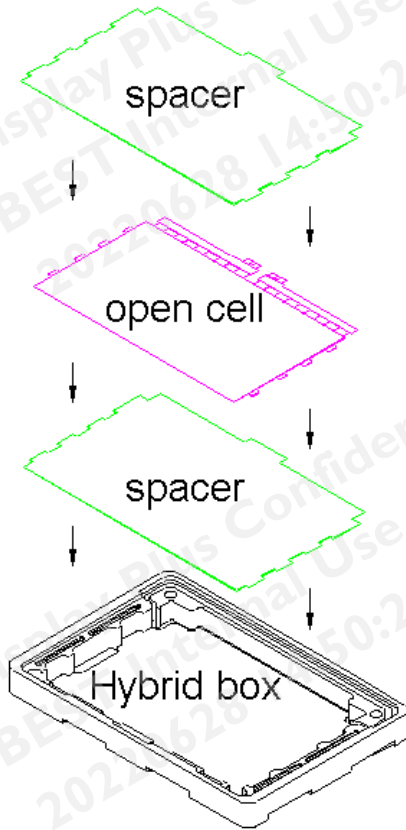
CARTON NO: 

Made in XXXXXX *XXXXXXXX-XXXXXXXXXXXX*



Carton label alignment mark →

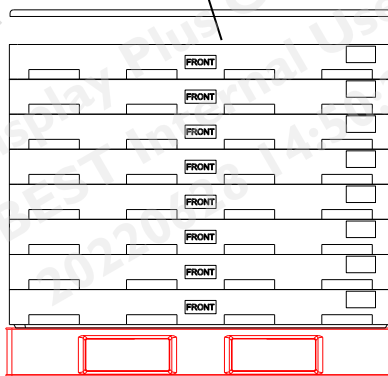
Packing Process:



Box for 13 pcs open cells & 14 pcs spacers



EPP Top Cover

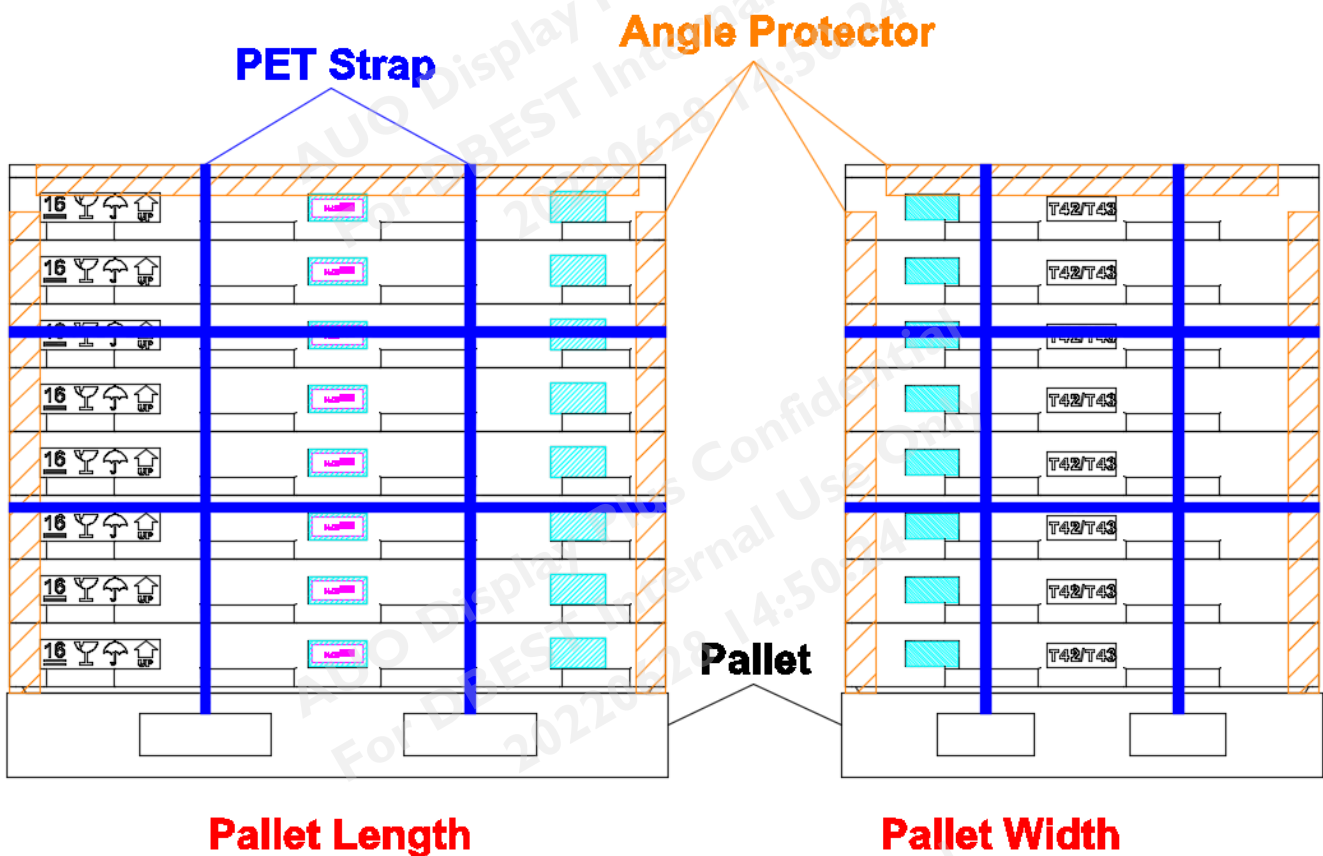


Pallet Dimension: 1100*800*132 mm

8 Boxes/Pallet, after stack 8 boxes, then put EPP top cover on it.

Pallet and Shipment Information

	Item	Specification			Packing Remark
		Qty.	Dimension	Weight (kg)	
1	Packing BOX	13pcs/box	1090(L)*786.6(W)*116(H)	24.9kg/box	PKG : 4.1kg/set O/C : 1.6kg/pcs
2	Pallet	1	1100(L)*800(W)*132(H)	13.3kg/pcs	
3	Boxes per Pallet	8 boxes/pallet			
4	Panels per Pallet	104 pcs/pallet			
5	Tray (Inner block)	≤ 10^10 [ohms/sq (25°C/50% R.H.)]			Surface Resistance
6	Sapcer	≤ 10^10 [ohms/sq (25°C/50% R.H.)]			
	Pallet after packing	104pcs/pallet	1100(L)*800(W)*1010(H)	212.5kg	



8. Precautions

Please pay attention to the followings when you use this TFT LCD Open Cell unit and strongly recommended to contact AUO if module process advice is required.

8.1 Storage

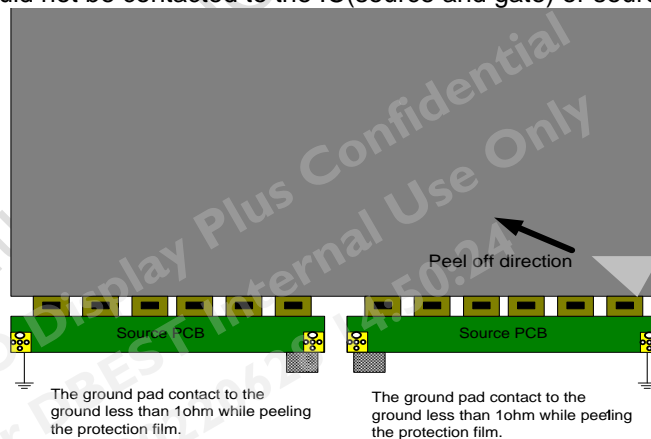
When storing open cell units, the following precautions are necessary.

- Store them in a dark place. Do not expose the open cell unit to sunlight or fluorescent light.
- Store them at the advised storage temperature between 5°C and 35°C at normal humidity(35%rH~75%rH).
- The polarizer surface should not come in contact with any other object. It is recommended that they be stored in the container in which they were shipped.
- Be careful of condensation. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.

8.2 Module Assembly

8.2.1 Protection film peeling

- The protection films of polarizer had attached on the both sides of open cell polarizer surfaces. Handlers should peel them off with care. While the protection film is being peeled off, static electricity is easily generated on the polarizer surface. Please follow the instructions listed below to reduce ESD failure risk.
- People who handle the unit should wear antistatic wristbands on hands. The band should be connected to the common ground with a current limiting resistor which is most commonly one megohm, rated at least 1/4 watt with a working voltage rating of 250 volts.
- Connect the grounded pads on source PCB to ground with less than 1 ohm resistance as below figure.
- The peeling direction is recommended in below figure.
- During peeling off process, ionized air should continuously & stably be blown on the surfaces of protection film and polarizer. The flow rate of ionized air should be monitored periodically.
- It is recommended to peel protection films off as slowly as possible. (constant speed more than 8 seconds per film.)
- The protection film should not be contacted to the IC(source and gate) or source PCB.



8.2.2 Assembly Precautions

- Remove the stains with finger-stalls wearing soft gloves in order to keep the display clean in the process of the incoming inspection and the assembly process. When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach front/ rear polarizers. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.
- Do not touch, push or rub the exposed polarizers with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of polarizer with bare hands or greasy clothes. (Some cosmetics are detrimental to the polarizer.)
- Use the tray to transport open cell can prevent open cell broken and electrical components damage.
- You should consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the cell. And the frame on which a cell is mounted should have sufficient strength so that external force is not transmitted directly to the cell

- (e) Be careful not to give any extra mechanical stress to the panel when designing the set, and BLU kit.
- (f) Do not use cover case which made of acetic acid type and chlorine type materials because acetic acid type materials generates corrosive gas which will damage the polarizer at high temperature and chlorine type materials causes circuit break by electro-chemical reaction.
- (g) When the panel kit and BLU kit are assembled, the panel kit and BLU kit should be attached to the set system firmly by combining each mounted holes. Be careful not to give the mechanical stress. Electrostatic discharge may easily damage the electronic circuits on the open cell unit. Make certain that treatment persons are grounded, (ex: anti-static wristband or etc) and don't touch interface pin directly.

8.2.3 FFC & PCB Precautions

- (a) Refrain from applying any forces to the source PCB and the drive IC in the process of the handling or installing to the set. If any forces are applied to the product, it may cause damage or a malfunction in the panel kit.
- (b) Do not pull, fold or bend the source COF and the gate COF in any processes.
- (c) This panel has its circuitry of PCB's on the rear side, so it should be handled carefully in order for a force not to be applied.
- (d) Do not touch the pins of the interface connector directly with bare hands.
- (e) The connector is a precision device to connect PCB and transmit electrical signals. Operators should plug/un-plug the connector in parallel way during module assembly.
- (f) The cables between TV SET connector and Control PCB interface should be connected directly to have a minimized length. A longer cable between TV SET connector and Control PCB interface maybe operate abnormal display.

8.2.4 Flicker adjust

In order to prevent potential problems, flicker should be adjusted by optimizing the Vcom value in customer LCM Line through the I2C Interface. Detail settings please refer to appendix section.

8.3 Aging

Be sure to age for over 1 hour at least, which the product is driving initially to stabilize TFT Characteristic.

8.4 Operating Precautions

- (a) Be cautious not to give any strong mechanical shock or any forces to the panel kit. Applying any forces to the panel may cause the abnormal operation or the damage to the panel kit and the back light unit kit.
- (b) Avoid the condensation of water which may result in the improper operation of product.
- (c) It is recommended to operate the LCD product under normal operating conditions as below
 - VDD=12V
 - Temperature=25±10°C
 - Display pattern: continually changing pattern
- (d) Response time depends on the temperature. (In lower temperature, it becomes longer)
- (e) If the product will be used under extreme conditions such as under high temperature, humidity, display patterns or the operation time etc., it is strongly recommended to contact AUO for the advice about the application of engineering. Otherwise, its reliability and the function may not be guaranteed. Extreme conditions are commonly found at airports, transit stations, banks, stock markets, and controlling systems.
- (f) Operation usage to protect against image sticking due to long-term static display.
 - A. Suitable operating time: 24 hours a day or less.
 - B. Liquid Crystal refresh time is required. Cycling display between 5 minutes' information (static) display and 10 seconds' moving image.
 - C. Periodically change background and character (image) color.
 - D. Avoid combination of background and character with large different luminance.
- (g) Periodically adopt one of the following actions after long time display.
 - A. Running the screen saver (motion picture or black pattern)
 - B. Power off the system for a while
- (h) Product reliability and functions are only guaranteed when the product is used under right operation usages. If product will be used in extreme conditions, such as high temperature/ humidity, display stationary patterns, or long operation time etc., it is strongly recommended to contact AUO for filed application engineering advice. Otherwise, its reliability and function may not be guaranteed. Extreme conditions are

commonly found at airports, transit stations, banks, stock market and controlling systems.

8.5 Others

- (a) Module designer should apply adequate thermal solutions to keep the electrical components surface temperature under control limit (ex: Source Driver IC 100°C, Components on T-con PCB 85°C) Operations over the temperature can cause damages or decrease of lifetime.
- (b) Protect the TFT LCD open cell unit out of the static electricity in all process. Otherwise the circuit IC could be damaged.

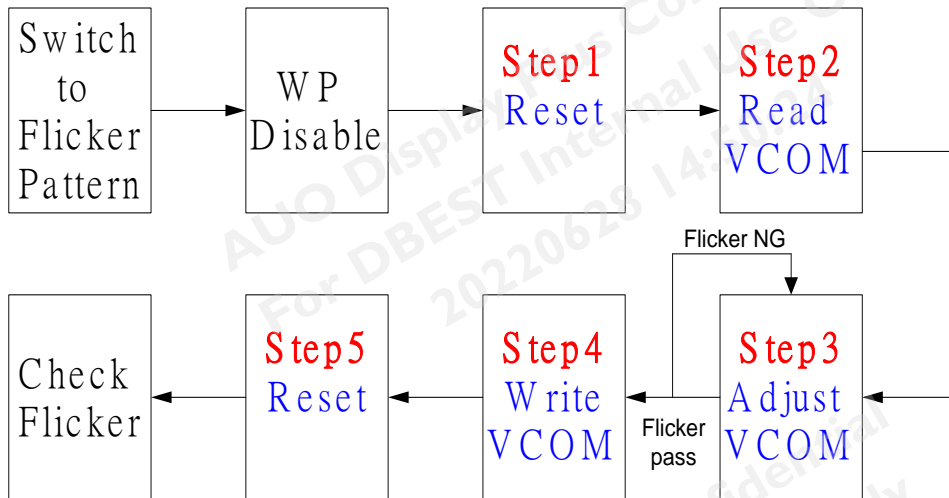
Reference: The environment ESD control standard of AUO

Item	Control standard
ESD	All environment ESD controlled under 200V
Ground resistance	All equipment ground should be less than 1ohm.

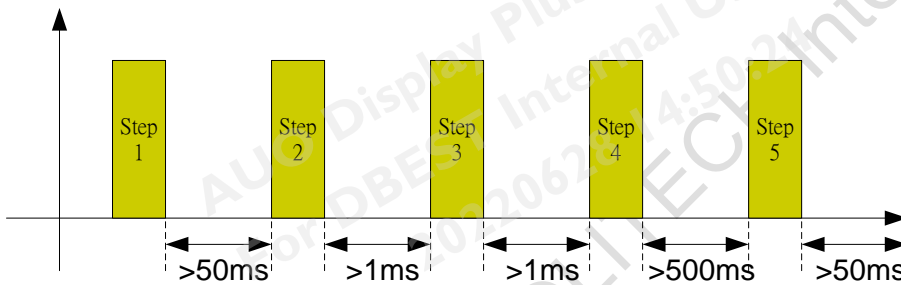
- (b) Note that polarizer could be damaged easily. Do not press or scratch the bare surface with the material which is harder than a HB pencil lead.
- (c) Wipe off water droplets or oil immediately. If you leave the droplets for a long time on the product, the stain or the discoloration may occur.
- (d) If the surface of the polarizer is dirty, clean it using the absorbent cotton or the soft cloth.
- (e) If the liquid crystal material leaks from the panel, this should be kept away from the eyes or mouth. If this contacts to hands, legs, or clothes, you must washed it away with soap thoroughly and see a doctor for the medical examination.
- (f) The module has high frequency circuits. The sufficient suppression to the electromagnetic interference should be done by the system manufacturers. The grounding and shielding methods is important to minimize the interference. The sufficient suppression to the EMI should be done by the set manufacturers.

Appendix I – Vcom adjustment

VCOM I2C Tuning Steps



Step to step interval must follow below figure



Flicker Pattern



WP function

	Writable	Protection	Default (NC)
WP	H	L	L

Adjust SOP

Step1 Reset

* Device Address is 0x74 (7Bits)

S	Slave Address	W	A	Index Address 0	A	Control Byte	A	P
	1 1 1 0 1 0 0 0	0		0 0 0 0 0 0 0 0		0 0 0 1 0 0 1 0		
	0xE8			0x00		0x12		
	Device Address + W			Control Address		Reset + OUT_EN		

Step2 Read VCOM

* Data = 7Bits

S	Slave Address	W	A	Index Address 1	A	S	Slave Address	R	A	DATA	NA	P
	1 1 1 0 1 0 0 0	0		0 0 0 0 0 0 0 1			1 1 1 0 1 0 0 1			X X X X X X X X	X	
	0xE8			0x01			0xE9					
	Device Address + W			VCOM Address			Device Address + R			Data		

Step3 Adjust VCOM

* DVCOM = 8Bits

S	Slave Address	W	A	Index Address 1	A	DVCOM	A	P
	1 1 1 0 1 0 0 0	0		0 0 0 0 0 0 0 1		0000000X~1111111X		
	0xE8			0x01		0x00~0xFF		
	Device Address + W			VCOM Address		VCOM value		

Step4 Write VCOM

S	Slave Address	W	A	Index Address 0	A	Control Byte	A	P
	1 1 1 0 1 0 0 0	0		0 0 0 0 0 0 0 0		0 0 0 0 1 0 1 0		
	0xE8			0x00		0x0A		
	Device Address + W			Control Address		Write DAC to NVM+ OUT_EN		

Step5 Reset

* Device Address is 0x74 (7Bits)

S	Slave Address	W	A	Index Address 0	A	Control Byte	A	P
	1 1 1 0 1 0 0 0	0		0 0 0 0 0 0 0 0		0 0 0 1 0 0 1 0		
	0xE8			0x00		0x12		
	Device Address + W			Control Address		Reset + OUT_EN		