(V) Preliminary Specifications
( ) Final Specifications

Module	5” Inch Color TFT-LCD
Model Name	G050TAN01.0

Customer	**Date**	**Approved by**	**Date**
Checked & Approved by		**Prepared by**	
		Ken Wang	2017/04/17
		General Display Business Unit / AU Optronics corporation	

Contents

Record of Revision

Version and Date	Page	Old description	New Description
0.0 Apr 17, 2017	All	First draft specification	-

1. Operating Precautions

1) Since front polarizer is easily damaged, please be cautious and not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or soft cloth.
5) Since the panel is made of glass, it may be broken or cracked if dropped or bumped on hard surface.
6) To avoid ESD (Electro Static Discharde) damage, be sure to ground yourself before handling TFT-LCD Module.
7) Do not open nor modify the module assembly.
8) Do not press the reflector sheet at the back of the module to any direction.
9) In case if a module has to be put back into the packing container slot after it was taken out from the container, do not press the center of the LED light bar edge. Instead, press at the far ends of the LED light bar edge softly. Otherwise the TFT Module may be damaged.
10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) TFT-LCD Module is not allowed to be twisted & bent even force is added on module in a very short time. Please design your display product well to avoid external force applying to module by end-user directly.
12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
13) Severe temperature condition may result in different luminance, response time and lamp ignition voltage.
14) Continuous operating TFT-LCD display under low temperature environment may accelerate lamp exhaustion and reduce luminance dramatically.
15) The data on this specification sheet is applicable when LCD module is placed in landscape position.
16) Continuous displaying fixed pattern may induce image sticking. It's recommended to use screen saver or shuffle content periodically if fixed pattern is displayed on the screen.

2. General Description

This specification applies to the Color Active Matrix Liquid Crystal Display G050TAN01.0 composed of a TFT-LCD display, a driver and power supply circuit, and a LED backlight system. The screen format is intended to support HD (720(H) x 1280(V)) screen and 16.7M (8-bits). And LED driving board for backlight unit is included in G050TAN01.0.

All input signals are LVDS interface.

G050TAN01.0 designed with wide viewing angle; wide temperature and long life LED backlight is well suited for industial applications.

G050TAN01.0 is a RoHS product.

2.1 Display Characteristics

The following items are characteristics summary on the table under 25 °C condition:

Items	Unit	Specifications
Screen Diagonal	[inch]	4.99
Active Area	[mm]	62.1 x 110.4
Pixels H x V		720 (RGB) x 1280
Pixel Pitch	[mm]	0.086 X 0.086
Pixel Arrangement		R.G.B. Vertical Stripe
Display Mode		Normally Black
Nominal Input Voltage VDD	[Volt]	VDDI=1.8V, VCI=2.8V
Typical Power Consumption	[Watt]	TBD
Weight	[Grams]	65
Physical Size	[mm]	66.7(H) ×120.3(V)
Electrical Interface		MIPI
Surface Treatment		AG, (3H)
Support Color		16.7M colors
Temperature Range Operating Storage (Non-Operating)	 [°C] [°C]	 -20 to +70 -30 to +80
RoHS Compliance		RoHS Compliance

2.2 Display Optical Characteristics

The optical characteristics are measured under stable conditions at 25°C (Room Temperature):

Item	Unit	Conditions	Min.	Typ.	Max.	Note
White Luminance	[cd/m2]	I_{LED}= 25.4 mA (center point)		600		1
Uniformity	%	5 points	75			2,3
Contrast Ratio				1000		4
Response Time	[msec]	Rising				5
	[msec]	Falling				
	[msec]	Rising + Falling		35		
Viewing Angle	[degree] [degree]	Horizontal (Right) CR = 10 (Left)		80 80		6
	[degree] [degree]	Vertical (Upper) CR = 10 (Lower)		80 80		
Color / Chromaticity Coordinates (CIE 1931)		Red x				
		Red y				
		Green x				
		Green y				
		Blue x				
		Blue y				
		White x	0.263	0.313	0.363	
		White y	0.279	0.329	0.379	
Color Gamut	%			70		

Note 1: Measurement method

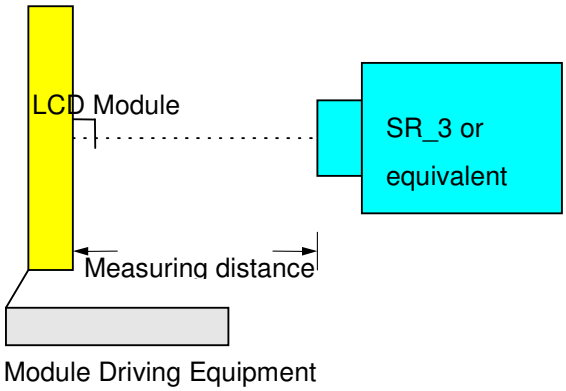
1.1. Before lamination touch

1.2. Equipment Pattern Generator, Power Supply, Digital Voltmeter, Luminance meter (SR_3 or equivalent)

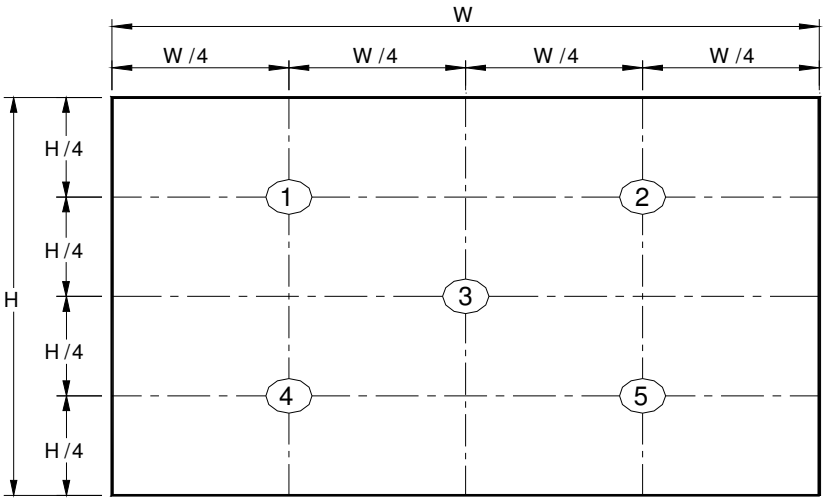
Aperture 1° with 50cm viewing distance

Test Point Center

Environment *< 1 lux*



Note 2: Definition of 5 points position (Display active area: 62.1 x 110.4)



Note 3: The luminance uniformity of 5 points is defined by dividing the minimum luminance values by the maximum test point luminance

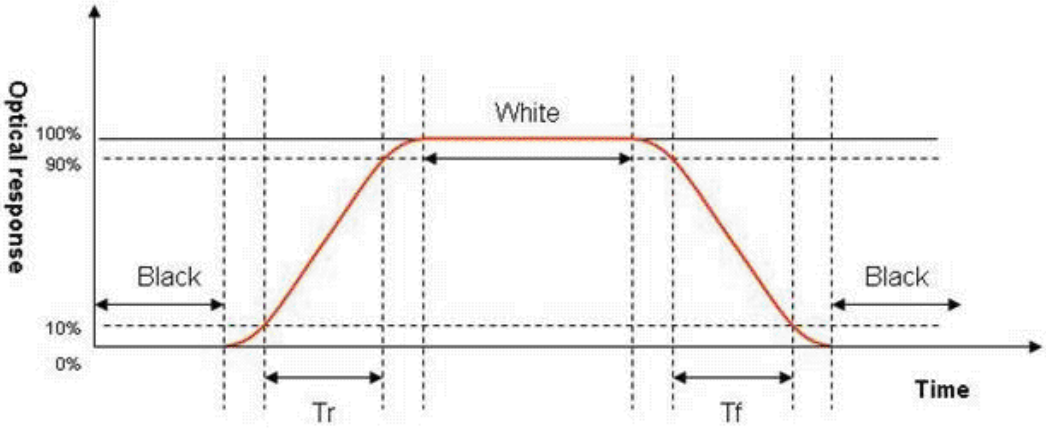
$$\delta_{W5} = \frac{\text{Minimum Brightness of five points}}{\text{Maximum Brightness of five points}}$$

Note 4: Definition of contrast ratio (CR):

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

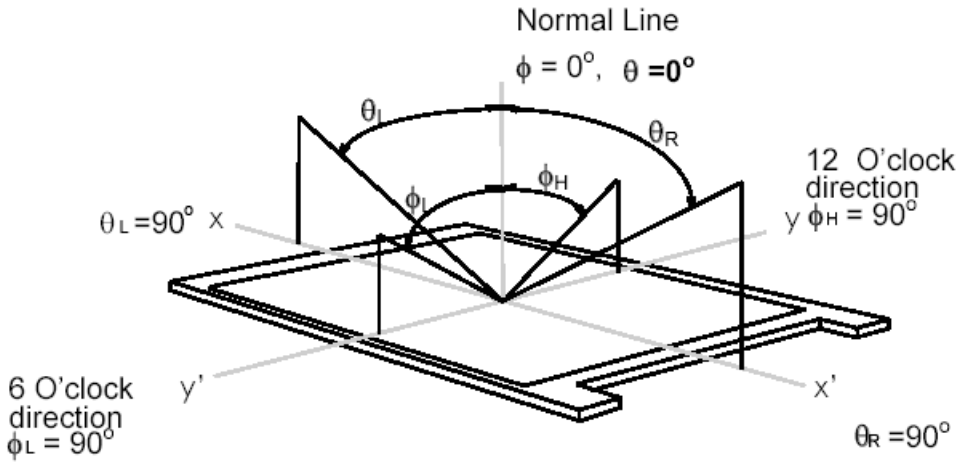
Note 5: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “White” to “Black” (falling time) and from “Black” to “White” (rising time), respectively. The response time interval is between 10% and 90% of amplitudes. Please refer to the figure as below.



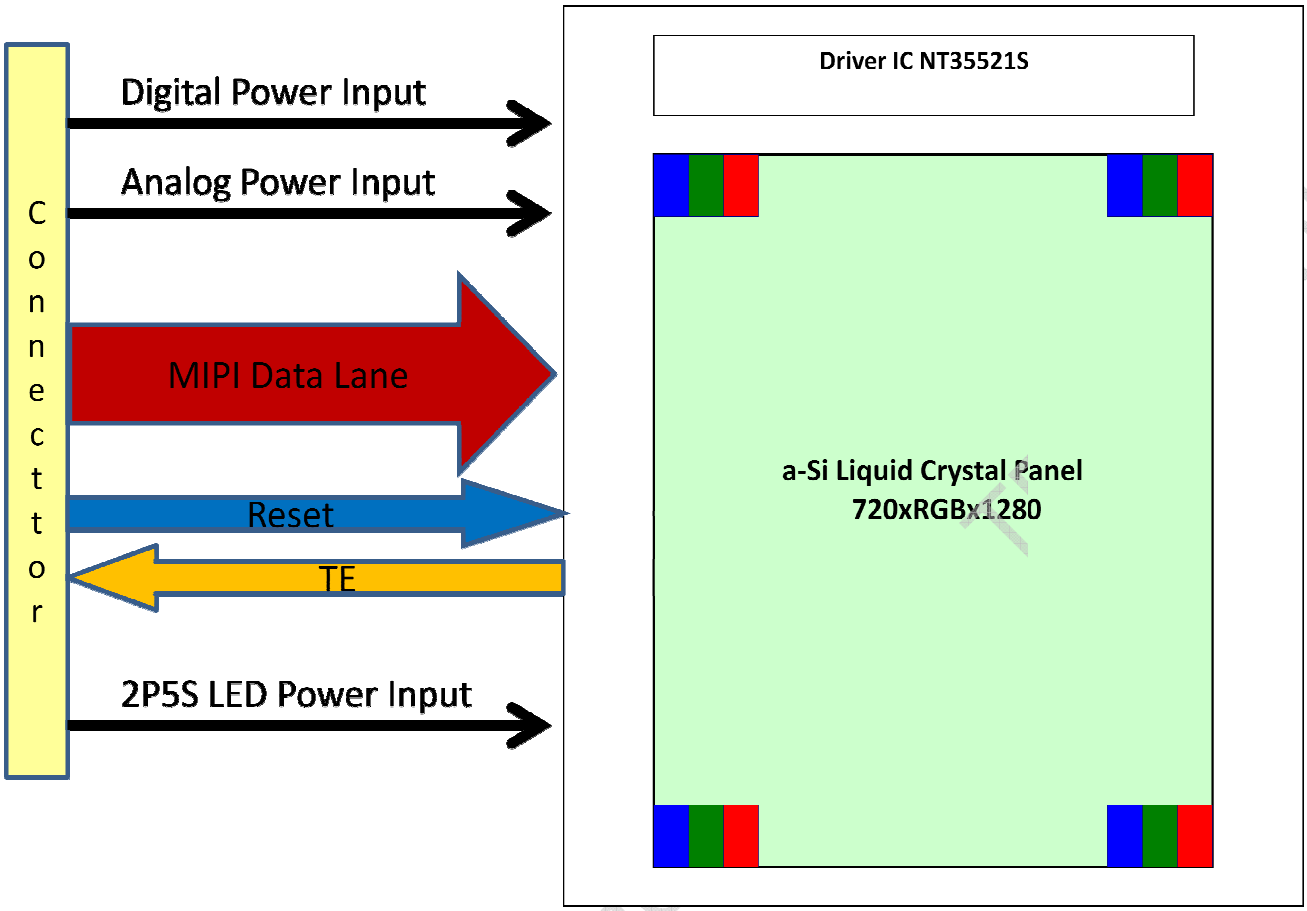
Note 6: Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as below: 90° (θ) horizontal left and right, and 90° (Φ) vertical high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated to its center to develop the desired measurement viewing angle.



3. Functional Block Diagram

The following diagram shows the functional block of the 5 inch color TFT/LCD module:



4. Absolute Maximum Ratings

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit
Logic Supply Voltage	VDDI	-0.3	5.5	[Volt]
Analog Supply Voltage	VCI	-0.3	5.5	[Volt]

Note: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

4.2 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit
Operating Temperature	TOP	-20	70	[°C]
Storage Temperature	TST	-30	80	[°C]

Note: Maximum Wet-Bulb should be 39 °C and no condensation.

5. Electrical Characteristics

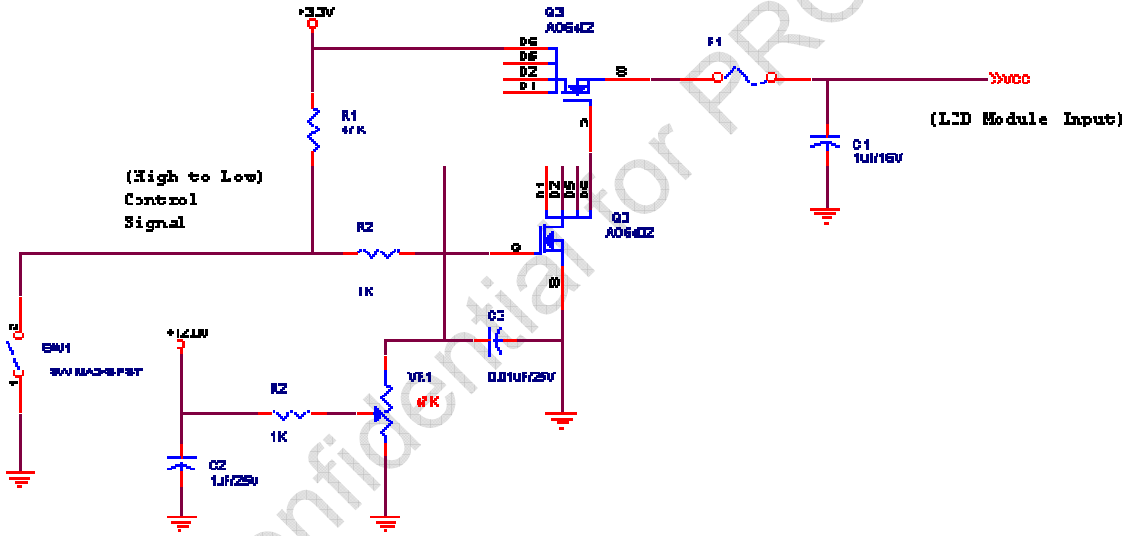
5.1 TFT LCD Module

5.1.1 Power Specification

Input power specifications are shown as follows;

Symbol	Parameter	Min	Typ	Max	Units	Remark
VDDI	Logic Operating Voltage	1.65	1.8	3.6	[Volt]	
VCI	Analog Operating Voltage	2.5	2.8	3.6	[mA]	Black Pattern (VDDI=1.8V, at 60Hz)
IVDDII	VDDI Current	-	-		[A]	Note 1
IVCII	VCI Current	-	-		[A]	Note 1
P_{VCC}	VCC Power	-			[Watt]	Black Pattern (VDDI=1.8V, VCI=2.8V, at 60Hz)
VCCrp	Allowable Logic/LCD Drive Ripple Voltage			100	[mV] p-p	

Note 1: Measurement condition:



5.1.2 Signal Electrical Characteristics

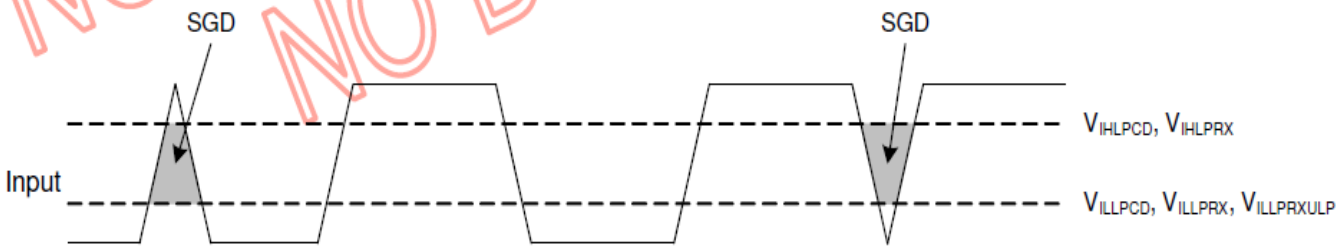
- DC characteristics for DSI LP Mode

Parameter	Symbol	Conditions	Specification			UNIT
			MIN	TYP	MAX	
Logic high level input voltage	V_{IHLPCD}	LP-CD	450	-	1350	mV
Logic low level input voltage	V_{ILLPCD}	LP-CD	0	-	200	mV
Logic high level input voltage	V_{IHLPRX}	LP-RX (CLK, D0)	880	-	1350	mV
Logic low level input voltage	V_{ILLPRX}	LP-RX (CLK, D0)	0	-	550	mV
Logic low level input voltage	$V_{ILLPRXULP}$	LP-RX (CLK ULP mode)	0	-	300	mV
Logic high level output voltage	V_{OHLPTX}	LP-TX (D0)	1.1	-	1.3	V
Logic low level output voltage	V_{OLLPTX}	LP-TX (D0)	-50	-	50	mV
Logic high level input current	I_{IH}	LP-RX, Vin=0~1.3V	-	-	10	μA
Logic low level input current	I_{IL}	LP-RX, Vin=0~1.3V	-10	-	-	μA
Input pulse rejection	SGD	DSI-CLK+/-, DSI-Dn+/- (Note 3)	-	-	300	Vps

Note 1) VDDI=1.65~3.6V, VCI=2.5 to 3.6V, VSSI=VSS=VSSAM=0V, Ta=-30 to 70 ºC (to +85 ºC no damage). VCI means VDDR, VDDB and VSS means VSSAM, VSSR, VSSB, AVSS.

Note 2) DSI high speed is off.

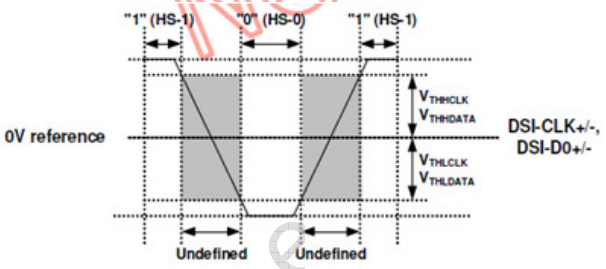
Note 3) Peak interference amplitude max. 200mV and interference frequency min. 450MHz.

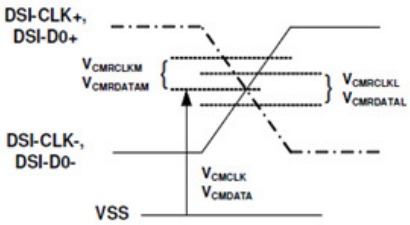


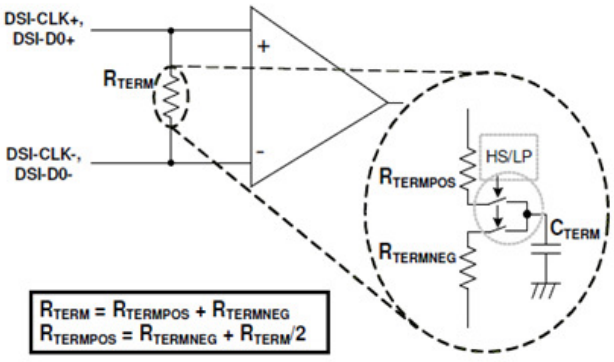
- DC characteristics for DSI HS Mode

Parameter	Symbol	Conditions	Specification			UNIT
			MIN	TYP	MAX	
Input voltage common mode range	V_{CMCLK} V_{CMDATA}	DSI-CLK+/-, DSI-Dn+/- (Note2, 3)	70	-	330	mV
Input voltage common mode variation (≤ 450MHz)	$V_{CMRCLKL}$ $V_{CMRDATAL}$	DSI-CLK+/-, DSI-Dn+/- (Note 4)	-50	-	50	mV
Input voltage common mode variation (≥ 450MHz)	$V_{CMRCLKM}$ $V_{CMRDATAM}$	DSI-CLK+/-, DSI-Dn+/-	-	-	100	mV
Low-level differential input voltage threshold	V_{THLCLK} $V_{THLDATA}$	DSI-CLK+/-, DSI-Dn+/-	-70	-	-	mV
High-level differential input voltage threshold	V_{THHCLK} $V_{THHDATA}$	DSI-CLK+/-, DSI-Dn+/-	-	-	70	mV
Single-ended input low voltage	V_{ILHS}	DSI-CLK+/-, DSI-Dn+/- (Note 3)	-40	-	-	mV
Single-ended input high voltage	V_{IHHS}	DSI-CLK+/-, DSI-Dn+/- (Note 3)	-	-	460	mV
Differential input termination resistor	R_{TERM}	DSI-CLK+/-, DSI-Dn+/-	80	100	125	Ω
Single-ended threshold voltage for termination enable	$V_{TERM-EN}$	DSI-CLK+/-, DSI-Dn+/-	-	-	450	mV
Termination capacitor	C_{TERM}	DSI-CLK+/-, DSI-Dn+/-	-	-	14	pF

Note 1) VDDI=1.65~3.6V, VCI=2.5 to 3.6V, VSSI=VSS=VSSAM=0V, Ta=-30 to 70 ºC (to +85 ºC no damage). VCI means VDDR, VDDB and VSS means VSSAM, VSSR, VSSB, AVSS.
Note 2) Includes 50mV (-50mV to 50mV) ground difference.
Note 3) Without $V_{CMRCLKM}$ / $V_{CMRDATAM}$.
Note 4) Without 50mV (-50mV to 50mV) ground difference.
Note 5) Dn=D0, D1, D2 and D3.







5.2 Backlight Unit

5.2.1 Parameter guideline for LED

Following characteristics are measured under a stable condition using an inverter at 25℃ (Room Temperature):

Symbol	Parameter	Min.	Typ.	Max.	Unit	Remark
IFB	LED Forward Current	-	50.8	-	mA	Ta = 25℃ With 2 parallel
VLED	LED Forward Voltage	-	28.5	31.0	[Volt]	IF = 25.4mA, Ta = 25°C Total 2 parallel
PLED	LED Power Consumption	-	1.45	-	Watt	IF = 25.4mA, Ta = 25°C Total 2 parallel
LED life time			10,000	-	Hrs	I_F = 50.8 mA, Ta = 25°C

Note 1: Ta means ambient temperature of TFT-LCD module.

Note 2: IFB, VLED , PLED are defined for LED Light Bar. There is two LED channel (AN1-CA1, AN2-CA2) in back light unit.

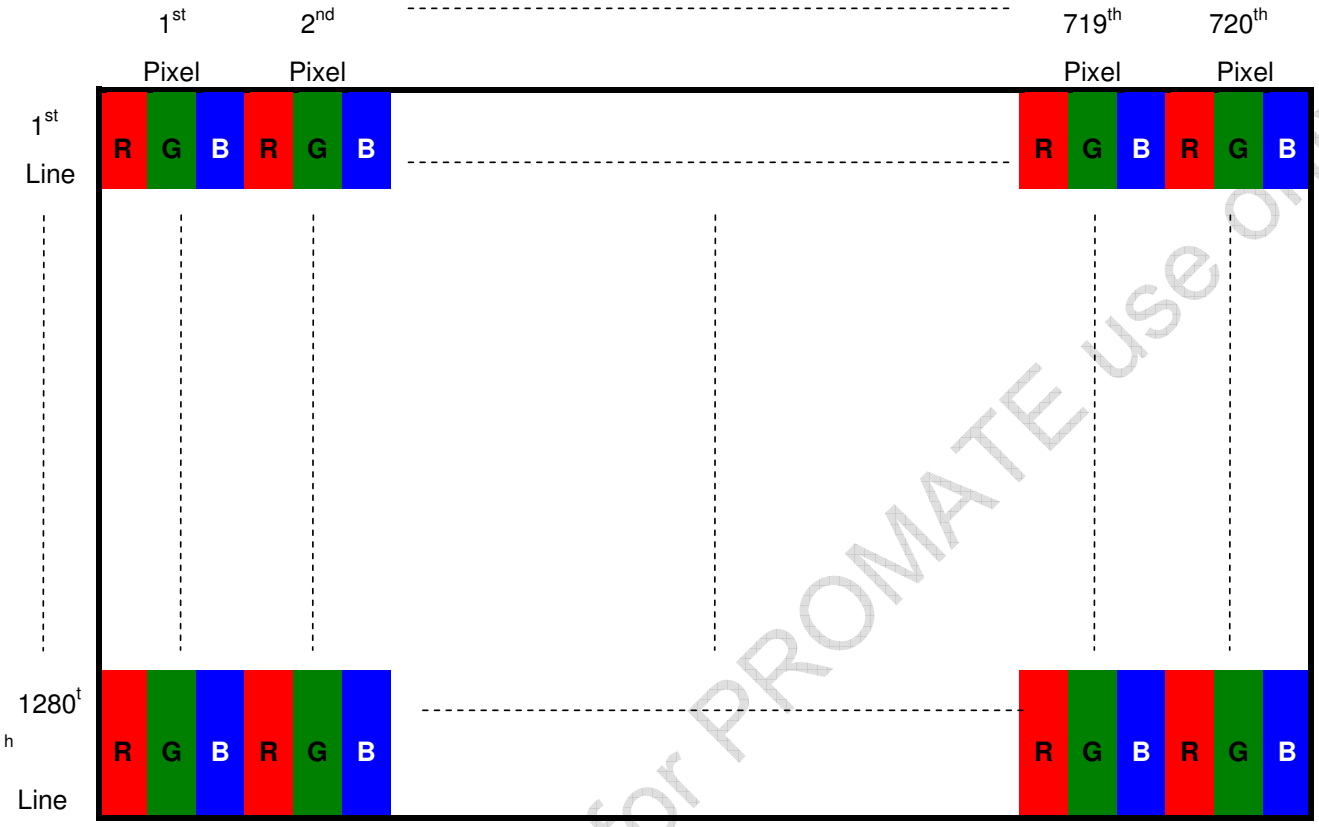
Note 3: If G050TAN01.0 module is driven by high current or at high ambient temperature & humidity condition. The operating life will be reduced.

Note 4: Operating life means brightness goes down to 50% initial brightness. Typical operating life time is estimated data.

6. Signal Characteristic

6.1 Pixel Format Image

Following figure shows the relationship between input signal and LCD pixel format.



6.2 Signal Description

6.2.1 TFT LCD Module Connector

Connector Name / Designation	Signal Connector
Manufacturer	Molex
Connector Model Number	5565-3078

6.2.2 LCD MIPI Interface pin description

Pin no	Symbol	Description	Remark
1	D0-	DSI_D0- differential data signal	
2	GND	Ground	
3	D0+	DSI_D0+ differential data signal	
4	NC		
5	GND	Ground	
6	TE	Frame head pulse signal	
7	D1-	DSI_D1- differential data signal	
8	RESET		
9	D1+	DSI_D1+ differential data signal	
10	NC		
11	GND	Ground	
12	VDDI	I/O supply voltage range 1.65V~3.6V	
13	CLK-	DSI_CLK- differential data signal	
14	GND	Ground	
15	CLK+	DSI_CLK+ differential data signal	
16	VCI	Analog supply voltage range 2.5V~3.6V	
17	GND	Ground	
18	GND	Ground	
19	D2-	DSI_D2- differential data signal	
20	LED_A1	LED+	
21	D2+	DSI_D2+ differential data signal	
22	LED_A2	LED+	
23	GND	Ground	
24	LED_C1	LED-	
25	D3-	DSI_D3- differential data signal	
26	LED_C2	LED-	
27	D3+	DSI_D3+ differential data signal	
28	GND	Ground	
29	GND	Ground	
30	GND	Ground	

6.3 Interface Timing

- **High Speed Mode**

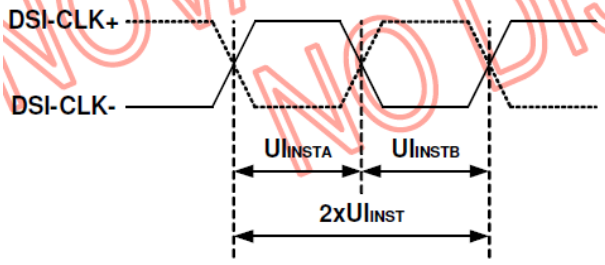
(VSS=VSSI=DVSS=0V, VDDI=1.65V to 3.6V, VCI=2.5V to 3.6V,Ta = -30 to 70°C)

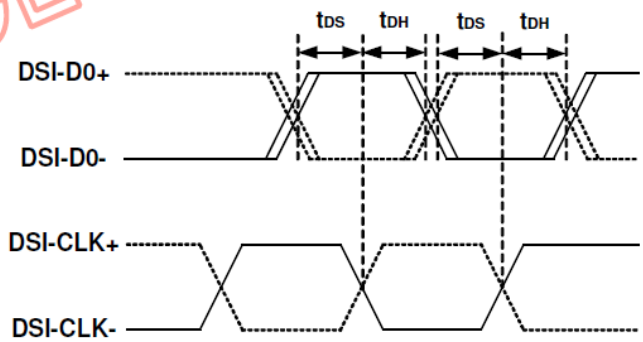
Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
DSI-CLK+/-	$2xUI_{INST}$	Double UI instantaneous	3.2	-	8	ns	4 Lane (Note 2)
			2.5	-	8	ns	3 Lane (Note 2)
			2.352	-	8	ns	2 Lane (Note 3)
DSI-CLK+/-	UI_{INSTA} UI_{INSTB}	UI instantaneous halfs ($UI = UI_{INSTA} = UI_{INSTB}$)	1.6	-	4	ns	4 Lane (Note 2)
			1.25	-	4	ns	3 Lane (Note 2)
			1.176	-	4	ns	2 Lane (Note 3)
DSI-Dn+/-	t_{DS}	Data to clock setup time	0.15xUI	-	-	ps	
DSI-Dn+/-	t_{DH}	Data to clock hold time	0.15xUI	-		ps	
DSI-CLK+/-	t_{DRTCLK}	Differential rise time for clock	150	-	0.3xUI	ps	
DSI-Dn+/-	$t_{DRTDATA}$	Differential rise time for data	150	-	0.3xUI	ps	
DSI-CLK+/-	t_{DFTCLK}	Differential fall time for clock	150	-	0.3xUI	ps	
DSI-Dn+/-	$t_{DFTDATA}$	Differential fall time for data	150	-	0.3xUI	ps	

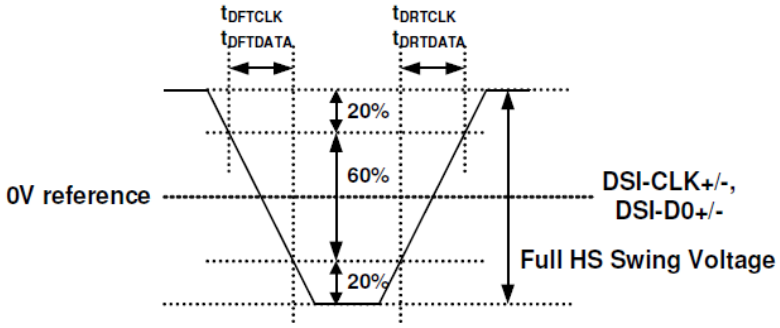
Note 1) Dn = D0, D1, D2 and D3.

Note 2) Maximum total bit rate is 2.4Gbps for 24-bit data format, 1.8Gbps for 18-bit data format and 1.6Gbps for 16-bit data format in 3 lanes or 4 lanes application which support to 800RGBx 1280 resolution.

Note 3) Maximum total bit rate is 1.7Gbps for 24-bit data format, 1.275Gbps for 18-bit data format and 1.13Gbps for 16-bit data format in 2 lanes application which support to 720RGBx1280 resolution.



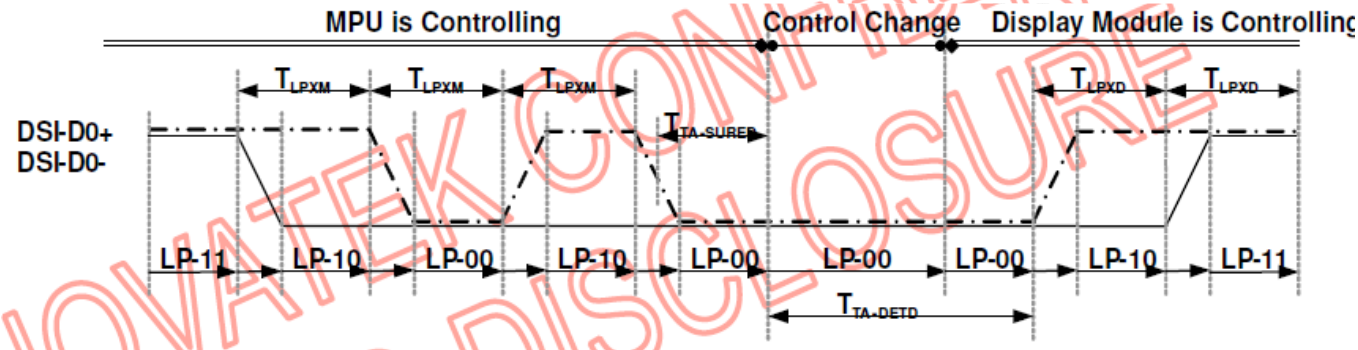


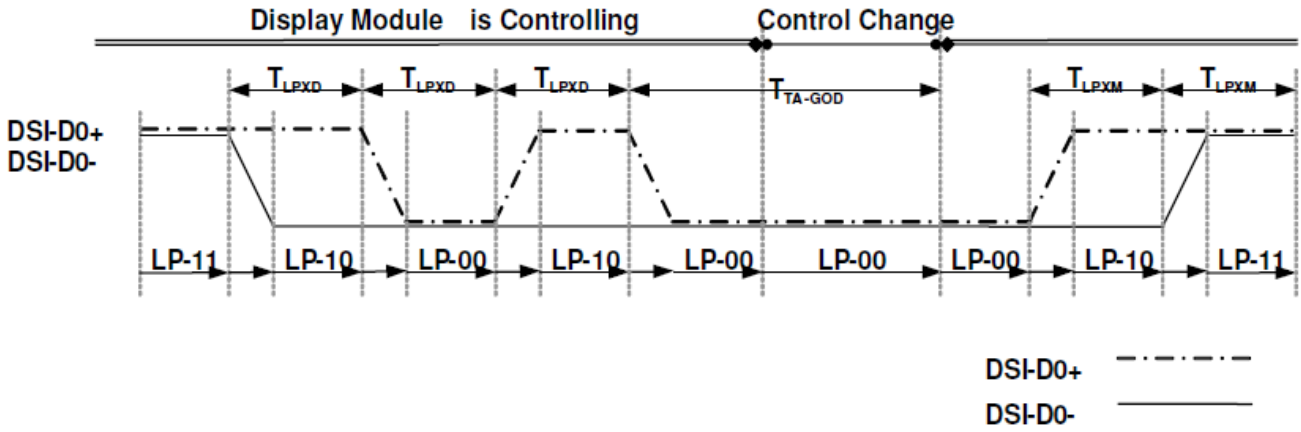


Low Power Mode

(VSS=VSSI=DVSS=0V, VDDI=1.65V to 3.6V, VCI=2.5V to 3.6V,Ta = -30 to 70°C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
DSI-D0+/-	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU → Display Module	50	-	75	ns	Input
DSI-D0+/-	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module → MPU	50	-	75	ns	Output
DSI-D0+/-	$T_{TA-SURED}$	Time-out before the MPU start driving	T_{LPXD}	-	$2xT_{LPXD}$	ns	Output
DSI-D0+/-	$T_{TA-GETD}$	Time to drive LP-00 by display module	$5xT_{LPXD}$	-	-	ns	Input
DSI-D0+/-	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MPU	$4xT_{LPXD}$	-	-	ns	Output





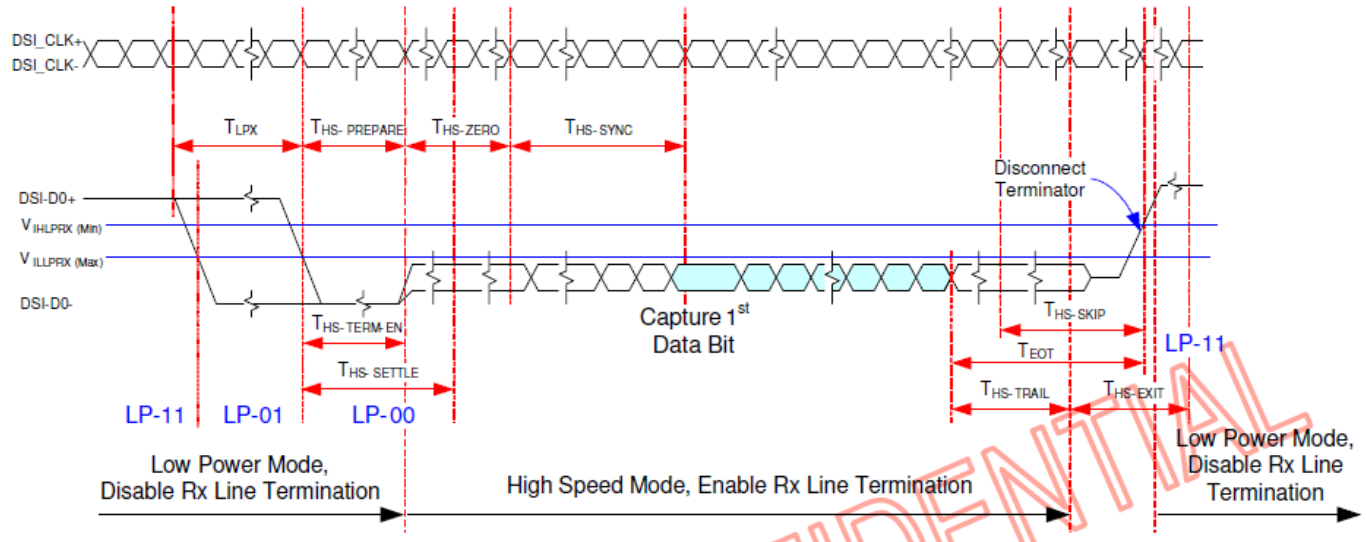
● DSI Bursts

(VSS=VSSI=DVSS=0V, VDDI=1.65V to 3.6V, VCI=2.5V to 3.6V,Ta = -30 to 70 C)

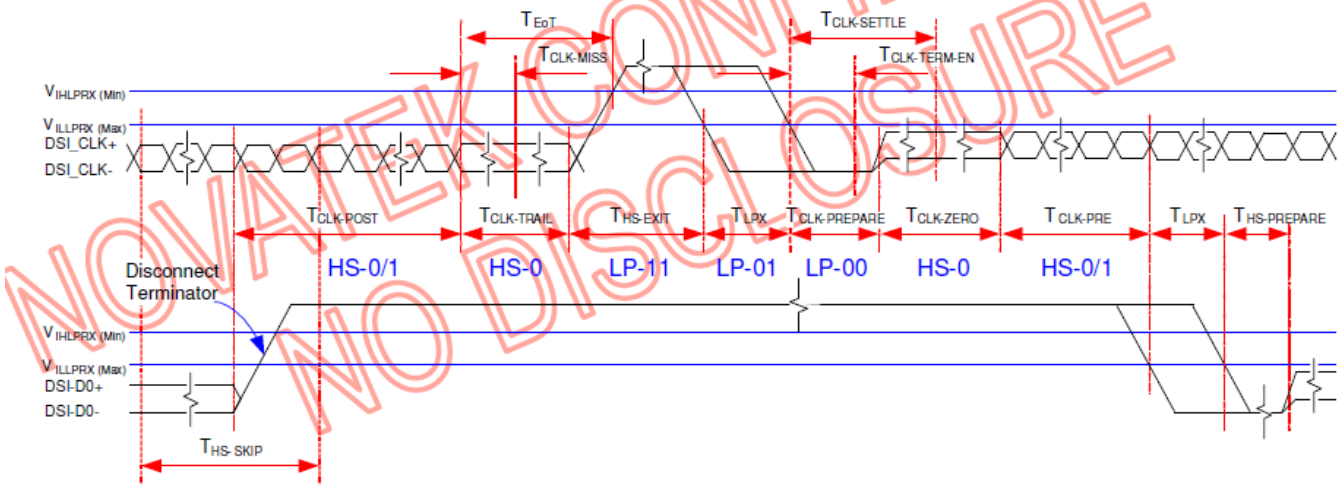
Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
Low Power Mode to High Speed Mode Timing							
DSI-Dn+/-	T_{LPX}	Length of any low power state period	50	-	-	ns	Input
DSI-Dn+/-	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	40+4xUI	-	85+6xUI	ns	Input
DSI-Dn+/-	$T_{HS-TERM-EN}$	Time to enable data receiver line termination measured from when Dn crosses V_{ILMAX}	-	-	35+4xUI	ns	Input
High Speed Mode to Low Power Mode Timing							
DSI-Dn+/-	$T_{HS-SKIP}$	Time-out at display module to ignore transition period of EoT	40	-	55+4xUI	ns	Input
DSI-Dn+/-	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	-	ns	Input
DSI-Dn+/-	$T_{HS-TRAIL}$	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60+4xUI	-	-	ns	Input
High Speed Mode to/from Low Power Mode Timing							
DSI-CLK+/-	$T_{CLK-POS}$	Time that the MPU shall continue sending HS clock after the last associated data lane has transition to LP mode	60+52xUI	-	-	ns	Input
DSI-CLK+/-	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	-	ns	Input
DSI-CLK+/-	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	-	ns	Input
DSI-CLK+/-	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	-	95	ns	Input
DSI-CLK+/-	$T_{CLK-TERM-EN}$	Time-out at clock lane display module to enable HS transmission	-	-	38	ns	Input
DSI-CLK+/-	$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	Minimum lead HS-0 drive period before starting clock	300	-	-	ns	Input
DSI-CLK+/-	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8xUI	-	-	ns	Input

Note 1) Dn = D0, D1, D2 and D3.

Note 2) Two HS transmission can be sent with a break as short as $T_{HS-EXIT}$ from each other in continuous clock mode. In discontinuous mode, the break is longer which account $T_{CLK-POS}$, $T_{CLK-TRAIL}$ and $T_{HS-EXIT}$, before activity in clock and data lanes again.

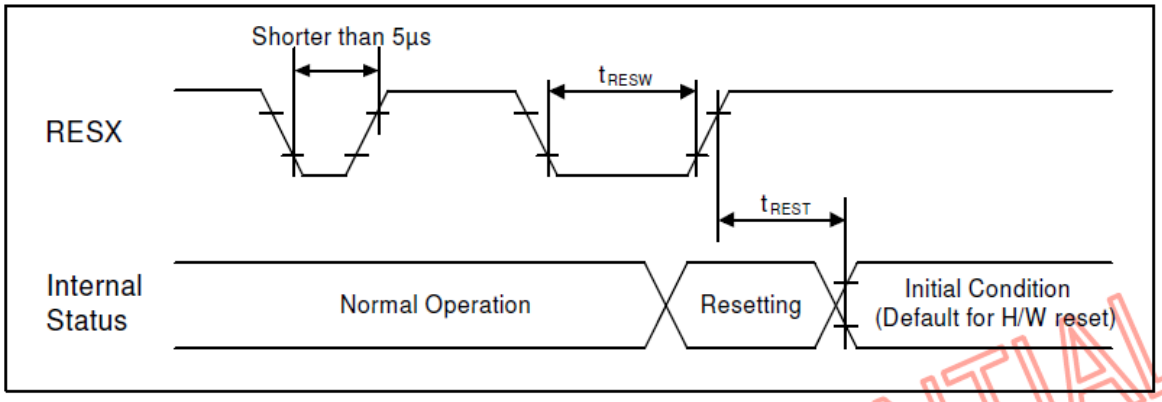


Data lanes-Low Power Mode to/from High Speed Mode Timing



Clock lanes- High Speed Mode to/from Low Power Mode Timing

- **Reset input timing**



(VSS=VSSI=DVSS=0V, VDDI=1.65V to 3.6V, VCI=2.5V to 3.6V,Ta = -30 to 70 C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
RESX	tRESW	Reset "L" pulse width (Note 1)	10	-	-	µs	
	tREST	Reset complete time (Note 2)	-	-	5	ms	When reset applied during Sleep In Mode
			-	-	120	ms	When reset applied during Sleep Out Mode and Note 5

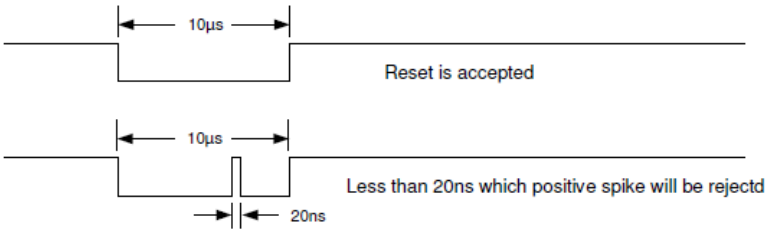
Note 1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	*Action*
Shorter than 5µs	*Reset Rejected*
Longer than 10µs	*Reset*
Between 5µs and 10µs	*Reset Start*

Note 2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In–mode) and then return to Default condition for H/W reset.

Note 3) During Reset Complete Time, values in OTP memory will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (t_{REST}) within 5ms after a rising edge of RESX.

Note 4) Spike Rejection also applies during a valid reset pulse as shown below:



Note 5) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec

6.4 Power ON/OFF Sequence

VDDI must be applied in advance of VCI (VDDR/VDDB) or at the same time.
VCI (VDDR/VDDB) must be powered down in advance of VDDI or at the same time.
During power off, if LCD is in the Sleep Out mode, VCI (VDDR/VDDB) and VDDI must be powered down minimum 120msec after RESX has been released.
During power off, if LCD is in the Sleep In mode, VDDI or VCI (VDDR/VDDB) can be powered down minimum 0msec after RESX has been released.
Notes:

1. *There will be no damage to the display module if the power sequences are not met.*
2. *There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.*
3. *There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.*
4. *If RESX line is not held stable by host during Power On Sequence as defined in Sections 5.6.1 and 5.6.2, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.*
5. *There is not a limit for Rise/Fall time on VDDI and VCI (VDDR/VDDB).*
6. *The display module can also initialize and calibrate DSI-CLK+/- and DSI-D0+/- lanes within 5ms after LP-11 (Clock and Data Channels), VDDI and VCI (VDDR/VDDB) are applied and H/W Reset is not active (5ms is as same as the Reset Cancelling Time).*

6.4.1 Power ON Sequence

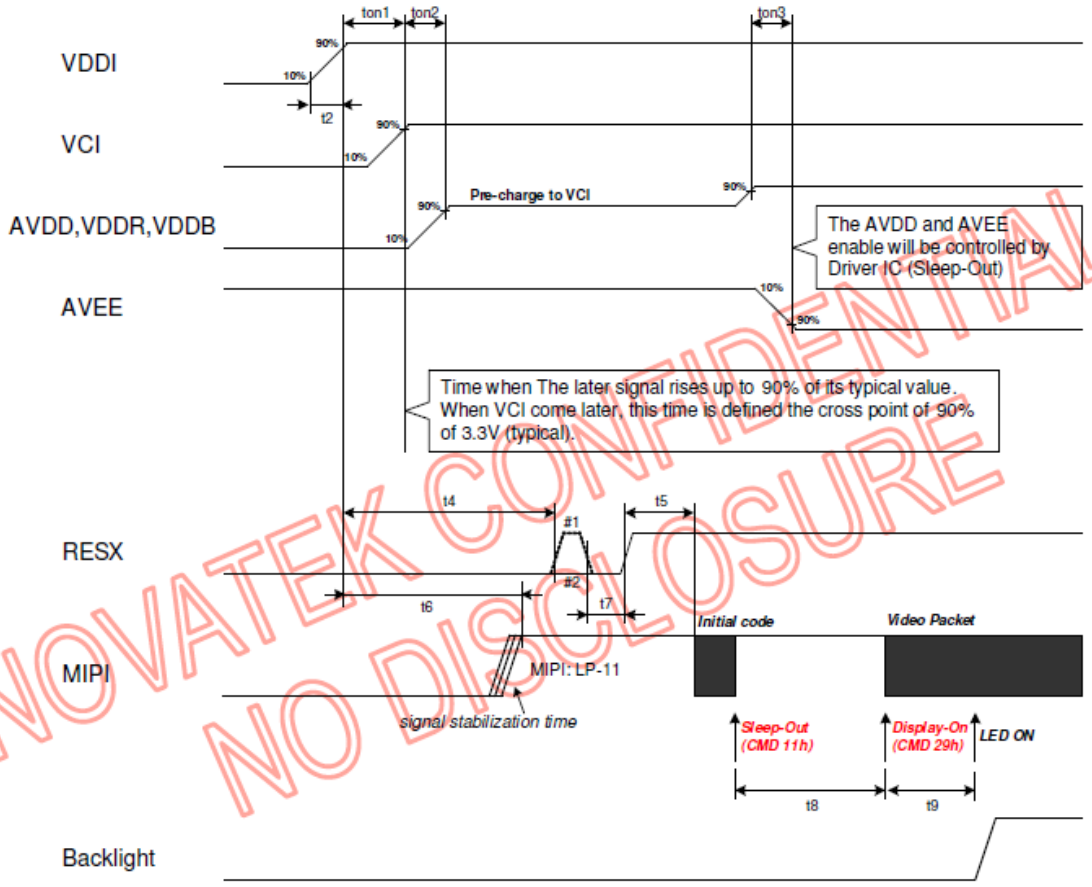
If RESX line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VCI and VDDI have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.

If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10µsec after both VCI and VDDI have been applied.

The power on sequence for different power input modes are shown below figures.

Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
ton1	0	-	-	ms	
ton2	0	-	-	ms	
ton3	0	-	-	ms	
ton4	0	-	-	ms	
t2	-	No limit	-	µs	
t4	10	-	-	ms	
t5	20	-	-	ms	
t6	0	-	T4	ms	
t7	10	-	-	µs	
t8	120	-	-	ms	
t9	0	No limit	-	ms	

- 3 Input power (BTM[2:0]="100" or "101") with NT50198 on FPC of LCM:
  VDDI=1.65~3.6V, VCI=2.5~3.6V (to NT50198), AVDD=VDDR=VDDB=4.5~6.0V, AVEE=-4.5~-6.0V



Note 1: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

Note 2: This power-on sequence is based on adding schottky diode on VGLX pin to ground. (use NT50198)

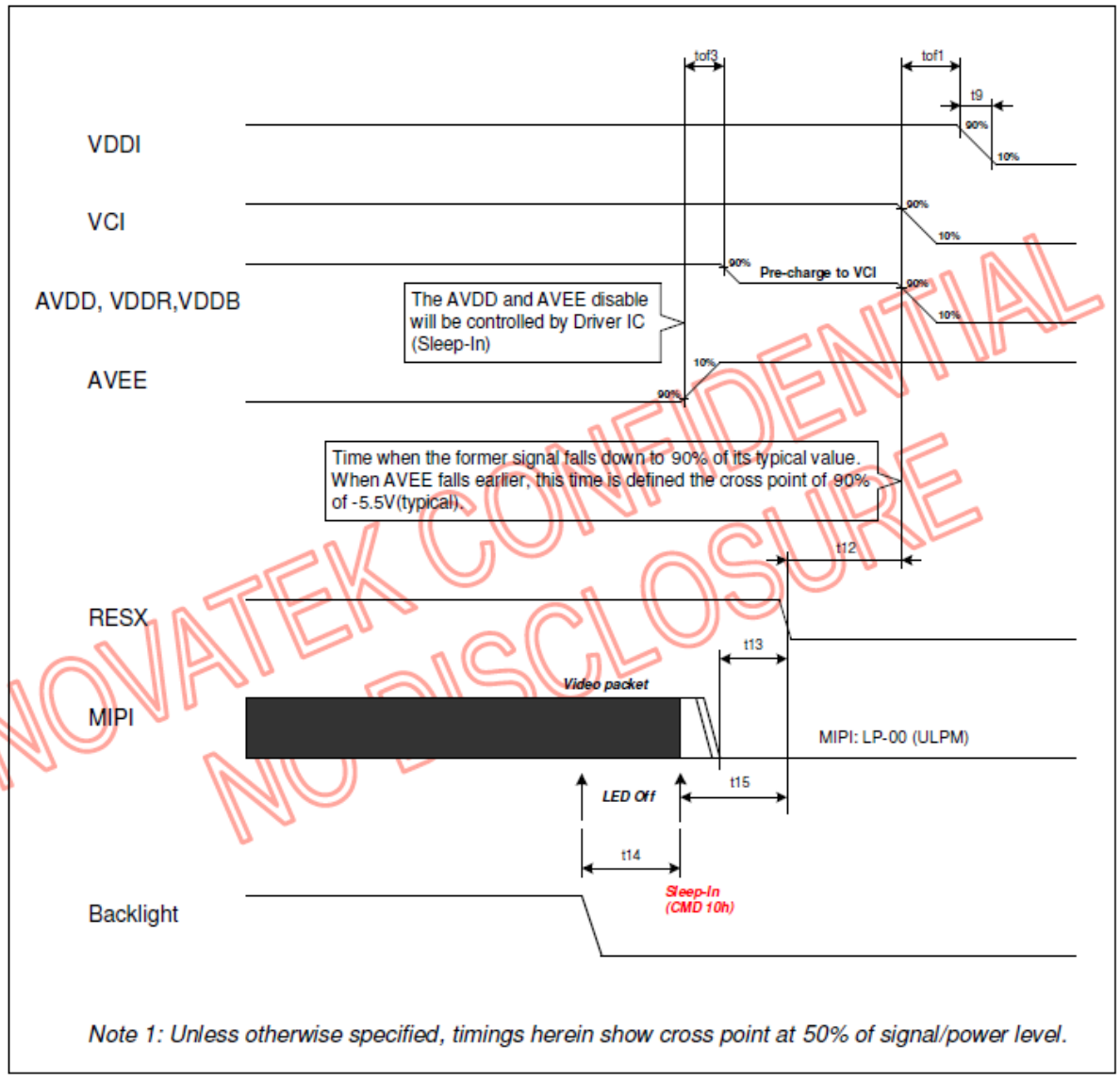
Note 3: Reset signal H to L to H (#1) is better than only L to H (#2).

6.4.2 Power OFF Sequence

The power off sequence for different power input modes are shown below figures.

Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
t9	150	-	-	μs	
tof1	0	-	-	ms	
tof2	0	-	-	ms	
tof3	0	-	-	ms	
tof4	0	-	-	ms	
t12	0	-	-	ms	
t13	0	-	-	ms	
t14	0	-	-	ms	
t15	100			ms	

- 3 Input power (BTM[2:0]="100" or "101") with NT50198 on FPC of LCM:
  VDDI=1.65~3.6V, VCI=2.5~3.6V (to NT50198), AVDD=VDDR=VDDB=4.5~6.0V, AVEE=-4.5~-6.0V



The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an uncontrolled power off the display will go blank and there will not be any visible effects within 1 second on the display (blank display) and remains blank until "Power On Sequence" powers it up.

7. Reliability Test Criteria

Items	Required Condition	Note
Temperature Humidity Bias	60 °C, 90%RH, 300 hours	
High Temperature Operation	70 °C, 300 hours	
Low Temperature Operation	-20 °C, 300 hours	
Hot Storage	80 °C, 300 hours	
Cold Storage	-30 °C, 300 hours	
Thermal Shock Test	-20 °C / 30 min, 60 °C / 30 min, 100cycles, 40 °C minimun ramp rate	
Shock Test (Non-Operating)	50G, 20ms, Half-sine wave, (±X, ±Y, ±Z)	
Vibration Test (Non-Operating)	1.5G, (10~200Hz, Sine wave) 30 mins/axis, 3 direction (X, Y, Z)	
On/off test	On/10 sec, Off/10 sec, 30,000 cycles	
ESD	Contact = ± 4 kV, class B (R=330,C=150pF) Air = ± 8 kV, class B (R=330,C=150pF) 1sec, 5 points, 5 times/point	Note 1
EMI	30-230 MHz, limit 40 dBu V/m, 230-1000 MHz, limit 47 dBu V/m	

Note1: According to EN61000-4-2, ESD class B: Some performance degradation allowed. No data lost Self-recoverable. No hardware failures.

Note2:

- Water condensation is not allowed for each test items.
- Each test is done by new TFT-LCD module. Don't use the same TFT-LCD module repeatedly for reliability test.
- The reliability test is performed only to examine the TFT-LCD module capability.
- To inspect TFT-LCD module after reliability test, please store it at room temperature and room humidity for 24 hours at least in advance.
- In the standard condition, there is not display function NG issue occurred.

8. Mechanical Characteristics

8.1 Outline Dimension