Product Specification

AU OPTRONICS CORPORATION

(V) Preliminary Specifications
() Final Specifications

Module	**10.1” WUXGA Color TFT-LCD with LED Backlight design**
Model Name	**G101UAN02.0**

Customer	**Date**	**Approved by**	**Date**
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Record of Revision

Version and Date	Page	Old description	New Description
0.1 2017/04/20	All	First draft specification	-

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1. Operating Precautions

1) Since front polarizer is easily damaged, please be cautious and not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or soft cloth.
5) Since the panel is made of glass, it may be broken or cracked if dropped or bumped on hard surface.
6) To avoid ESD (Electro Static Discharde) damage, be sure to ground yourself before handling TFT-LCD Module.
7) Do not open nor modify the module assembly.
8) Do not press the reflector sheet at the back of the module to any direction.
9) In case if a module has to be put back into the packing container slot after it was taken out from the container, do not press the center of the LED light bar edge. Instead, press at the far ends of the LED light bar edge softly. Otherwise the TFT Module may be damaged.
10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
11) TFT-LCD Module is not allowed to be twisted & bent even force is added on module in a very short time. Please design your display product well to avoid external force applying to module by end-user directly.
12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
13) Severe temperature condition may result in different luminance, response time and lamp ignition voltage.
14) Continuous operating TFT-LCD display under low temperature environment may accelerate lamp exhaustion and reduce luminance dramatically.
15) The data on this specification sheet is applicable when LCD module is placed in landscape position.
16) Continuous displaying fixed pattern may induce image sticking. It's recommended to use screen saver or shuffle content periodically if fixed pattern is displayed on the screen.

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2. General Description

G101UAN01.x is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:10 WUXGA, 1920(H) x1200(V) screen and 16.7M colors (RGB 6-bits + Hi-FRC) with LED backlight driving circuit**.** All input signals are MIPI interface compatible.

2.1 Display Characteristics

The following items are characteristics summary under 25 °C condition:

Items	**Unit**	**Specifications**
Screen Diagonal	[inch]	10.1”
Active Area	[mm]	216.81(H) x 135.5(V)
Pixels H x V		1920 x 3(RGB) x 1200
Pixel Pitch	[mm]	0.11292 X 0.11292
Pixel Arrangement		R.G.B. Vertical Stripe
Display Mode		AHVA, Normally Black
Nominal Input Voltage VDD	[Volt]	+3.3 Typ
Power Consumption	[Watt]	3.45W (with LED driver)
Weight	[Grams]	170 Max
Physical Size	[mm]	229.9 x 150.5 x 4.95 Max (PCBA side)
Electrical Interface		MIPI
Surface Treatment		Glare
Support Color		16.7M colors (RGB 6-bit + Hi-FRC)
Temperature Range Operating Storage (Non-Operating)	 [°C] [°C]	 -10 to +60 -20 to +70
RoHS Compliance		RoHS Compliance

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2.2 Optical Characteristics

The optical characteristics are measured under stable conditions at 25 °C (Room Temperature):

Item	Unit	Conditions	Min.	Typ.	Max.	Note
White Luminance	[cd/m2]	I_{LED}= 20mA (5p average)	600	800		
Uniformity	%	5 points	70%			
Contrast Ratio			600	800	-	
Response Time	[msec]	Rising + Falling	---	25	35	
Viewing Angle	[degree] [degree]	Horizontal (Right) CR = 10 (Left)	80 80	85 85	--- ---	
	[degree] [degree]	Vertical (Upper) CR = 10 (Lower)	80 80	85 85	--- ---	
Color / Chromaticity Coordinates (CIE 1931)		Red x	TBD	TBD	TBD	
		Red y	TBD	TBD	TBD	
		Green x	TBD	TBD	TBD	
		Green y	TBD	TBD	TBD	
		Blue x	TBD	TBD	TBD	
		Blue y	TBD	TBD	TBD	
		White x	TBD	TBD	TBD	
		White y	TBD	TBD	TBD	
Color Gamut	%		-	50	-	

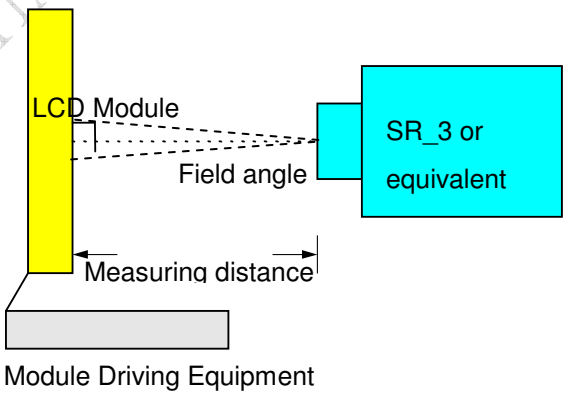
Note 1: Measurement method

Equipment Pattern Generator, Power Supply, Digital Voltmeter, Luminance meter (SR_3 or equivalent)

Aperture Field angle 2° with 50cm measuring distance

Test Point Follow Note 2 position

Environment *< 1 lux*



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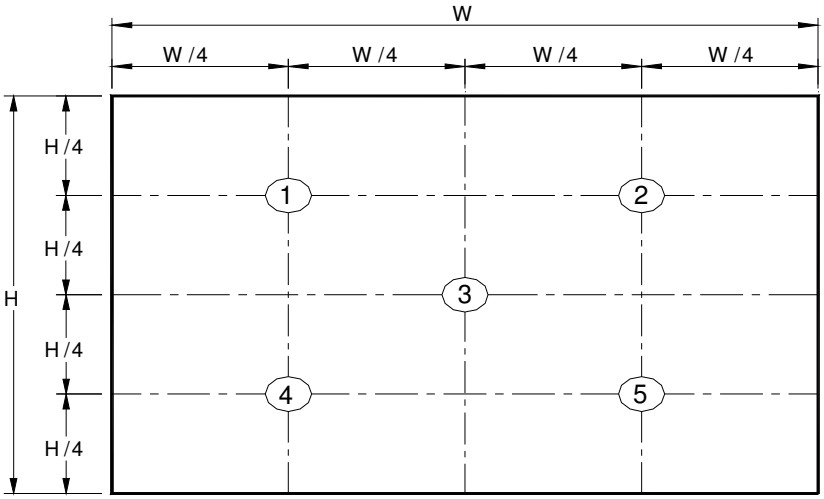
Note 2: Definition of 5 points position



Note 3: The luminance uniformity of 5 points is defined by dividing the minimum luminance values by the maximum test point luminance

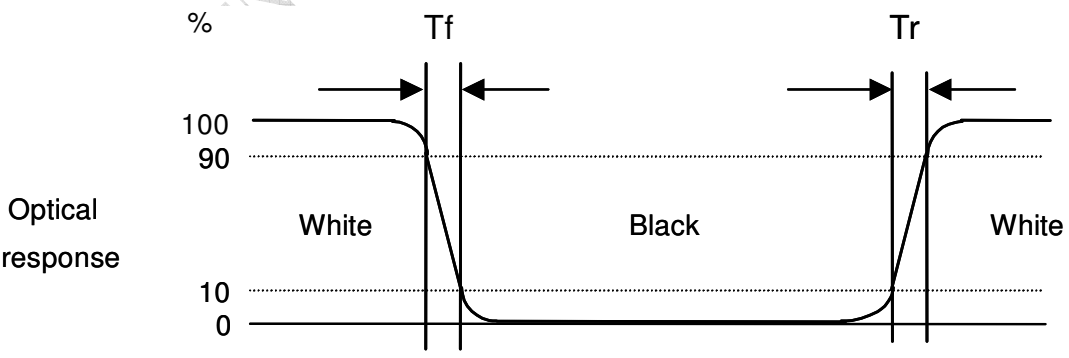
$$\delta_{W9} = \frac{\text{Minimum Brightness of five points}}{\text{Maximum Brightness of five points}}$$

Note 4: Definition of contrast ratio (CR):

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

Note 5: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “White” to “Black” (falling time) and from “Black” to “White” (rising time), respectively. The response time interval is between 10% and 90% of amplitudes. Please refer to the figure as below.



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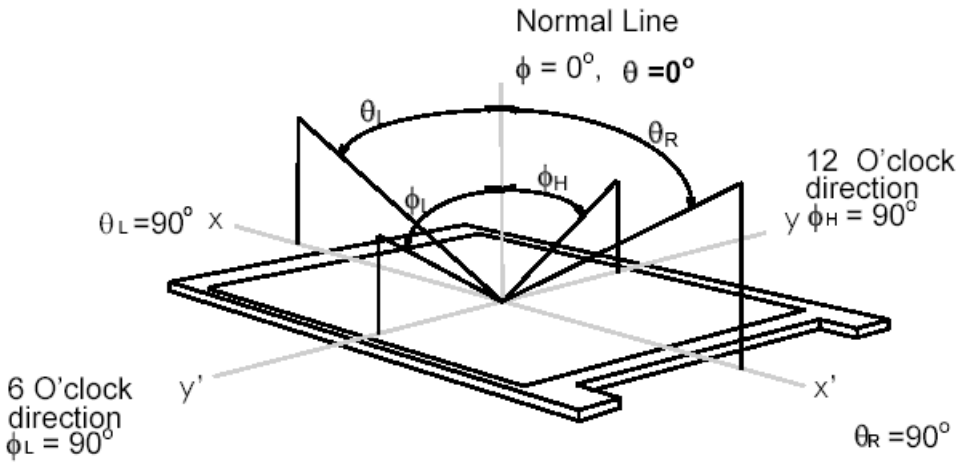
Note 6: Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as below: 90° (θ) horizontal left and right, and 90° (Φ) vertical high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated to its center to develop the desired measurement viewing angle.



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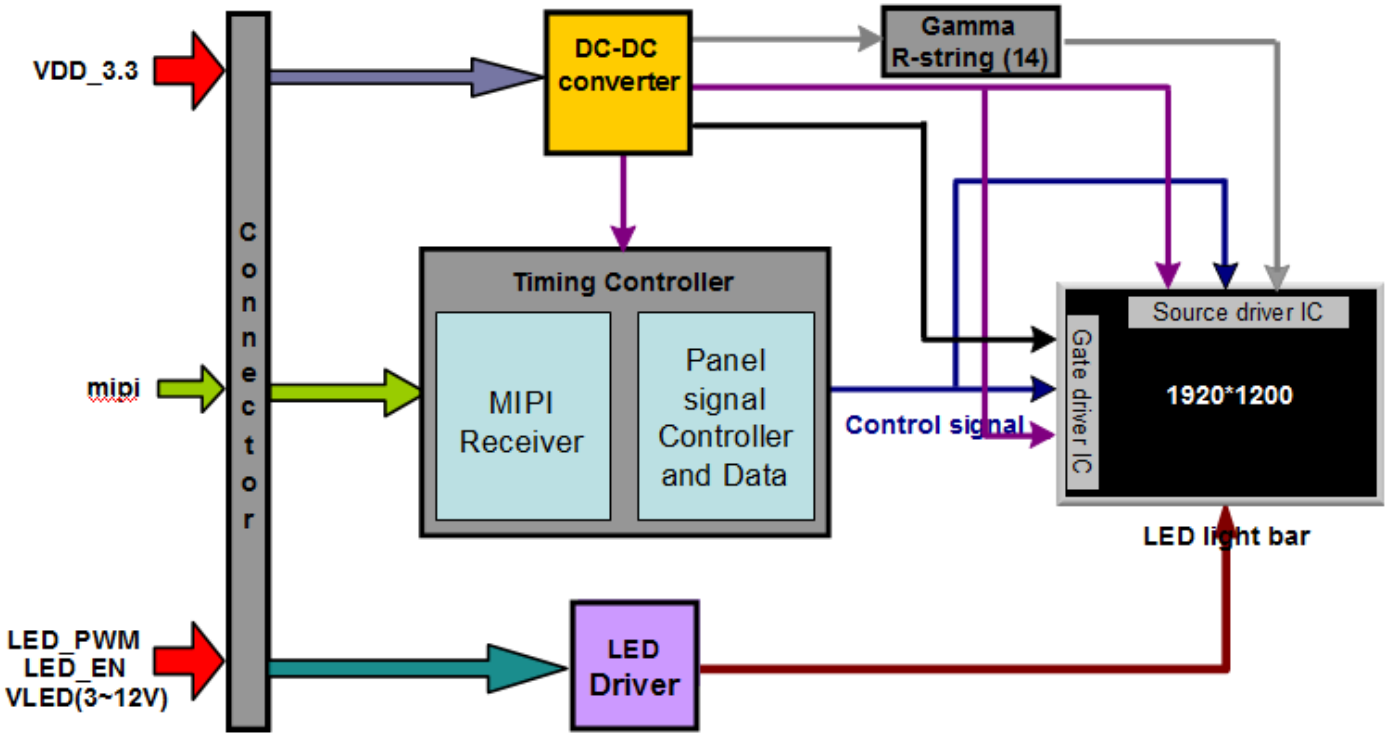
3. Functional Block Diagram

The following diagram shows the functional block of the 10.1 inch color TFT/LCD module:



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4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD drive Voltage	Vin	-0.3	+4.5	[Volt]	Note 1,2

4.2 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit
Operating Temperature	TOP	-10	+60	[°C]
Operation Humidity	HOP	5	90	[%RH]
Storage Temperature	TST	-20	+70	[°C]
Storage Humidity	HST	5	90	[%RH]

Note 1: At Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: Maximum wet-bulb temperature is less than 39℃ and no condensation

Note 4: Operating temperature means “Front and rear surface” of panel

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5. Electrical Characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

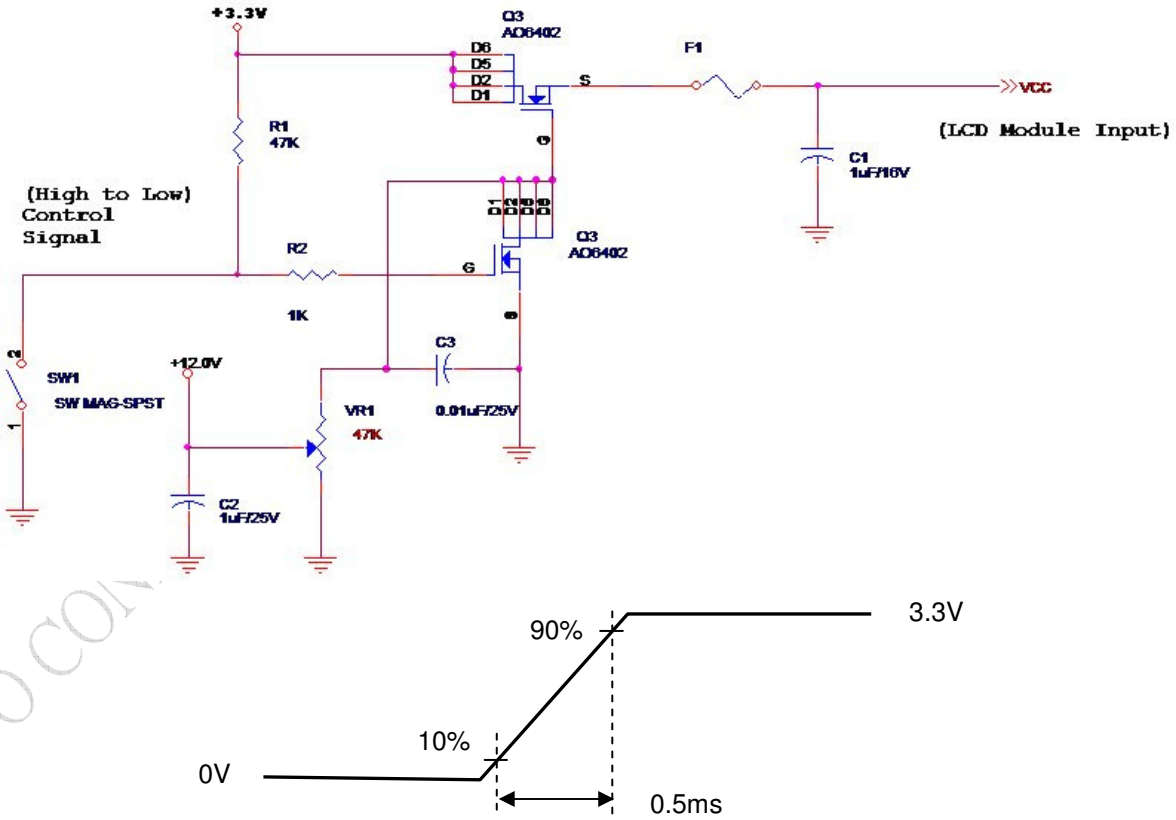
Input power specifications are as follows;

The power specification are measured under 25℃ and frame frenquency under 60Hz

Symbol	Parameter	Min	Typ	Max	Units	Remark
VDD	Logic/LCD Drive Voltage	3.0	3.3	4.2	[Volt]	
PDD	VDD Power	-	-	0.95	[Watt]	Note 1
IDD	IDD Current	-	-	316	[mA]	Note 1
IRush	Inrush Current	-	-	2000	[mA]	Note 2
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	

Note 1 : Maximum Measurement Condition：White Pattern at 3.3V driving voltage. ($P_{max}=V_{3.3} \times I_{white}$)

Note 2：Measure Condition



VDD rising time

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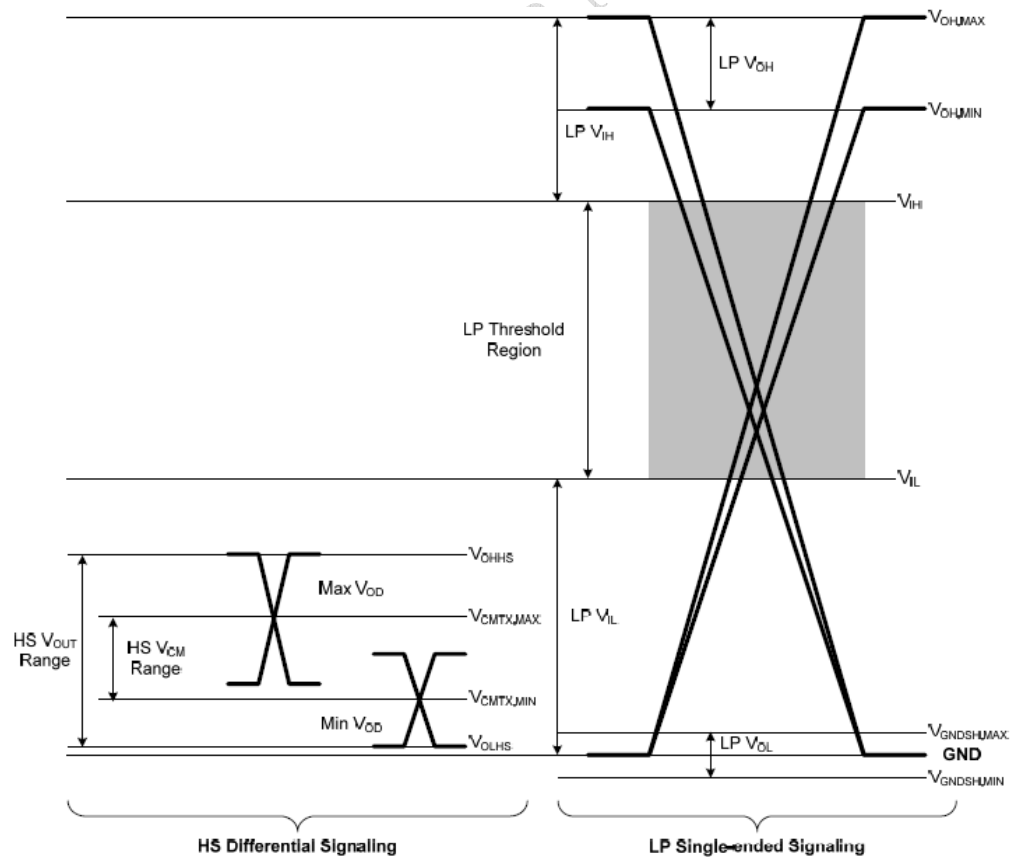
5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.
MIPI DC/AC Characteristics are as follows;

MIPI Receiver Differential Input (DC Characteristics)					
Symbol	Parameter	Min	Typ	Max	Unit
BR_{MIPI}	Input data bit rate	200	-	1000	Mbps
V_{CMRX}	Common-mode voltage(HS Rx mode)	70	-	330	mV
V_{IDTH}	Differential input high threshold (HS Rx mode)	-	-	70	mV
V_{IDTL}	Differential input low threshold (HS Rx mode)	-70	-	-	mV
$\lvert V_{IDM} \rvert$	Differential input voltage range (HS Rx mode)	70	-	500	mV
V_{IHHS}	Single-end input high voltage (HS Rx mode)	-	-	460	mV
V_{ILHS}	Single-end input low voltage (HS Rx mode)	-40	-	-	mV
Z_{ID}	Differential input impedance	80	100	125	Ω
V_{IHLP}	Logic 1 input voltage (LP Rx mode)	880			mV
V_{ILLP}	Logic 0 input voltage (LP Rx mode)			550	mV
V_{OH}	Output high level (LP Tx mode)	1.08	1.2	1.32	V
V_{OL}	Output low level (LP Tx mode)	-50		50	mV



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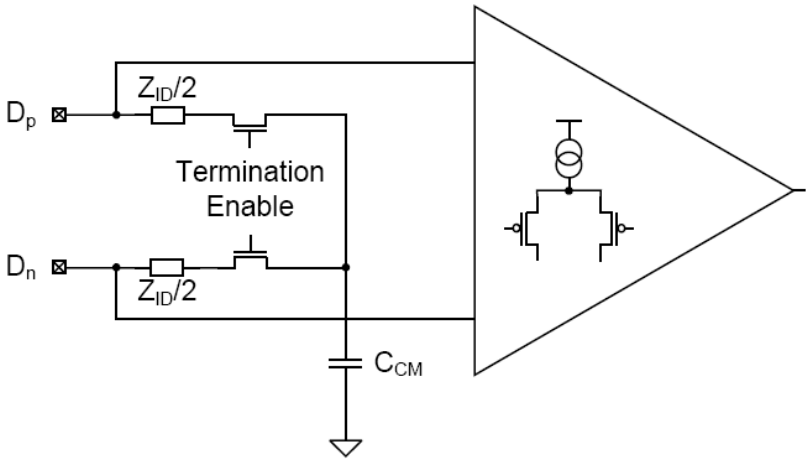
MIPI Receiver Differential Input (AC Characteristics)						
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\Delta V_{CMRX(HF)}$	Common-mode interference beyond 450MHz		-	-	100	mV
$\Delta V_{CMRX(LF)}$	Common-mode interference 50MHz ~ 450MHz		-50	-	50	mV
C_{CM}	Common-mode termination		-	-	60	pF
UI_{INST}	UI instantaneous		1		12.5	ns

HS RX Scheme

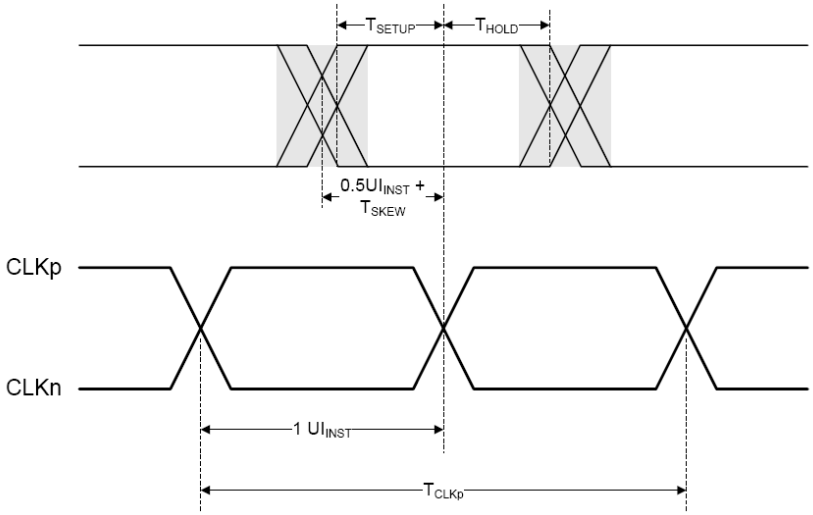


Symbol	Parameter	Min	Typ	Max	Unit	Notes
$T_{SKEW[TX]}$	Data to Clock Skew (mesured at transmitter)	-0.15		0.15	UI_{INST}	1
$T_{SETUP[RX]}$	Data to Clock Setup Time (receiver)	0.15			UI_{INST}	2
$T_{HOLD[RX]}$	Data to Clock Hold Time (receiver)	0.15			UI_{INST}	2

Note:

1. Total silicon and package delay budget of $0.3*UI_{INST}$
2. Total setup and hold window for receiver of $0.3*UI_{INST}$

High Speed Data Transmission: Data to Clock Timing



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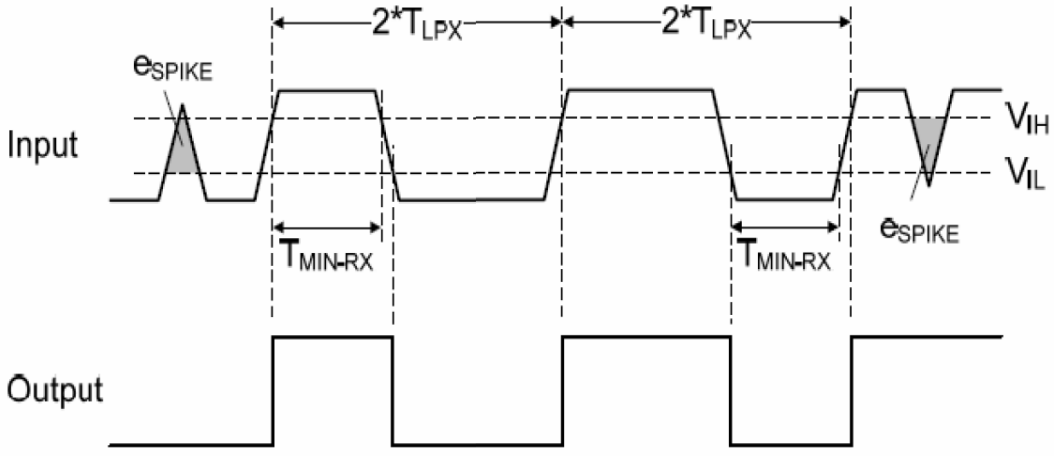
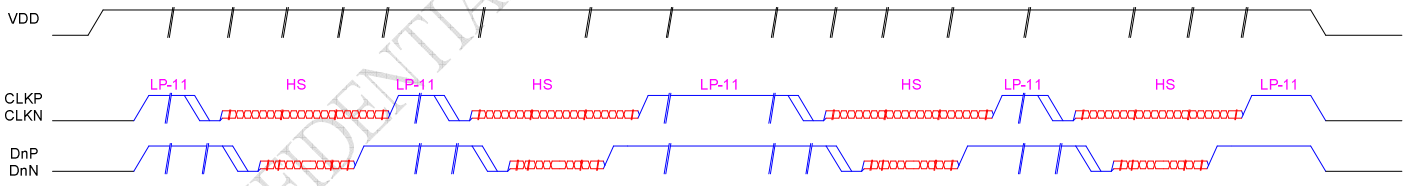
LP Receiver AC Specifications						
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
e_{SPIKE}	Input pulse rejection		-	-	300	V · ps
T_{MIN-RX}	Minimum pulse width response		50	-	-	ns
V_{INT}	Peak interference amplitude		-	-	200	mV
f_{INT}	Interference frequency		450	-	-	MHz

Input Glitch Rejection of Low-Power Receivers



For MIPI data transmission from TX to TCON works properly in video mode, it is suggested that all of MIPI lanes status follow the scheme showed in below. When power is turned on, all lanes (include clock lane) are into LP-11 status first. When TX wants to start transmitting data to TCON, the clock lane is into HS and start toggling. Then data lanes are into HS and data are transmitted. After data transmissions are finished (ex. H-blanking, V-blanking), the data lanes are returned to LP-11, then clock lane, too. The transmission start from LP-11 and stop in LP-11 on all lanes (include clock lane) are the recommended proper operation sequence for MIPI video mode.



The timing definitions are listed in below,

Parameter	Description	Min	Typ	Max	Unit
TCLK-MISS	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX.			60	ns
TCLK-POST	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of THS-TRAIL to the beginning of TCLK-TRAIL.	60 ns + 52*UI			ns
TCLK-PRE	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			UI

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TCLK-PREPARE	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	ns
TCLK-SETTLE	Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of TCLK-PREPARE.	95		300	ns
TCLK-TERM-EN	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX.			38	ns
TCLK-TRAIL	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns
TCLK-PREPARE + TCLK-ZERO	TCLK-PREPARE + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			ns
TD-TERM-EN	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses VIL,MAX.			35 ns + 4*UI	ns
TEOT	Transmitted time interval from the start of THS-TRAIL or TCLK-TRAIL, to the start of the LP-11 state following a HS burst.			105 ns + 12*UI	ns
THS-EXIT	Time that the transmitter drives LP-11 following a HS burst.	100			ns
THS-SYNC	HS Sync-Sequence '00011101' period		8		UI
THS-PREPARE	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40 ns + 4*UI		85 ns + 6*UI	ns
THS-PREPARE + THS-ZERO	THS-PREPARE + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145 ns + 10*UI			ns
THS-SETTLE	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of THS-PREPARE.	85 ns + 6*UI		145 ns + 10*UI	ns
THS-SKIP	Time interval during which the HS-RX should ignore any transitions on the Data Lane, following a HS burst. The end point of the interval is defined as the beginning of the LP-11 state following the HS burst.	40		55 ns + 4*UI	ns
THS-TRAIL	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	60 ns + 4*UI			ns
TLPX	Transmitted length of any Low-Power state period	50			ns
Ratio TLPX	Ratio of TLPX(MASTER)/TLPX(SLAVE) between Master and Slave side	2/3		3/2	
TTA-GET	Time that the new transmitter drives the Bridge state (LP-00) after accepting control during a Link Turnaround.		5*TLPX		ns
TTA-GO	Time that the transmitter drives the Bridge state (LP-00) before releasing control during a Link Turnaround.		4*TLPX		ns
TTA-SURE	Time that the new transmitter waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	TLPX		2*TLPX	ns

Note:

1. The minimum value depends on the bit rate. Implementations should ensure proper operation for all the supported bit rates.
2. TLPX is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.

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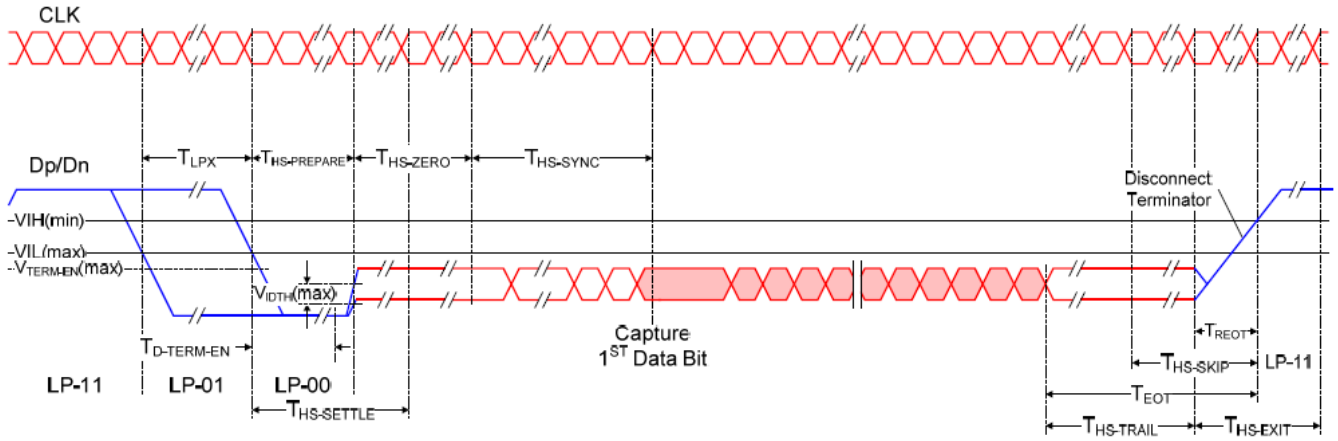
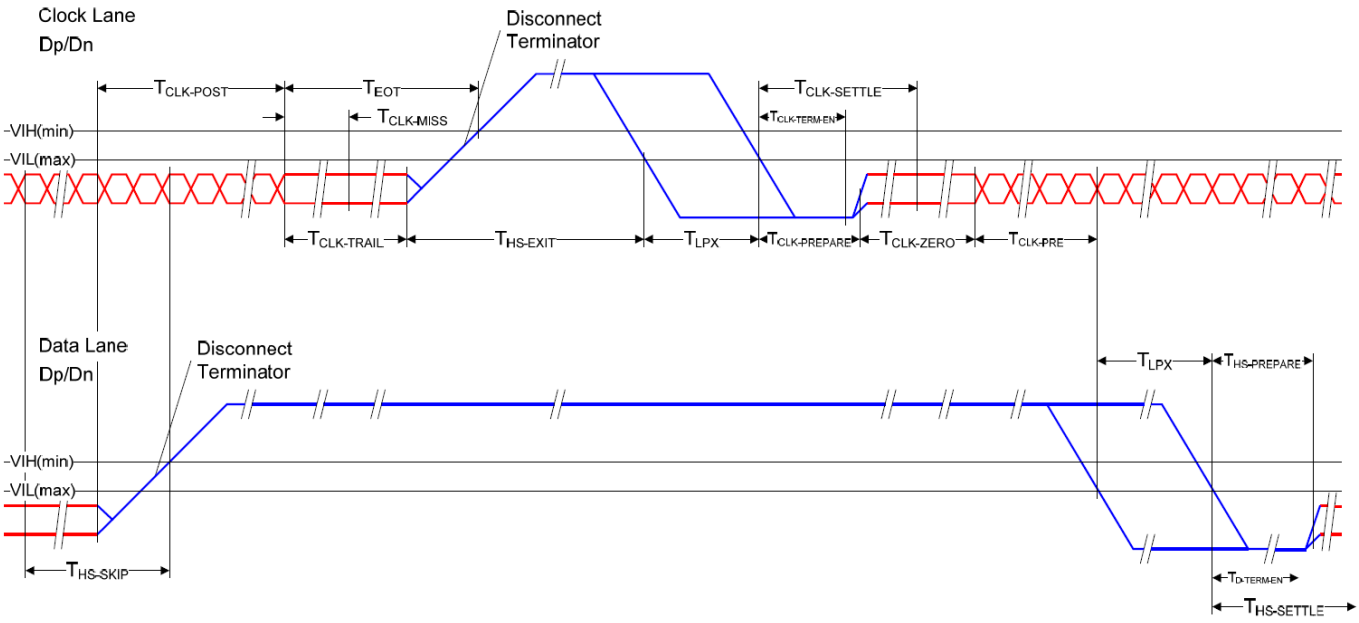
High-Speed Data Transmission in Bursts



Switching the Clock Lane between Clock Transmission and Low-Power Mode



Turnaround Procedure

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5.2 Backlight Unit

5.2.1 LED characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Backlight Power Consumption	PLED	-	-	4.9	[Watt]	(Ta=25℃@ 800 nits)
LED Life-Time	N/A	15,000	20,000	-	Hour	(Ta=25℃@ 800 nits) Note1.
LED Forward Voltage	VF	5.5	5.65	5.8	[Volt]	(Ta=25℃)
LED Forward Voltage of every LED string	VF-string	-	-	34.8	[Volt]	(Ta=25℃) Note2.
LED Forward Current	IF	-	20	-	[mA]	(Ta=25℃)

Note 1. The LED life-time define as the estimated time to 50% degradation of initial luminous.

Note 2. LED Array 6 parallel * 6 series

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5.2.2 Backlight input signal characteristics

Parameter	Symbol	Min	Typ	Max	Units	Remark
LED Power Supply	VLED	3		12	[Volt]	Define as Connector Interface (Ta=25℃) Note1.
LED Enable Input High Level	VLED_EN	1.7	-	5.5	[Volt]	
LED Enable Input Low Level		-	-	0.8	[Volt]	
PWM Logic Input High Level	VPWM_EN	1.7	-	5.5	[Volt]	
PWM Logic Input Low Level		-	-	0.8	[Volt]	
PWM Input Frequency	FPWM	200	-	10K	Hz	
PWM Duty Ratio	Duty	1		100	%	

Note 1: The input high level voltage conversion to 2.5V by level shift circuit.

Note 2: The LED PWM Logic Input Low Level Voltage must have an output impedance close to 0 ohm in front of input connector.

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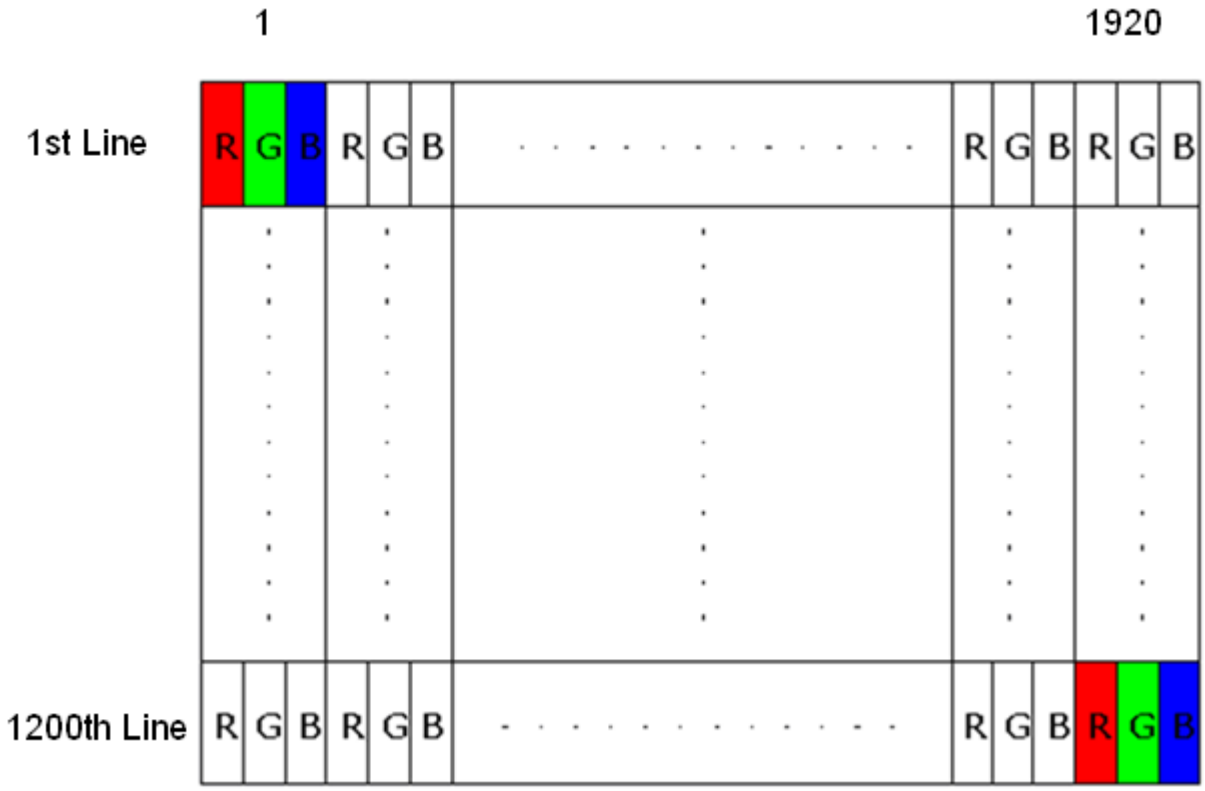
6. Signal Interface Characteristic

6.1 Pixel Format Image

Following figure shows the relationship between input signal and LCD pixel format.



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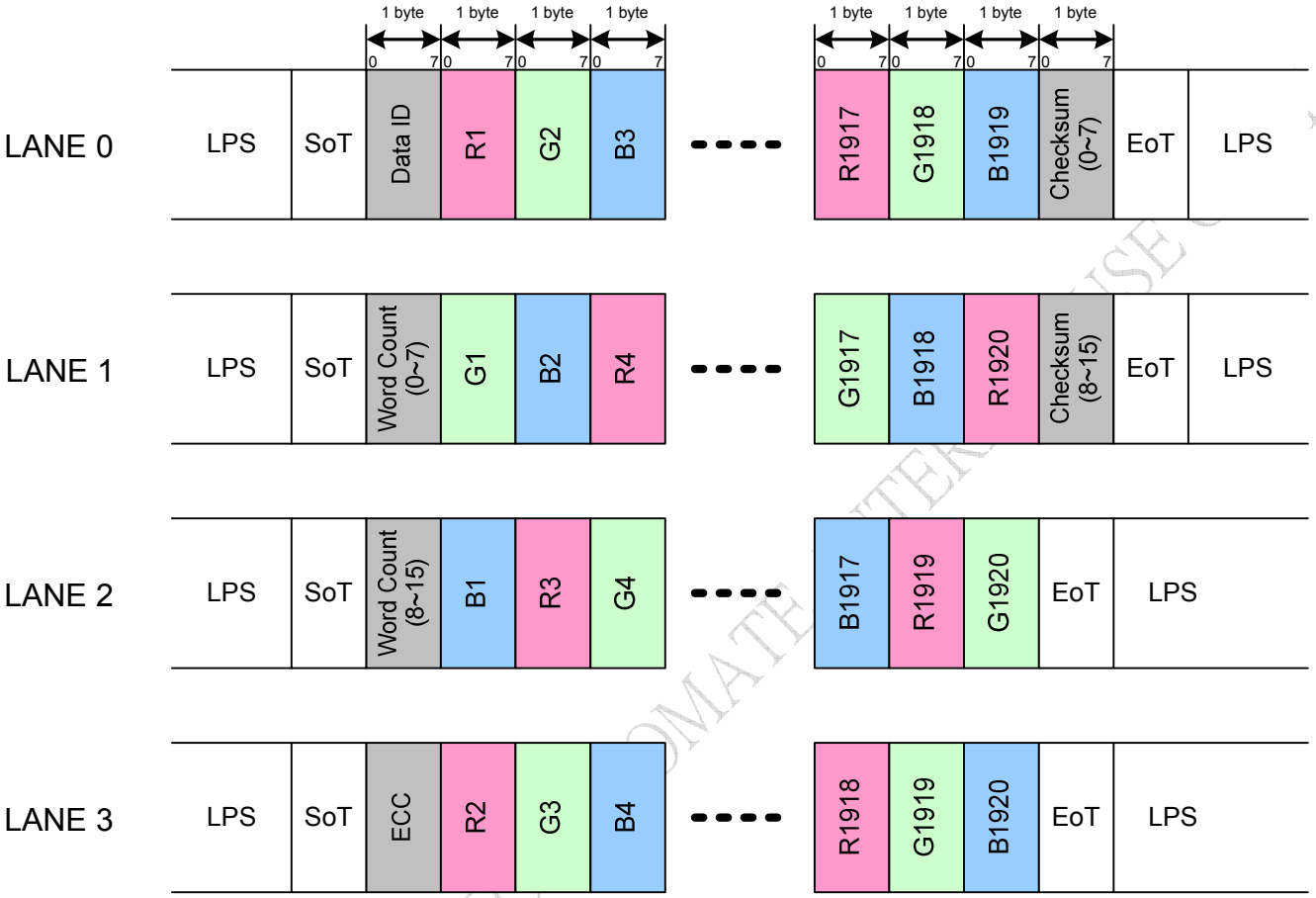
6.2 The Input Data Format

Input Pixel Stream Format (1920RGB in 4 Lanes with RGB 8-8-8 format)



LPS : Low Power State
SoT : Start of Transmission
EoT : End of Transmission
ECC : Error-Correcting Code

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6.3 Integration Interface Requirement

6.3.1 MIPI Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	For Signal Connector
Manufacturer	HIROSE
Type / Part Number	FH34SJ-34S-0.5SH(50) or compatible
Mating Housing/Part Number	FPC Cable

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6.3.2 MIPI Pin Assignment

MIPI is a differential signal technology for LCD interface and high speed data transfer device.

No.	Pin Name	Description
1	VDD	DC-DC circuit supply voltage
2	VDD	DC-DC circuit supply voltage
3	Hsync	Yoe signal output to system
4	LED_EN	LED driver Enable Input
5	LED_PWM	Backlight LED driver PWM Input
6	ID	Pull high (10Kohm to 1.8V)
7	ID	Pull high (10Kohm to 1.8V)
8	NC	Not Connection
9	GND	Ground
10	DSI_D2P/Rx-IN2P	MIPI data pair 2 positive signal
11	DSI_D2N/Rx-IN2N	MIPI data pair 2 negative signal
12	GND	Ground
13	DSI_D1P/Rx-IN1P	MIPI data pair 1 positive signal
14	DSI_D1N/Rx-IN1N	MIPI data pair 1 negative signal
15	GND	Ground
16	DSI_CLKP/Rx-CLKP	MIPI Clock positive signal
17	DSI_CLKN/Rx-CLKN	MIPI Clock negative signal
18	GND	Ground
19	DSI_D0P/Rx-IN0P	MIPI data pair 0 positive signal
20	DSI_D0N/Rx-IN0N	MIPI data pair 0 negative signal
21	GND	Ground
22	DSI_D3P/Rx-IN3P	MIPI data pair 3 positive signal
23	DSI_D3N/Rx-IN3N	MIPI data pair 3 negative signal
24	GND	Ground
25	GND	Ground
26	GND	Ground
27	GND	Ground
28	ID	Pull low (4.7Kohm to Ground)
29	Aging	Aging Mode Power Supply (AUO only)
30	NC	Not Connection
31	LED+	LED Power Supply
32	LED+	LED Power Supply
33	LED+	LED Power Supply
34	LED+	LED Power Supply

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6.4 MIPI Interface Timing

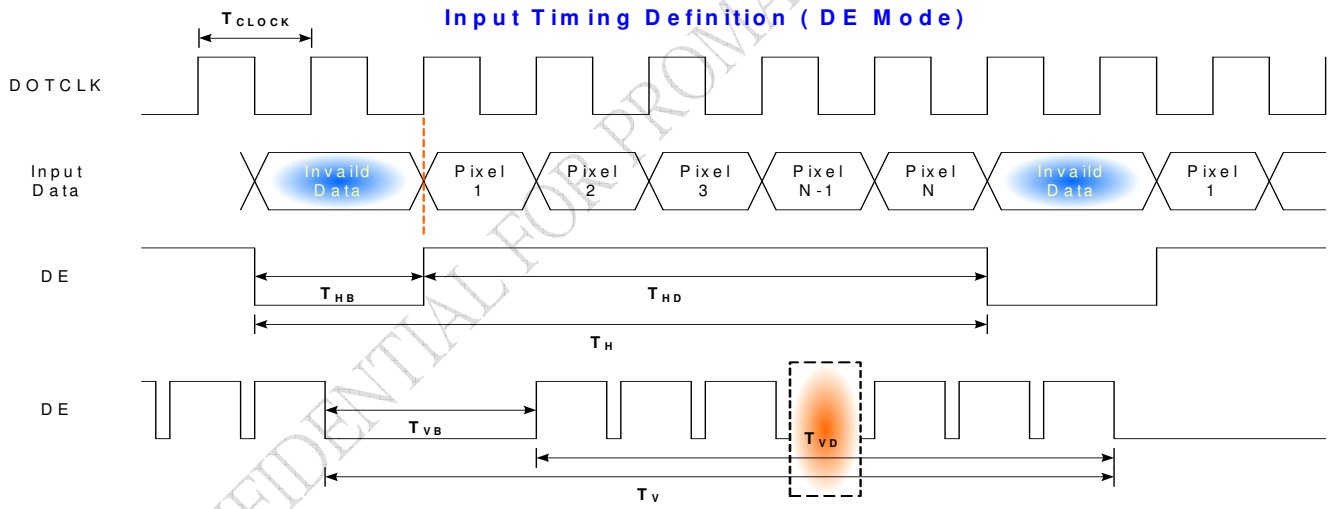
6.4.1 Timing Characteristics

Basically, interface timings should match the 1920x1200 /60Hz manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		---	---	60	---	Hz
Clock frequency		1/ T_{Clock}	148.04	149.9	151.27	MHz
Vertical Section	Period	T_V	1206	1212	1218	T_{Line}
	Active	T_{VD}	1200			
	Blanking	T_{VB}	6	12	18	
Horizontal Section	Period	T_H	2046	2058	2070	T_{Clock}
	Active	T_{HD}	1920			
	Blanking	T_{HB}	126	138	150	

Note : DE mode only

6.4.2 Timing diagram



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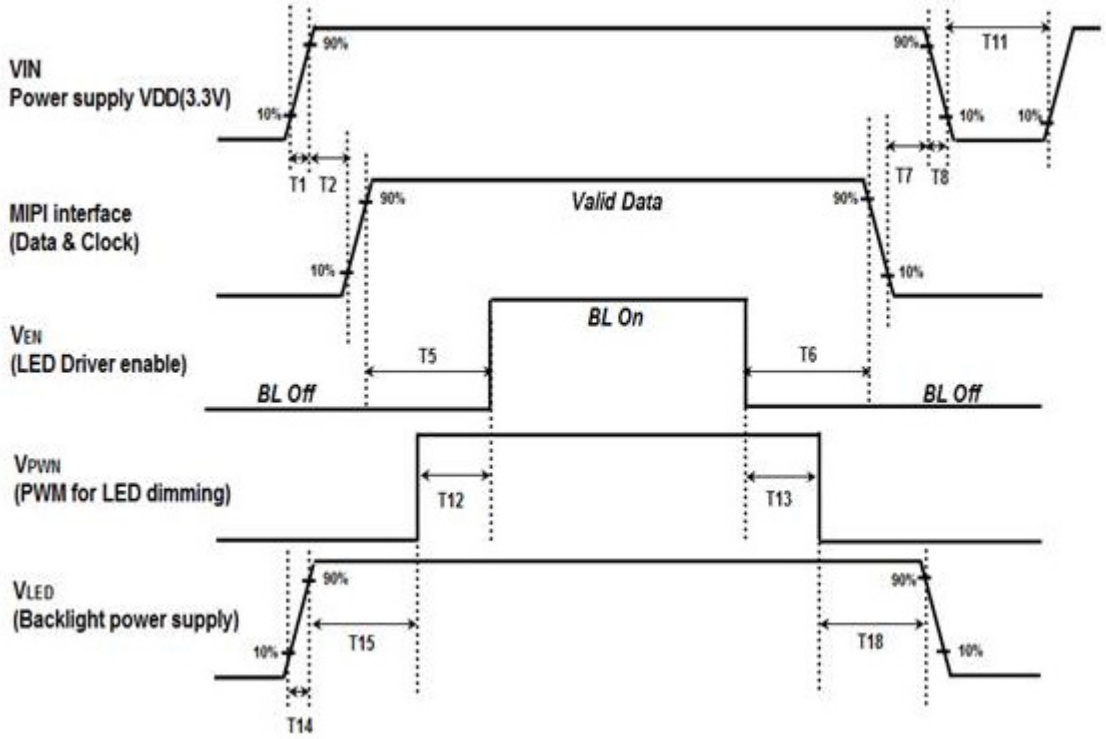
6.5 Power ON/OFF Sequence

Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart.



Power Sequence Timing			
Parameter	Value		Units
	Min.	Max.	
T1	0.5	10	ms
T2	40	-	
T5	120	-	
T6	50	-	
T7	0	-	
T8	0	10	
T11	500	-	
T12	10	-	
T13	10	-	
T14	0.5	10	
T15	10	-	
T18	10	-	

Note: LED_PWM must be pull low(GND) when it is not pull high.

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7. Reliability Test Criteria

Items	Required Condition	Note
Temperature Humidity Bias	40 °C /90%,300Hr	
High Temperature Operation	60 °C, 300Hr	
Low Temperature Operation	-10 °C, 300Hr	
Hot Storage	70 °C, 300Hr	
Cold Storage	-20 °C, 300Hr	
Thermal Shock Test	-10 °C /30 min , 60 °C /30 min , 20cycles	
Hot Start Test	60 °C /1 Hr min. power on/off per 5 minutes, 5 times	
Cold Start Test	-10 °C /1 Hr min. power on/off per 5 minutes, 5 times	
On/off test	On/10 sec, Off/10 sec, 30,000 cycles	
Shock Test	Acceleration: 220 G Half sine wave Active time: 2 ms Pulse: X,Y,Z .one time for each side Test method: Non-Operation	
Vibration Test	Acceleration: 1.5 G Frequency: 10 - 500Hz Random Sweep: 30 Minutes each Axis (X, Y, Z) Test method: Non-Operation	
ESD	Contact : ± 8KV/ operation, Class B Air : ± 15KV / operation, Class B	Note 1

Note1: According to EN61000-4-2 , ESD class B: Some performance degradation allowed. No data lost

. Self-recoverable. No hardware failures.

Note2:

- Water condensation is not allowed for each test items.
- Each test is done by new TFT-LCD module. Don't use the same TFT-LCD module repeatedly for reliability test.
- The reliability test is performed only to examine the TFT-LCD module capability.
- To inspect TFT-LCD module after reliability test, please store it at room temperature and room humidity for 24 hours at least in advance.

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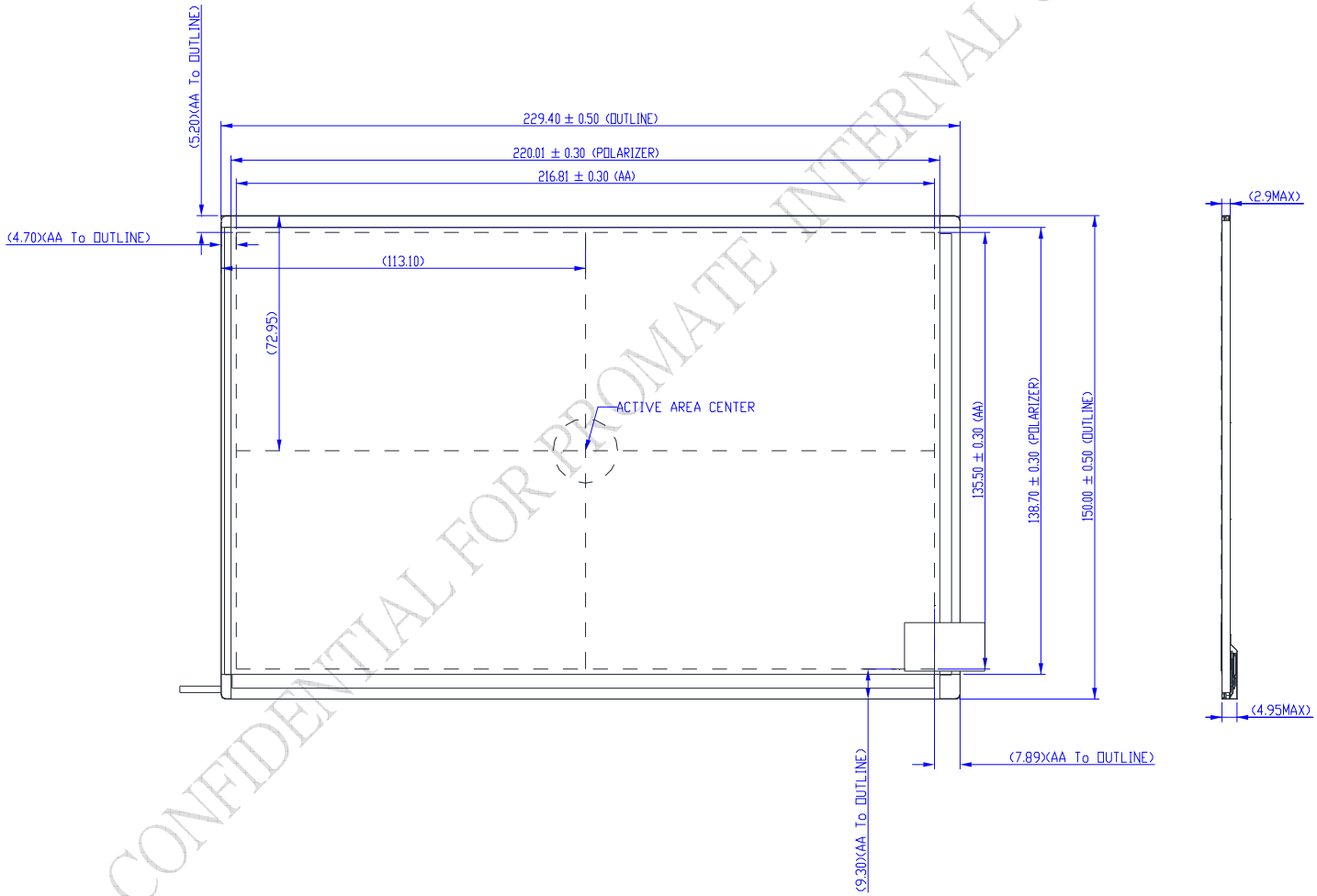
8. Mechanical Characteristics

8.1 LCM Outline Dimension (Front View)



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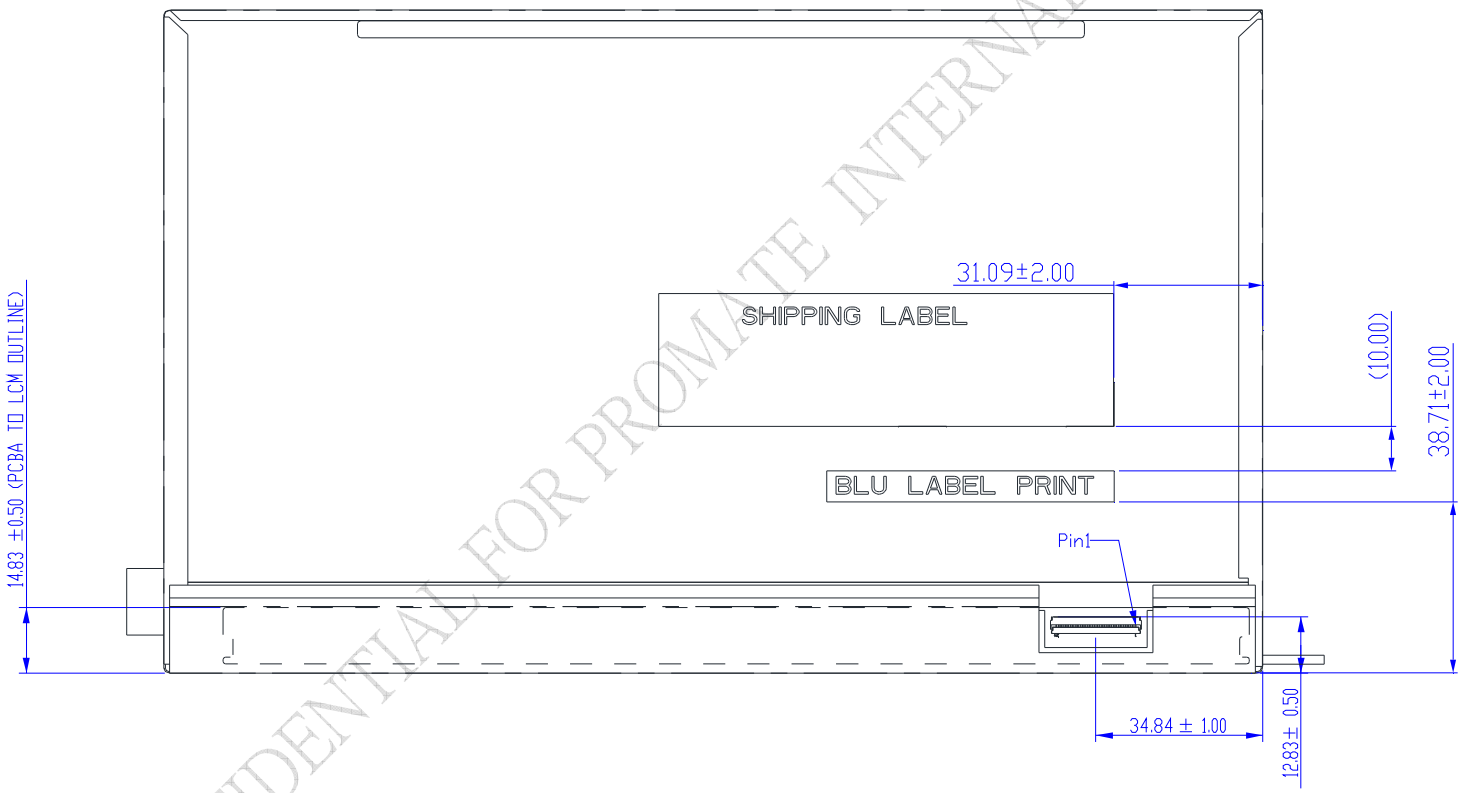
8.2 LCM Outline Dimension (Rear View)



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9. Label and Packaging

9.1 Shipping Label (on the rear side of TFT-LCD display)

TBD

9.2 Carton/Pallet Package

TBD

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10 Safety

10.1 Sharp Edge Requirements

There will be no sharp edges or comers on the display assembly that could cause injury.

10.2 Materials

10.2.1 Toxicity

There will be no carcinogenic materials used anywhere in the display module. If toxic materials are used, they will be reviewed and approved by the responsible AUO toxicologist.

10.2.2 Flammability

All components including electrical components that do not meet the flammability grade UL94-V1 in the module will complete the flammability rating exception approval process.

The printed circuit board will be made from material rated 94-V1 or better. The actual UL flammability rating will be printed on the printed circuit board.

10.3 Capacitors

If any polarized capacitors are used in the display assembly, provisions will be made to keep them from being inserted backwards.

10.4 National Test Lab Requirement

The display module will satisfy all requirements for compliance to:

UL 60950-1 second edition	U.S.A. Information Technology Equipment

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