

# SPECIFICATION

PART NO. OEL9M0087-R-E

**OLED**  
**128X64** **1.54"**

This specification maybe changed without any notice in order to improve performance or quality etc.

Please contact TRULY Semiconductors LTD. OLED R&D department for update specification and product status before design for this product or release the order.

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### REVISION HISTORY

Rev.	Contents	Date
1.0	First release	2014-11-20

**■ PHYSICAL DATA**

No.	Items:	Specification:	Unit
1	Diagonal Size	1.54	Inch
2	Resolution	128 (H) x 64(V)	Dots
3	Active Area	35.04 (W) x 17.51 (H)	mm <sup>2</sup>
4	Outline Dimension (Panel)	42.04 (W) x 27.22(H)	mm <sup>2</sup>
5	Pixel Pitch	0.274 (W) x 0.274 (H)	mm <sup>2</sup>
6	Pixel Size	0.249(W) x 0.249(H)	mm <sup>2</sup>
7	Driver IC	SSD1309Z	-
8	Display Color	Red	-
9	Grayscale	1	Bit
10	Interface	Parallel / SPI/ IIC	-
11	IC package type	COG	-
12	Module connecting type	ZIF	-
13	Panel Thickness	1.5±0.1	mm
14	Weight	TBD	g
15	Duty	1/64	-

**■ ABSOLUTE MAXIMUM RATINGS**

 Unless otherwise specified,  $V_{SS} = 0V$ 

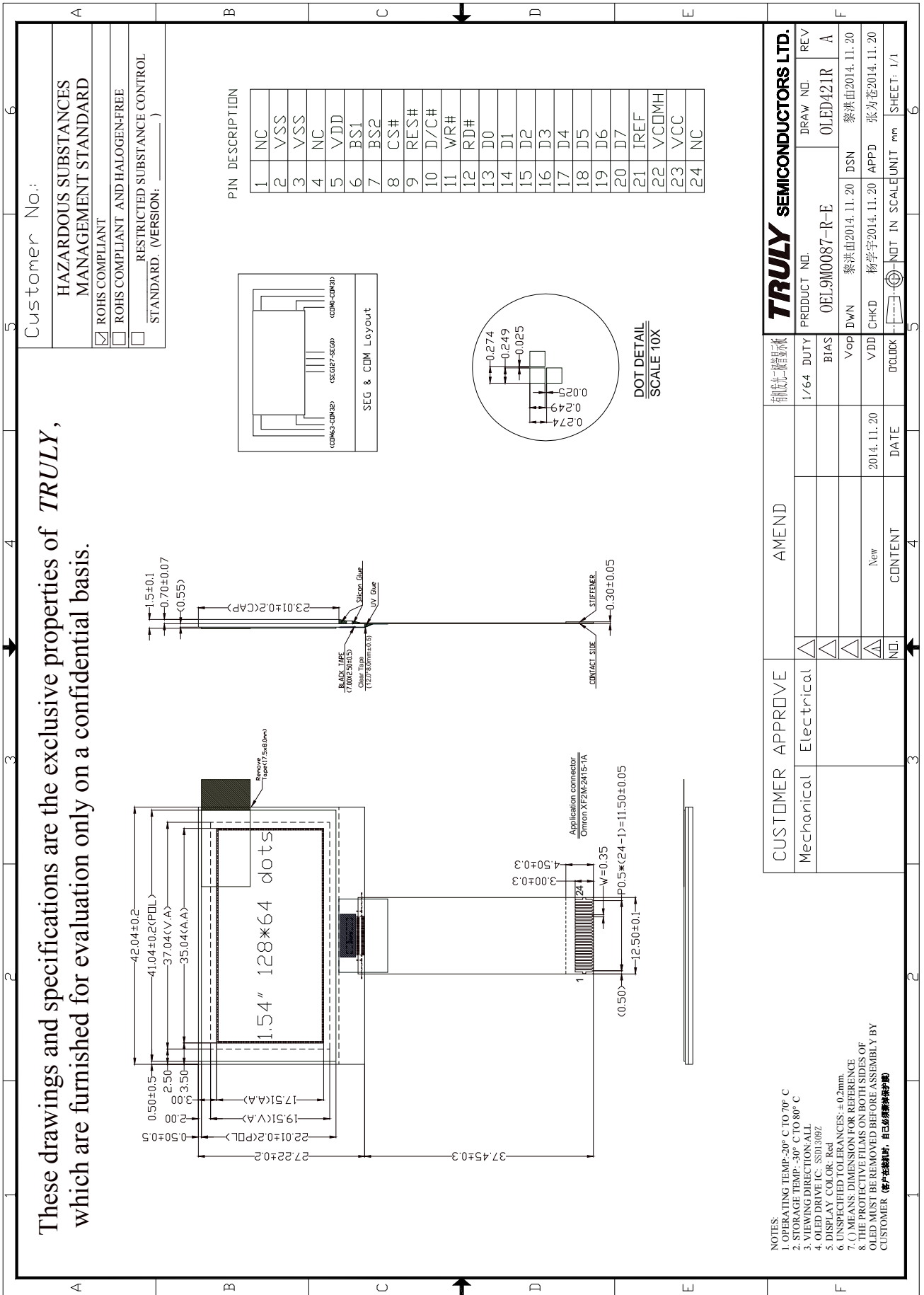
 (  $T_a = 25^{\circ}C$  )

Items		Symbol	Min	Typ.	Max	Unit
Supply Voltage	Logic	$V_{DD}$	-0.3	-	+4.0	V
	Driving	$V_{CC}$	0	-	17.0	V
Operating Temperature		Top	-20	-	70	°C
Storage Temperature		Tst	-30	-	80	°C
Humidity		-	-	-	90	%RH

**NOTE:**

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

EXTERNAL DIMENSION



NOTES:  
 1. OPERATING TEMP: -20° C TO 70° C  
 2. STORAGE TEMP: -30° C TO 80° C  
 3. VIEWING DIRECTION: ALL  
 4. OLED DRIVE IC: SS31309Z  
 5. DISPLAY COLOR: Red  
 6. UNSPECIFIED TOLERANCES: ±0.2mm.  
 7. ( ) MEANS DIMENSION FOR REFERENCE  
 8. THE PROTECTIVE FILMS ON BOTH SIDES OF OLED MUST BE REMOVED BEFORE ASSEMBLY BY CUSTOMER (客户在组装前, 自己必须撕掉保护膜)

**■ ELECTRICAL CHARACTERISTICS****◆ DC Characteristics**Unless otherwise specified,  $V_{SS} = 0V$ ,  $V_{DD} = 1.65V$  to  $3.3V$  (  $T_a = 25^\circ C$  )

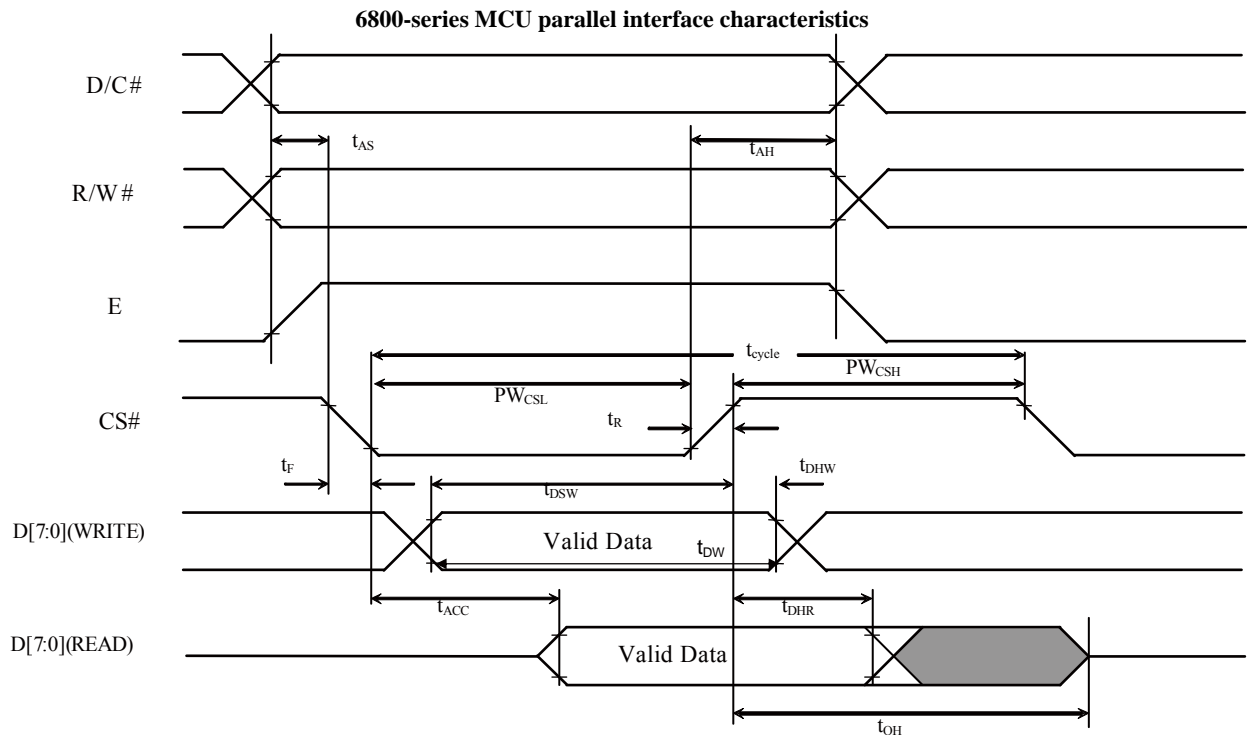
Items		Symbol	Min	Typ.	Max	Unit
Supply Voltage	Logic	$V_{DD}$	1.65	3.0	3.3	V
	Operating	$V_{CC}$	7.0	13.0	16.0	V
Input Voltage	High Voltage	$V_{IH}$	$0.8 \times V_{DD}$	-	-	V
	Low Voltage	$V_{IL}$	-	-	$0.2 \times V_{DD}$	V
Output Voltage	High Voltage	$V_{OH}$	$0.9 \times V_{DD}$	-	-	V
	Low Voltage	$V_{OL}$	-	-	$0.1 \times V_{DD}$	V

◆ AC Characteristics

1. 6800-Series MCU Parallel Interface Timing Characteristics

$V_{DD}=1.65V$  to  $3.3V$  ( $T_a = 25^{\circ}C$ )

Symbol	Parameter	Min	Typ	Max	Unit
$t_{cycle}$	Clock Cycle Time	300	-	-	ns
$t_{AS}$	Address Setup Time	20	-	-	ns
$t_{AH}$	Address Hold Time	0	-	-	ns
$t_{DW}$	Data Write Time	80	-	-	ns
$t_{DSW}$	Write Data Setup Time	40	-	-	ns
$t_{DHW}$	Write Data Hold Time	20	-	-	ns
$t_{DHR}$	Read Data Hold Time	20	-	-	ns
$t_{OH}$	Output Disable Time	-	-	70	ns
$t_{ACC}$	Access Time	-	-	140	ns
$PW_{CSL}$	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
$PW_{CSH}$	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
$t_R$	Rise Time	-	-	40	ns
$t_F$	Fall Time	-	-	40	ns

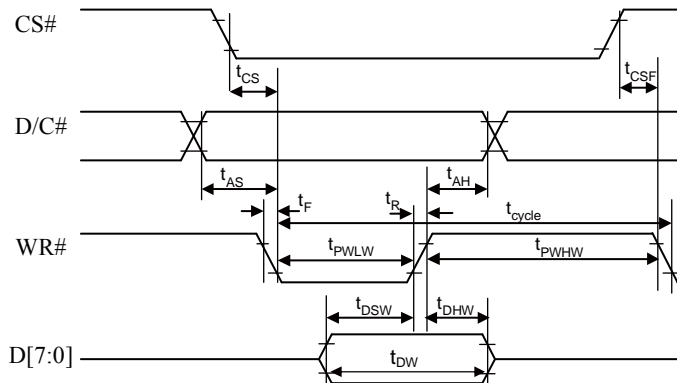


**2. 8080 Series MPU Parallel Interface**

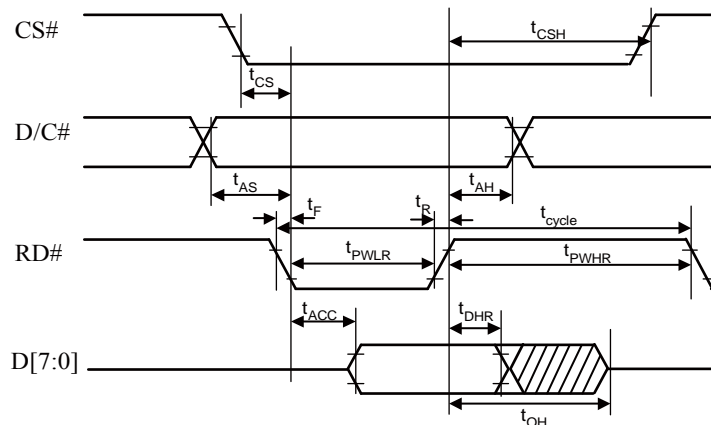
$V_{DD}=1.65V$  to  $3.3V$  ( $T_a = 25^\circ C$ )

Symbol	Parameter	Min	Typ	Max	Unit
$t_{cyle}$	Clock Cycle Time	300	-	-	ns
$t_{AS}$	Address Setup Time	20	-	-	ns
$t_{AH}$	Address Hold Time	0	-	-	ns
$t_{DW}$	Data Write Time	70	-	-	ns
$t_{DSW}$	Write Data Setup Time	40	-	-	ns
$t_{DHW}$	Write Data Hold Time	15	-	-	ns
$t_{DHR}$	Read Data Hold Time	20	-	-	ns
$t_{OH}$	Output Disable Time	-	-	70	ns
$t_{ACC}$	Access Time	-	-	140	ns
$t_{PWL R}$	Read Low Time	120	-	-	ns
$t_{PWL W}$	Write Low Time	60	-	-	ns
$t_{PWH R}$	Read High Time	60	-	-	ns
$t_{PWH W}$	Write High Time	60	-	-	ns
$t_R$	Rise Time	-	-	40	ns
$t_F$	Fall Time	-	-	40	ns
$t_{CS}$	Chip select setup time	0	-	-	ns
$t_{CSH}$	Chip select hold time to read signal	0	-	-	ns
$t_{CSF}$	Chip select hold time	20	-	-	ns

**8080-series parallel interface characteristics**  
Write cycle



Read Cycle



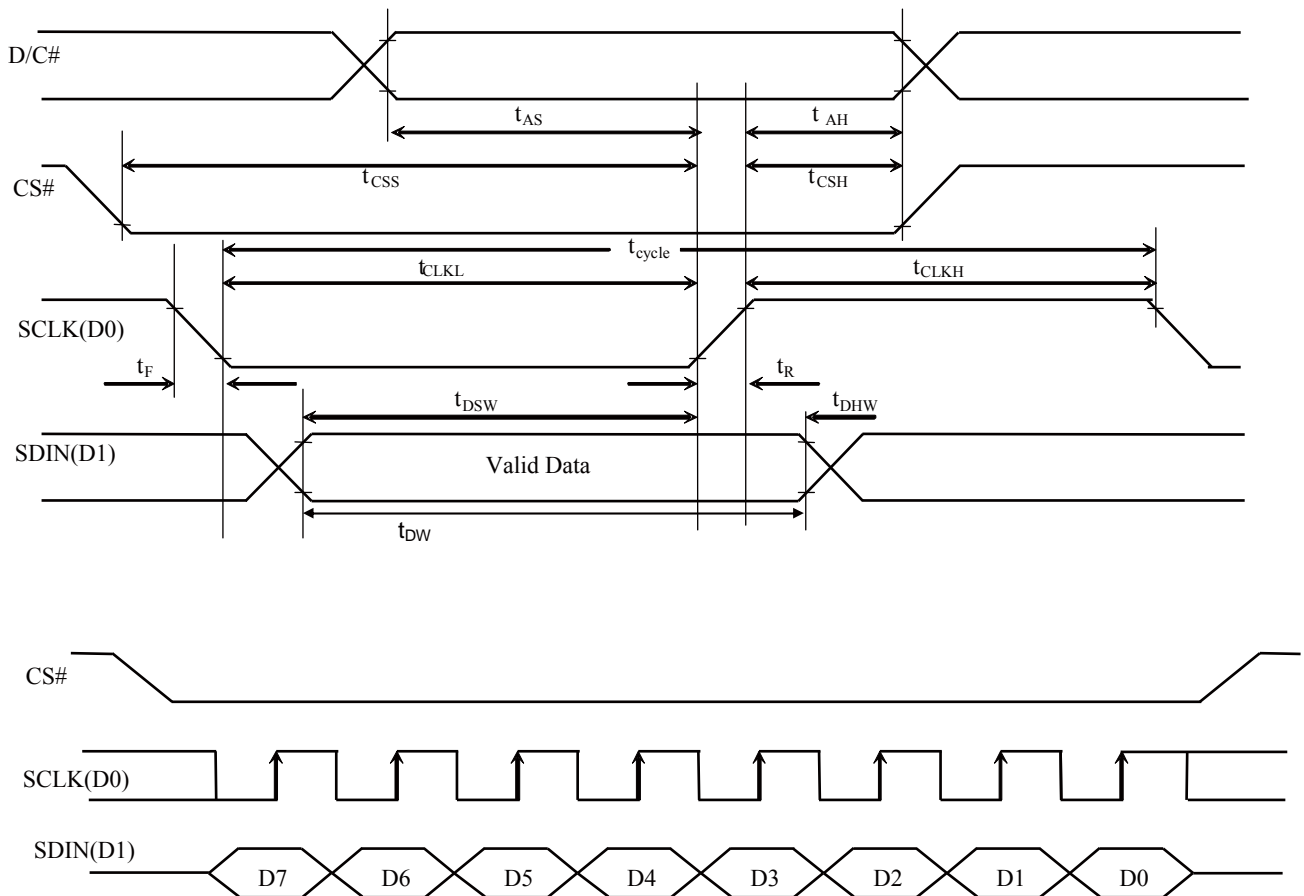


### 3. Serial Interface

$V_{DD}=1.65V$  to  $3.3V$  ( $T_a = 25^\circ C$ )

Symbol	Parameter	Min	Typ	Max	Unit
$t_{cycle}$	Clock Cycle Time	100	-	-	ns
$t_{AS}$	Address Setup Time	15	-	-	ns
$t_{AH}$	Address Hold Time	15	-	-	ns
$t_{CSS}$	Chip Select Setup Time	20	-	-	ns
$t_{CSH}$	Chip Select Hold Time	50	-	-	ns
$t_{DW}$	Data Write Time	55	-	-	ns
$t_{DSW}$	Write Data Setup Time	15	-	-	ns
$t_{DHW}$	Write Data Hold Time	15	-	-	ns
$t_{CLKL}$	Clock Low Time	50	-	-	ns
$t_{CLKH}$	Clock High Time	50	-	-	ns
$t_R$	Rise Time	-	-	40	ns
$t_F$	Fall Time	-	-	40	ns

Serial interface characteristics (4-wire SPI)

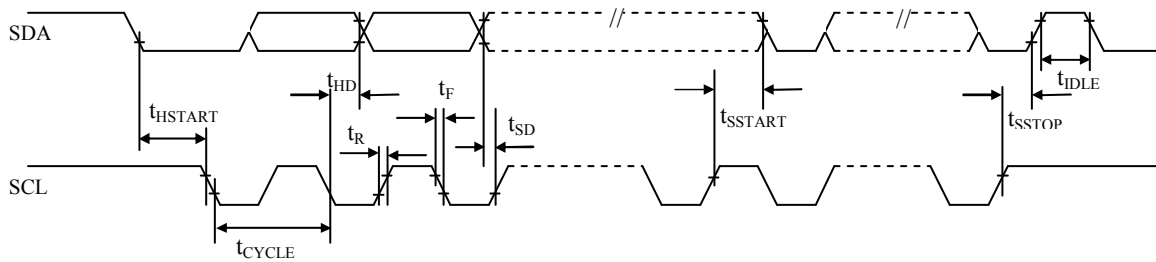


### 4. IIC Interface

$V_{DD}=1.65V$  to  $3.3V$  (  $T_a = 25^{\circ}C$  )

Symbol	Parameter	Min	Typ	Max	Unit
$t_{cycle}$	Clock Cycle Time	2.5	-	-	us
$t_{HSTART}$	Start condition Hold Time	0.6	-	-	us
$t_{HD}$	Data Hold Time (for "SDA <sub>OUT</sub> " pin)	0	-	-	ns
	Data Hold Time (for "SDA <sub>IN</sub> " pin)	300	-	-	ns
$t_{SD}$	Data Setup Time	100	-	-	ns
$t_{SSTART}$	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
$t_{SSTOP}$	Stop condition Setup Time	0.6	-	-	us
$t_R$	Rise Time for data and clock pin	-	-	300	ns
$t_F$	Fall Time for data and clock pin	-	-	300	ns
$t_{IDLE}$	Idle Time before a new transmission can start	1.3	-	-	us

IIC interface Timing characteristics

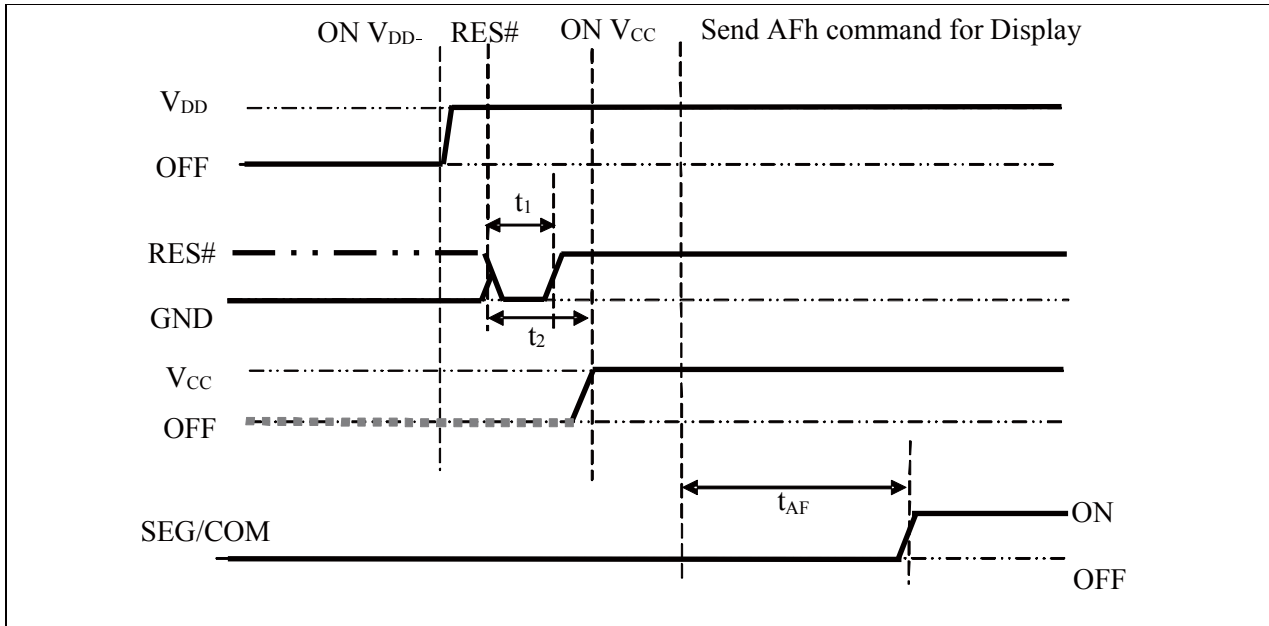


## ■ TIMING OF POWER SUPPLY

*Power ON sequence:*

1. Power ON  $V_{DD}$
2. After  $V_{DD}$  become stable, set RES# pin LOW (logic low) for at least 3us ( $t_1$ )<sup>(3)</sup> and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 3us ( $t_2$ ). Then Power ON  $V_{CC}$ .<sup>(1)</sup>
4. After  $V_{CC}$  become stable, send command AFh for display ON. SEG/COM will be ON after 100ms ( $t_{AF}$ ).

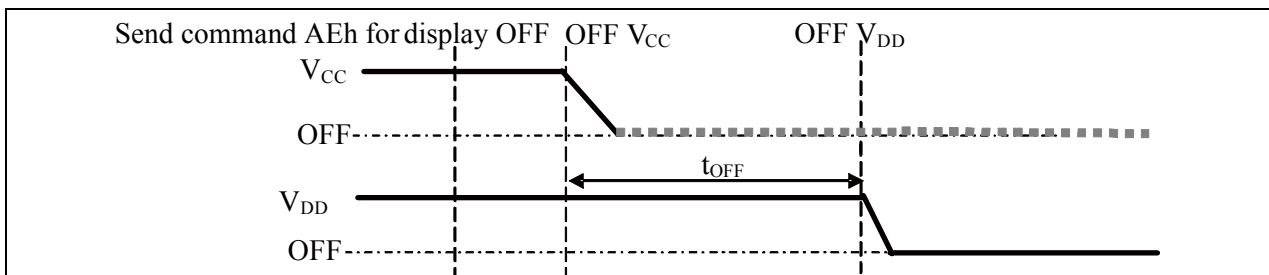
**The Power ON sequence**



*Power OFF sequence:*

1. Send command AEh for display OFF.
2. Power OFF  $V_{CC}$ .<sup>(1),(2)</sup>
3. Power OFF  $V_{DD}$  after  $t_{OFF}$ .<sup>(4)</sup> (where Minimum  $t_{OFF}=0ms$ , typical  $t_{OFF}=100ms$ )

**The Power OFF sequence**



**Note:**

- <sup>(1)</sup>  $V_{CC}$  should be kept float (i.e. disable) when it is OFF.
- <sup>(2)</sup> Power Pins ( $V_{DD}$ ,  $V_{CC}$ ) can never be pulled to ground under any circumstance.
- <sup>(3)</sup> The register values are reset after  $t_1$ .
- <sup>(4)</sup>  $V_{DD}$  should not be Power OFF before  $V_{CC}$  Power OFF.

**■ ELECTRO-OPTICAL CHARACTERISTICS (Ta=25°C)**

Items		Symbol	Min.	Typ.	Max.	Unit	Remark
Operating Luminance		L	50	60*	-	cd /m <sup>2</sup>	Red
Power Consumption		P	-	80	95	mW	30% pixels ON L= 60 cd/m <sup>2</sup>
Frame Frequency		Fr	-	100	-	Hz	-
Color Coordinate	Red	CIE x	0.63	0.67	0.71	CIE1931	Darkroom
		CIE y	0.29	0.33	0.37		
Response Time	Rise	Tr	-	-	0.02	ms	-
	Decay	Td	-	-	0.02	ms	-
Contrast Ratio*		Cr	10000:1	-	-	-	Darkroom
Viewing Angle Range		△θ	160	-	-	Degree	-
Operating Life Time*		Top	35,000	-	-	Hours	L= 60 cd/m <sup>2</sup>

**Note:**

1. 60cd/m<sup>2</sup> is base on V<sub>DD</sub>=3.0V, V<sub>CC</sub>=13.0V, contrast command setting **0x3F**;

2. **Contrast ratio** is defined as follows:

$$\text{Contrast ratio} = \frac{\text{Photo - detector output with OLED being "white"}}{\text{Photo - detector output with OLED being "black"}}$$

3. **Life Time** is defined when the Luminance has decayed to less than 50% of the initial Luminance specification. (Odd and even chess board alternately displayed), (The initial value should be closed to the typical value after adjusting.).

**■ INTERFACE PIN CONNECTIONS**

No	Symbol	Description
1	NC	No connection
2	VSS	Ground
3	VSS	Ground
4	NC	No connection
5	VDD	Voltage supply for core logic and interface logic.
6	BS1	MCU bus interface selection pins.Please refer to table followed for details of setting.
7	BS2	MCU bus interface selection pins.Please refer to table followed for details of setting.
8	CS#	The chip select pin. Active low.
9	RES#	This pin is reset signal input. When the pin is LOW, initialization of the chip is executed.Keep this pin HIGH (i.e. connect to VDD) during normal operation.
10	D/C#	Data/Command data control pin.Low for command while high for data.
11	WR#	This is read / write control input pin connecting to the MCU interface. When interfacing to a 6800-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH and write mode when LOW. When 8080 interface mode, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected. When serial interface, this pin must be connected to VSS.
12	RD#	When interfacing to a 6800-series microprocessor, this pin will be used as the Enable (E)signal. Read/write operation is initiated when this pin is pulled HIGH and the chip is selected. When connecting to an 8080-microprocessor, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected. Serial interface, this pin must be connected to VSS.
13-20	D0-D7	These are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial interface mode is selected, D0 will be the serial clock input: SCLK; D1 will be the serial data input: SDIN and D2 should be left opened. When I2C mode is selected, D2, D1 should be tied together and serve as SDAout, SDAin in application and D0 is the serial clock input, SCL.
21	IREF	This is segment output current reference pin.A resistor should be connected between this pin and VSS to maintain the IREF current at 10uA.
22	VCOMH	The pin for COM signal deselected voltage level.A capacitor should be connected between this pin and VSS.
23	VCC	Power supply for panel driving voltage.
24	NC	No connection

**MCU Bus Interface Pin Selection**

Pin Name	6800- parallel interface	8080- parallel Interface	4-SPI Interface	IIC Interface
BS1	0	1	0	1
BS2	1	1	0	0

**Note:**

- 0 is connect to VSS
- 1 is connect to VDD

■ **COMMAND TABLE**

(D/C#=0, R/W#(WR#) = 0, E(RD#=1) unless specific setting is stated)

1. Fundamental Command Table											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0	81 A[7:0]	1 A <sub>7</sub>	0 A <sub>6</sub>	0 A <sub>5</sub>	0 A <sub>4</sub>	0 A <sub>3</sub>	0 A <sub>2</sub>	0 A <sub>1</sub>	1 A <sub>0</sub>	Set Contrast Control	Double byte command to select 1 out of 256 contrast steps. Contrast increases as the value increases. (RESET = 7Fh)
0	A4/A5	1	0	1	0	0	1	0	X <sub>0</sub>	Entire Display ON	A4h, X <sub>0</sub> =0b: Resume to RAM content display (RESET) Output follows RAM content  A5h, X <sub>0</sub> =1b: Entire display ON Output ignores RAM content
0	A6/A7	1	0	1	0	0	1	1	X <sub>0</sub>	Set Normal/Inverse Display	A6h, X[0]=0b: Normal display (RESET) 0 in RAM: OFF in display panel 1 in RAM: ON in display panel  A7h, X[0]=1b: Inverse display 0 in RAM: ON in display panel 1 in RAM: OFF in display panel
0	AE/AF	1	0	1	0	1	1	1	X <sub>0</sub>	Set Display ON/OFF	AEh, X[0]=0b: Display OFF (sleep mode) (RESET) AFh X[0]=1b: Display ON in normal mode
0	E3	1	1	1	0	0	0	1	1	NOP	Command for no operation
0 0	FD A[2]	1 0	1 0	1 0	1 1	1 0	1 A <sub>2</sub>	0 1	1 0	Set Command Lock	A[2]: MCU protection status.  A[2] = 0b, Unlock OLED driver IC MCU interface from entering command (RESET) A[2] = 1b, Lock OLED driver IC MCU interface from entering command  <b>Note</b> <sup>(1)</sup> The locked OLED driver IC MCU interface prohibits all commands and memory access except the FDh command

**2. Scrolling Command Table**

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description									
0	2C/2D	0	0	1	0	1	1	0	X <sub>0</sub>	Content Scroll Setup	2Ch, X[0]=0, Right Horizontal Scroll by one column									
0	A[7:0]	0	0	0	0	0	0	0	0											
0	B[2:0]	*	*	*	*	*	B <sub>2</sub>	B <sub>1</sub>	B <sub>0</sub>		2Dh, X[0]=1, Left Horizontal Scroll by one column									
0	C[7:0]	0	0	0	0	0	0	0	1											
0	D[2:0]	*	*	*	*	*	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>		A[7:0] : Dummy byte (Set as 00h) Horizontal scroll by 1 column									
0	E[7:0]	0	0	0	0	0	0	0	0											
0	F[7:0]	F <sub>7</sub>	F <sub>6</sub>	F <sub>5</sub>	F <sub>4</sub>	F <sub>3</sub>	F <sub>2</sub>	F <sub>1</sub>	F <sub>0</sub>											
0	G[7:0]	G <sub>7</sub>	G <sub>6</sub>	G <sub>5</sub>	G <sub>4</sub>	G <sub>3</sub>	G <sub>2</sub>	G <sub>1</sub>	G <sub>0</sub>											
											B[2:0] : Define start page address <table border="1"> <tr> <td>000b – PAGE0</td> <td>011b – PAGE3</td> <td>110b – PAGE6</td> </tr> <tr> <td>001b – PAGE1</td> <td>100b – PAGE4</td> <td>111b – PAGE7</td> </tr> <tr> <td>010b – PAGE2</td> <td>101b – PAGE5</td> <td></td> </tr> </table>	000b – PAGE0	011b – PAGE3	110b – PAGE6	001b – PAGE1	100b – PAGE4	111b – PAGE7	010b – PAGE2	101b – PAGE5	
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010b – PAGE2	101b – PAGE5																			
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											D[2:0] : Define end page address <table border="1"> <tr> <td>000b – PAGE0</td> <td>011b – PAGE3</td> <td>110b – PAGE6</td> </tr> <tr> <td>001b – PAGE1</td> <td>100b – PAGE4</td> <td>111b – PAGE7</td> </tr> <tr> <td>010b – PAGE2</td> <td>101b – PAGE5</td> <td></td> </tr> </table>	000b – PAGE0	011b – PAGE3	110b – PAGE6	001b – PAGE1	100b – PAGE4	111b – PAGE7	010b – PAGE2	101b – PAGE5	
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001b – PAGE1	100b – PAGE4	111b – PAGE7																		
010b – PAGE2	101b – PAGE5																			
											E[7:0] : Dummy byte (Set as 00h)									
											F[7:0] : Define the start column (RESET = 00h)									
											G[7:0] : Define the end column address (RESET = 7Fh)									
											<b>Note</b> (1) The value of D[2:0] must be larger than or equal to B[2:0] (2) The value of G[7:0] must be larger than F[7:0] (3) A delay time of $2/FrameFreq$ must be set if sending the command of 2Ch / 2Dh consecutively.									

3. Addressing Setting Command Table											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	00~0F	0	0	0	0	X <sub>3</sub>	X <sub>2</sub>	X <sub>1</sub>	X <sub>0</sub>	Set Lower Column Start Address for Page Addressing Mode	Set the lower nibble of the column start address register for Page Addressing Mode using X[3:0] as data bits. The initial display line register is reset to 0000b after RESET.  <b>Note</b> (1) This command is only for page addressing mode
0	10~1F	0	0	0	1	X <sub>3</sub>	X <sub>2</sub>	X <sub>1</sub>	X <sub>0</sub>	Set Higher Column Start Address for Page Addressing Mode	Set the higher nibble of the column start address register for Page Addressing Mode using X[3:0] as data bits. The initial display line register is reset to 0000b after RESET.  <b>Note</b> (1) This command is only for page addressing mode
0 0	20 A[1:0]	0 *	0 *	1 *	0 *	0 *	0 *	0 A <sub>1</sub>	0 A <sub>0</sub>	Set Memory Addressing Mode	A[1:0] = 00b, Horizontal Addressing Mode A[1:0] = 01b, Vertical Addressing Mode A[1:0] = 10b, Page Addressing Mode (RESET) A[1:0] = 11b, Invalid
0 0 0	21 A[7:0] B[7:0]	0 A <sub>7</sub> B <sub>7</sub>	0 A <sub>6</sub> B <sub>6</sub>	1 A <sub>5</sub> B <sub>5</sub>	0 A <sub>4</sub> B <sub>4</sub>	0 A <sub>3</sub> B <sub>3</sub>	0 A <sub>2</sub> B <sub>2</sub>	0 A <sub>1</sub> B <sub>1</sub>	1 A <sub>0</sub> B <sub>0</sub>	Set Column Address	Setup column start and end address A[7:0] : Column start address, range : 0-127d, (RESET=0d)  B[7:0]: Column end address, range : 0-127d, (RESET =127d)  <b>Note</b> (1) This command is only for horizontal or vertical addressing mode.
0 0 0	22 A[2:0] B[2:0]	0 * *	0 * *	1 * *	0 * *	0 * *	0 A <sub>2</sub> B <sub>2</sub>	1 A <sub>1</sub> B <sub>1</sub>	0 A <sub>0</sub> B <sub>0</sub>	Set Page Address	Setup page start and end address A[2:0] : Page start Address, range : 0-7d, (RESET = 0d)  B[2:0] : Page end Address, range : 0-7d, (RESET = 7d)  <b>Note</b> (1) This command is only for horizontal or vertical addressing mode.
0	B0~B7	1	0	1	1	0	X <sub>2</sub>	X <sub>1</sub>	X <sub>0</sub>	Set Page Start Address for Page Addressing Mode	Set GDDRAM Page Start Address (PAGE0~PAGE7) for Page Addressing Mode using X[2:0].  <b>Note</b> (1) This command is only for page addressing mode



4. Hardware Configuration (Panel resolution & layout related) Command Table											
D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	40~7F	0	1	X <sub>5</sub>	X <sub>4</sub>	X <sub>3</sub>	X <sub>2</sub>	X <sub>1</sub>	X <sub>0</sub>	Set Display Start Line	Set display RAM display start line register from 0-63 using X <sub>5</sub> X <sub>3</sub> X <sub>2</sub> X <sub>1</sub> X <sub>0</sub> . Display start line register is reset to 000000b during RESET.
0	A0/A1	1	0	1	0	0	0	0	X <sub>0</sub>	Set Segment Re-map	A0h, X[0]=0b: column address 0 is mapped to SEG0 (RESET)  A1h, X[0]=1b: column address 127 is mapped to SEG0
0	A8	1	0	1	0	1	0	0	0	Set Multiplex Ratio	Set MUX ratio to N+1 MUX  N=A[5:0] : from 16MUX to 64MUX, RESET= 11111b (i.e. 63d, 64MUX) A[5:0] from 0 to 14 are invalid entry.
0	C0/C8	1	1	0	0	X <sub>3</sub>	0	0	0	Set COM Output Scan Direction	C0h, X[3]=0b: normal mode (RESET) Scan from COM0 to COM[N-1]  C8h, X[3]=1b: remapped mode. Scan from COM[N-1] to COM0  Where N is the Multiplex ratio.
0	D3	1	1	0	1	0	0	1	1	Set Display Offset	Set vertical shift by COM from 0d~63d The value is reset to 00h after RESET.
0	DA	1	1	0	1	1	0	1	0	Set COM Pins Hardware Configuration	A[4]=0b, Sequential COM pin configuration A[4]=1b (RESET), Alternative COM pin configuration  A[5]=0b (RESET), Disable COM Left/Right remap A[5]=1b, Enable COM Left/Right remap

5. Timing & Driving Scheme Setting Command Table																							
00	D5 A[7:0]	1 A <sub>7</sub>	1 A <sub>6</sub>	0 A <sub>5</sub>	1 A <sub>4</sub>	0 A <sub>3</sub>	1 A <sub>2</sub>	0 A <sub>1</sub>	1 A <sub>0</sub>	Set Display Clock Divide Ratio/Oscillator Frequency	<p>A[3:0] : Define the divide ratio (D) of the display clocks (DCLK): Divide ratio= A[3:0] + 1, RESET is 0000b (divide ratio = 1)</p> <p>A[7:4] : Set the Oscillator Frequency, F<sub>OSC</sub>. Oscillator Frequency increases with the value of A[7:4] and vice versa. RESET is 1000b</p> <p>Range:0000b~1111b Frequency increases as setting value increases.</p>												
00	D9 A[7:0]	1 A <sub>7</sub>	1 A <sub>6</sub>	0 A <sub>5</sub>	1 A <sub>4</sub>	1 A <sub>3</sub>	0 A <sub>2</sub>	0 A <sub>1</sub>	1 A <sub>0</sub>	Set Pre-charge Period	<p>A[3:0] : Phase 1 period of up to 15 DCLK Clock 0 is invalid entry (RESET=2h)</p> <p>A[7:4] : Phase 2 period of up to 15 DCLK Clock 0 is invalid entry (RESET=2h)</p>												
00	DB A[5:2]	1 0	1 0	0 A <sub>5</sub>	1 A <sub>4</sub>	1 A <sub>3</sub>	0 A <sub>2</sub>	1 0	1 0	Set V <sub>COMH</sub> Deselect Level	<table border="1"> <thead> <tr> <th>A[5:2]</th> <th>Hex code</th> <th>V<sub>COMH</sub> deselect level</th> </tr> </thead> <tbody> <tr> <td>0000b</td> <td>00h</td> <td>~ 0.64 x V<sub>CC</sub></td> </tr> <tr> <td>1101b</td> <td>34h</td> <td>~ 0.78 x V<sub>CC</sub> (RESET)</td> </tr> <tr> <td>1111b</td> <td>3Ch</td> <td>~ 0.84 x V<sub>CC</sub></td> </tr> </tbody> </table>	A[5:2]	Hex code	V <sub>COMH</sub> deselect level	0000b	00h	~ 0.64 x V <sub>CC</sub>	1101b	34h	~ 0.78 x V <sub>CC</sub> (RESET)	1111b	3Ch	~ 0.84 x V <sub>CC</sub>
A[5:2]	Hex code	V <sub>COMH</sub> deselect level																					
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1101b	34h	~ 0.78 x V <sub>CC</sub> (RESET)																					
1111b	3Ch	~ 0.84 x V <sub>CC</sub>																					

**■ INITIALIZATION CODE**

```
void InitOLED_MASTER_SSD1309Z(void)
{
    MainOLED_WCom(0xFD);           // SET COMMAND LOCK
    MainOLED_WCom(0x12);
    MainOLED_WCom(0xAE);          //DOT MARTIX DISPLAY OFF
    MainOLED_WCom(0x81);          //CONTARST CONTROL(00H-0FFH)
    MainOLED_WCom(0xA4);          //ENTIRE DISPLAY OFF(0A4H-0A5H)
    MainOLED_WCom(0xA6);          //SET NORMAL DISPLAY(0A6H-0A7H)

    MainOLED_WCom(0x00);          // SET LOW COLUMN START ADDRESS
    MainOLED_WCom(0x10);          //SET HIGH COLUMN START ADDRESS
    MainOLED_WCom(0x20);          //SET MEMORRY ADDRESSING MODE
    MainOLED_WCom(0x02);          //PAGE ADDRESSING MODE (RESET)
    MainOLED_WCom(0xB0);

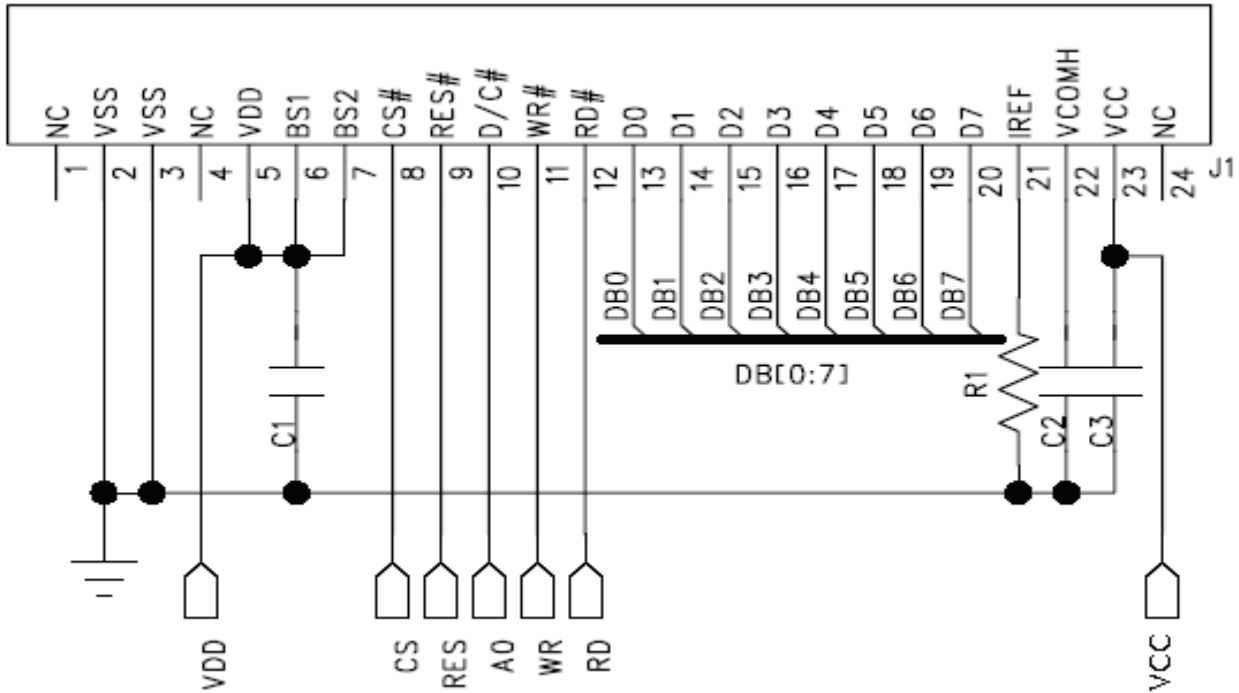
    MainOLED_WCom(0x40);          //SET DISPLAY STRART LINE (040H-07FH)
    MainOLED_WCom(0xA1);          //SET SEGMENT RE-MAP(0A0H-0A1H)
    MainOLED_WCom(0xA8);          //SET MULTIPLEX RATIO 64
    MainOLED_WCom(0x3F);
    MainOLED_WCom(0xC8);          //COM SCAN COM1-COM64(0C8H,0C0H)

    MainOLED_WCom(0xD3);          //SET DISPLAY OFFSET
    MainOLED_WCom(0x00);
    MainOLED_WCom(0xDA);          //COM PIN CONFIGURATION
    MainOLED_WCom(0x12);
    MainOLED_WCom(0xD5);          //SET FRAME FREQUENCY
    MainOLED_WCom(0x80);
    MainOLED_WCom(0xD9);          //SET PRE_CHARGE PERIOD
    MainOLED_WCom(0xA2);
    MainOLED_WCom(0xDB);          //SET VCOM DESELECT LEVEL
    MainOLED_WCom(0x34);

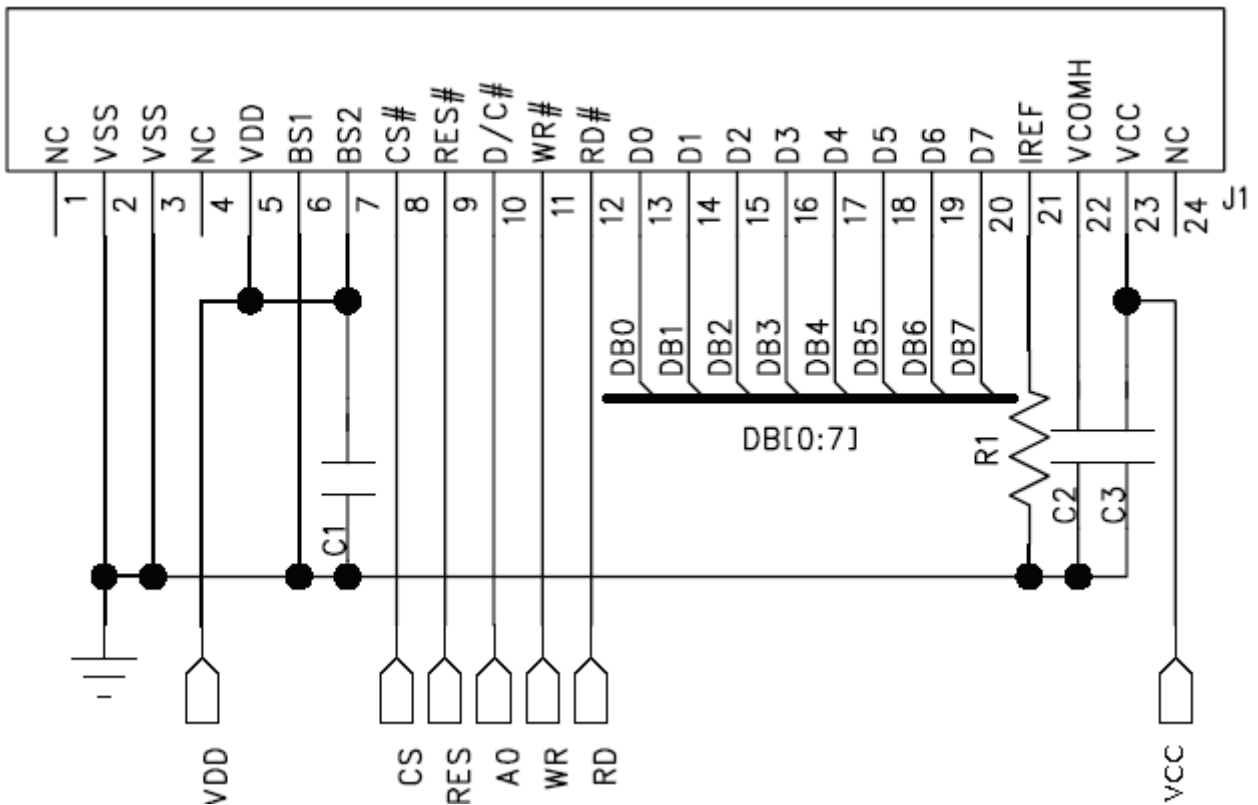
    MainOLED_WCom(0xAF);          //DSPLAY ON
}
```

■ SCHEMATIC EXAMPLE

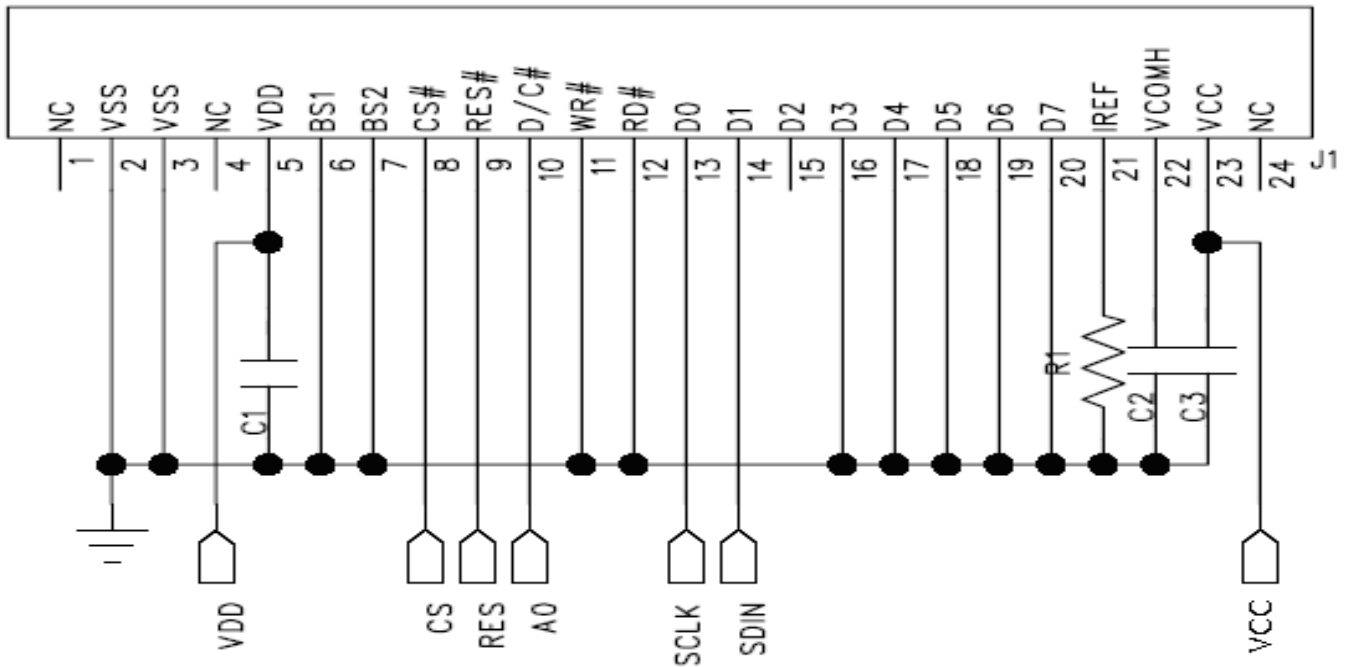
◆ 8080 Series Interface Application Circuit:



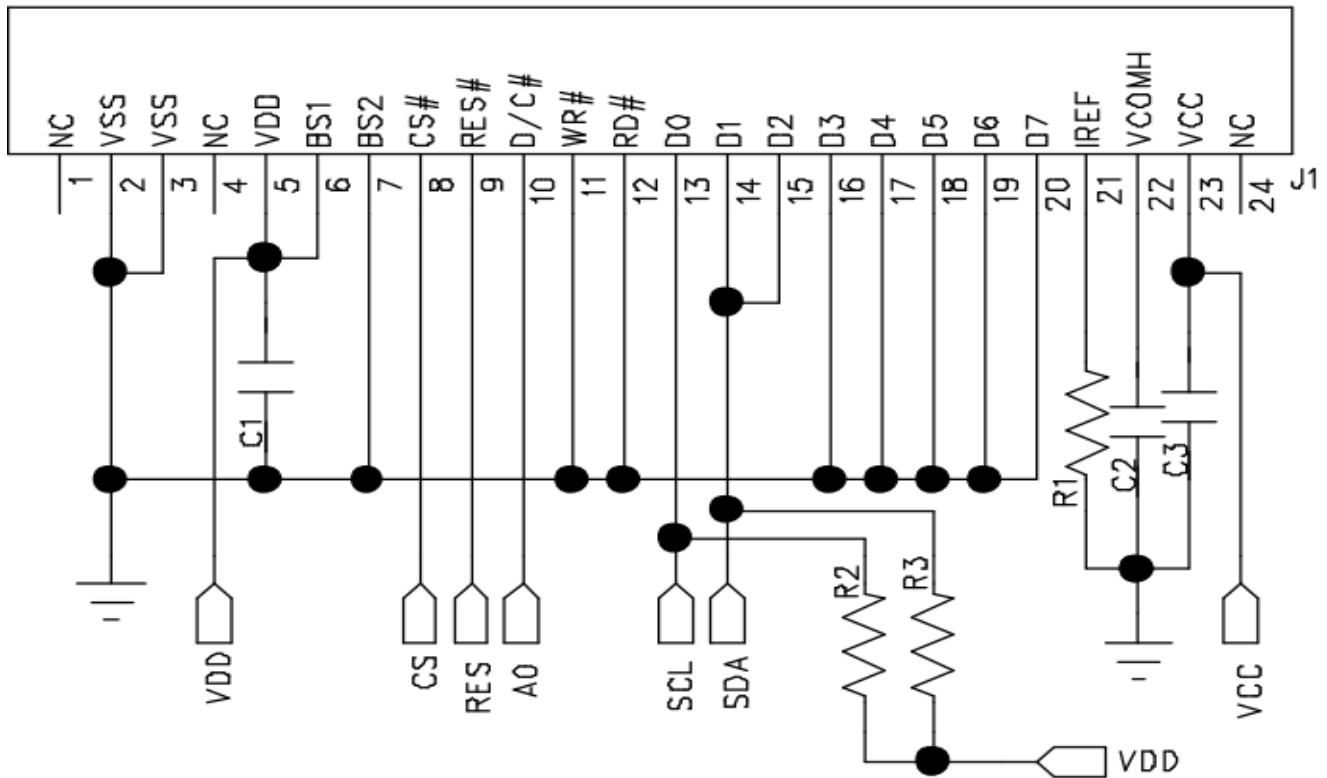
◆ 6800 Series Interface Application Circuit:



◆4-SPI Interface Application Circuit:



◆IIC Interface Application Circuit:



NOTE:

1.  $R1=(V_{CC}-3)V/10\mu A=(13.0-3.0)V/10\mu A\approx 1M\Omega$ ;  $R2=R3=10K$ ;  $C1=1.0UF$   $C2=C3=2.2UF$ 。
2. The  $V_{CC}$  should connect an external voltage.
3. The capacitors and the resistors value are recommended value. Select the appropriate value against module application.

**■ RELIABILITY TESTS**

Item		Condition	Criterion
High Temperature Storage (HTS)		80±2℃, 200 hours	1. After testing, the function test is ok. 2. After testing, no addition to the defect. 3. After testing, the change of luminance should be within +/- 50% of initial value. 4. After testing, the change for the mono and area color must be within (+/-0.02, +/- 0.02) and for the full color it must be within (+/-0.04, +/-0.04) of initial value based on 1931 CIE coordinates. 5. After testing, the change of total current consumption should be within +/- 50% of initial value.
High Temperature Operating (HTO)		70±2℃, 96 hours	
Low Temperature Storage (LTS)		-30±2℃, 200 hours	
Low Temperature Operating (LTO)		-20±2℃, 96 hours	
High Temperature / High Humidity Storage (HTHHS)		50±3℃, 90%±3%RH, 120 hours	
Thermal Shock (Non-operation) (TS)		-20±2℃ ~ 25℃ ~ 70±2℃ (30min) (5min) (30min) 10cycles	
Vibration (Packing)	10~55~10Hz, amplitude 1.5mm, 1 hour for each direction x, y, z	1. One box for each test. 2. No addition to the cosmetic and the electrical defects.	
Drop (Packing)	Height : 1 m, each time for 6 sides, 3 edges, 1 angle		
ESD (finished product housing)	±4kV (R: 330Ω C: 150pF, 10times, air discharge)	1. After testing, cosmetic and electrical defects should not happen. 2. In case of malfunction or defect caused by ESD damage, it would be judged as a good part if it would be recovered to normal state after resetting.	

- Note: 1) For each reliability test, the sample quantity is 3, and only for one test item.  
 2) The HTHHS test is requested the Pure Water(Resistance>10MΩ).  
 3) The test should be done after 2 hours of recovery time in normal environment.

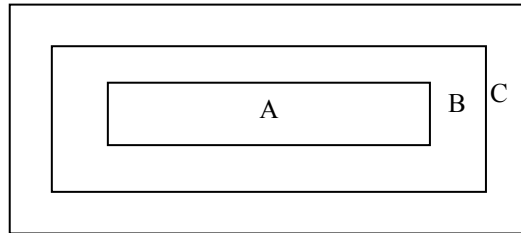
**■ OUTGOING QUALITY CONTROL SPECIFICATION**

**◆ Standard**

According to GB/T2828.1-2003/ISO 2859-1: 1999 and ANSI/ASQC Z1.4-1993, General Inspection Level II.

**◆ Definition**

- 1 Major defect : The defect that greatly affect the usability of product.
- 2 Minor defect : The other defects, such as cosmetic defects, etc.
- 3 Definition of inspection zone:



Zone A: Active Area

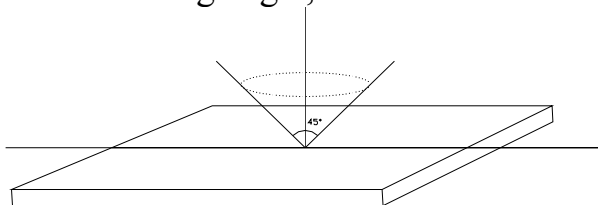
Zone B: Viewing Area except Zone A

Zone C: Outside Viewing Area

Note: As a general rule, visual defects in Zone C are permissible, when it is no trouble of quality and assembly to customer`s product.

**◆ Inspection Methods**

- 1 The general inspection : under 20W x 2 or 40W fluorescent light, about 30cm viewing distance, within 45° viewing angle, under 25±5°C.



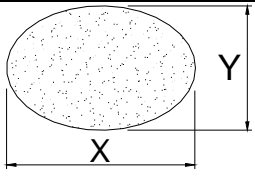
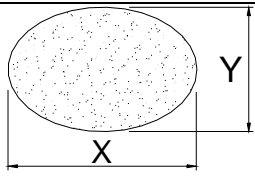
- 2 The luminance and color coordinate inspection : By PR705 or BM-7 or the equal equipments, in the dark room, under 25±5°C.

**◆ Inspection Criteria**

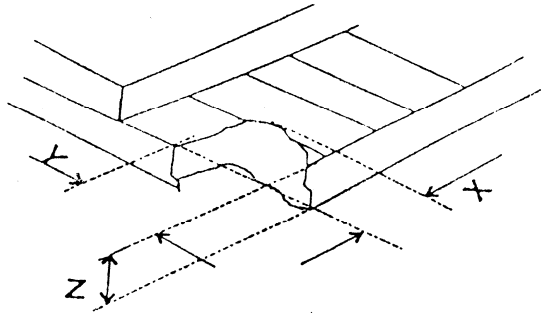
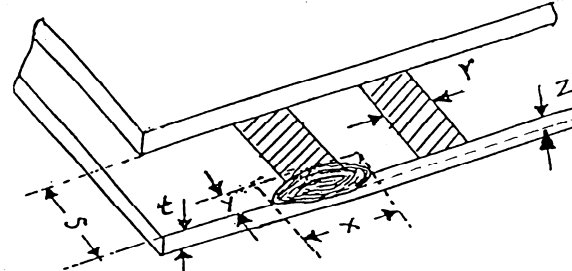
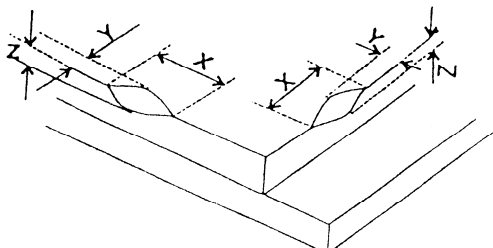
- 1 Major defect : AQL= 0.65

Item	Criterion
Function Defect	1. No display or abnormal display is not accepted
	2. Open or short is not accepted.
	3. Power consumption exceeding the spec is not accepted.
Outline Dimension	Outline dimension exceeding the spec is not accepted.
Glass Crack	Glass crack tends to enlarge is not accepted.

2 Minor Defect : AQL= 1.5

Item	Criterion			
Spot Defect (dimming and lighting spot)	Size (mm)		Accepted Qty	
			Area A + Area B	Area C
			Ignored	
			3	Ignored
			1	
Note : $\Phi = (x + y) / 2$		0		
Line Defect (dimming and lighting line)	L ( Length ) : mm	W ( Width ) : mm	Area A + Area B	Area C
	/	$W \leq 0.02$	Ignored	
	$L \leq 3.0$	$0.02 < W \leq 0.03$	2	Ignored
	$L \leq 2.0$	$0.03 < W \leq 0.05$	1	
	/	$0.05 < W$	As spot defect	
Remarks: The total of spot defect and line defect shall not exceed 4 pcs. The distance between two lines defects must exceed 1 mm				
Polarizer Stain	Stain which can be wiped off lightly with a soft cloth or similar cleaning is accepted, otherwise, according to the Spot Defect and the Line Defect.			
Polarizer Scratch	1. If scratch can be seen during operation, according to the criterions of the Spot Defect and the Line Defect.			
	2. If scratch can be seen only under non-operation or some special angle, the criterion is as below :			
	L ( Length ) : mm	W ( Width ) : mm	Area A + Area B	Area C
	/	$W \leq 0.02$	Ignore	
	$3.0 < L \leq 5.0$	$0.02 < W \leq 0.04$	2	Ignore
$L \leq 3.0$	$0.04 < W \leq 0.06$	1		
/	$0.06 < W$	0		
Polarizer Air Bubble	Size		Area A + Area B	Area C
			Ignored	
			2	Ignored
			1	
			0	



Glass Defect (Glass Chipped)	<p>1. On the corner</p>  <p>(mm)</p> <table border="1" data-bbox="1053 302 1420 470"> <tr> <td>x</td> <td><math>\leq 1.5</math></td> </tr> <tr> <td>y</td> <td><math>\leq 1.5</math></td> </tr> <tr> <td>z</td> <td><math>\leq t</math></td> </tr> </table>	x	$\leq 1.5$	y	$\leq 1.5$	z	$\leq t$
	x	$\leq 1.5$					
	y	$\leq 1.5$					
z	$\leq t$						
<p>2. On the bonding edge</p>  <p>(mm)</p> <table border="1" data-bbox="1053 761 1420 929"> <tr> <td>x</td> <td><math>\leq a / 4</math></td> </tr> <tr> <td>y</td> <td><math>\leq s / 3 \ \&amp;\leq 0.7</math></td> </tr> <tr> <td>z</td> <td><math>\leq t</math></td> </tr> </table>	x	$\leq a / 4$	y	$\leq s / 3 \ \&\leq 0.7$	z	$\leq t$	
x	$\leq a / 4$						
y	$\leq s / 3 \ \&\leq 0.7$						
z	$\leq t$						
<p>3. On the other edges</p>  <p>(mm)</p> <table border="1" data-bbox="1053 1187 1420 1355"> <tr> <td>x</td> <td><math>\leq a / 8</math></td> </tr> <tr> <td>y</td> <td><math>\leq 0.7</math></td> </tr> <tr> <td>z</td> <td><math>\leq t</math></td> </tr> </table>	x	$\leq a / 8$	y	$\leq 0.7$	z	$\leq t$	
x	$\leq a / 8$						
y	$\leq 0.7$						
z	$\leq t$						
<p>Note: t: glass thickness ; s: pad width ; a: the length of the edge</p>							
TCP Defect	Crack, deep fold and deep pressure mark on the TCP are not accepted						
Pixel Size	The tolerance of display pixel dimension should be within $\pm 20\%$ of the spec						
Luminance	Refer to the spec or the reference sample						
Color	Refer to the spec or the reference sample						

**■ CAUTIONS IN USING OLED MODULE****◆ Precautions For Handling OLED Module:**

1. OLED module consists of glass and polarizer. Pay attention to the following items when handling:
  - i. Avoid drop from high, avoid excessive impact and pressure.
  - ii. Do not touch, push or rub the exposed polarizers with anything harder than an HB pencil lead.
  - iii. If the surface becomes dirty, breathe on the surface and gently wipe it off with a soft dry cloth. If it is terrible dirty, moisten the soft cloth with Isopropyl alcohol or Ethyl alcohol. Other solvents may damage the polarizer. Especially water, Ketone and Aromatic solvents.
  - iv. Wipe off saliva or water drops immediately, contact the polarizer with water over a long period of time may cause deformation.
  - v. Please keep the temperature within specified range for use and storage. Polarization degradation, bubble generation or polarizer peeling-off may occur with high temperature and high humidity.
  - vi. Condensation on the surface and the terminals due to cold or anything will damage, stain or dirty the polarizer, so make it clean as the way of iii.
2. Do not attempt to disassemble or process the OLED Module.
3. Make sure the TCP or the FPC of the Module is free of twisting, warping and distortion, do not pull or bend them forcefully, especially the soldering pins. On the other side, the SLIT part of the TCP is made to bend in the necessary case.
4. When assembling the module into other equipment, give the glass enough space to avoid excessive pressure on the glass, especially the glass cover which is much more fragile.
5. Be sure to keep the air pressure under 120 kPa, otherwise the glass cover is to be cracked.
6. Be careful to prevent damage by static electricity:
  - i. Be sure to ground the body when handling the OLED Modules.
  - ii. All machines and tools required for assembling, such as soldering irons, must be properly grounded.
  - iii. Do not assemble and do no other work under dry conditions to reduce the amount of static electricity generated. A relative humidity of 50%-60% is recommended.
  - iv. Peel off the protective film slowly to avoid the amount of static electricity generated.
  - v. Avoid to touch the circuit, the soldering pins and the IC on the Module by the body.
  - vi. Be sure to use anti-static package.
7. Contamination on terminals can cause an electrochemical reaction and corrode the terminal circuit, so make it clean anytime.
8. All terminals should be open, do not attach any conductor or semiconductor on the terminals.
9. When the logic circuit power is off, do not apply the input signals.
10. Power on sequence:  $V_{DD} \rightarrow V_{CC}$ , and power off sequence:  $V_{CC} \rightarrow V_{DD}$ .
11. Be sure to keep temperature, humidity and voltage within the ranges of the spec, otherwise shorten Module's life time, even make it damaged.
12. Be sure to drive the OLED Module following the Specification and datasheet of IC controller, otherwise something wrong may be seen.

13. When displaying images, keep them rolling, and avoid one fixed image displaying more than 30 seconds, otherwise the residue image is to be seen. This is the speciality of OLED.

#### ◆ **Precautions For Soldering OLED Module:**

1. Soldering temperature :  $260^{\circ}\text{C} \pm 10^{\circ}\text{C}$ .
2. Soldering time : 3-4 sec.
3. Repeating time : no more than 3 times.
4. If soldering flux is used, be sure to remove any remaining flux after finishing soldering operation. (This does not apply in the case of a non-halogen type of flux.) It is recommended to protect the surface with a cover during soldering to prevent any damage due to flux spatters.

#### ◆ **Precautions For Storing OLED Module:**

1. Be sure to store the OLED Module in the vacuum bag with dessicant.
2. If the Module can not be used up in 1 month after the bag being opened, make sure to seal the Module in the vacuum bag with dessicant again.
3. Store the Module in a dark place, do not expose to sunlight or fluorescent light.
4. The polarizer surface should not touch any other objects. It is recommended to store the Module in the shipping container.
5. It is recommended to keep the temperature between  $0^{\circ}\text{C}$  and  $30^{\circ}\text{C}$  , the relative humidity not over 60%.

#### ◆ **Limited Warranty**

Unless relevant quality agreements signed with customer and law enforcement, for a period of 12 months from date of production, all products (except automotive products) TRULY will replace or repair any of its OLED modules which are found to be functional defect when inspected in accordance with TRULY OLED acceptance standards (copies available upon request). Cosmetic/visual defects must be returned to TRULY within 90 days of shipment. Confirmation of such date should be based on freight documents. The warranty liability of TRULY is limited to repair and/or replacement on the terms above. TRULY will not be responsible for any subsequent or consequential events.

#### ◆ **Return OLED Module Under Warranty:**

1. No warranty in the case that the precautions are disregarded.
2. Module repairs will be invoiced to the customer upon mutual agreement. Modules must be returned with sufficient description of the failures or defects.

#### ◆ **PRIOR CONSULT MATTER**

1. For TRULY standard products , we keep the right to change material ,process ... for improving the product property without any notice on our customer.
2. If you have special requirement about reliability condition, please let us know before you start the test on our samples.