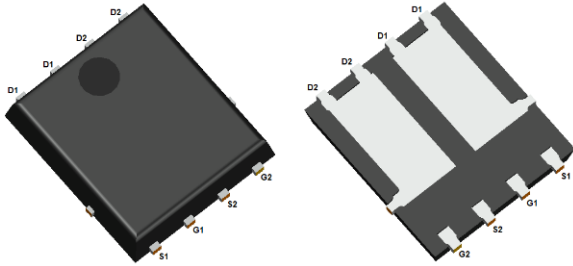


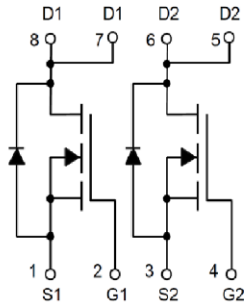
N-Channel Enhancement Mode Field Effect Transistor



Top View

Bottom View

PDFN5060-8L



Product Summary

- V_{DS} 60V
- I_D 22A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) $<33m\Omega$
- $R_{DS(ON)}$ (at $V_{GS}=4.5V$) $<55m\Omega$
- 100% EAS Tested
- 100% ∇V_{DS} Tested

General Description

- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Part no. with suffix "Q" means AEC-Q101 qualified

Applications

- Power switching application
- Uninterruptible power supply
- DC-DC convertor
- 12V and 24V Automotive systems

■ Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	60	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_A=25^\circ C$	I_D	4.4	A
	$T_A=100^\circ C$		3.1	
	$T_C=25^\circ C$		22	
	$T_C=100^\circ C$		15	
Pulsed Drain Current ^A		I_{DM}	88	A
Avalanche energy ^B		EAS	30	mJ
Total Power Dissipation ^C	$T_A=25^\circ C$	P_D	2.5	W
	$T_A=100^\circ C$		1.25	
	$T_C=25^\circ C$		62	
	$T_C=100^\circ C$		31	
Thermal Resistance Junction-to-Ambient ^D		$R_{\theta JA}$	60	$^\circ C/W$
Thermal Resistance Junction-to-Case		$R_{\theta JC}$	2.4	$^\circ C/W$
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+175	$^\circ C$

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJGD22N06AHQ	F1	YJGD22N06A	5000	10000	100000	13" reel



YJGD22N06AHQ

■ Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA	60			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =60V, V _{GS} =0V			1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	1.5	2	2.5	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =10V, I _D =20A		25	33	mΩ
		V _{GS} =4.5V, I _D =10A		38	55	mΩ
Diode Forward Voltage	V _{SD}	I _S =15A, V _{GS} =0V		0.85	1.2	V
Gate resistance	R _G	f=1MHz		1.7		Ω
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V, f=1MHz		940		pF
Output Capacitance	C _{oss}			100		
Reverse Transfer Capacitance	C _{riss}			73		
Switching Parameters						
Total Gate Charge	Q _g	VGS=10V, VDS=30V, ID=10A	-	17.2	-	nC
Gate-Source Charge	Q _{gs}		-	3.3	-	
Gate-Drain Charge	Q _{gd}		-	4.5	-	
Reverse Recovery Charge	Q _{rr}	IF=10A, di/dt=360A/us	-	50	-	nC
Reverse Recovery Time	t _{rr}		-	19.4	-	ns
Turn-on Delay Time	t _{D(on)}	VGS=10V, VDS=30V, ID=10A, Rg=2.2ohm	-	7.4	-	ns
Turn-on Rise Time	t _r		-	38.5	-	
Turn-off Delay Time	t _{D(off)}		-	19.3	-	
Turn-off fall Time	t _f		-	3	-	

A. Repetitive rating; pulse width limited by max. junction temperature.

B. T_J=25°C, V_{DD}=40V, V_G=10V, L=0.5mH, I_{AS}=11A.

C. P_q is based on max. junction temperature, using junction-case thermal resistance.

D. The value of R_{θJA} is measured with the device mounted on 1 in² FR-4 board with 2oz. Copper, in the still air environment with T_A=25°C. The maximum allowed junction temperature of 175°C. The value in any given application depends on the user's specific board design.



YJGD22N06AHQ

Typical Electrical and Thermal Characteristics Diagrams

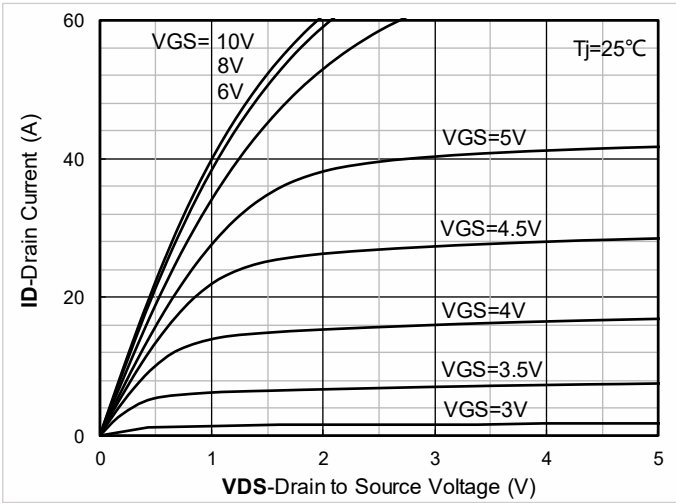


Figure 1. Output Characteristics

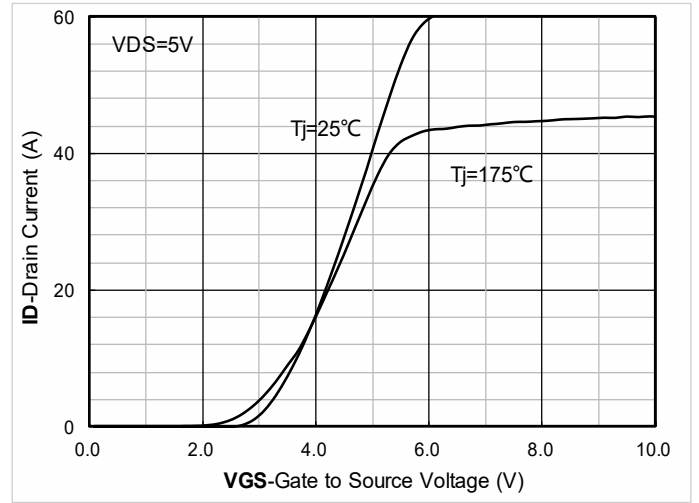


Figure 2. Transfer Characteristics

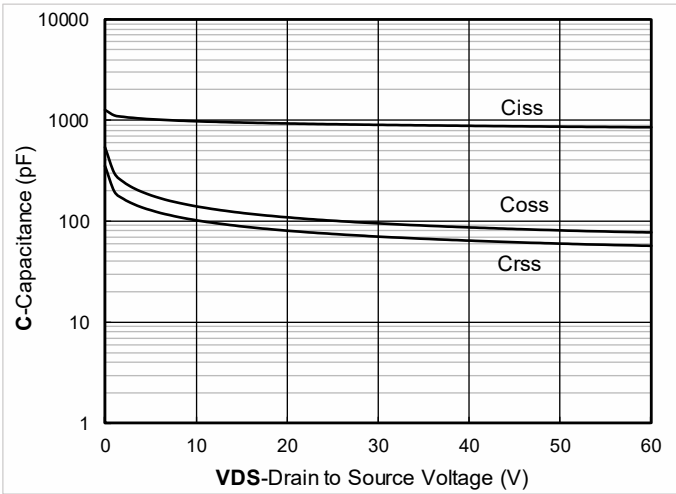


Figure 3. Capacitance Characteristics

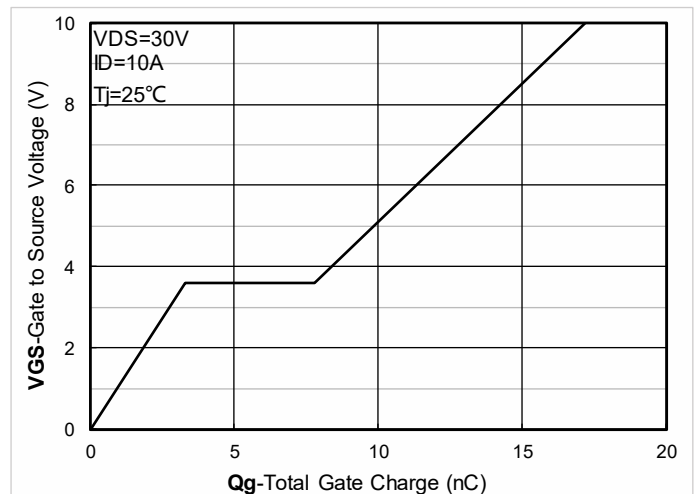


Figure 4. Gate Charge

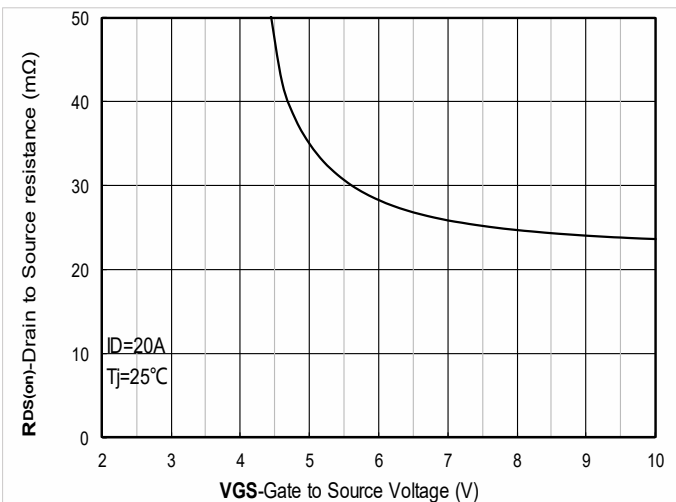


Figure 5. On-Resistance vs Gate to Source Voltage

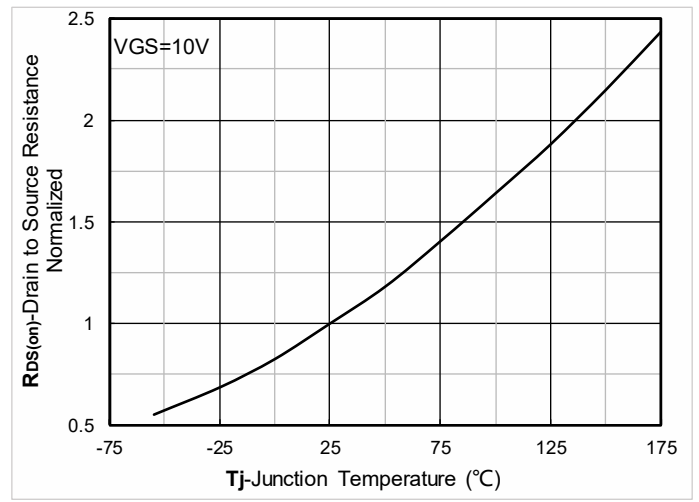


Figure 6. Normalized On-Resistance



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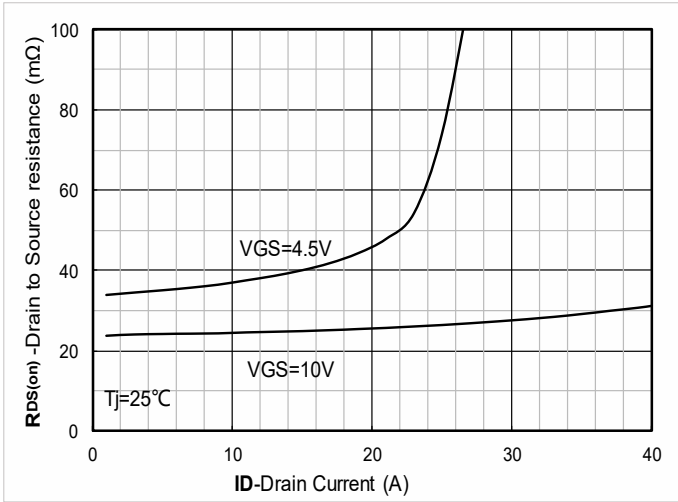


Figure 7. RDS(on) VS Drain Current

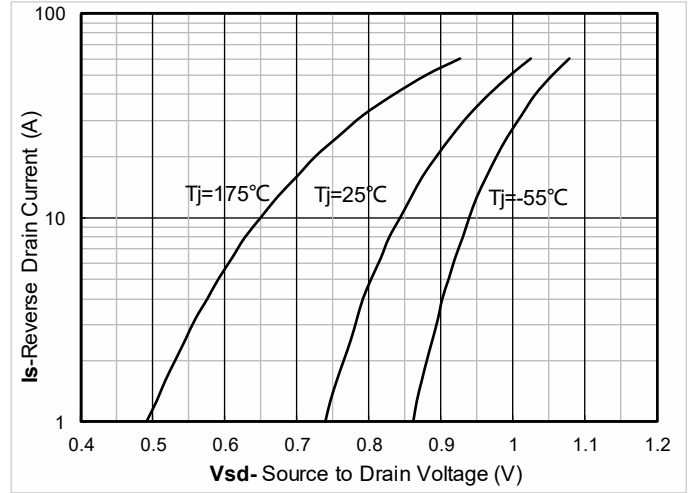


Figure 8. Forward characteristics of reverse diode

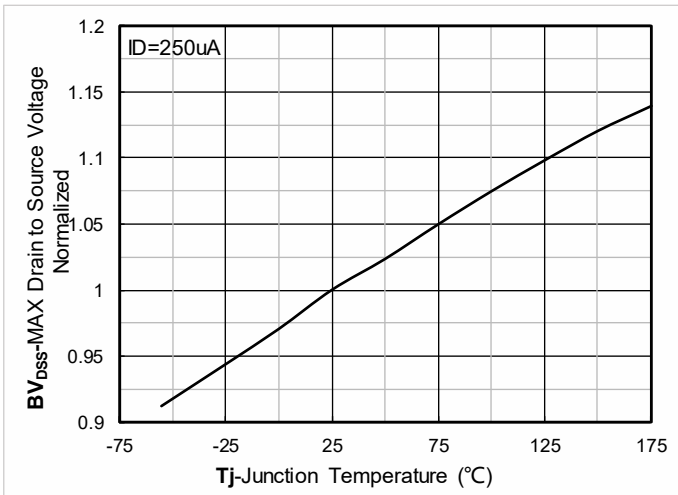


Figure 9. Normalized breakdown voltage

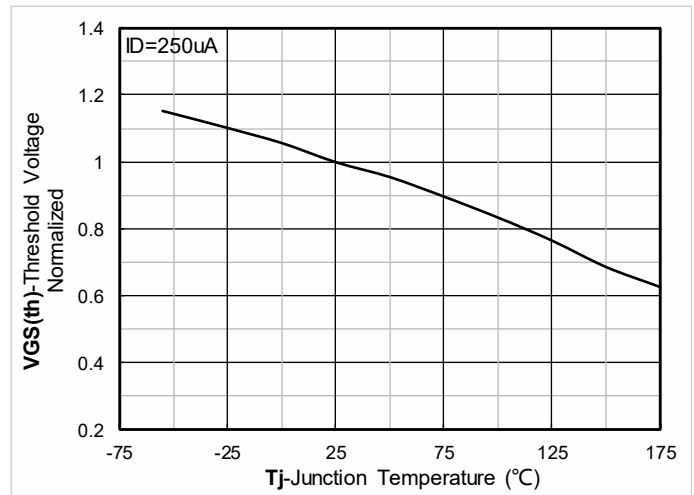


Figure 10. Normalized Threshold voltage

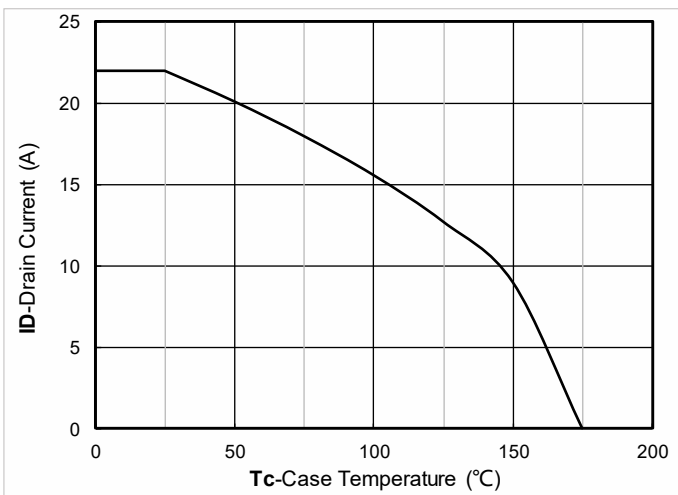


Figure 11. Current dissipation

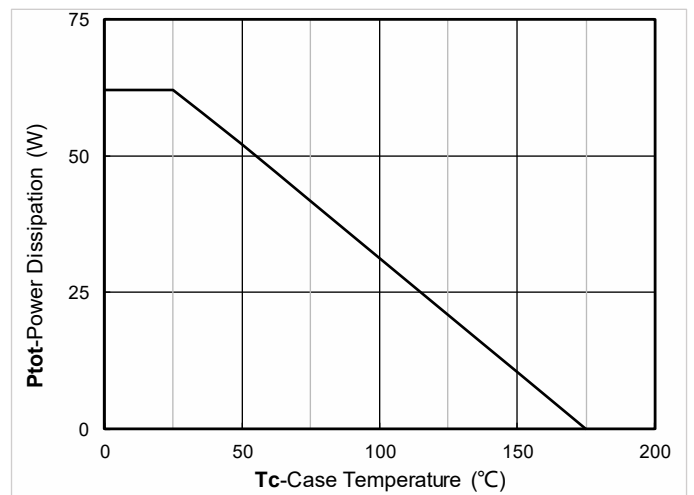


Figure 12. Power dissipation



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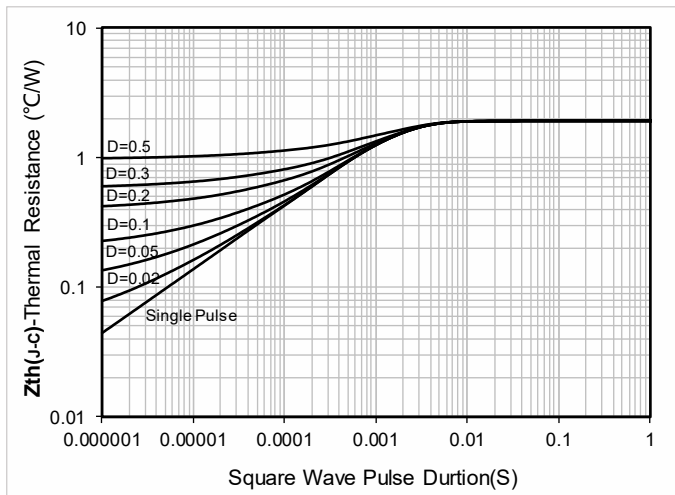


Figure 13. Maximum Transient Thermal Impedance

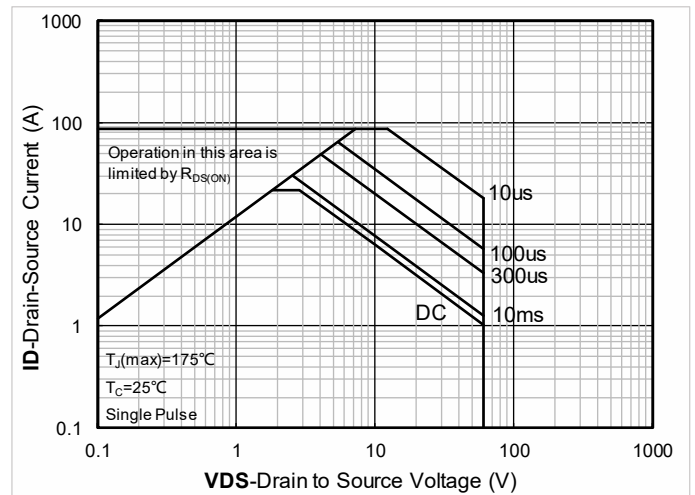
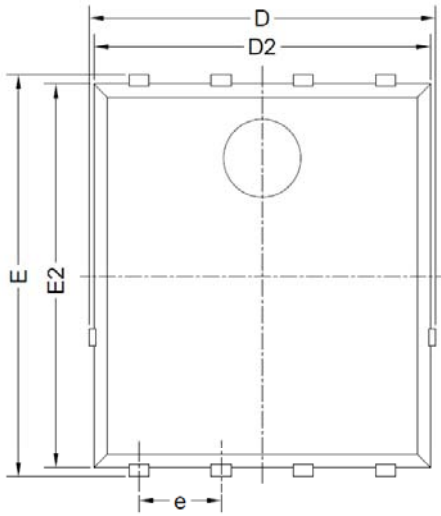


Figure 14. Safe Operation Area

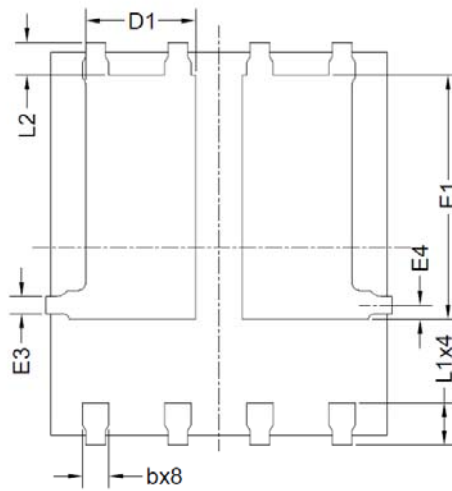


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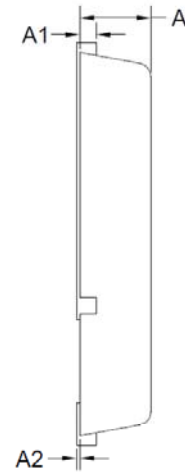
■ PDFN5060-8L-1.1MM Package information



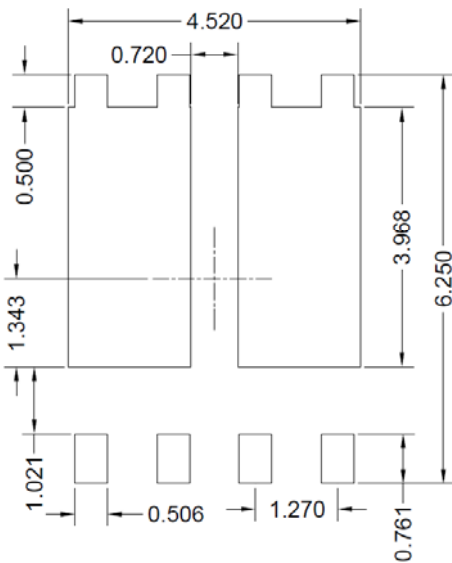
Top View
正面视图



Bottom View
背面视图



Side View
侧面视图



Suggested Solder Pad Layout
Top View

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	5.15	5.35	5.55
E	5.95	6.15	6.35
A	1.00	1.10	1.20
A1	0.254 BSC		
A2			0.10
D1	1.50	1.70	1.90
E1	3.52	3.72	3.92
D2	5.00	5.20	5.40
E2	5.66	5.86	6.06
E3	0.254REF		
E4	0.21REF		
L1	0.56	0.66	0.76
L2	0.50 BSC		
b	0.31	0.41	0.51
e	1.27 BSC		

Note:

1. Controlling dimension: in millimeters.
2. General tolerance: ± 0.10 mm.
3. The pad layout is for reference purposes only.



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