SPECIFICATION
FOR
APPROVAL

( ) **Preliminary Specification**

(●) **Final Specification**

Title	55.0" WUXGA OLED

BUYER	-
MODEL	

SUPPLIER	LG Display Co., Ltd.
*MODEL	LW550JUL
SUFFIX	HMA1

*When you obtain standard approval,
please use the above model name without suffix

APPROVED BY	SIGNATURE DATE
/	
/	
/	

Please return 1 copy for your confirmation with your signature and comments.

APPROVED BY	SIGNATURE DATE
Nak Jin Seong / Team Leader	
REVIEWED BY	
Seung Woo Yu / Project Leader	
PREPARED BY	
Jae Ho Shin/ Engineer	

OLED TV Development Dept.
LG Display Co., Ltd.

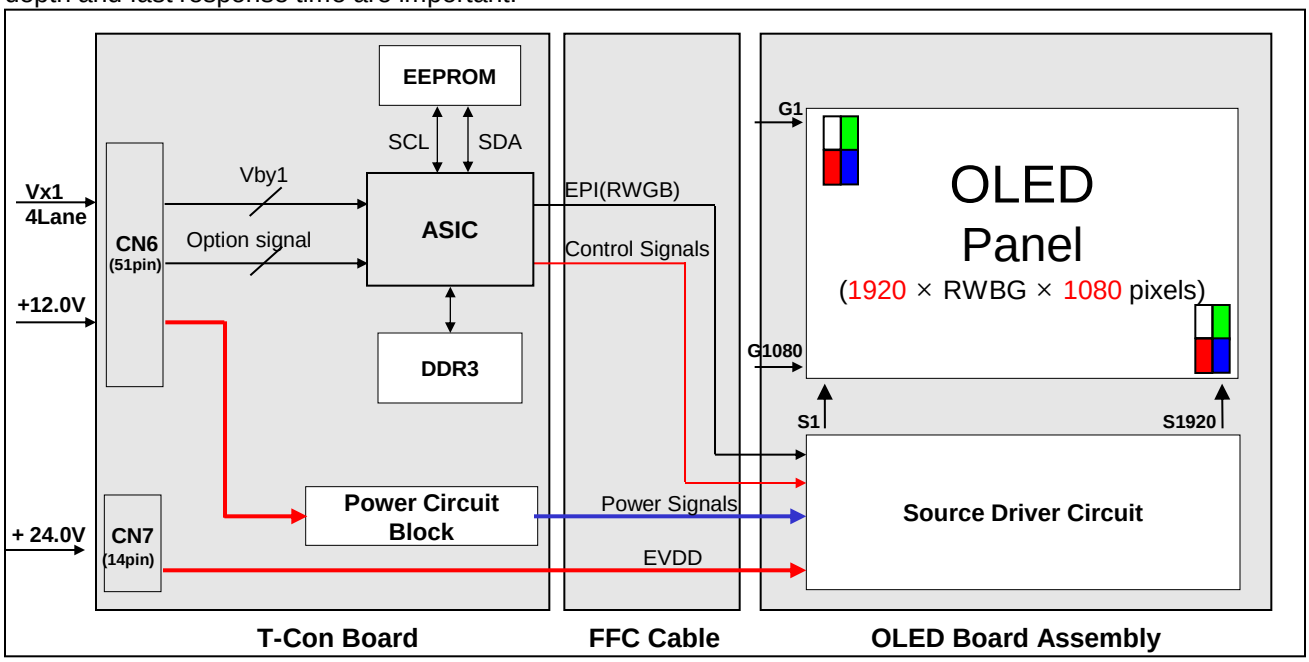
CONTENTS

RECORD OF REVISIONS

Revision No.	Revision Date	Page	Description
0.1	July, 18, 2018	-	Pre Specification (First Draft)
0.2	Oct, 15, 2018	4,6	Update EVDD Power for IEC62087
		17	Update Color Coordinates for Red, Green, Blue
0.3	Nov, 27, 2018	4	Update Outline Dimension
		6	Update Duration of Rush Current
		16	JB T2 Timing 13s→9.5s
		21	Update Mechanical Characteristics
		22~23	Update Mechanical Drawing
		26	Add Pallet packing vibration test
		35	Update Box & Pallet Label Customer P/No
		45~46	Update Design Guide
0.4	Dec, 26, 2018	4	Transparent Ratio 40%→38% (due to H/C Film) Modify Surface Treatment Description (due to H/C Film)
		21,22	Update Mechanical Characteristics, Drawing (Thickness 1.6→1.72)
		43,44	Update G to G, MPRT Measured Data
		45	Update Design Guide Drawing
0.5	Jan, 08, 2019	4	Add Reflectivity
0.6	Feb, 25, 2019	34	Change Board Ass'y Label
0.7	Apr, 04, 2019	22	Update Mechanical Drawing
		34	Change C-PCB Label
	Apr, 09, 2019	24	Update C-PCB Drawing for C-PCB Label
		4,7	Connector Name Correction CN6
		27	Update International Standards for Safety
1.0	Jun, 18, 2019		Final CAS Release
1.1	Jun, 27, 2019	27	Update International Standards for Environment

1. General Description

The LW550JUL is a Color Active Matrix Organic Light Emitting Diode Display (OLED).
The matrix employs Oxide Thin Film Transistor as the active element. It is a Top emission display type.
It has a 55 inch diagonally measured active display area with WUXGA resolution (1080 vertical by 1920 horizontal pixel array).
Each pixel is divided into Red, Green, Blue and White sub-pixels or dots which are arrayed in Quad.
Gray scale or the luminance of the sub-pixel color is determined with a 10-bit gray scale signal for each dot.
Therefore, it can present a palette of more than 1.07B(true) colors.
It has been designed to apply the 10-bit 4 Lane V by One interface.
It is intended to Public Display where high brightness, super wide viewing angle, high color gamut, high color depth and fast response time are important.



General Features

Active Screen Size	54.64 inches(1387.86 mm) diagonal
Outline Dimension	1221.5(H) x 699.35(V) mm (Typ.)
Pixel Pitch	0.630 mm x 0.630 mm
Pixel Format	1920 horiz. by 1080 vert. Pixels, RWBG Quad arrangement
Color Depth	10bit(R), 1.07Billon colors
Luminance, White	400 / 150 cd/m^2 (Center 1point ,Typ.)
Color Viewing Angle	R/L 120 (min.), U/D 120 (min.) (Δu'v' ≤ 0.026)
Power Consumption	Total 62.52W (Typ.) [Logic=11.52W, EVDD=51W @ IEC62087]
Weight	3.14kg (Typ.) (W/O C-PCB & Shield)
Display Mode	Normally Transparent
Transparent Ratio	38%(typ.)
Reflectivity	14% (typ.)
Surface Treatment	Hard coating(2H)

2. Absolute Maximum Ratings

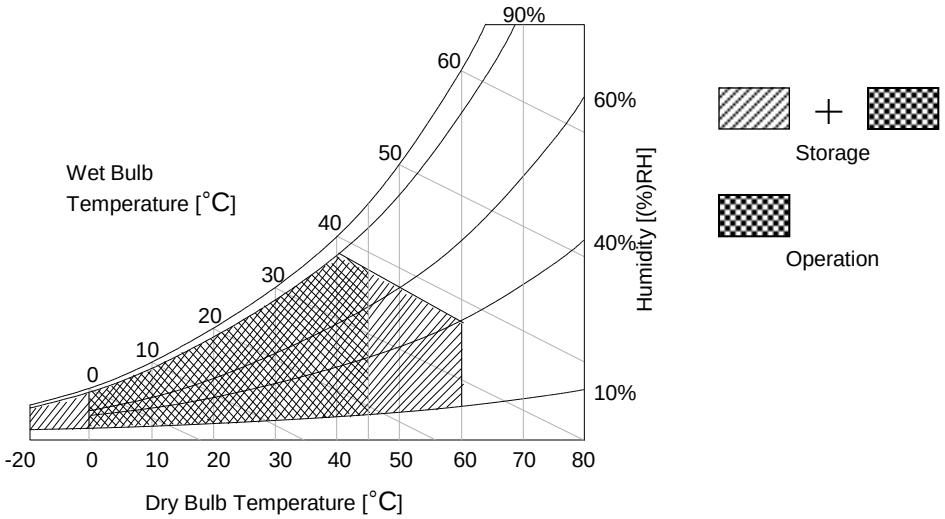
The following items are maximum values which, if exceeded, may cause faulty operation or damage to the OLED module.

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Value		Unit	Note
			Min	Max		
Power Input Voltage	Logic	VDD	-0.3	+14.0	V_{DC}	1
	OLED Panel	EVDD	-0.3	+ 26.0	V_{DC}	
T-Con Option Selection Voltage		V_{LOGIC}	-0.3	+3.7	V_{DC}	
Operating Temperature		T_{OP}	0	+45	˚C	2
Storage Temperature		T_{ST}	-20	+60	˚C	
Panel Front Temperature		T_{SUR}	-	(+68)	˚C	3
Operating Ambient Humidity		H_{OP}	10	90	%RH	2
Storage Humidity		H_{ST}	10	90	%RH	

Notes

1. Ambient temperature condition (Ta = 25 ± 2 ˚C)
2. Temperature and relative humidity range are shown in the figure below.
   Wet bulb temperature should be Max 39˚C, and no condensation of water.
3. The maximum operating temperatures is based on the test condition that the surface temperature of display area is less than or equal to 68˚C with OLED module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 68℃. The range of operating temperature may be degraded in case of improper thermal management in final product design.



3. Electrical Specifications

3-1. Electrical Characteristics

It requires two power inputs. One is employed to power for the circuit. The other is used for the EVDD.

Table 2. Electrical Characteristics

Parameter	Symbol		Values			Unit	Notes
			Min	Typ	Max		
Power Input Voltage	VDD		10.8	12.0	13.2	V	
	EVDD		22.8	24.0	25.2		
Power Input Current	I_{VDD}		-	0.96	1.14	A	1
			-	1.21	1.44		2
	I_{EVDD}		-	2.13	2.55		1
			-	9	10		3
Power Consumption	P_{VDD}		-	11.52	13.71	Watt	1
			-	14.52	17.28		2
	P_{EVDD}		-	51	61.2		1
			-	216	240		3
Rush current	I_{RUSH}	I_{RUSH_VDD}	-	-	7.5	A	
		I_{RUSH_EVDD}			13.6		
		T_{RUSH_VDD}	-	-	2	ms	4
		T_{RUSH_EVDD}	-	-	6		5

Note

1. The specified current and power consumption are under the VDD=12.0V, EVDD=24.0V Ta=25 ± 2°C, f_V=120Hz condition whereas standard moving picture(IEC62087) is displayed and f_V is the frame frequency.
2. The current (I_{VDD}) is specified at the maximum current pattern (1by1 Horizontal Pattern)
3. The current (I_{EVDD}) is specified at the maximum current pattern (Secondary Color Pattern).
4. The duration of VDD rush current is about 2ms and rising time of power input is 1ms (min)
5. The duration of EVDD rush current is about 6ms and rising time of power input is 5ms (min)

3-2. Interface Connections

This OLED module employs two kinds of interface connection, 51-pin connector is used for the module electronics and 14-pin connector is used for the EVDD.

3-2-1. OLED Module

- VDD Connector (CN6): GT05S-51S-H38(LSM)
- Mating Connector : FI-RE51HL(JAE) or compatible

Table 3. MODULE CONNECTOR(CN6) PIN CONFIGURATION

No	Symbol	Description	No	Symbol	Description
1	VDD	Power Supply +12.0V	27	GND	Ground
2	VDD	Power Supply +12.0V	28	Rx0N	V-by-One HS Data Lane0
3	VDD	Power Supply +12.0V	29	Rx0P	V-by-One HS Data Lane0
4	VDD	Power Supply +12.0V	30	GND	Ground
5	NC	No Connection	31	Rx1N	V-by-One HS Data Lane1
6	GND	Ground	32	Rx1P	V-by-One HS Data Lane1
7	GND	Ground	33	GND	Ground
8	GND	Ground	34	Rx2N	V-by-One HS Data Lane2
9	GND	Ground	35	Rx2P	V-by-One HS Data Lane2
10	Off RS	Off RS Done(H), Set←Module (note 3)	36	GND	Ground
11	AC_DET	AC_DET (H= On), Set → Module	37	Rx3N	V-by-One HS Data Lane3
12	Error Detection	H' = Error , 'L' = Normal (note 4)	38	Rx3P	V-by-One HS Data Lane3
13	I2C_SDA	I2C for Customer	39	GND	Ground
14	I2C_SCL		40	NC	No Connection
15	NC	Reserved	41	NC	No Connection
16	NC	Reserved	42	NC	No Connection
17	NC	For LGD Internal Use	43	NC	No Connection
18	NC	I2C for LGD Internal Use (note5)	44	NC	No Connection
19	NC		45	NC	No Connection
20	EVDD_DET	EVDD reset, Set ← Module (note6)	46	NC	No Connection
21	Bit Select	Bit Selection (10bit only)	47	NC	No Connection
22	NC	AGP2 (note 7)	48	NC	For LGD Internal Use
23	NC	AGP1 (note 7)	49	NC	For LGD Internal Use
24	GND	Ground	50	NC	On_RF_Done Set ← Module
25	HTPDN	Hot plug detect	51	NC	For LGD Internal Use
26	LOCKN	Lock detect	-	-	-

Notes

1. All GND(ground) pins should be connected together.
2. All Input levels of V-by-One signals are based on the V-by-One HS Standard.
3. Specific pin No. **#10** is used for compensation when Power turn off.
4. Specific pin No. **#12** is used for "Power Error detection" of the OLED module.
5. Specific pins **#18** and **#19** are used only for LGD. (Do not connect)
6. Specific pin No. **#20** is used only for EVDD level monitoring of the OLED module. (For set system)
7. Specific pins No. **#22** and **#23** are used for "No signal detection" of system signal interface.
   It should be GND for NSB (No Signal Black) while the system interface signal is not.
   If this pin is "H" or "NC", OLED module displays AGP (Auto Generation Pattern).

3-2-2. OLED Module (EVDD)

- EVDD Connector (CN7) : 20022WR-H14B2 (manufactured by Yeon Ho)
- Mating Connector : 2022HS-14B2(BK) (manufactured by Yeon Ho)
- VLC Connector (CN8, 9) : 12507WR-H05G (manufactured by Yeon Ho)

Table 4. EVDD CONNECTOR(CN7) PIN CONFIGURATION

No	Symbol	Description
1	EVSS	OLED Panel Ground
2	EVSS	OLED Panel Ground
3	EVSS	OLED Panel Ground
4	EVSS	OLED Panel Ground
5	EVSS	OLED Panel Ground
6	EVSS	OLED Panel Ground
7	EVSS	OLED Panel Ground
8	EVDD	OLED Panel Power Supply +24V
9	EVDD	OLED Panel Power Supply +24V
10	EVDD	OLED Panel Power Supply +24V
11	EVDD	OLED Panel Power Supply +24V
12	EVDD	OLED Panel Power Supply +24V
13	EVDD	OLED Panel Power Supply +24V
14	EVDD	OLED Panel Power Supply +24V

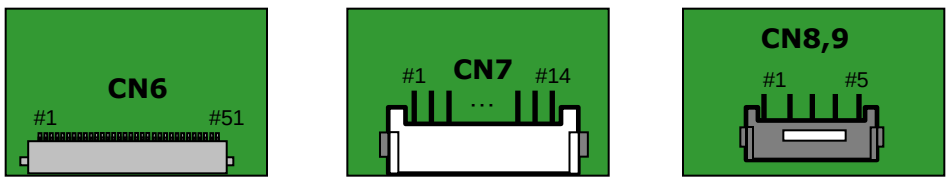
Table 5-1. VLC Tx CONNECTOR(CN8) PIN CONFIGURATION

No	Symbol	Description
1	APLC_TXCLK_P	VLC LVDS Tx CLK +
2	APLC_TXCLK_N	VLC LVDS Tx CLK -
3	GND	Ground
4	APLC_TXDAT_P	VLC LVDS Tx Data +
5	APLC_TXDAT_N	VLC LVDS Tx Data -

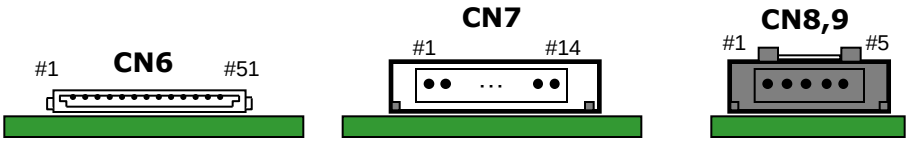
Table 5-2. VLC Rx CONNECTOR(CN9) PIN CONFIGURATION

No	Symbol	Description
1	APLC_RXDAT_N	VLC LVDS Rx Data -
2	APLC_RXDAT_P	VLC LVDS Rx Data +
3	GND	Ground
4	APLC_RXCLK_N	VLC LVDS Rx CLK -
5	APLC_RXCLK_P	VLC LVDS Rx CLK +

◆ **Rear view of OLED Module**



< Top view of PCB >



< Side view of PCB >

3-3. Signal Timing Specifications

Table 6 shows the signal timing required at the input of the **Vx1** transmitter. All of the interface signal timings should be satisfied with the following specification for normal operation.

Table 6. TIMING TABLE (DE Only Mode)

ITEM		Symbol	Min	Typ	Max	Unit	Note
Horizontal	Display Period	t_{HV}	480	480	480	tCLK	1920 / 4
	Blank	t_{HB}	60	70	100	tCLK	1
	Total	t_{HP}	540	550	580	tCLK	
Vertical	Display Period	t_{VV}	1080	1080	1080	Lines	
	Blank	t_{VB}	44 (252)	45 (270)	46 (276)	Lines	1
	Total	t_{VP}	1124 (1332)	1125 (1350)	1126 (1356)	Lines	

ITEM		Symbol	Min	Typ	Max	Unit	Note
Frequency	DCLK	f_{CLK}	73.25	74.25	75.25	MHz	
	Horizontal	f_H	133.20	135	136.80	KHz	2
	Vertical	f_V	118.42 (98.68)	120 (100)	121.62 (101.32)	Hz	2 NTSC : 118.42~121.62Hz (PAL : 98.68~101.32Hz)

Notes

1. The input of HSYNC & VSYNC signal does not have an effect on normal operation (DE Only Mode). If you use spread spectrum of EMI, add some additional clock to minimum value for clock margin.
2. The performance of the electro-optical characteristics may be influenced by variance of the vertical refresh rate and the horizontal frequency

※ Timing should be set based on clock frequency.

3-4. V by One input Signal Characteristics

3-4-1. V by One Input Signal Timing Diagram

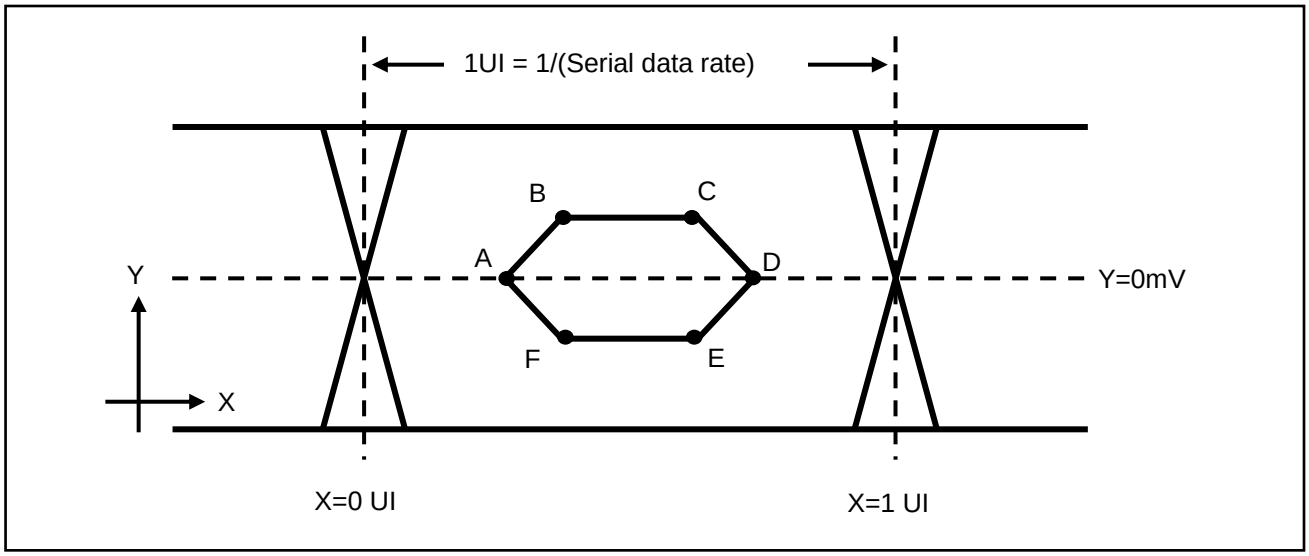
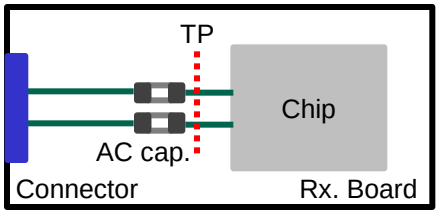


Table 7. Eye Mask Specification

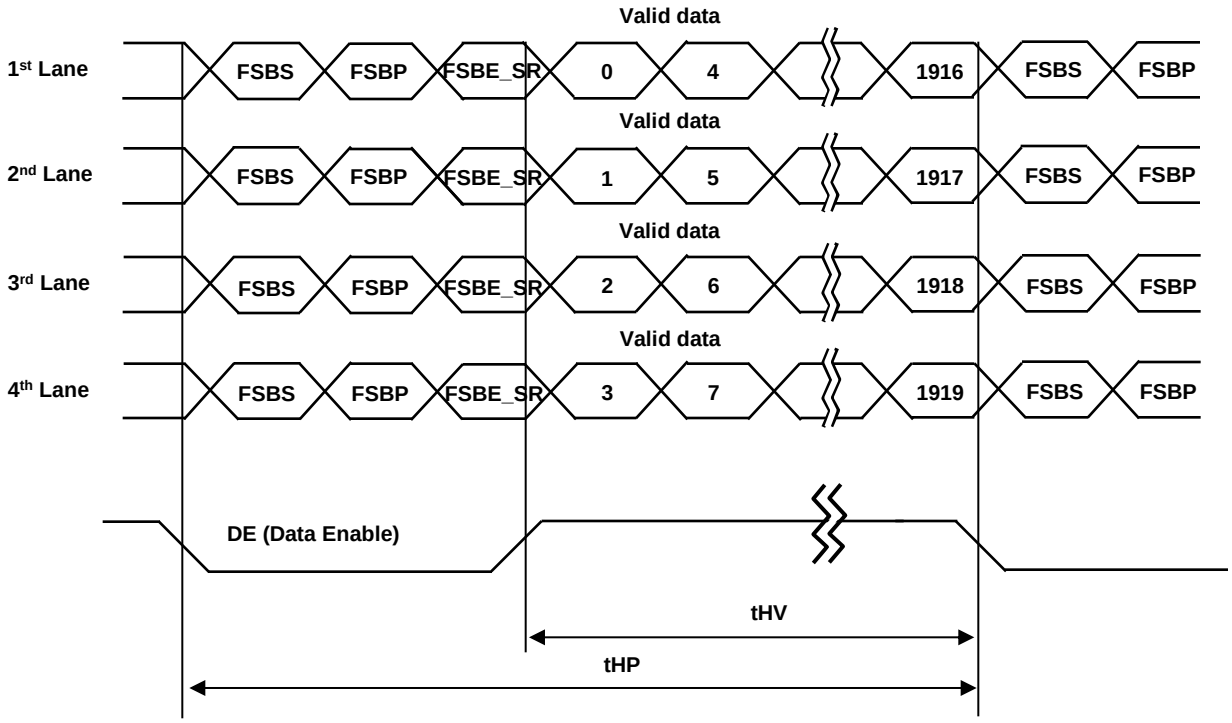
	X [mV]	Note	Y [UI]	Note
A	0.25 (max)	2	0	-
B	0.30 (max)	2	50	3
C	0.70 (min)	3	50	3
D	0.75 (min)	3	0	-
E	0.70 (min)	3	|-50|	3
F	0.30 (max)	2	|-50|	3

Notes

1.1 All Input levels of V by One signals are based on the V by One HS Standard.
1.2 When using the Tx's Pre-Emphasis function to be set to a minimum value that meets the EYE Mask Spec
2. This is allowable maximum value.
3. This is allowable minimum value
4. The eye diagram is measured by the oscilloscope and receiver CDR characteristic must be emulated.
   - PLL Type : 2nd Order
   - PLL bandwidth : 10MHz
   - Damping Factor : 2
5. EYE mask measuring point

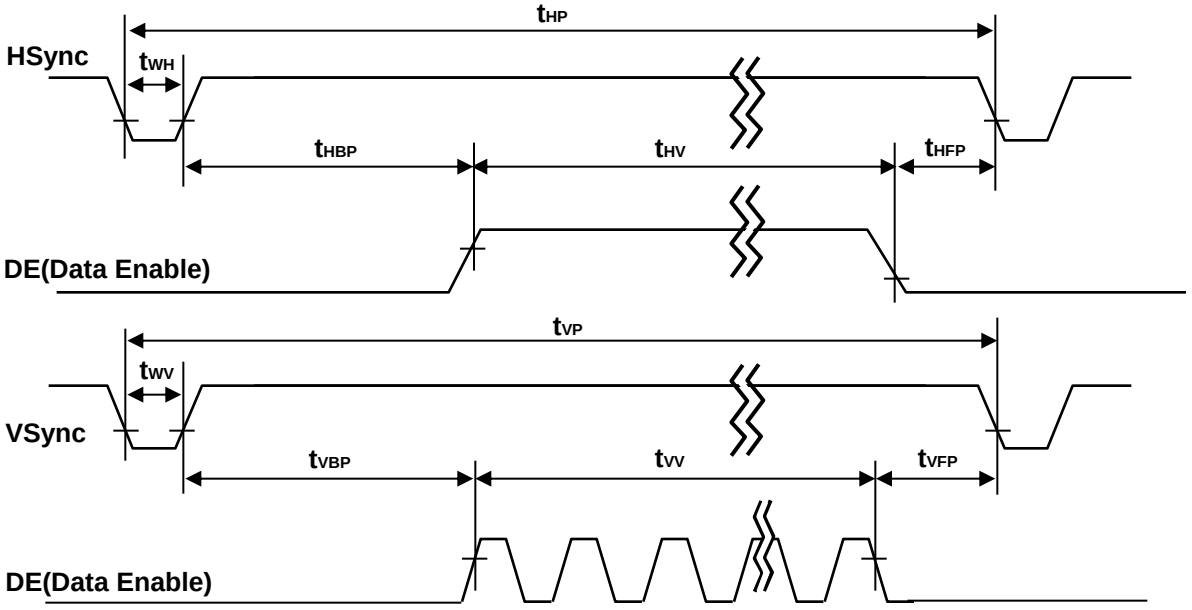


3-4-2. V by One Input Signal Timing Diagram



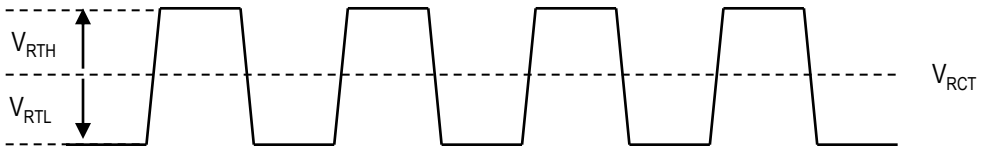
* Reference: Sync. Relation

* tHB = tHFP + tWH +tHBP
* t_{VB} = t_{VFP} + t_{WV} +t_{VBP}



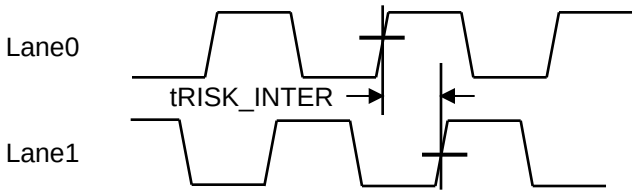
3-4-3. DC Specification

1) DC Specification

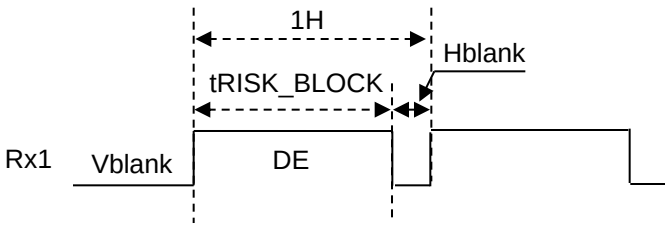


Description	Symbol	Min	Typ	Max	Unit	Note
CML Differential Input High Threshold	V_{RTH}	-	-	50	mV	-
CML Differential Input Low Threshold	V_{RTL}	-50	-	-	mV	-
CML Common Mode Bias Voltage	VRCT	-	0.75	-	V	-

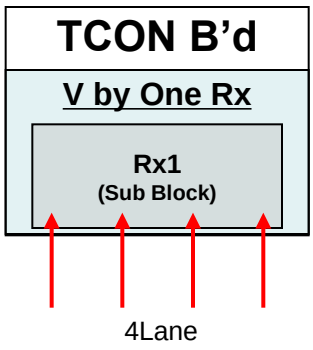
2) AC Specification



<Inter-pair skew between two lanes>



<Inter-pair skew between two sub-blocks>



<V by One Brief Diagram >

Description	Symbol	Min	Max	Unit	Note
Allowable inter-pair skew between lanes	tRISK_INTER	-	5	UI	1, 3
Allowable inter-pair skew between sub-blocks	tRISK_BLOCK	-	1	DE	1, 4

Notes: 1.1UI = 1/serial data rate

2. it is the time difference between the true and complementary single-ended signals.
3. it is the time difference of the differential voltage between any two lanes in one sub block.
4. it is the time difference of the differential voltage between any two blocks in one IP.

3-5. Color Data Reference

The brightness of each primary color (red,green,blue) is based on the 10bit gray scale data input for the color. The higher binary input, the brighter the color. Table 8 provides a reference for color versus data input.

Table 8. COLOR DATA REFERENCE

Packer input & Unpacker output		30bpp RGB (10bit)
Byte0	D[0]	R[2]
	D[1]	R[3]
	D[2]	R[4]
	D[3]	R[5]
	D[4]	R[6]
	D[5]	R[7]
	D[6]	R[8]
	D[7]	R[9]
Byte1	D[8]	G[2]
	D[9]	G[3]
	D[10]	G[4]
	D[11]	G[5]
	D[12]	G[6]
	D[13]	G[7]
	D[14]	G[8]
	D[15]	G[9]
Byte2	D[16]	B[2]
	D[17]	B[3]
	D[18]	B[4]
	D[19]	B[5]
	D[20]	B[6]
	D[21]	B[7]
	D[22]	B[8]
	D[23]	B[9]
Byte3	D[24]	Don't care
	D[25]	Don't care
	D[26]	B[0]
	D[27]	B[1]
	D[28]	G[0]
	D[29]	G[1]
	D[30]	R[0]
	D[31]	R[1]

Notes 1. 30bpp RGB (10bit) is 4 byte mode

3-6. Power Sequence

3-6-1. OLED Driving circuit

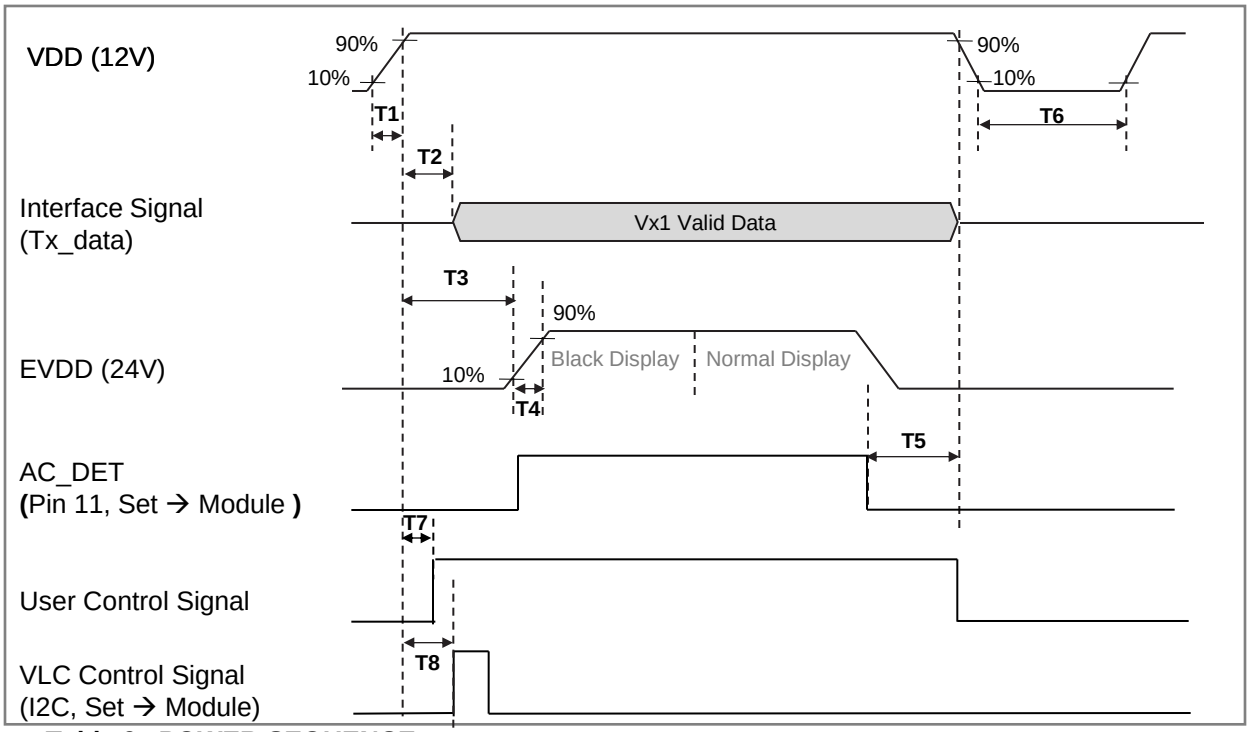


Table 9. POWER SEQUENCE

Parameter	Value			Unit	Notes
	Min	Typ	Max		
T1	1	-	60	ms	1
T2	1	-	-	ms	
T3	2.0	-	-	sec	2
T4	4	-	60	ms	
T5	60	-	-	ms	
T6	2.0	-	-	sec	3
T7	0	-	T2	ms	4
T8	1	-	T3	sec	

Notes

1. Even though T1 is over the specified value, there is no problem if I2T spec of fuse is satisfied.
2. The T3 is recommended value, the case when failed to meet a minimum specification, abnormal display would be shown. There is no reliability problem. T3 should be larger than T2.
3. T6 should be measured after the module has been fully discharge between power off and on period.
4. If the on time of signals (Interface signal and user control signals) precedes the on time of Power(VDD) it will be happened abnormal display. When T7 is NC status, T7 doesn't need to be measured

※ Black pattern is displayed during black display period before normal display. (ON RF Time 3.0S)

※ When the power for logic (VDD_12V) turns off, EVDD should be less than 8.0V. But, it does not matter if there is no garbage image.

※ Please avoid floating state of interface signal at invalid period.

3-6-2. TFT compensation operation(OFF RS)

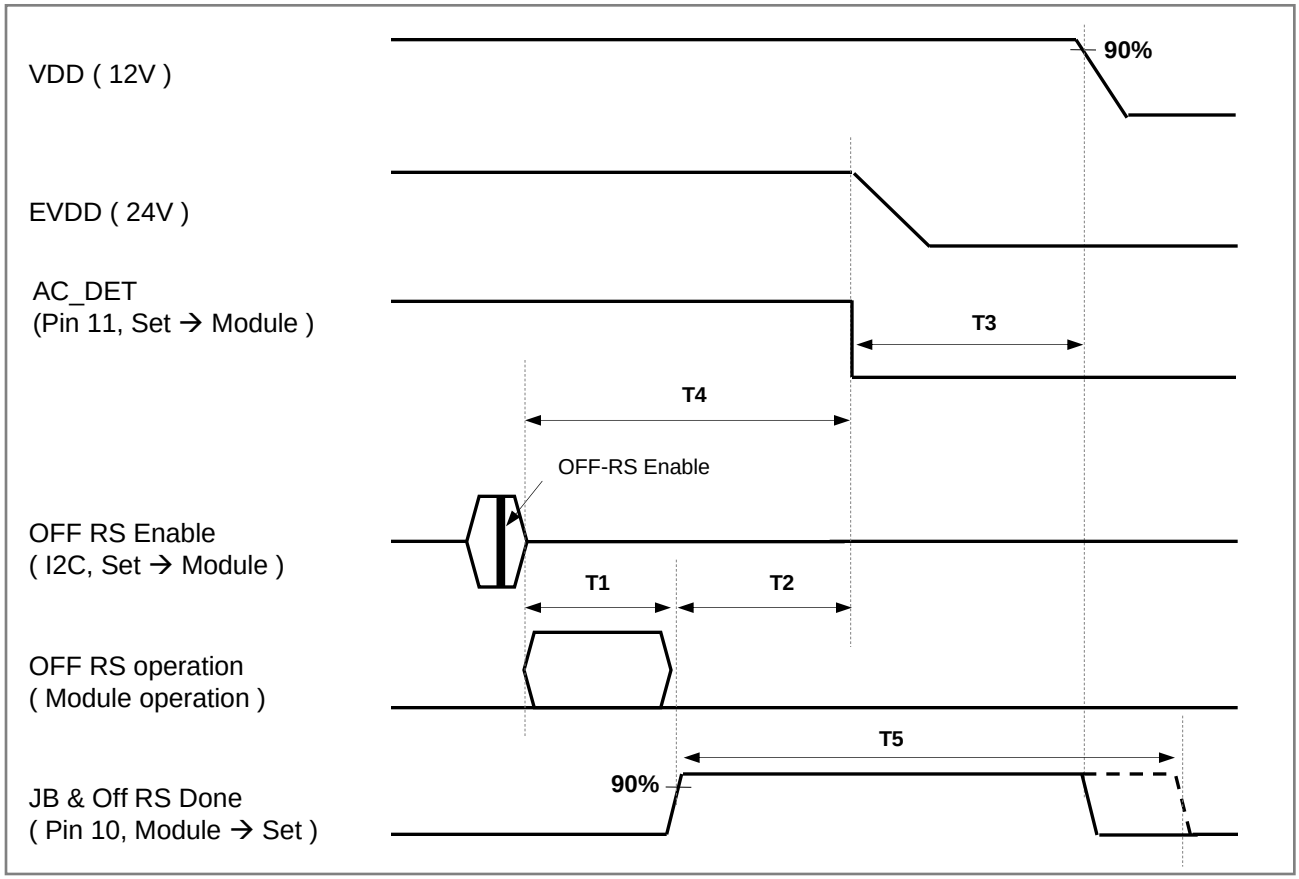


Table 10. POWER SEQUENCE

Parameter	Value			Unit	Notes
	Min	Typ	Max		
T1	50	-	150	sec	
T2	0.5	-	10	sec	
T3	60	-	-	ms	
T4	55	-	160	sec	
T5	0.56	7	10	sec	

Notes

1. T4 is for unstable OFF RS Done.
   TV system is recommended to be turned off after T4 although Off-RS Done signal is not transferred.

※ When there is power on action before completing OFF RS operation, don't change OFF RS enable signal(1→0).
Just do power off and power on.

3-6-3. OLED compensation operation(JB)

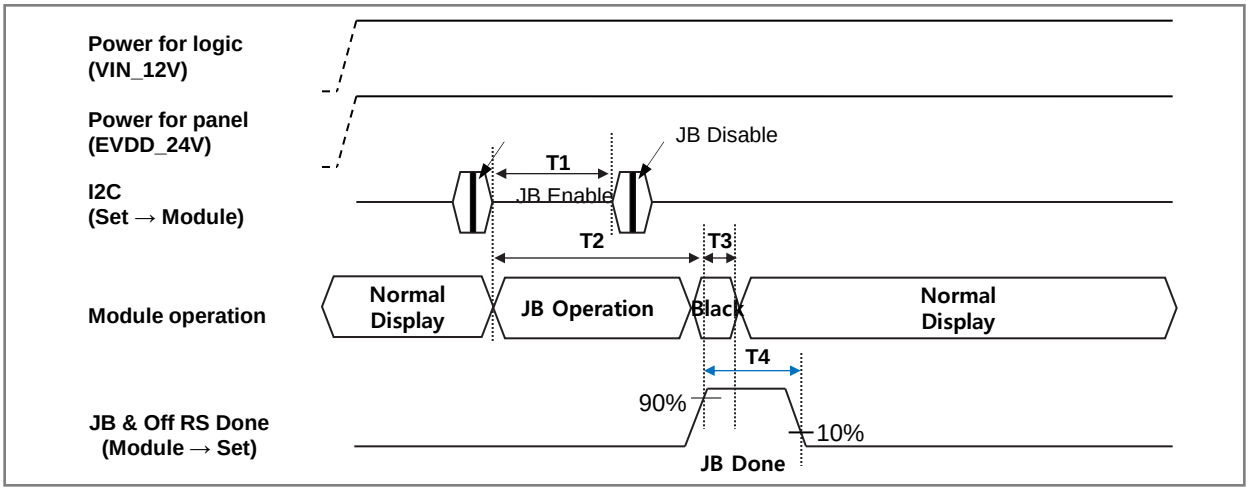


Table 11. JB Power Sequence

Parameter	Value			Unit	Notes
	Min	Typ	Max		
T1	10	-	20	sec	
T2	9.5	-	25	sec	
T3	8	24	40	ms	
T4	0.5	7	10	sec	

Notes

※ OLED Compensation is to be operated in conjunction with the OFF RS and it must be operated in the temperature range of JB operation, 10 to 40℃.

※ OLED compensation needs to be cooled during at least 1 hour more before it is operated and at this time, the Commercial System needs to be at the standby mode.

4. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable in a dark environment at 25±2°C. The values are specified at distance 50cm from the OLED surface at a viewing angle of Φ and θ equal to 0 °. FIG. 1 shows additional information concerning the measurement equipment and method.

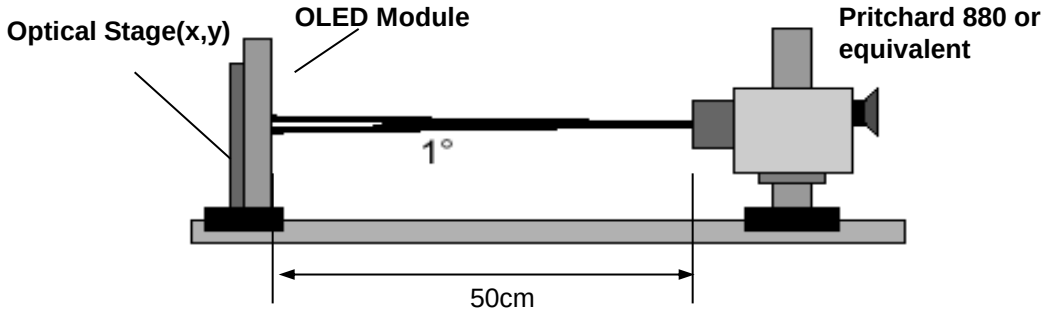


FIG. 1 Optical Characteristic Measurement Equipment and Method

Table 12. OPTICAL CHARACTERISTICS Ta= 25±2°C, VDD=12.0V, EVDD=24V, fv=120Hz, Dclk=74.25MHz

Parameter		Symbol			Value			Unit	Note
					Min	Typ	Max		
Contrast Ratio		CR			120,000	150,000	-		1
Surface Luminance, white		L_{WH}	2D	Normal	120	150		cd/m²	2
				Peak	320	400			
Luminance Uniformity		δ_{WHITE}	9P		75	85	-	%	3
Response Time	Gray-to-Gray	G to G			-	1	3	ms	4
	MPRT	MPRT			-	8	12	ms	5
Color Coordinates [CIE1931]	RED	Rx			Typ -0.02	0.674	Typ +0.02		
		Ry				0.327			
	GREEN	Gx				0.278			
		Gy				0.655			
	BLUE	Bx				0.142			
		By				0.054			
	WHITE	Wx				0.285			
		Wy				0.294			
Color Temperature						9,300		K	
Color Gamut (BT709)						120		%	
Color Viewing Angle									
(Δu'v' ≤ 0,026)	x axis, right(ϕ=0°)	θr			60	-	-	degree	6
	x axis, left (ϕ=180°)	θl			60	-	-		
	y axis, up (ϕ=90°)	θu			60	-	-		
	y axis, down (ϕ=270°)	θd			60	-	-		
Life Time (B10)		Hrs			-	30,000	-		7
Gray Scale						2.2			8

Notes

1. Contrast Ratio(CR) is defined mathematically as :

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

It is measured at center 1-point.

2. Surface luminance is determined after the unit has been 'ON' and 60minutes after lighting the module in a dark environment at 25±2°C. Surface luminance is the luminance value at center 1-point across the OLED surface 50cm from the surface with all pixels displaying white. For more information see the FIG. 2.
   ※ Normal : APL 100% (Full white) / Peak : APL 25%
3. The variation in surface luminance , δ WHITE is defined as :
   δ WHITE(9P) = Minimum($L_{on1,,}$…. L_{on9}) / Maximum(L_{on1}….. L_{on9})
   Where L_{on1} to L_{on9} are the luminance with all pixels displaying white at 9 locations .
   For more information, see the FIG. 2.
4. Response time is the time required for the display to transit from G(N) to G(M) (Rise Time, Tr_R) and from G(M) to G(N) (Decay Time, Tr_D). For additional information see the FIG. 3. (N<M)
   ※ G to G Spec stands for average value of all measured points.
   Photo Detector : RD-80S / Field : 2°
5. MPRT is defined as the 10% to 90% blur-edge width Bij(pixels) and scroll speed U(pixels/frame)at the moving picture. For more information, see FIG 4
6. Viewing Angle Color Shift (VACS) is defined as follows after measuring color coordinates at each angle.; VACS=sqrt(du3+dv3) (@ CIE (u', v') color space) For more information, see the FIG. 5.
7. Test Condition : IEC62087 standard video with OFF-RS every 4 hours at room temperature 25℃ (If the cumulative time of usage is over 4 hours, OFF-RS compensation should be performed.)
8. Gray scale specification. Gamma Value is approximately 2.2. For more information, see the Table 13.

Table 13. GRAY SCALE SPECIFICATION

Gray Level	Luminance [%] (Typ)
L0	0.001
L15	0.20
L31	0.97
L47	2.42
L63	4.61
L79	7.59
L95	11.4
L111	16.0
L127	21.6
L143	28.0
L159	35.4
L175	43.7
L191	53.0
L207	63.2
L223	74.5
L239	86.7
L255	100

Measuring point for surface luminance & measuring point for luminance variation.

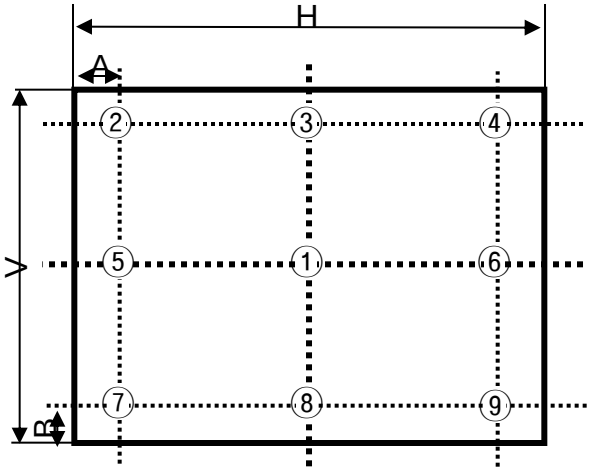


FIG. 2-1 9 Points for Luminance Measure with 100% APL

A: H/9 B: V/9 @ H,V: Active Area

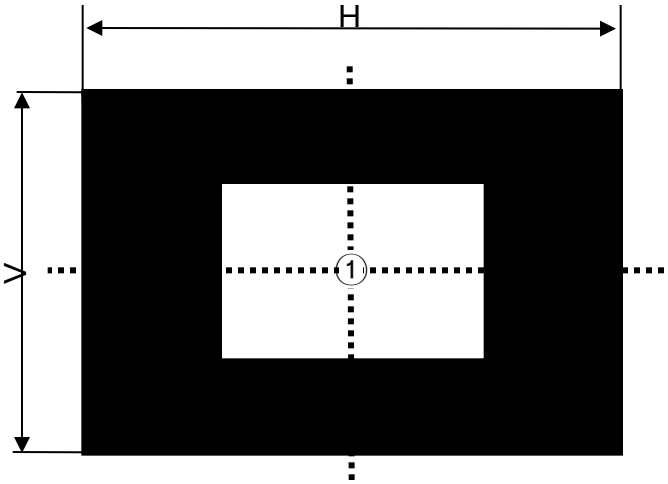


FIG. 2-2. 1 Points for peak luminance measure with 25% APL

@ H,V: Active Area

Response time is defined as the following figure and shall be measured by switching the input signal for "Gray(N)" and "Gray(M)".

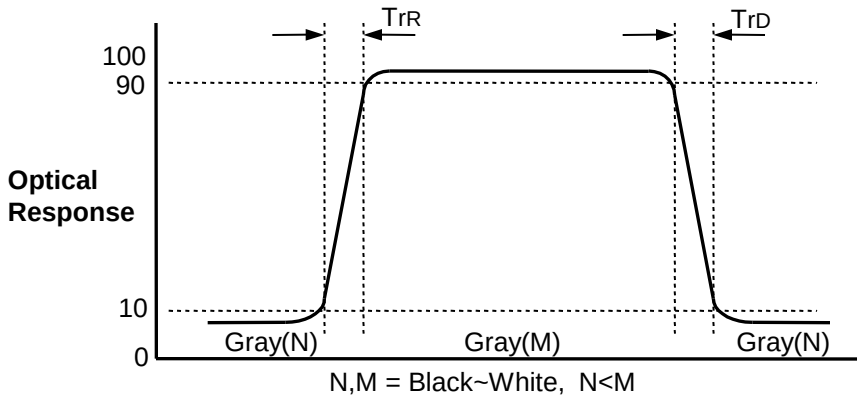
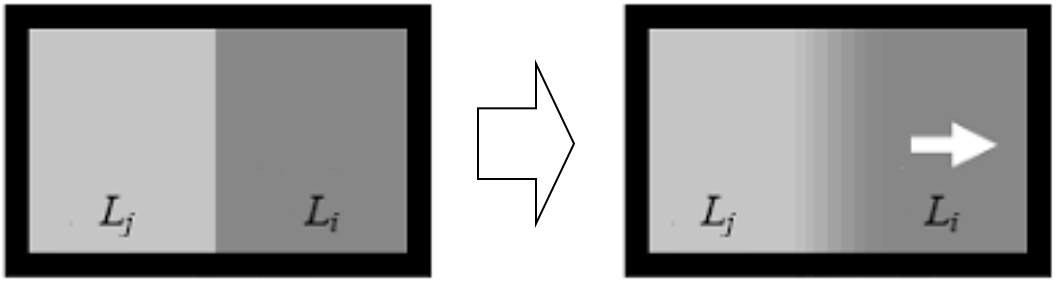
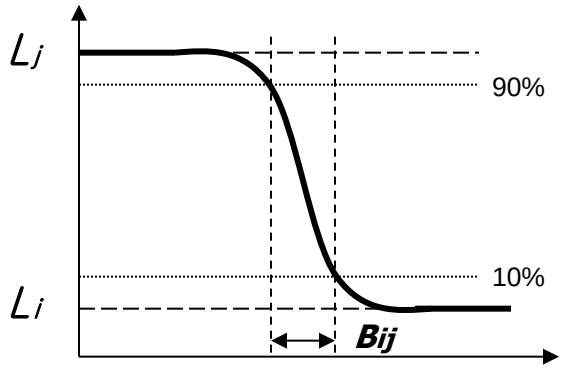


FIG. 3 Response Time

MPRT is defined as the 10% to 90% blur-edge with Bij(pixels) and scroll speed U(pixels/frame)at the moving picture.



$$M = \frac{1}{U} Bij \ (i \neq j)$$



Example) Bij = 12pixels, U = 10pixels / 120Hz
M = 12pixels / (10pixels / 120Hz)
= 12pixels / {10pixels / (1/120)s}
= 12 / 1,200 s
= 10 ms

FIG. 4 MPRT

Dimension of viewing angle range

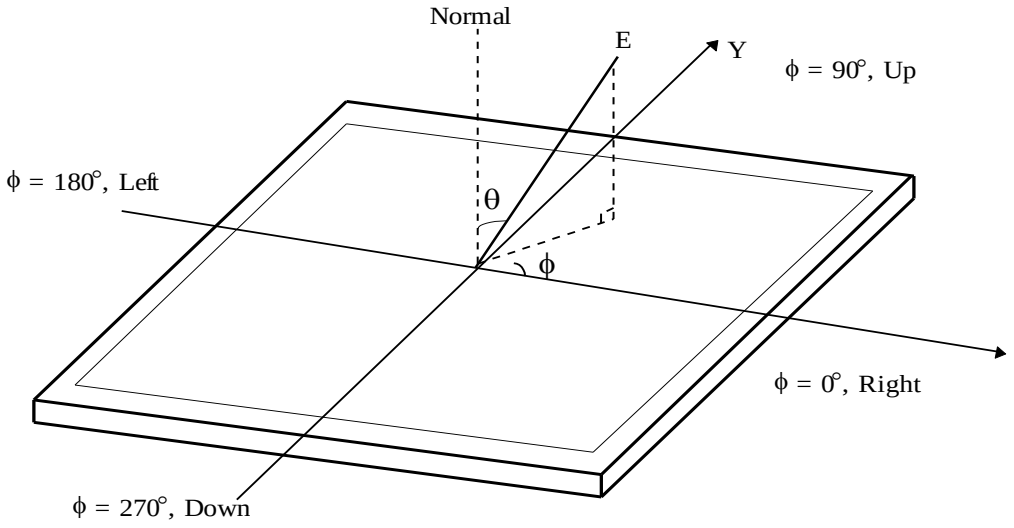


FIG. 5 Viewing Angle

5. Mechanical Characteristics

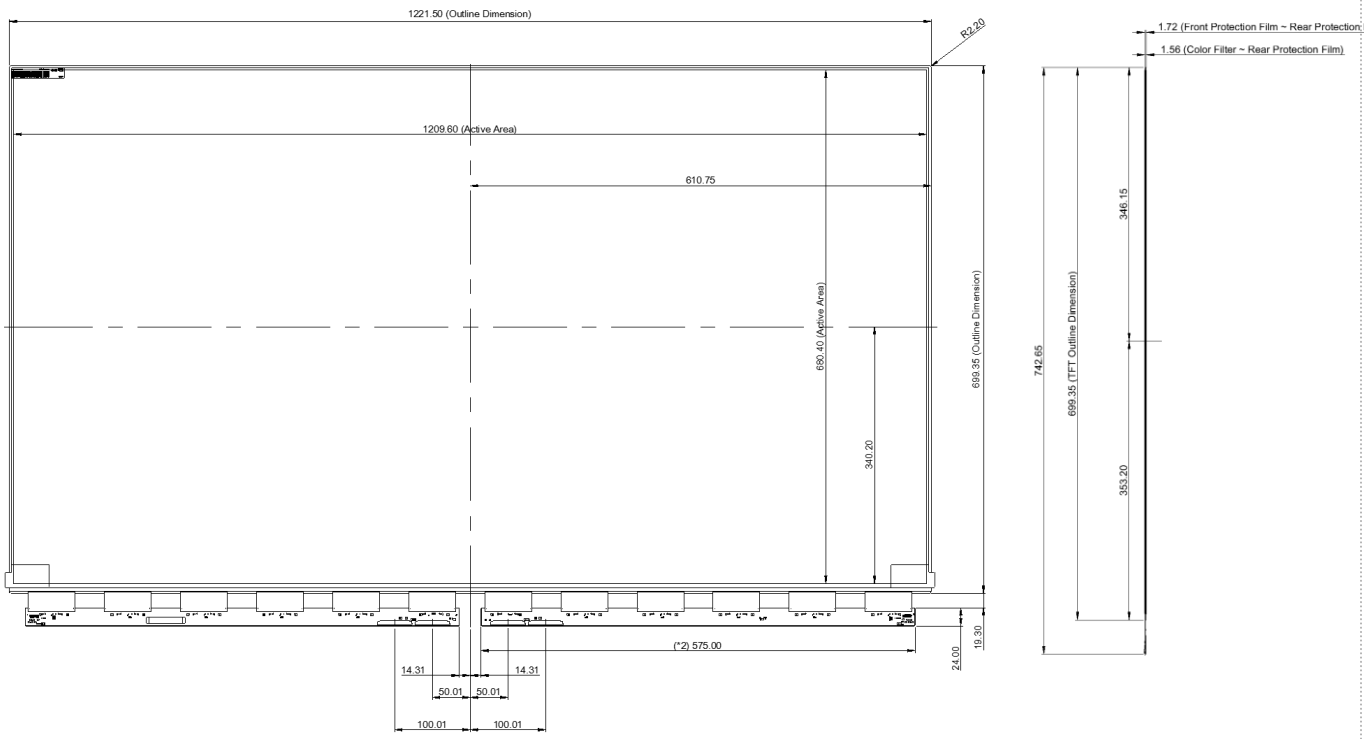
Table 14 provides general mechanical characteristics.

Table 14. MECHANICAL CHARACTERISTICS

Item	Value	
Outline Dimension (Sealing Board Ass'y)	Horizontal	1221.5mm
	Vertical	699.35mm
	Thickness	1.72mm (Front Film to Rear Film)
Active Display Area (Base On Board Ass'y)	Horizontal	1209.6 mm
	Vertical	680.4mm
On Bezel (Active Area ~ Glass Edge)	Horizontal	5.95mm(Left) / 5.95mm(Right)
	Vertical	5.95mm(Top) / 13.0mm(Bottom)
Weight	3.14kg (Typ.) (W/O C-PCB & Shield)	

Note : Please refer to a mechanical drawing in terms of tolerance at the next page.

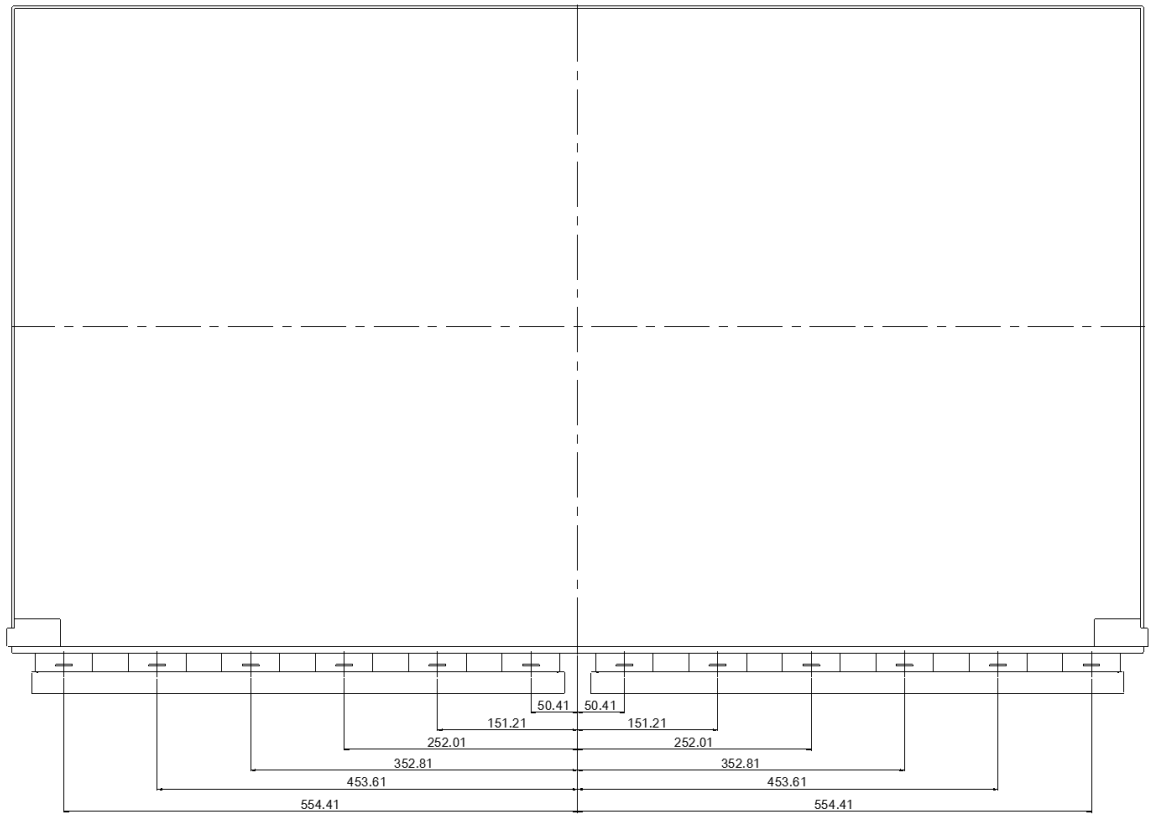
[Front View of Board Assembly]



NOTE

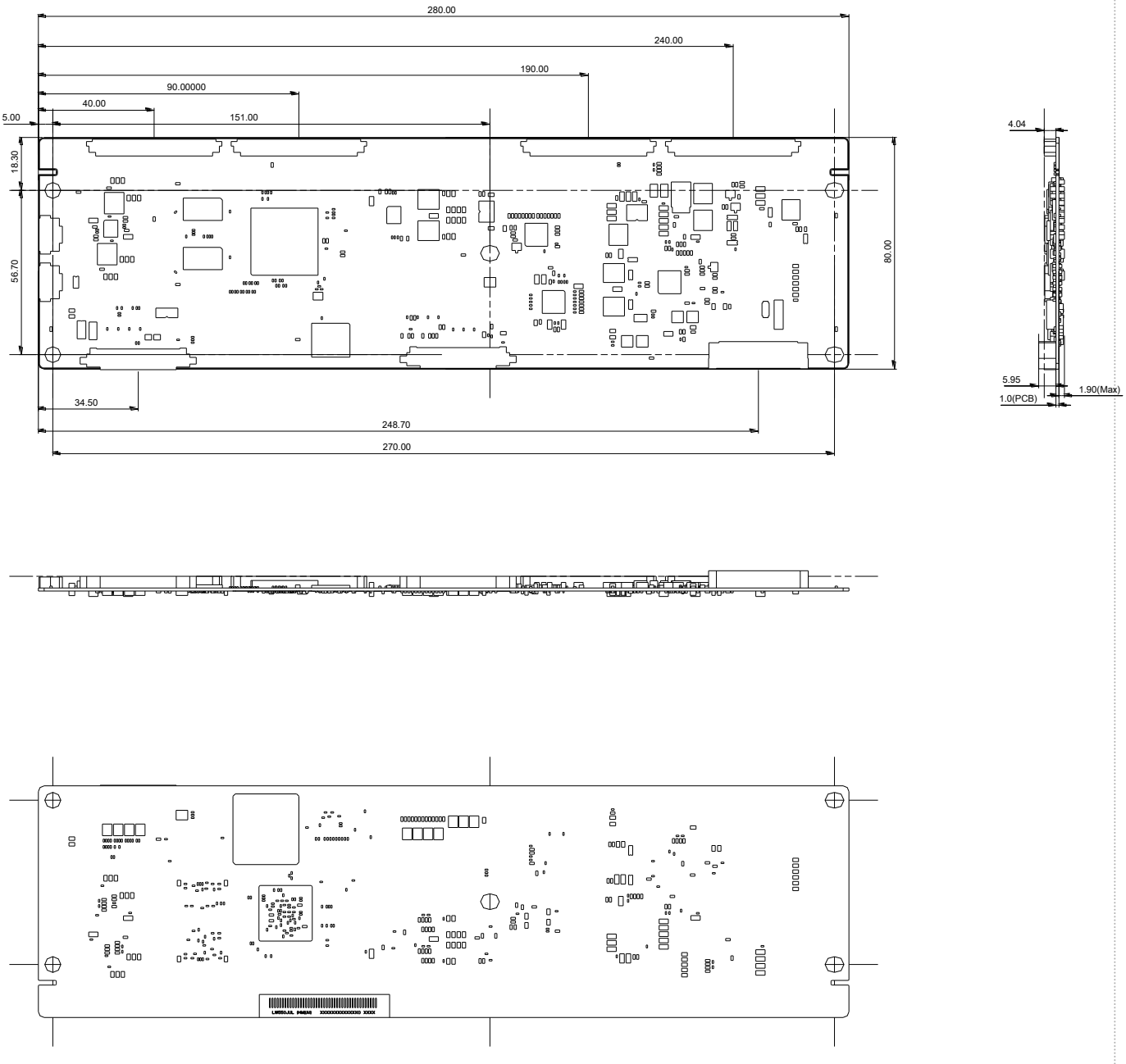
1. Unspecified tolerance is ±1.0mm.

[Rear View of Board Assembly]



Note
1. Unspecified tolerance is ± 1.0mm

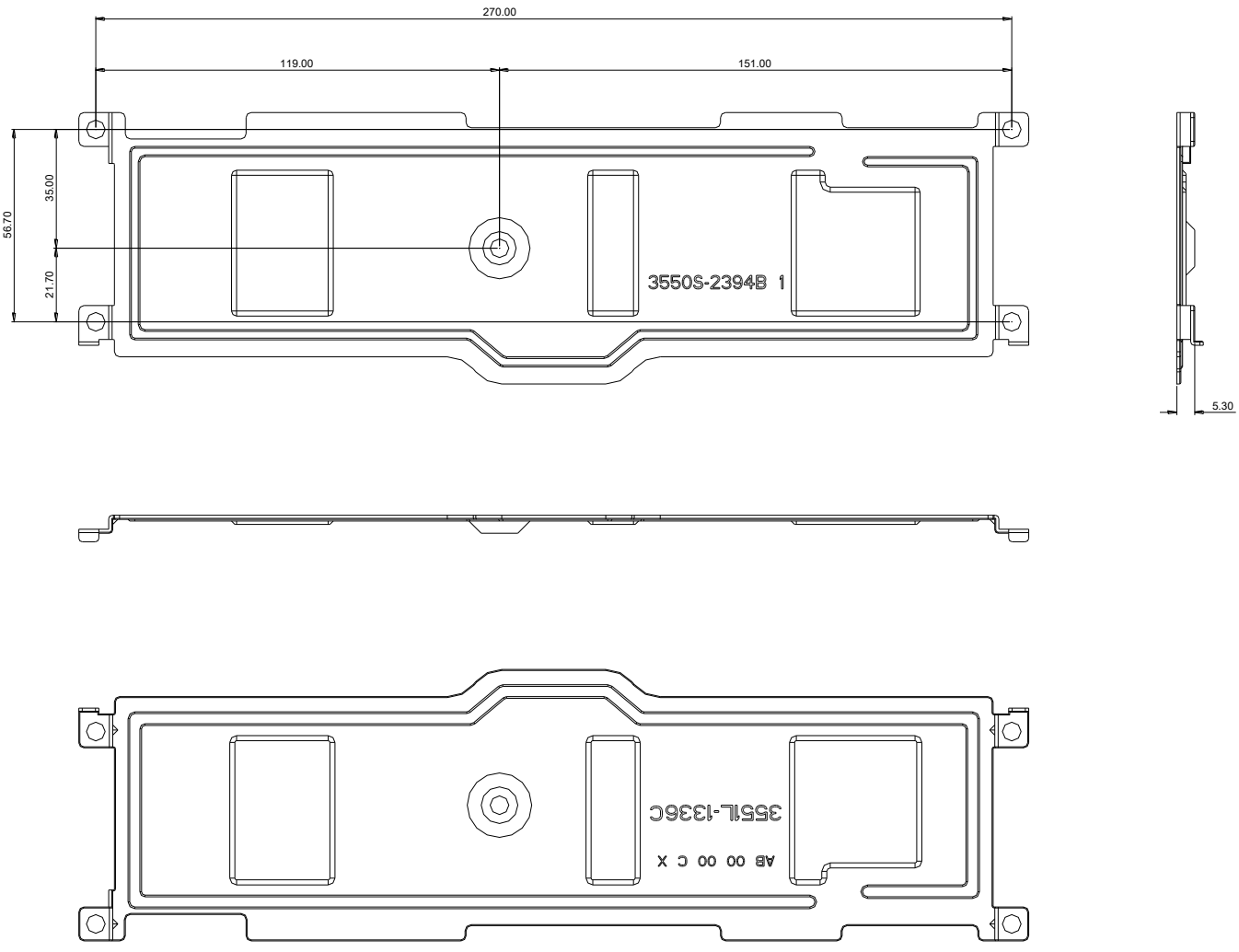
[Control Board Assembly Dimension]



NOTE

1. Unspecified tolerance is ±1.0mm

[Control PCB Shield Dimension]



NOTE

1. Unspecified tolerance is ±1.0mm

6. Reliability

Table 15. ENVIRONMENT TEST CONDITION

No.	Test Item	Condition
1	High temperature storage test	Ta= 60˚C 240h
2	Low temperature storage test	Ta= -20˚C 240h
3	High temperature operation test	Ta= 50˚C 50%RH 240h
4	Low temperature operation test	Ta= 0˚C 240h
5	Pallet packing vibration test (non-operating)	Wave form : random Vibration level : 1.15Grms Bandwidth : 1-200Hz Duration : Z, 60 min
6	Humidity condition Operation	Ta= 40 °C, 90%RH
7	Altitude operating storage / shipment	0 - 15,000 ft 0 - 40,000 ft

7. International Standards

7-1. Safety

(1) UL 60950-1, Underwriters Laboratories Inc.
Information Technology Equipment - Safety - Part 1 : General Requirements.

(2) CAN/CSA-C22.2 No.60065:03, , Canadian Standards Association.
Information Technology Equipment - Safety - Part 1 : General Requirements.

(3) EN 60950-1, European Committee for Electrotechnical Standardization (CENELEC).
Information Technology Equipment - Safety - Part 1 : General Requirements.

(4) IEC 60950-1, The International Electrotechnical Commission (IEC).
Information Technology Equipment - Safety - Part 1 : General Requirements

7-2. Environment

(1) RoHS, Commission Delegated Directive (EU) 2015/863 of 31 March 2015 amending Annex II to Directive 2011/65/EU of the European Parliament and of the Council

8. Packing

8-1. Information of OLED Module Label

(1) Lot Mark

A	B	C	D	E	F	G	H	I	J	K	L	M

A,B,C : SIZE(INCH)
D : YEAR
E : MONTH
F ~ M : SERIAL NO.

Note

1. YEAR

Year	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020
Mark	A	B	C	D	E	F	G	H	J	K

2. MONTH

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Mark	1	2	3	4	5	6	7	8	9	A	B	C

(2) Location of Lot Mark

Serial NO. is printed on the label. The label is attached to the backside of the OLED module.
This is subject to change without prior notice.

8-2. Packing Form

(1) Package quantity in one Pallet : 80 pcs
(10*pcs/Packing * 8packings = Total 80 pcs/pallet)

(2) Pallet Size : 1440 mm(W) X 1140 mm(D) X 1095 mm(H)

9. Precautions

Please pay attention to the followings when you use this OLED Board Assembly.

9-1 Operating Precautions

(1) The spike noise causes the mis-operation of circuits. It should be lower than following voltage :
V=±200mV(Over and under shoot voltage)
(2) Response time depends on the temperature.(In lower temperature, it becomes longer.)
(3) Be careful for condensation at sudden temperature change.Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
(4) When fixed patterns are displayed for a long time, remnant image is likely to occur.
(5) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimized the interference.
(6) Please do not give any mechanical and/or acoustical impact to Module. Otherwise, Module can't be operated its full characteristics perfectly.
(7) A screw which is fastened up the steels should be a machine screw.
(if not, it can causes conductive particles and deal Module a fatal blow)
(8) Please do not set OLED on its edge.

9-2. Electrostatic Discharge Control

Since a Board Assembly is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wrist band etc. And don't touch interface pin directly.
Please refer to design guide for Electrostatic discharging design for BOARD Assembly at the Appendix IX(Page45).

9-3. Precautions for Strong Light Exposure

Strong light exposure causes degradation of polarizer and color filter.

9-4. Storage

When storing modules as spares for a long time, the following precautions are necessary.

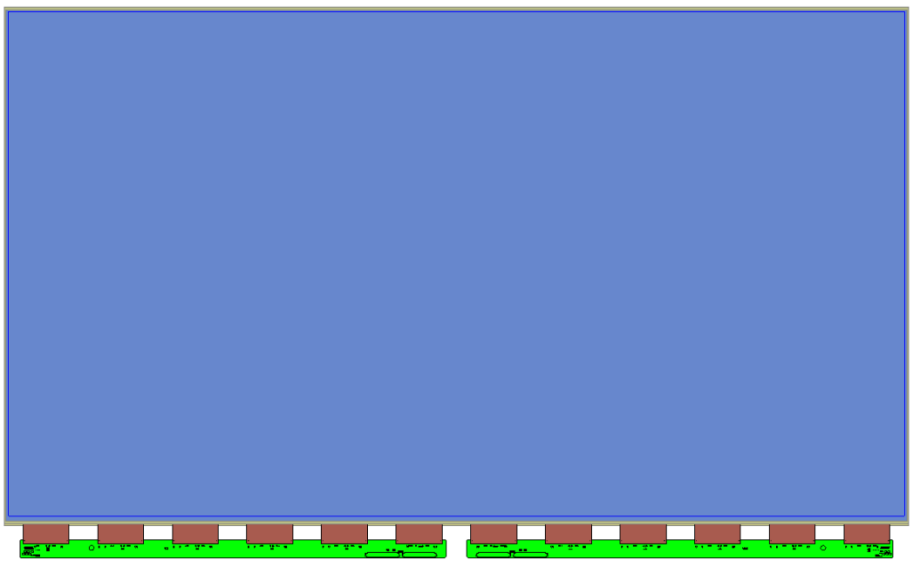
(1) Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5°C and 35°C at normal humidity.
(2) The polarizer surface should not come in contact with any other object.
It is recommended that they are stored in the container in which they were shipped.
(3) Wet bulb temperature should be Max 39°C, and no condensation of water.

9-5. Handling Precautions

(1) The protection film is attached to the bezel with a small masking tape.
When the protection film is peeled off, static electricity is generated between the film and polarizer.
This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.
(2) When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the bezel after the protection film is peeled off.
(3) The Glass Encap surfaces(Rear of Board Assembly) should not be any residual moisture & Salinity.
- Always handle the Board Assembly with gloves.
- Chlorine or water from human sweat can accelerate the corrosion of Glass encapsulation
- Glass Encap surface should be protected by the moisture, salinity

(4) You can remove the glue easily. When the glue remains on the bezel surface or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.
Using a dry towel or fabric, remove water or solution like a cleaner from Board Assembly after finishing the install
- Do not use the cleaner containing acid or chlorine ingredient

(5) Be careful that the washing droplet is not flooded into the border gap on the panel edge, when cleaning the surface of OLED Module. It may cause abnormal operating or a malfunction in the OLED Module.
(6) When the OLED Module is assembled , mechanical stress may not be put on the panel.
(7) Be careful not to place any extra mechanical stress to the OLED module when designing the set .
(8) Be cautious not to any extra strong force (mechanical shock, strong tapping, shooting etc.) to the OLED module. It may cause abnormal operating or a malfunction in the OLED Module.
(9) If the panel is broken, glass should be kept away from the eyes and mouth. When it comes to contact to hands, legs, skin, or clothes, wash thoroughly with soap, and seek medical attention if necessary.
(10) Surface temperature of the Component on PCB should be controlled under 100℃ with TV Set status.
If not, problems such as IC damage or decrease of lifetime could occur.



[Board Assembly]

9-6. Appropriate Condition for Commercial Display

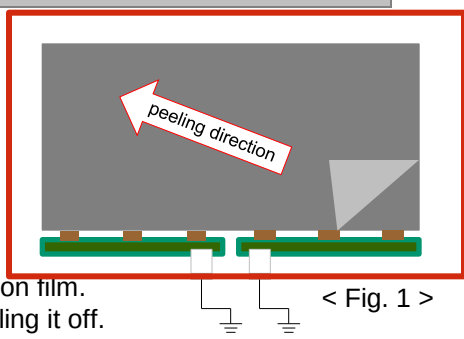
- To extend the lifetime and optimize a function of module, the below-mentioned operating conditions are required.

(1) Normal operating condition
a. Temperature: 20 ± 15 ℃
b. Operating Ambient Humidity : 55 ± 25 %
c. Only for indoor operation.
d. Display pattern: dynamic pattern (Moving picture)
- The sudden image on the screen can be displayed after the static image is shown in the long-term.
e. TFT Compensation should need at least one time in a day.
- Refer to the 3-6-2. TFT compensation operation(Page15).
f. Lifetime in this spec. is guaranteed only when Display is used according to operating usages.

(2) Operating usages under abnormal condition
a. Ambient condition
- Well-ventilated place is recommended to set up Commercial system.

(3) Operating usages to reduce the risk of image sticking due to static image
a. Suitable operating time: under 18 hours a day.
b. OLED compensation should need.
- Refer to the 3-6-3. OLED compensation operation(Page16).
c. Information display recommended to use with moving picture.
d. Logo (image) and characteristics
- Logo image recommended not to use.
If needed, recommend that its position needs to be periodically shifted.
- Change colors themselves periodically.
e. The below-mentioned conditions are not recommended .
- Combination of Logo(or character) and background with largely different luminance.
- Using a single moving picture. (Recommend to use several different moving pictures.)
- The masked image with aspect ratio other than 16:9
- The division of screen
Note1) Abnormal condition just means conditions except normal condition.
Note2) Black image or moving image is strongly recommended as a screen saver.

(4) If the module will be used under severe conditions such as high temperature, high humidity, display patterns or operation time etc., it is strongly recommended to contact LG Display for the advice about usage and applications. Otherwise, its reliability and function may not be guaranteed.



< Fig. 1 >

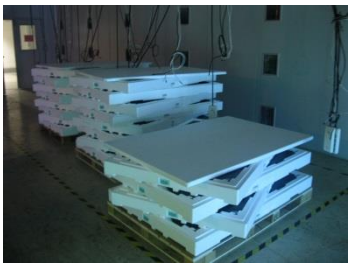
9-7. Protection Film

(1) Please don't remove the protection film before assembly.
(2) Please peel off the protection film slowly.
(3) Please peel off the protection film just like shown in the Fig.1
(4) Ionized air should be blown over during the peeling.
(5) Source PCB should be connected to the ground when peel off the protection film.
(6) The protection film should not be contacted to the source D-IC during peeling it off.

9-8. B/A Box Pretreatment Precautions

In winter season , in particular, please be aware of the following precautions.

(1) Before putting B/A boxes on the line, aging process is required to make the temperature of products similar to the temperature of workplace.
(2) Place the lid open on the B/A box and allowed to stand for 24 hours in the similar environment of work place. It was shown in Fig.2



< Fig. 2>

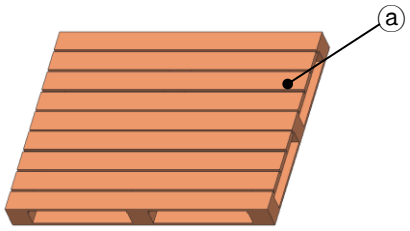
9-9. Packing Precautions

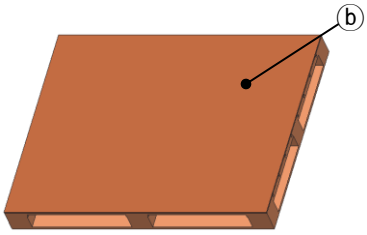
Product assembled into module should be stored in the Al-bag (cover case).

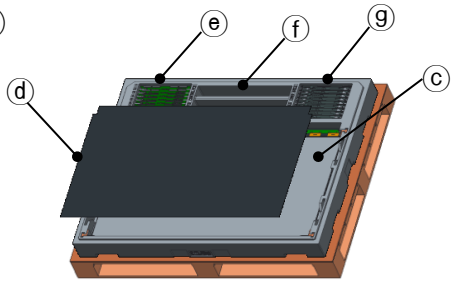
APPENDIX-I

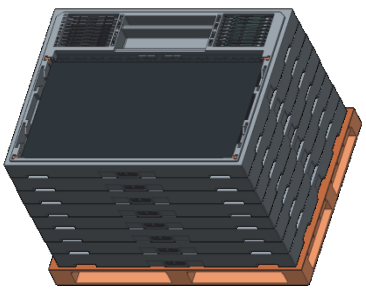
■ Pallet Ass'y

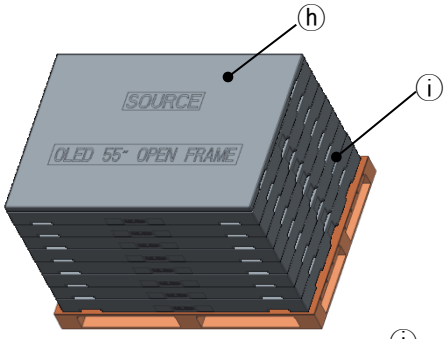
a) B/Ass'y Qty + PE Sheet / Box : 10pcs + 11pcs
b) B/Ass'y Qty / Pallet : 80pcs
c) Box Qty / Pallet : 8Box

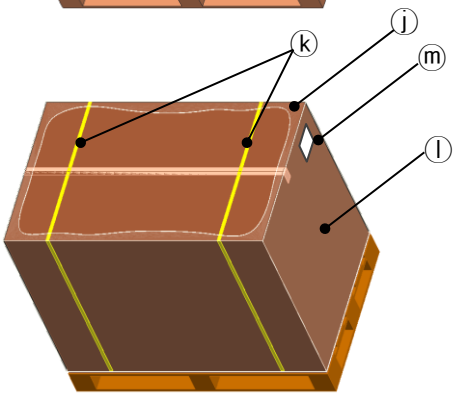
① 

② 

③ 

④ 

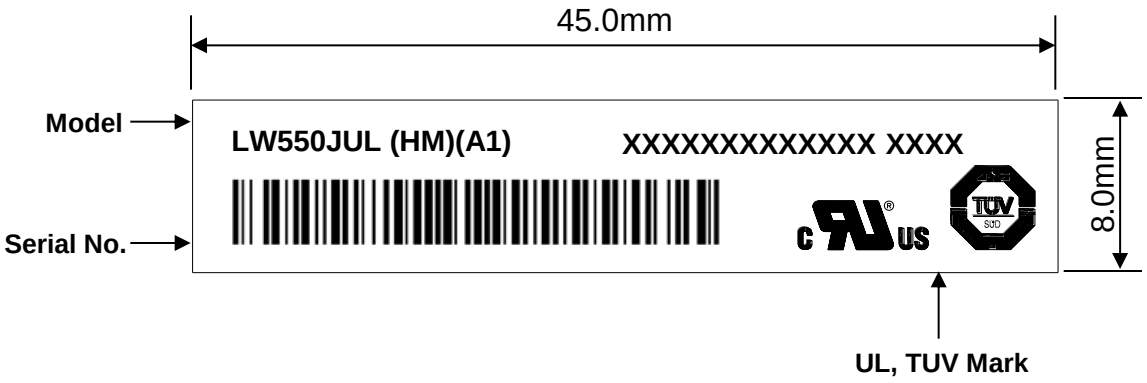
⑤ 

⑥ 

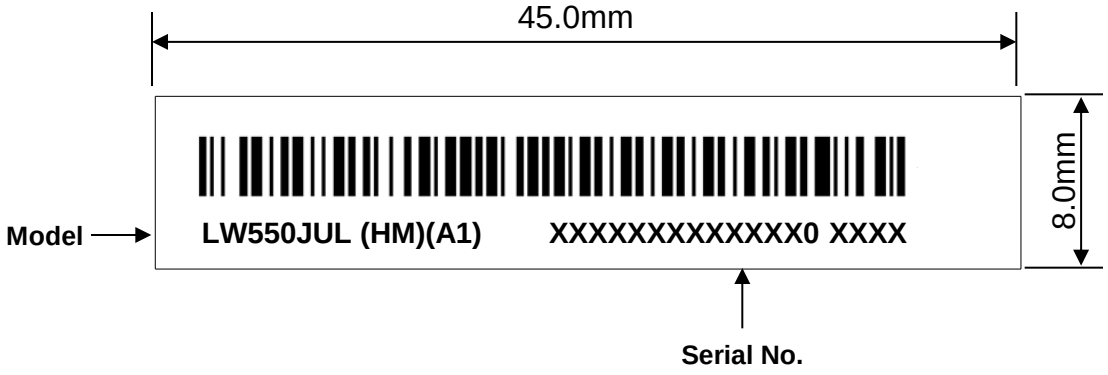
No.	Description	Material
ⓐ	Pallet	Plywood
ⓑ	Carton Plate	Paper(SW)
ⓒ	Board Ass'y	-
ⓓ	PE Sheet	LDPE
ⓔ	Control PCB	PCB
ⓕ	FFC	CABLE
ⓖ	Cover Shield	AL
ⓗ	Top Packing	EPS
ⓘ	Bottom Packing	EPS
ⓙ	Angle Packing	Paper(SW)
ⓚ	Band	PP
ⓛ	Wrap	L-LDPE
ⓜ	Label	YUPO

APPENDIX- II

■ Board Ass'y Label

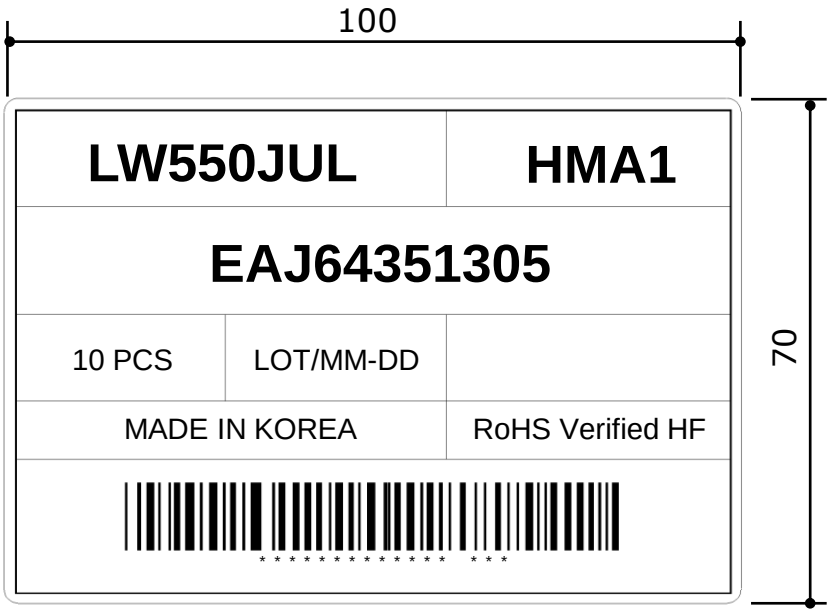


■ Control PCB Label

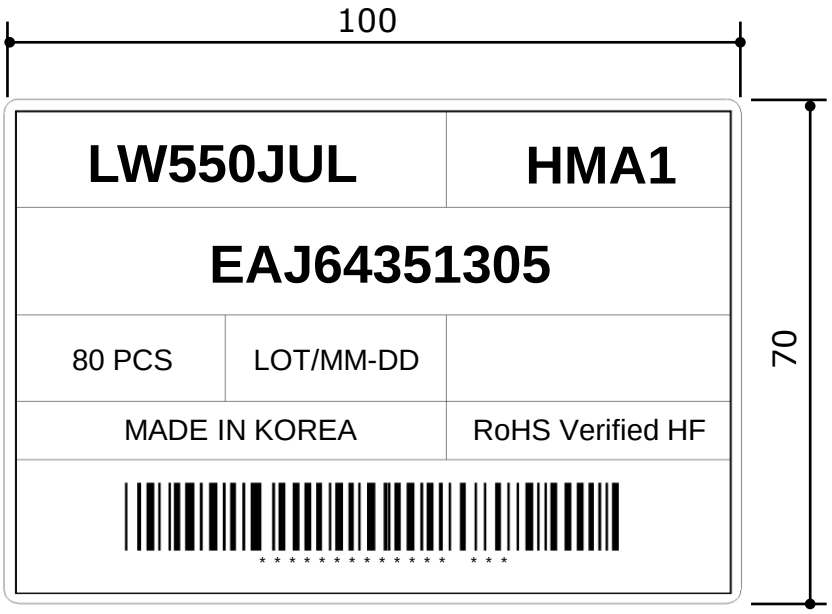


 # APPENDIX- III

■ Box Label

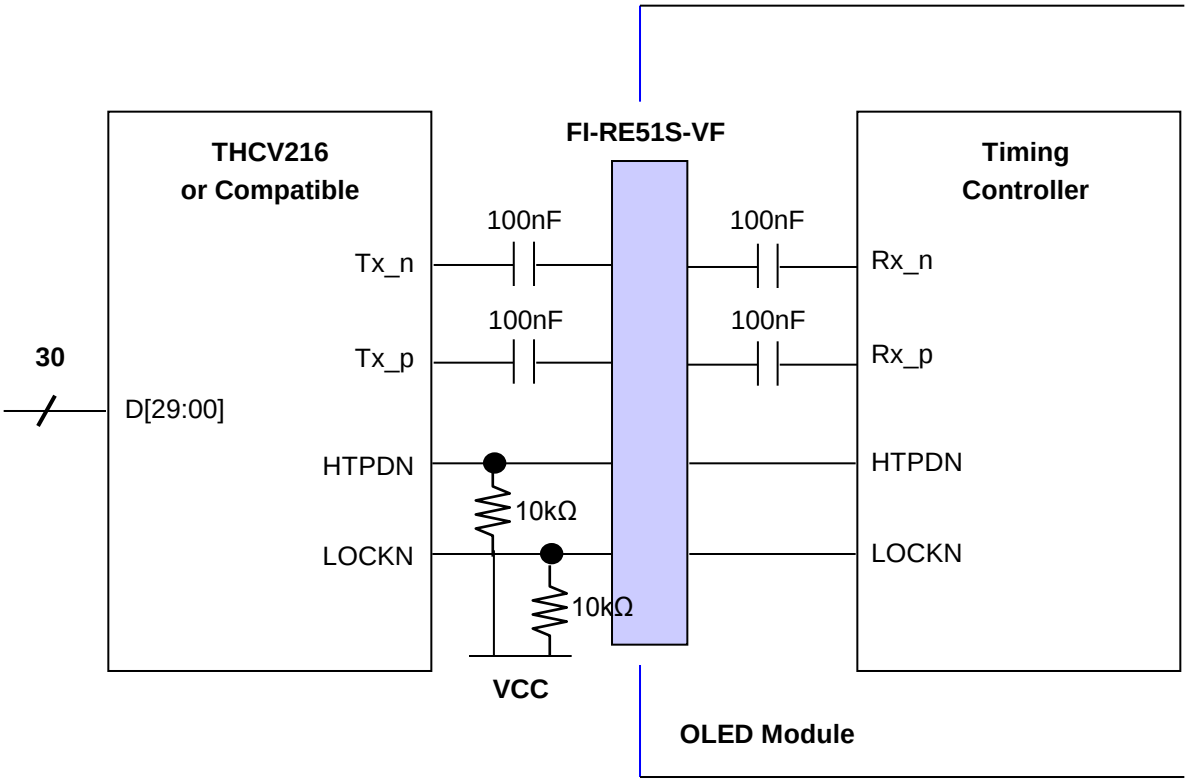


■ Pallet Label



APPENDIX - IV

■ Required signal assignment for Flat Link (Thine : THCV216) Transmitter

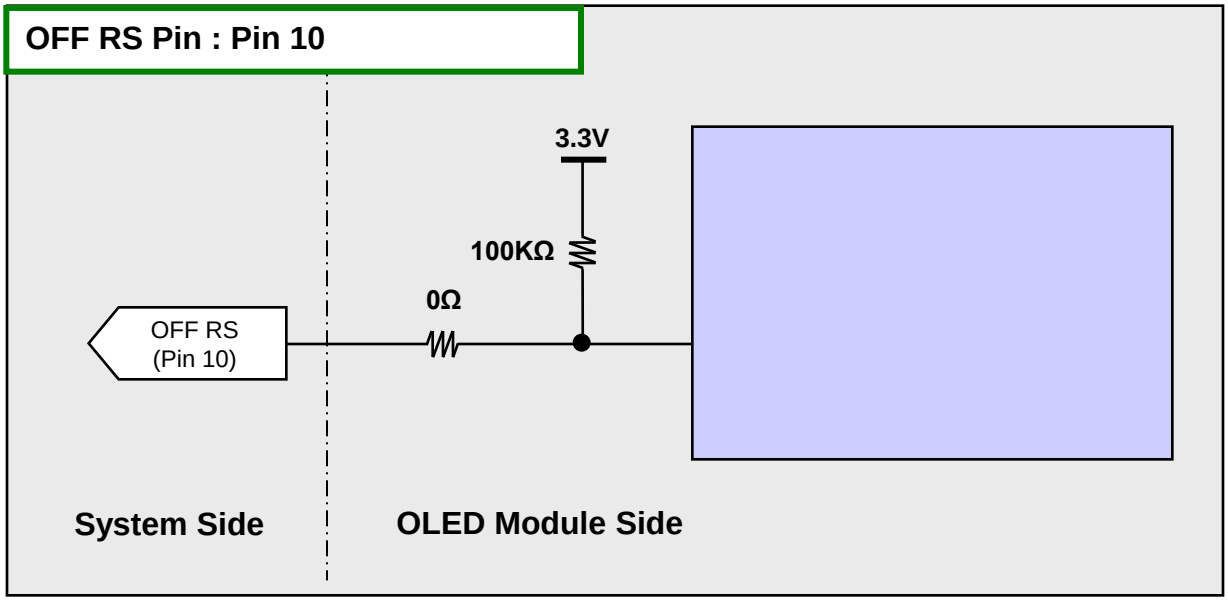


Note: 1. The OLED module uses a 100 nF capacitor on positive and negative lines of each receiver input.
2. Refer to VbyOne Transmitter Data Sheet for detail descriptions. (THCV216 or Compatible)
3. About Module connector pin configuration, Please refer to the Page 7.

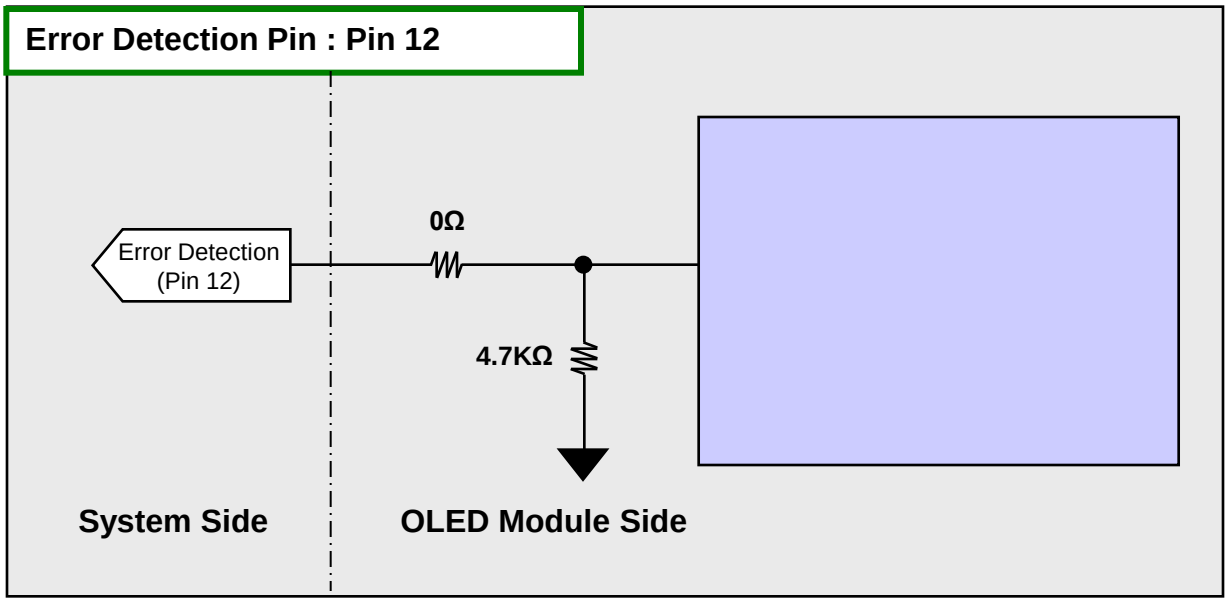
APPENDIX- V-1

■ **Option Pin** Circuit Block Diagram

1) Circuit Block Diagram of **OFF RS** pin



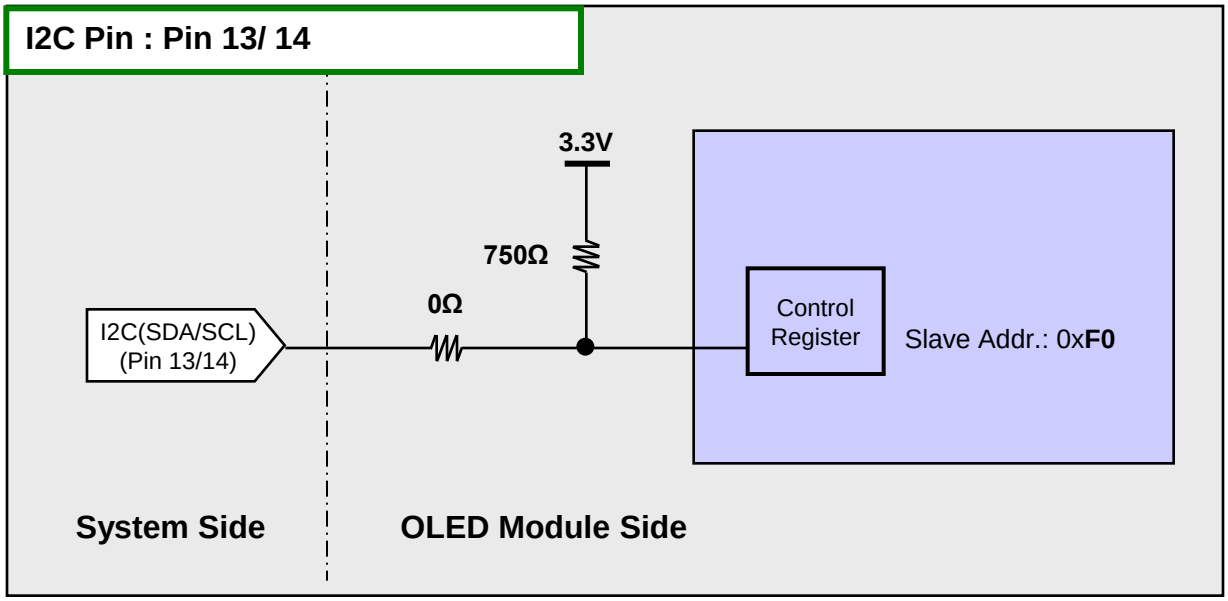
2) Circuit Block Diagram of **Error Detection** pin



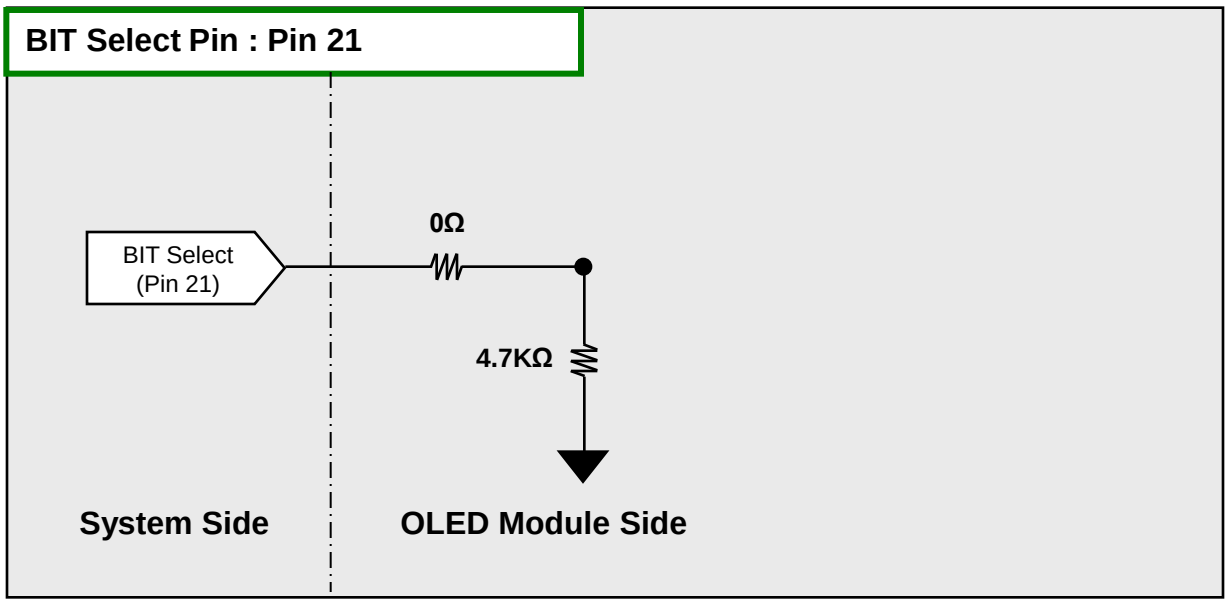
APPENDIX- V-2

■ **Option Pin** Circuit Block Diagram

3) Circuit Block Diagram of **I2C(SDA/SCL)** pin



4) Circuit Block Diagram of **BIT** Selection pin



APPENDIX- VI

■ Register map

The following register is controlled by I2C Interface.

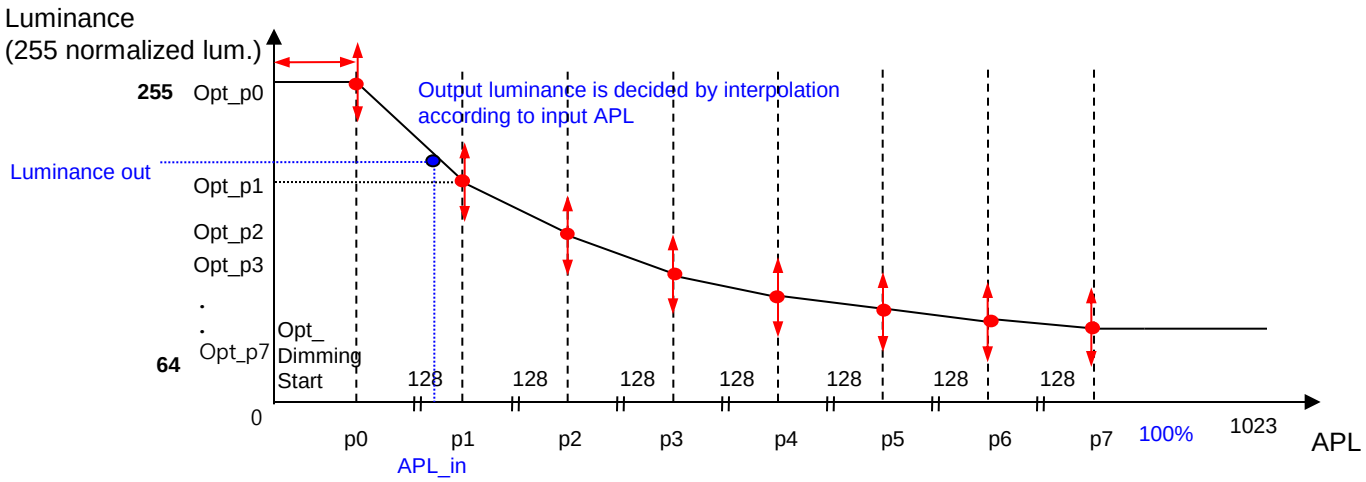
	Bit[7]: MSB	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]: LSB
Addr : 0x001	**Not used**	**TPC EN**	**Not used**	**OFF RS enable**	**Not used**	**Not used**	**Opt_ Dimmin_ start[9]**	**Opt_ Dimming start[8]**

Device Address: 0xF0

Address [10:0]	Register Name	Description	Remark
0x000	Valid	Read only register (LGD use)	
0x001	[7] : Not used	LGD reserved	
	[6] : TPC enable	1: enable (default), 0: disable	
	[5] : Not used	LGD reserved	
	[4] : Off RS enable	1: enable, 0: disable	
	[3] : Not used	LGD reserved	
	[2] : Not used	LGD reserved	
	[1:0] Opt_Dimming_start[9:8]	APL value of P0 point	
0x002	Opt_Dimming_start[7:0]		
0x003	Opt_p0	APL P0 point corresponds to the 255 normalized luminance	(Opt_p0 /114) * 200 nit
0x004	Opt_p1	APL P1 point corresponds to the 255 normalized luminance	(Opt_p1 /114) * 200 nit
0x005	Opt_p2	APL P2 point corresponds to the 255 normalized luminance	(Opt_p2 /114) * 200 nit
0x006	Opt_p3	APL P3 point corresponds to the 255 normalized luminance	(Opt_p3 /114) * 200 nit
0x007	Opt_p4	APL P4 point corresponds to the 255 normalized luminance	(Opt_p4 /114) * 200 nit
0x008	Opt_p5	APL P5 point corresponds to the 255 normalized luminance	(Opt_p5 /114) * 200 nit
0x009	Opt_p6	APL P6 point corresponds to the 255 normalized luminance	(Opt_p6 /114) * 200 nit
0x00A	Opt_p7	APL P7 point corresponds to the 255 normalized luminance	(Opt_p7 /114) * 200 nit

Address [10:0]	Register Name	Description	Remark
0x00B	[7] : Not used	LGD reserved	
	[6:5] : Not used	LGD reserved	
	[4] : LEA refresh mode en	1: LEA disable , 0: LEA enable (default)	
	[3:0] : Not used	LGD reserved	

❑ PLC curve parameter

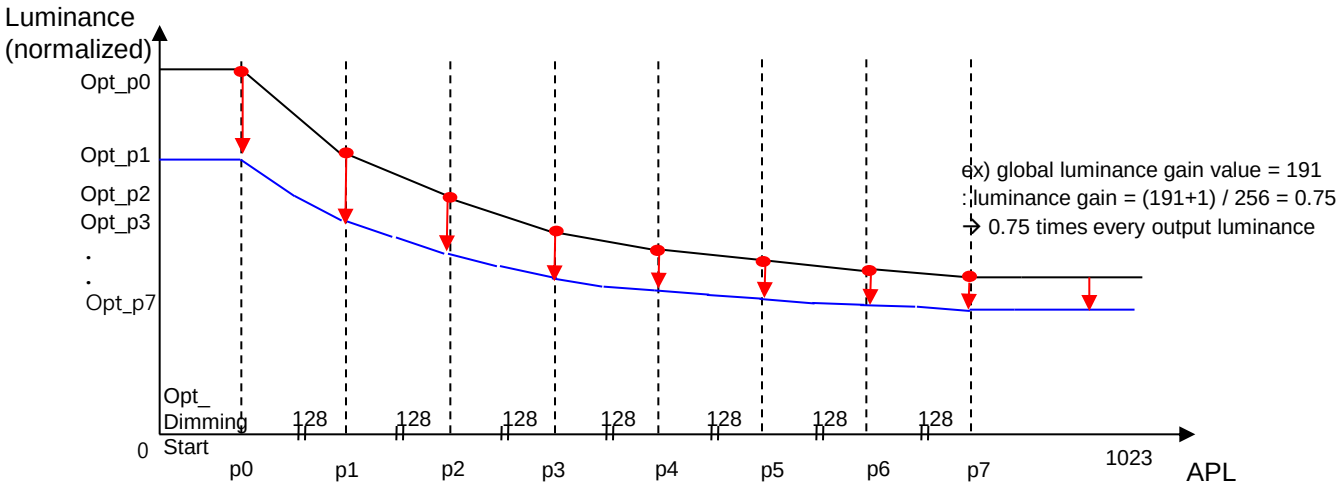


Every interval between each points except P0 is fixed to 128

- Luminance of p7~1023 interval are Opt_p7
- The point over 1023 is discarded

Address [10:0]	Register Name	Description	Remark
0x016	Opt_global_luminance_gain	Adjust global luminance gain 0~1 luminance gain according to 0~255 value (Same luminance gain is applied to every P0~P7 points)	Value Range: 0~255
0x05D	[7] vsJB_en	1: Enable, 0: Disable	
	[6:0] Not used	LGD reserved	
0x05E	Test_temp2[15:8]	1st temperature sensor	Read only
0x05F	Test_temp2[7:0]		

❑ Global luminance gain



❑ VLC Parameter

Address [11:0]	Register Name	Description	Remark
0x040	VLC_param_on_in [1:0]	**VLC Enable** "00" : VLC Off, "11" : VLC On	
	VLC_param_window_size_in[3:2]	**Peak gain Running Average Frame number** "00": not used , "01" : 2 frame, "10" : 4 frame, "11" : 8 frame	
0x041	VLC_param_hys_threshold_in [7:0]	**Hysteresis Threshold** Changes below the threshold value in the minus direction from the current value are not reflected	
0x048	VLC_param_my_M_ID_in_MSB [1:0]	**My Module ID (10bit)** Set ID, Min. 1 ~ Max. 1000 **(0, 1001~1023 : Do not use)**	
0x049	VLC_param_my_M_ID_in_LSB [7:0]		
0x04A	VLC_param_my_picture_ID_MSB [1:0]	**Picture ID (10bit)** Set group ID (1~1023)	
0x04B	VLC_param_my_picture_ID_MSB[7:0]		
0x04C	VLC_param_Peak_MSB [1:0]	**VLC final peak luminance value (10bit)**	**Read only**
0x04D	VLC_param_Peak_LSB [7:0]		
0x04E	VLC_param_tx_cnt_out_MSB [1:0]	**VLC Tx. Counter value (10bit)**	**Read only**
0x04F	VLC_param_tx_cnt_out_LSB [7:0]		
0x050	VLC_param_init_ACL_in _MSB [1:0]	**VLC Initial peak luminance value (10bit)** Output with set peak luminance (0 ~ 1023)	
0x051	VLC_param_init_ACL_in_LSB [7:0]		

 # APPENDIX- VII-1

Gray to Gray Response Time Uniformity

This is only the reference data of G to G and uniformity for LW550JUL-HMA1 model.

1. G to G Response Time :
   Response time is defined as FIG.1. and shall be measured by switching the input signal for "Gray (N) " and "Gray(M)".(32Gray Step at 8bit)

2. G to G Uniformity
   The variation of G to G Uniformity , $\delta_{G\ to\ G}$ is defined as :

$$\text{G to G Uniformity} = \frac{Maximum(GtoG) - Typical(GtoG)}{Typical(GtoG)} \leq 1$$

*Maximum (GtoG) means maximum value of measured time (N, M = 0 (Black) ~ 1023(White), 128 gray step).

	0Gray	127ray	255Gray	…	895Gray	1023Gray
0Gray		TrR:0G→127G	TrR:0G→255G	…	TrR:0G→895G	TrR:0G→1023G
127Gray	TrD:127G→0G		TrR:127G→255G	…	TrR:127G→895G	TrR:127G→1023G
255Gray	TrD:255G→0G	TrD:255G→127G		…	TrR:255G→895G	TrR:255G→1023G
…	…	…	…		…	…
895Gray	TrD:895G→0G	TrD:895G→127G	TrD:895G→255G	…		TrR:895G→1023G
1023Gray	TrD:1023G→0G	TrD:1023G→127G	TrD:1023G→255G	…	TrD:1023G→895G	

3. Sampling Size : 2 pcs

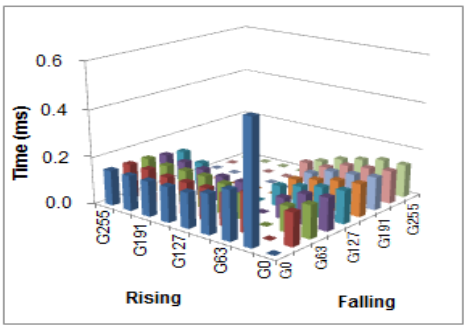
4. Measurement Method : Follow the same rule as optical characteristics measurement.

5. Current Status

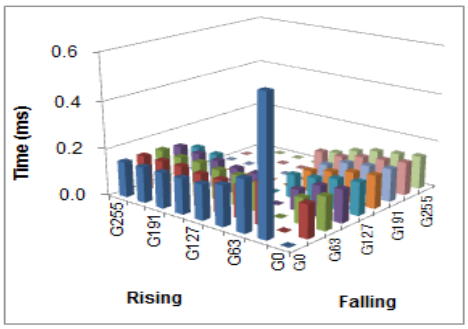
   Below table is actual data of production on **12. 10. 2018 (LGD DV Event Sample)**

	G to G Response Time [ms]		Average
	Min.	Max.	
# 1	0.07	0.51	0.14
# 2	0.07	0.57	0.14

FIG. 1



< # 1 >



< # 2 >

APPENDIX- VII-2

■ MPRT Response Time Uniformity (δ_{MPRT})

This is only the reference data of MPRT and uniformity for LW550JUL-HMA1 model.

1. MPRT Response Time :
   Response time is defined as FIG. 2.

2. MPRT Uniformity
   The variation of MPRT Uniformity , δ_{MPRT} is defined as :

$$\text{MPRT Uniformity} = \frac{Maximum\ (MPRT) - Typical\ (MPRT)}{Typical\ (MPRT)} \leq 1$$

3. Sampling Size : 2 pcs

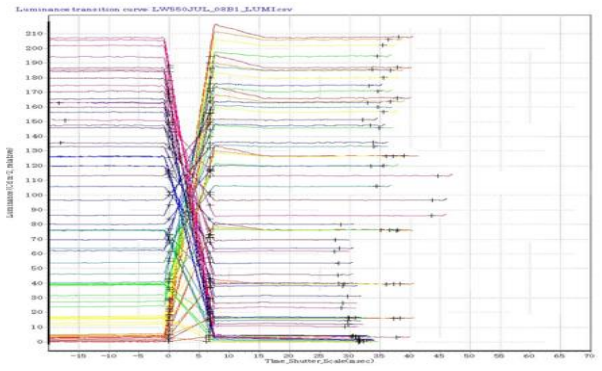
4. Measurement Method : Follow the same rule as optical characteristics measurement.

5. Current Status

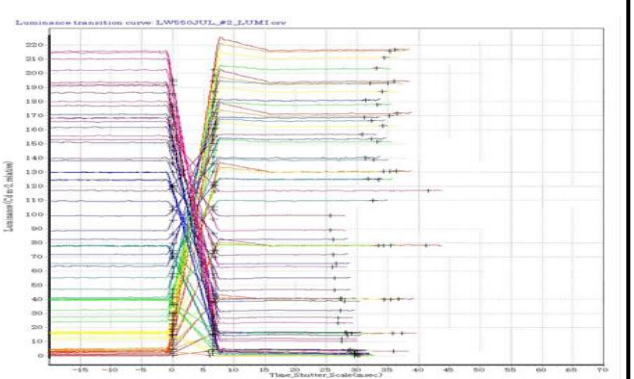
   Below table is actual data of production on **12. 10. 2018 (LGD DV Event Sample)**

Sample	MPRT Response Time [ms]		Average
	Min.	Max.	
# 1	6.40	6.80	6.70
# 2	6.50	6.80	6.70

FIG. 2



Sample #1		Final Value								
	Gray	G255	G223	G191	G159	G127	G95	G63	G31	G0
Initial Value	G255	-	6.7	6.7	6.7	6.7	6.7	6.7	6.7	6.7
	G223	6.6	-	6.7	6.7	6.7	6.7	6.7	6.7	6.7
	G191	6.7	6.7	-	6.7	6.7	6.7	6.7	6.7	6.7
	G159	6.6	6.7	6.8	-	6.7	6.7	6.7	6.7	6.7
	G127	6.7	6.7	6.7	6.7	-	6.7	6.7	6.7	6.6
	G95	6.7	6.7	6.7	6.7	6.7	-	6.7	6.6	6.6
	G63	6.7	6.7	6.7	6.7	6.7	6.7	-	6.6	6.6
	G31	6.7	6.6	6.6	6.6	6.7	6.7	6.6	-	-
	G0	6.7	6.7	6.6	6.7	6.6	6.6	6.4	-	-

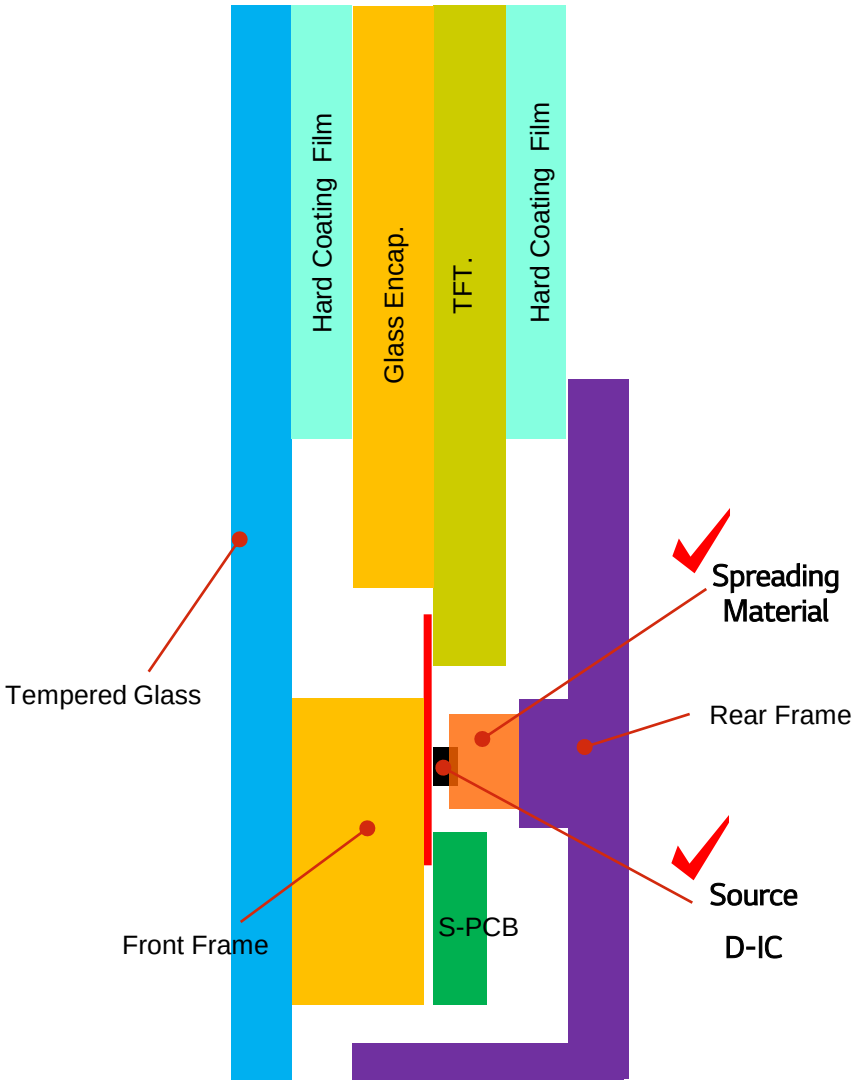


Sample #2		Final Value								
	Gray	G255	G223	G191	G159	G127	G95	G63	G31	G0
Initial Value	G255	-	6.8	6.7	6.7	6.7	6.7	6.7	6.7	6.7
	G223	6.7	-	6.7	6.7	6.7	6.7	6.7	6.7	6.7
	G191	6.7	6.7	-	6.7	6.7	6.7	6.7	6.7	6.7
	G159	6.7	6.7	6.7	-	6.7	6.7	6.7	6.7	6.7
	G127	6.7	6.7	6.7	6.7	-	6.7	6.7	6.7	6.7
	G95	6.7	6.7	6.7	6.7	6.8	-	6.8	6.7	6.6
	G63	6.7	6.7	6.7	6.7	6.7	6.7	-	6.7	6.6
	G31	6.7	6.7	6.7	6.7	6.7	6.6	6.6	-	-
	G0	6.7	6.7	6.7	6.7	6.7	6.6	6.5	-	-

APPENDIX- VIII

■ Design guide for Heat dissipation for SOURCE D-IC

1. Potential issue
   The heat transfer efficiency down if D-IC is not contacted.
2. Recommendation
   In case of using Heat spreading sheet
   1) Contact the SOURCE D-IC with embossment on Heat spreading sheet for heat dissipation.
   2) Not be overlapped much to prevent COF damage.
   3) The contact area to exceed the area of the SOURCE D-IC.



APPENDIX- IX

■ Design guide for Electrostatic Discharging design for Board Assembly

1. Purpose
   To design the contact structure for electrostatic discharging on Board Assembly
2. Recommendation
   Electrostatic discharging design for Board Assembly (Ground Path)
   1) To design the contact structure for electrostatic discharging on Board Assembly
   2) Attach Conductive Tape or Equivalent between S-PCB Ground and Set Ground