050SVGA Active Matrix Color OLED Panel Module

1. Overview/Application

SVGA050 AMOLED micro display fabricated by top emitting and high luminance efficiency Si-Base AMOLED technology with proprietary intellectual property rights. Characterized by low power consumption, high resolution (SVGA 800×600) and miniaturization, etc. SVGA050 supports less than or equal to SVGA resolutions format. With proper optic enhancement devices, SVGA050 micro display can provide high quality, large virtual image.

SVGA050 micro display's silicon substrate is fabricated by 0.18um CMOS technology, integrated full digital video signal processing and 804×604×3 active driving units. The input video signal is compatible with ITU-R BT. 656/601 and support 8/16/24 bit digital video. The function of micro display such as display mode, scanning direction, display position, brightness, contrast, R/G/B offset and gamma correction can be programmed through the two-wire serial communication interface. The digital interface voltage level is compatible with 1.8~3.3V CMOS standard. The micro display can be applied in various near-to-eye display systems that demand compact size, high resolution, low power consumption and wide working temperature range.

(Potential applications: Virtual Reality application（AR/VR）, Head mounted displays, Near-Eye Displays etc.)

2. Features

- Si-Base AMOLED Micro Display
  --0.18μm CMOS Technology
  --Full Digital Video Core
  --Active Driver Technology
  --High Efficiency Top Emission Structure
- 800×600 (SVGA) Resolution
  --View Area: 0.5 inch
  --Pixel Pitch: 12.6um×12.6um
  --Total Pixels: 804(×3)×604
  --PPI: 2000
- Digital Video Interface
  --Compatible with ITU-R BT.656/601
  --Accept 8/16/24 Bit Digital Video
  --Accept YCbCr/RGB Color or Mono
  --Support PAL/NTSC/SMPTE etc.
  --Support Progressive & Interlaced
- Digital Video Signal Enhancement
  --Brightness
  --Contrast
  --R/G/B Chromaticity Adjustment
- Gamma Correction
  --Piecewise-Linear by 17 Entry Lookup Table
  --Expand 8bit Input to 9bit Output
- Digital 8 Bit Input/9bit Output Gray Level
- Support Binocular Stereovision
- Horizontal/Vertical Mirror
- Shift and Position Control
- Embed Temperature Sensor
- Integrate Vcom DC-DC Module
- Built-in Test Patterns
- 2-Wire Series Interface

3. Module Structure

Active matrix color OLED display with on-chip driver based on single crystal silicon transistors

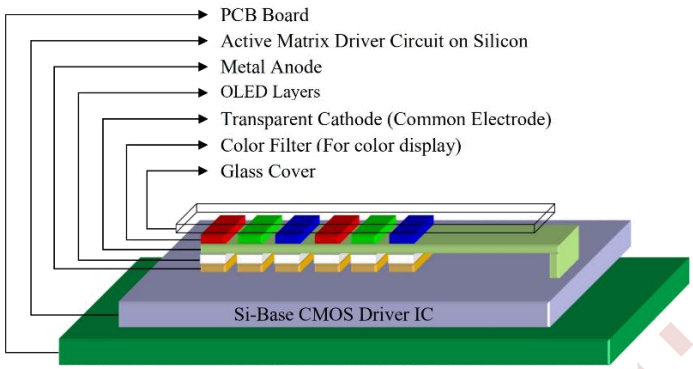


Figure 3-1 Structure of SVGA050 Micro Display Device

4. System Block Diagram

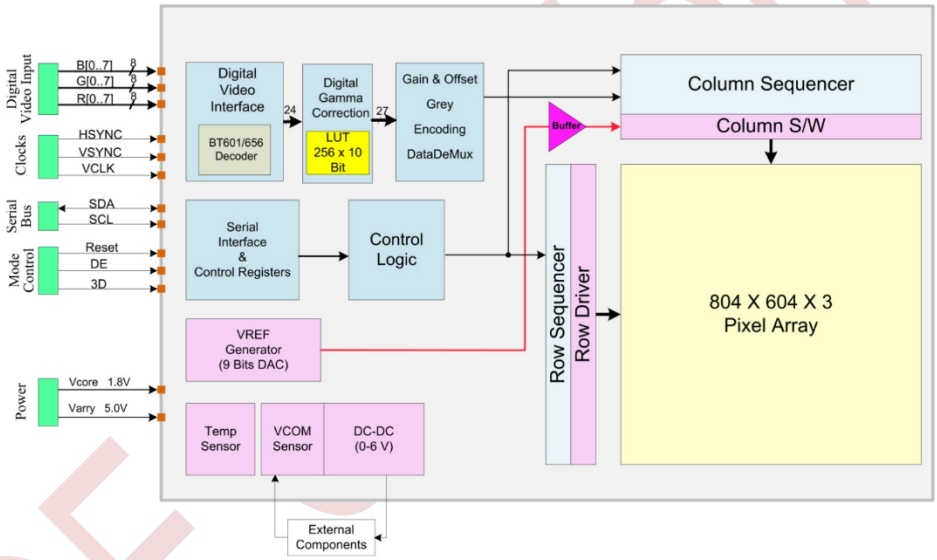


Figure 4-1 SVGA050 Architecture & Block Diagram

5. Pin Description

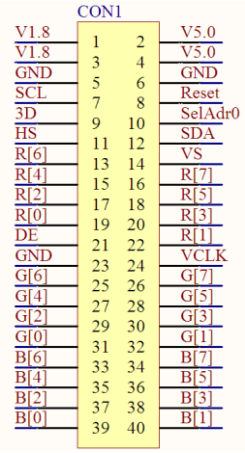


Figure 5-1 Connector PIN Map

5.1 Pin description of PCB Module

Pin No.	Signal	Type	Function	Remark
1	V1.8	P	1.8V Power，Core Power Suply	
2	V5.0	P	5.0V Power，OLED Pixels driver Power Suply	
3	V1.8	P	1.8V Power，Core Power Suply	
4	V5.0	P	5.0V Power，OLED Pixels driver Power Suply	
5	GND	P	0V Ground	
6	GND	P	0V Ground	
7	SCL	I	Serial Port Clock	
8	Reset	I	Master Reset, Active Low	Can't Floating
9	3D	I	3D Mode Select	If not use, pull-
10	SelAdr0	I	Serial Port Address select	Default pull-up
11	HS	I	Hsync Signal Input	
12	SDA	I/O	Serial Port Data I/O	
13	R[6]	I	Cr [6]/R[6] Video Input	
14	VS	I	Vsync Signal Input	
15	R[4]	I	Cr [4], Red[4] Video Data Input	
16	R[7]	I	Cr [7], Red[7] Video Data Input (MSB)	
17	R[2]	I	Cr [2], Red[2] Video Data Inpu	
18	R[5]	I	Cr [5], Red[5] Video Data Inpu	
19	R[0]	I	Cr [0], Red[0] Video Data Inpu	
20	R[3]	I	Cr [3], Red[3] Video Data Inpu	
21	DE	I	Data Enable Signal Input	
22	R[1]	I	Cr [1], Red[1] Video Data Inpu	
23	GND	P	0V Ground	
24	VCLK	I	Pixel Clock Input	
25	G[6]	I	YCbCr[6], Y[6], Green[6] Video Data Input	
26	G[7]	I	YCbCr[7], Y[7], Green[7] Video Data Input (MSB)	
27	G[4]	I	YCbCr[4], Y[4], Green[4] Video Data Input	
28	G[5]	I	YCbCr[5], Y[5], Green[5] Video Data Input	
29	G[2]	I	YCbCr[2], Y[2], Green[2] Video Data Input	
30	G[3]	I	YCbCr[3], Y[3], Green[3] Video Data Input	
31	G[0]	I	YCbCr[0], Y[0], Green[0] Video Data Input (LSB)	
32	G[1]	I	YCbCr[1], Y[1], Green[1] Video Data Input	
33	B[6]	I	CbCr[6], Cb[6], Blue[6] Video Data Inpu	
34	B[7]	I	CbCr[7], Cb[7], Blue[7] Video Data Input (MSB)	
35	B[4]	I	CbCr[4], Cb[4], Blue[4] Video Data Inpu	
36	B[5]	I	CbCr[5], Cb[5], Blue[5] Video Data Input	
37	B[2]	I	CbCr[2], Cb[2], Blue[2] Video Data Inpu	
38	B3]	I	CbCr[3], Cb[3], Blue[3] Video Data Input	
39	B[0]	I	CbCr[0], Cb[0], Blue[0] Video Data Input (LSB)	
40	B[1]	I	CbCr[1], Cb[1], Blue[1] Video Data Input	

6. Absolute Maximum Ratings

SIGNAL	FUNCTION	MIN	TYP	MAX	UNIT
V1.8	1.8V Power, Core Power Suply	1.62	1.8	2.5	V
V5.0	5.0V Power, OLED Pixels driver Power Suply	4.5	5.0	6.0	V
$V_{I/O}$	Digital Signal Voltage②	—	1.8	3.3	V
T-storage	Storage Temperature	-55 ~ 90			°C
T-operate	Operation Temperature	-40 ~ 65			°C

Notes:

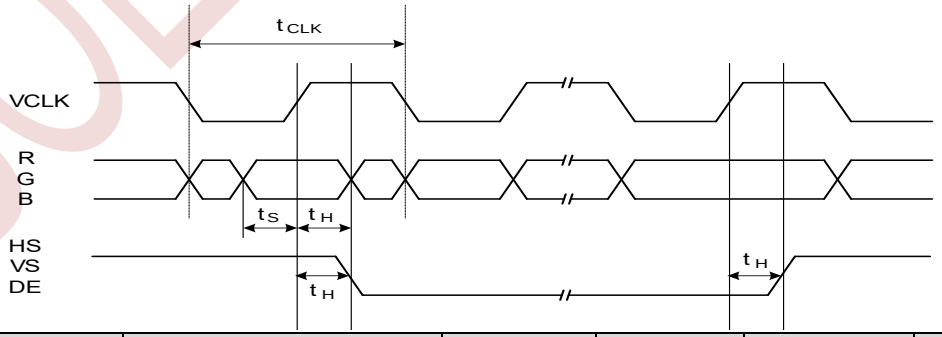
1. The absolute maximum rating values (except VI/O) of this product are not allowed to be exceeded at any time. If the product is used with its symbol value exceeding the maximum rating or in an extreme condition, the characteristics of the device maybe recovered and the lifetime of the device will decrease, even the device may be permanently destroyed.
2. Digital logic Pins (except the Power Pin) can support 1.8V/3.3V CMOS logic level.

7. Electrical Characteristics

7.1 DC Characteristics

PARAMETER	FUNCTION DESCRIPTION		MIN	TYP	MAX	UNIT
$I_{1.8}$	1.8V Power Current		9	10	12	mA
$I_{5.0}$	5.0V Power Current		4	8.5	250	
Vcom	Cathode Voltage		-5	-2	0	V
Typical Power Consumption	Working	Color (200Cd/m²)	80	120	200	mW
	Display Off		71	—	75	
	Power Down		0	—	0.4	

7.2 AC Characteristics



x	Symbol	MIN	TYP	MAX	UNIT
Digital Video Data Setup & Hold	t_S	1	-	-	ns
	t_H	0.5	-	-	ns
Video Clock Period	t_{CLK}	17.8	-	-	ns
Video Clock Duty	q	40	50	60	%

8. Power Supply Sequence

8.1 Power On/Off Sequence

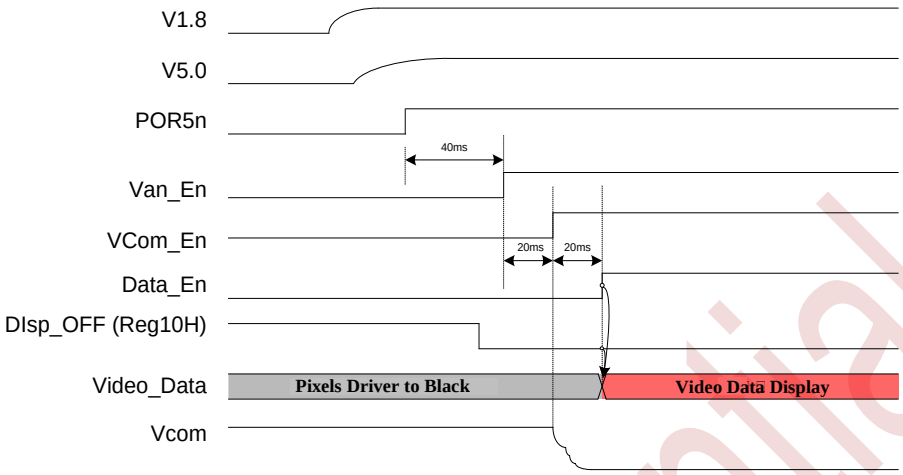


Figure 8-1 Power-on Sequence (1.8V power-on, threshold voltage = 1.2V)

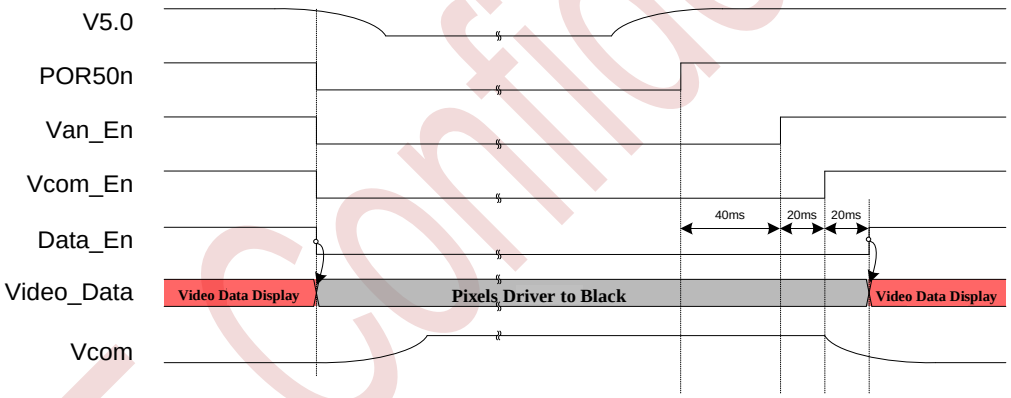


Figure 8-2 V5.0 Power Off & On (POR5n threshold Voltage = 4V)

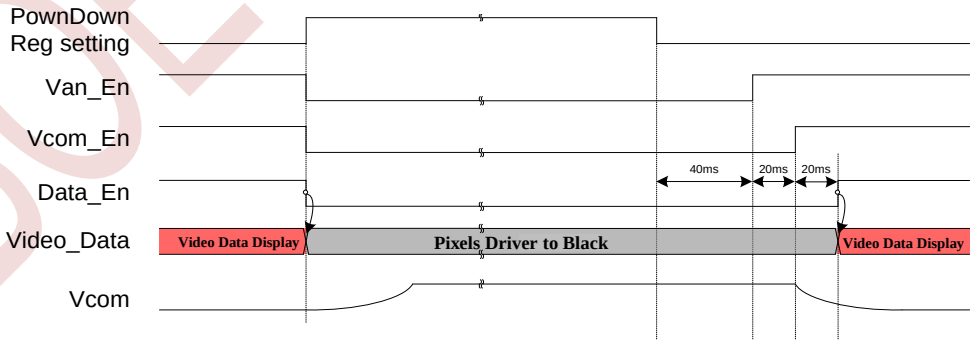


Figure 8-3 Register Control Power Off & On

8.2 Reset Sequence

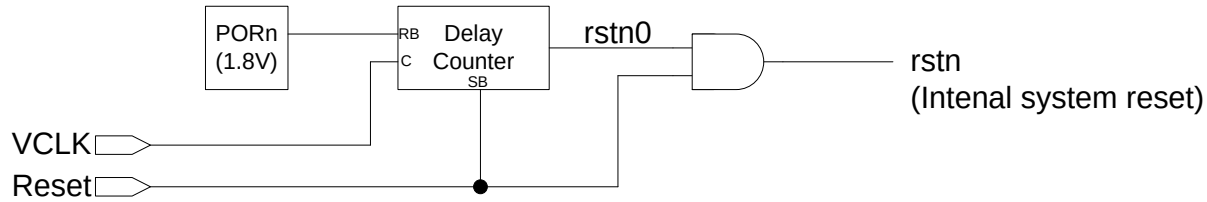


Figure 8-4 Reset Block Diagram

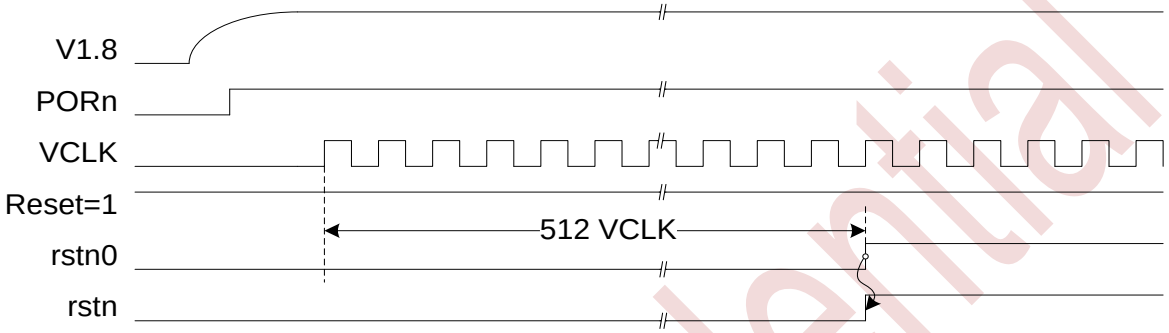


Figure 8-5 Reset Timing Case 1 – No external reset pin used (RESETB=1)

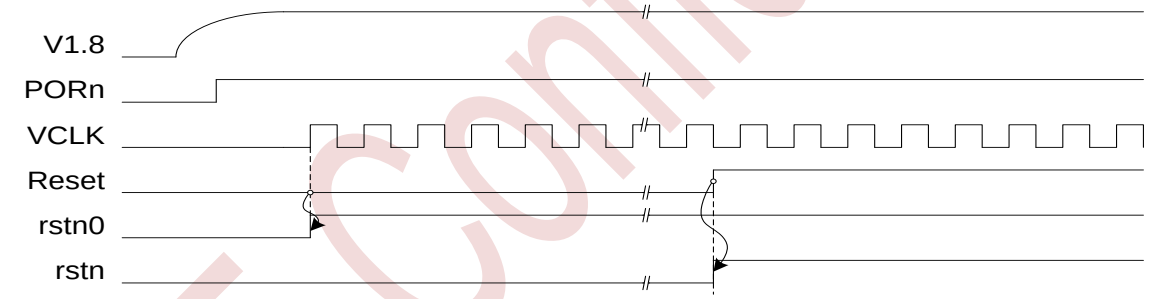


Figure 8-6 Reset Timing Case 2 – External reset pin depend on VCLK

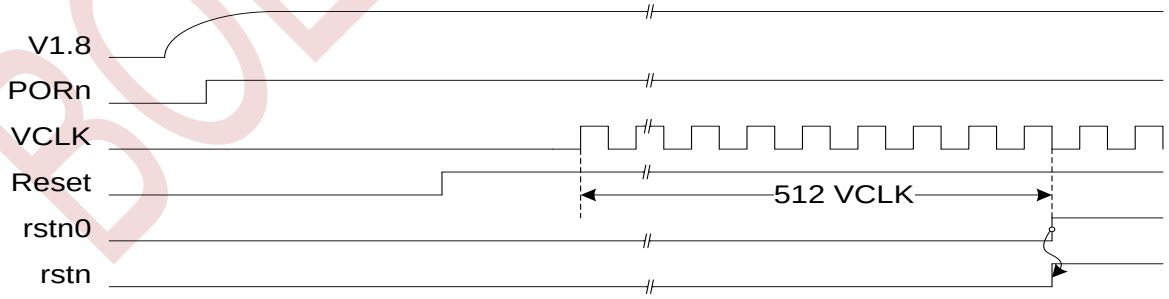


Figure 8-7 Reset Timing Case 3 – External reset pin applied

9. Description of Function

9.1 Digital Video Interface

The digital video interface has three 8-bit data channels, and additional horizontal and vertical sync (HS/VS), data enable (DE), pixel clock signals (VCLK). User should select the correct signals to connect according to different Video format. VCLK is always needed in any mode. When use 8bit with embedded sync signal (8bit ITU-R BT.656 YCbCr/Mono 4:2:2), only G[7..0] bus and VCLK is needed. Figure 9-1 shows digital video processing flow.

OLED Display receives data with BT601/656 format, like 8/16/24bit and 4:2:2/4:4:4 format, and transfers to 24bit 4:4:4 format RGB signal, then sends the signal to Video signal enhancement module, after scaling (only a scaled-down), gamma correction, RGB offset adjustment, finally outputs 27bit RGB signal (3*9bit).

If the input video format is CVBS, component, VGA (analog RGB), HDMI, DVI video signals, etc., an external video decoder is required, such as ADV7180, AD9883, TVP7002 and so on.

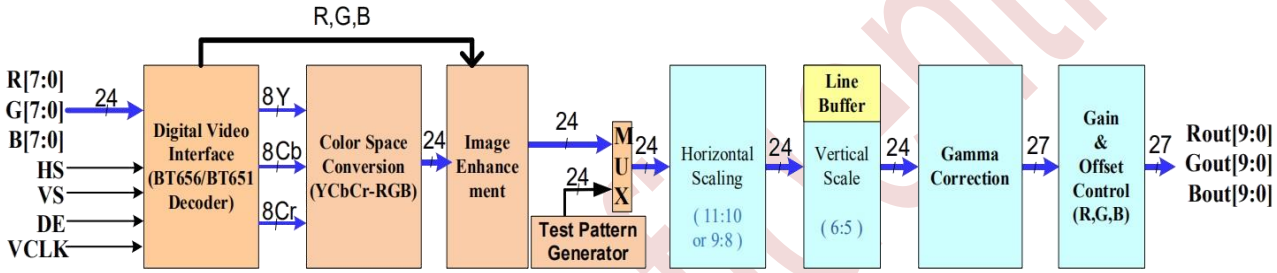


Figure 9-1 Digital Video Processing Flow Diagram

9.1.1 Input Video Standard

Video Standard	Color Space	PIN		
		R[7:0]	G[7:0]	B[7:0]
8-bit, 4:2:2	YCbCr	-	YCbCr[7:0]	-
8-bit, Mono	Y	-	Y[7:0]	-
16-bit, 4:2:2	YCbCr	-	Y[7:0]	CbCr[7:0]
24-bit, 4:4:4	YCbCr	Cr[7:0]	Y[7:0]	Cb[7:0]
24-bit, 4:4:4	RGB	R[7:0]	G[7:0]	B[7:0]

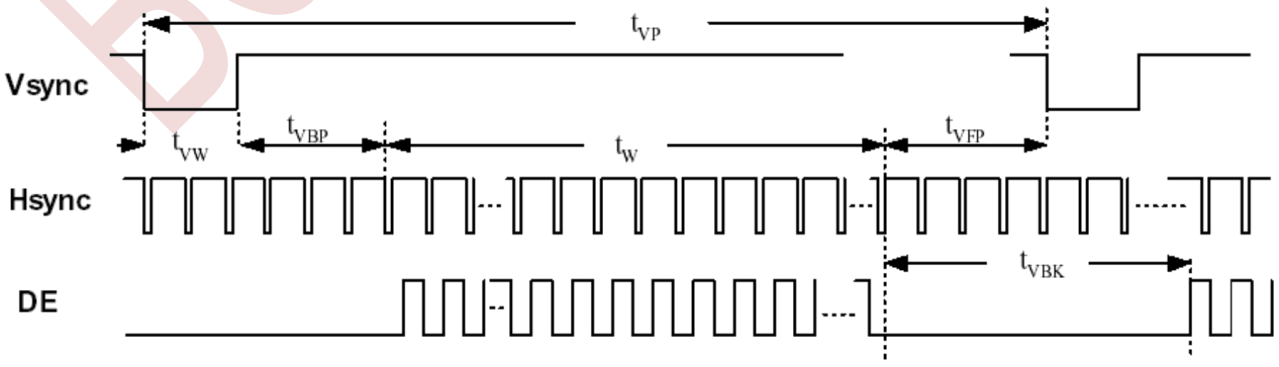


Figure 9-2 Input Sync Signals Timing (For All Formats)

9.1.2 Color Space

If the input data format is YCbCr, the device will change it to RGB format. Color space conversion block converts color space from YCbCr to RGB and uses the following equations. Output signal is 24-bit RGB format, 8-bit in each path.

$$R = 1.164 \times (Y - 16) + 1.596 \times (Cr - 128)$$
$$G = 1.164 \times (Y - 16) - 0.813 \times (Cr - 128) - 0.392 \times (Cb - 128)$$
$$B = 1.164 \times (Y - 16) + 2.017 \times (Cb - 128)$$

9.2 3D Video Display

Frame/field mode 3D video display can be set by the cooperation of register (02H) and 3DMODE pin. If 3DMODE pin state is the same as the ST_mode bit (02H) value, the screen display is updated to current input frame/field data. Otherwise, the data is invalid and the monitor maintains data from the previous frame/field. 3DMODE pin signal is detected at Vsync falling edge. 3D video display timing is shown in Figure 9-3.

In progressive mode, 3D video signal using frame timing mode, such as the odd frame is updated left display, and the even frame is updated right display.

In interlaced mode, 3D video signal using field timing mode, such as the odd field is updated left display, and the even field is updated right display. At this point, the vertical resolution of each field is lower compare with the source, the last two bit of register 01H should be set to “11”, display will repeat to display each line in next line automatically, to ensure that the image aspect ratio and display.

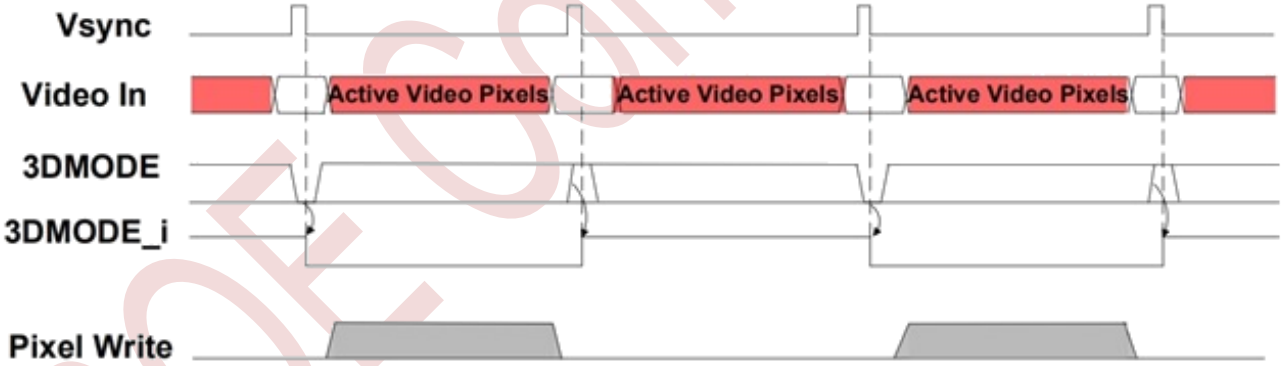


Figure 9-3 3D Video Display Timing

9.3 Two-wire Serial Interface

SVGA050 micro display acts as a slave for receiving and transmitting data, all read/write operations must be launched by the master. Compatible with I2C communication standard, the two-wire serial interface is used to read/write the registers to realize the display programmable control, such as digital video signal decoding and processing, gamma correction, Vcom adjustment and so on. Two-line serial interface depends on VCLK, VCLK signal must be given before the two-line serial communication. SVGA050 micro display The SDA and SCL line must be pull-up to1.8v or 3.3v power via a resistance by the outside communication controller.

Key Features and Tag:

- Communication speed (SCL) support from 100K to 1MHz.
- 8-bits Slave Address consists of 7-bits device address and 1-bit read/write flag.
- Start/Re-Start: SDA change from HIGH to LOW while SCL is HIGH, See Figure 9-4.
- Stop: SDA change from LOW to HIGH while SCL is HIGH, see Figure 9-4.
- ACK: SDA is LOW during the acknowledge clock pulse.
- NAK: SDA is HIGH during the acknowledge clock pulse.
- One transmission includes 8bit data and an acknowledge bit, total nine clock of SCL.
- Except Start and Stop condition:

  ----HIGH or LOW state of SDA can only being changed while SCL is LOW.

  ----Data on the SDA line must be stable during the HIGH period of the SCL.

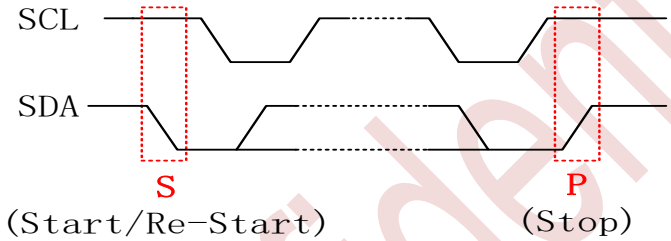


Figure 9-4 Start & Stop Timing

9.3.1 Communication Operating

- Steps of writing data (Figure 9-5):
  1. Master sends Start condition (S).
  2. Master sends 7bit Slave Address and 1bit write flag ($\overline{W}$) represents (Active low).
  3. Slave sends 1bit ACK (A) response (Active low).
  4. Master sends 8bit register address (Register).
  5. Slave sends 1bit ACK (A) response (Active low).
  6. Master sends 8bit data (Data).
  7. Slave sends 1bit ACK (A) response.
  8. Master sends stop condition (P).

S	Slave Addr	$\overline{W}$	A	Register	A	Data	A	P

Figure 9-5 Write Data format

- Steps of writing data (Figure 9-6):
  1. Master sends Start condition (S).
  2. Master sends 7bit Slave Address and 1bit write flag ($\overline{W}$) represents (Active low).
  3. Slave sends 1bit ACK (A) response (Active low).
  4. Master sends 8bit Register Address (Register)
  5. Slave sends 1bit ACK (A) response (Active low).

6. Master sends 1bit Re-Start condition (Sr).
7. Master sends 7bit Slave Address and 1bit Read flag (R) represents as high.
8. Slave sends 1bit ACK (A) response.
9. Slave sends 8bit Data (Data).
10. Master sends 1bit NAK ($\overline{A}$) response.
11. Master sends Stop condition (P).

S	Slave Addr	$\overline{W}$	A	Register	A	Sr	Slave Addr	R	A	Data	$\overline{A}$	P

Figure 9-6 Data format (Master reads from Slave)

9.3.2Serial Interface Bus Address Selection

Two salve address of SVGA050 series micro display can be selected by an externally SelAdr0 pin. The SelAdr0 pin has an internal pull up resistor (10K) to pull up to 1.8V power. One of micro display's SelAdr0 pin must be connected to GND when used in binocular stereovision application. Micro display's corresponding read/write address is shown as Table 9-1.

Table 9-1 3Slave Address list

A7 (MSB)	A6	A5	A4	A3	A2	A1 (SelAdr0)	A0 (R/$\overline{W}$)	Slave Address (R/$\overline{W}$)
0	0	0	1	1	1	0	1/0	1DH/1CH
0	0	0	1	1	1	1（Default）	1/0	1FH/1EH

10. Description of Function

10.1 Digital Video Interface

Table 10-1 Overview of Registers

Address	Bytes	Description	Default
00H	1	Driver Circuit Revision	00H
01H	1	Input Video Type Set	34H
02H	1	Sync signal Polarity Set & 3D functions	00H
03H	1	Vertical Blank Lines	00H
04H	1	Horizontal Blank Pixels	00H
05H	1	Adjust Start Active Video Position	01H
06H	1	Field Start Line Position Adjustment For Interlaced Video	00H
07H	1	Down Scaling for NTSC & PAL Video	00H
08H	1	Brightness Control (Video Signal Brightness)	80H
09H	1	Contrast Control (Video Signal Contrast)	80H

Address	Bytes	Description	Default
0AH	1	Reserved	4AH
0BH	1	Reserved	5AH
0CH	1	Reserved	00H
0DH	1	Reserved	00H
0EH	1	Reserved	00H
0FH	1	Power Down Mode Control	00H
10H	1	Display ON/Off & Scan Directions	04H
11H	1	Display Left Margin	02H
12H	1	Display Right Margin	02H
13H	1	Display Top Margin	02H
14H	1	Display Bottom Margin	02H
15H	1	Reserved	44H
16H	1	D/A Offset Setting	80H
17H	1	Discharge Current Setting	01H
18H	1	Discharge Enabled Control	00H
19H	1	Vcom Level Setting (Display’s Brightness)	FFH
1AH	1	Reserved	1DH
1BH	1	Reserved	74H
1CH	1	Reserved	FFH
1DH	1	Temperature Sensor Readout	—
1E～1FH	2	Reserved	—
[21,20H]	2	9 Bit Gamma Correction LUT0	000H
[23,22H]	2	9 Bit Gamma Correction LUT1	020H
[25,24H]	2	9 Bit Gamma Correction LUT2	040H
[27,26H]	2	9 Bit Gamma Correction LUT3	060H
[29,28H]	2	9 Bit Gamma Correction LUT4	080H
[2B,2AH]	2	9 Bit Gamma Correction LUT5	0A0H
[2D,2CH]	2	9 Bit Gamma Correction LUT6	0C0H
[2F,2EH]	2	9 Bit Gamma Correction LUT7	0E0H
[31,30H]	2	9 Bit Gamma Correction LUT8	100H
[33,32H]	2	9 Bit Gamma Correction LUT9	120H
[35,34H]	2	9 Bit Gamma Correction LUT10	140H
[37,36H]	2	9 Bit Gamma Correction LUT11	160H
[39,38H]	2	9 Bit Gamma Correction LUT 12	180H

Address	Bytes	Description	Default
[3B,3AH]	2	9 Bit Gamma Correction LUT13	1A0H
[3D,3CH]	2	9 Bit Gamma Correction LUT14	1C0H
[3F,3EH]	2	9 Bit Gamma Correction LUT15	1E0H
[41,40H]	2	9 Bit Gamma Correction LUT 16	200H
43H, 42H	2	Reserved	—
[45,44H]	2	9 Bit Red Signal Offset	100H
[47,46H]	2	9 Bit Green Signal Offset	100H
[49,48H]	2	9 Bit Blue Signal Offset	100H
4AH	1	Test Pattern Mode Selection	00H
4BH	1	Test Pattern Line Width Setting	02H
4CH	1	Test Pattern Line Space Setting	03H
4DH	1	Test Pattern Foreground & Background Color Setting	07H
4E～FFH	178	Reserved	—

10.2 Register Information

1) 00H--Revision information (Read Only)

Address	7	6	5	4	3	2	1	0
00H	N.A.					Revision		
Default	-					0	0	0

10.2.1 Video Signal Related Registers

2) 01H--Input video type set

Address	7	6	5	4	3	2	1	0
01H	N.A.		Data Mode		Sync signal		Scan mode	
Default	-	0	1	1	0	1	0	0

Data Mode	Input Video Format
000	16-bit 422, YCbCr
001	24-bit 444, YCbCr
010	8-bit MONO
011	24-bit 444, RGB
100	8-bit 422, YCbCr

Scan mode	Interlaced mode
00	Non-interlaced
01	Interlaced
10	Do not use
11	Pseudo-Interlaced

Sync signal	Sync Mode
00	Embedded Sync
01	External Sync with DE
10	N.A.
11	External Sync without DE

3) 02H--V sync/H sync Polarity& 3D function Setting

Address	7	6	5	4	3	2	1	0
02H	Reserved		3D Enable	N.A		3D Refresh	V_Pol	H_Pol
Default	0	0	0	0	0	0	0	0

3D function control

3D Enable	3D Refresh	3D Pin D	Display Mode	Operating
0	X	X	2D Mode	Refresh every Frame/Filed
1	0	0	3D Mode	Refresh
		1		Keep last data
	1	0		Keep last data
		1		Refresh

V_Pol/H_Pol setting: Select Vsync & Hsync polarity

Vs/Hs	Polarity Choice
0	Active High
1	Active Low

4) 03H--Input video vertical blank lines (VBlank)

Address	7	6	5	4	3	2	1	0
03H	VBlank							
Default	0	0	0	0	0	0	0	0

5) 04H--Input video horizontal blank pixels (HBlank)

Address	7	6	5	4	3	2	1	0
04H	HBlank							
Default								

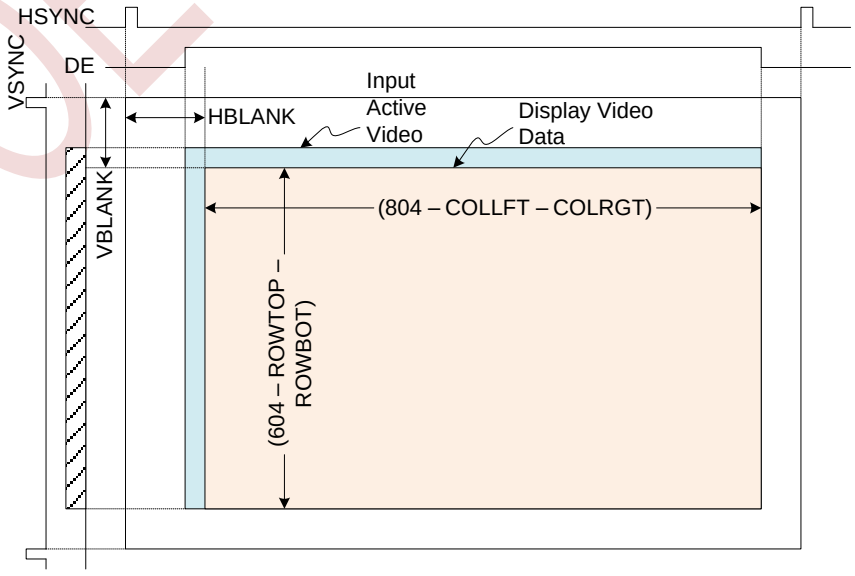


Figure 10-3 Vertical Blank Lines with DE

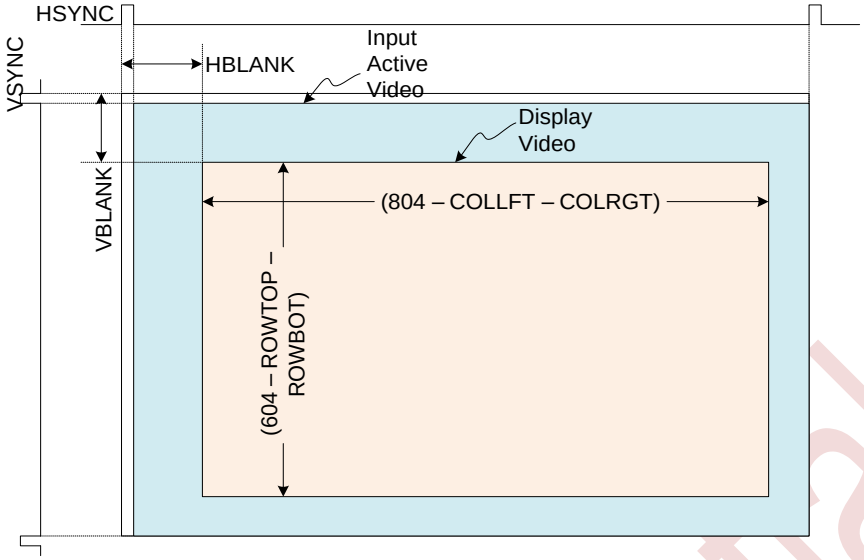


Figure 10-4 Vertical Blank Lines without DE

6) 05H--Adjust Start Active Video position

Address	7	6	5	4	3	2	1	0
05H	N.A.						SAV Offset	
Default	-						0	1

Adjust start active video (SAV) position

SAV Offset	Hsync position
00	1 pixel before input SAV
01	Same as input SAV
10	1 pixel after input SAV
11	2 pixel after input SAV

7) 06H--Field start line position adjust for Interlaced video (V_Offset)

Address	7	6	5	4	3	2	1	0
06H	N.A.						V_offset	
Default	-						0	0

V Offset: Adjust odd field active video start position when interlaced video mode

V_offset	Odd field start position
00	Same as Even field
01	1 line after Even field
10	N.A.
11	1 line before Even field

$$V_{out} = V_{in} \times Reg(09H) \div 128 \quad \text{(Limit Low 8Bit Data)}$$

8) 07H--Down scaling for NTSC & PAL video

Address	7	6	5	4	3	2	1	0
07H	N.A.					V_Scale	H_Scale	
Default	-					0	0	0

V Scale: Vertical 4/3downscale for PAL, for non-4:3 PAL signal input

V_Scale	Down scaling (In : Out)
0	1:1
1	6:5

H Scale: Horizontal 4/3downscale for PAL/NTS, for non-4:3 PAL signal input

H_Scale	Down scaling (In : Out)
00	1:1
01	11:10
10	9:8
11	N.A.

9) 08H--Brightness Control

Address	7	6	5	4	3	2	1	0
08H	Video Brightness							
Default	1	0	0	0	0	0	0	0

$V_{out} = V_{in} + Reg(08H) - 128$ (Limit Low 8Bit Data)

Video Brightness	Brightness adjustment effect
00H	Darkest setting
80H	No change
FFH	Brightest setting

10) 09H-- Contrast enhance control

Address	7	6	5	4	3	2	1	0
09H	Video Contrast							
Default	1	0	0	0	0	0	0	0

$V_{out} = V_{in} \times Reg(09H) \div 128$ (Limit Low 8Bit Data)

Video Contrast	Contrast adjustment effect
00H	Gain =0 (Black Screen)
80H	Gain =1 (Normal)
FFH	Gain =2 (Contrast Double)

11) 0AH--Reserved

Address	7	6	5	4	3	2	1	0
0AH	N.A.	Reserved						
Default	-	1	0	0	1	0	1	0

12) 0BH--Reserved

Address	7	6	5	4	3	2	1	0
0BH	N.A.	Reserved						
Default	-	1	0	1	1	0	1	0

13) 0FH--Power down

Address	7	6	5	4	3	2	1	0
0FH	PDOWN	N.A.		BSGENPD	RDACPD	RAMPPD	VCOMPD	TSENPD
Default	0	-		0	0	0	0	0

PDOWN：All system power off

RAMPPD：DAC Buffer module power off

RDACPD：DAC module power off

VCOMPD：Vcom power off

BSGENPD：Discharge current generator power off

TSENPD：Temperature sensor power of

10.2.2 Video Display Control Registers

14) 10H--Display off & Scan directions

Address	7	6	5	4	3	2	1	0
10H	N.A.					DispOff	VSCAN	HSCAN
Default	-					1	0	0

DispOff	Display
0	ON
1	OFF
VSCAN	**Direction**
0	Top → Bottom
1	Bottom → Top
HSCAN	**Direction**
0	Left → Right
1	Right → Left

15) 11H--Display Left Margin

Address	7	6	5	4	3	2	1	0
11H	COLLFT							
Default	0	0	0	0	0	0	1	0

16) 12H--Display Right Margin

Address	7	6	5	4	3	2	1	0
12H	COLRGT							
Default	0	0	0	0	0	0	1	0

17) 13H--Display Top Margin

Address	7	6	5	4	3	2	1	0
13H	ROWTOP							
Default	0	0	0	0	0	0	1	0

18) 14H--Display Bottom Margin

Address	7	6	5	4	3	2	1	0
14H	ROWBOT							
Default	0	0	0	0	0	0	1	0

19) 15H--Reserved

Address	7	6	5	4	3	2	1	0
15H	Reserved							
Default	0	1	0	0	0	1	0	0

20) 16H--D/A Conversion Offset control

Address	7	6	5	4	3	2	1	0
16H	DAOFFSETH				DAOFFSETL			
Default	0	0	0	0	0	0	0	0

Note:

DAOFFSETH = '1111': The maximum output of D/A is increased by 20%

DAOFFSETL = '1111': The maximum output of D/A is reduced by 20%

This register setting affects the gamma correction curve. Recommended to be configured as 0x0C.

21) 17H--Discharge Current Setting

Address	7	6	5	4	3	2	1	0
17H	Reserved						BIAS	
Default	-		0	0	-		0	1

BIAS: OLED pixel discharge current setting. Can enhance the display dynamic contrast ratio. May result in reduced display brightness.

BIAS	BIAS Current
00	0nA (OFF)
01	0.5nA
10	1nA
11	N.A.

22) 18H--Discharge Current Setting

Address	7	6	5	4	3	2	1	0
18H	N.A.							BIAS_En
Default	-							0

Note: BIAS_En: OLED pixel discharge function enable switch. 0 = OFF, 1 = ON

23) 19H--Vcom Level Setting

Address	7	6	5	4	3	2	1	0
19H	Vcom							
Default	0	1	0	1	0	0	0	1

Note:

The valid range of Vcom setting is 20H ~ FFH, and the corresponding cathode voltage is about-3V ~ 0V. 20H is the brightest, FFH is the darkest. The lower cathode voltage makes the display brighter. The curve of Vcom and cathode voltage sees section 3.5 (DC / DC converter).

10.2.3 Temperature Sensor Registers

24) Temperature Sensor

Address	7	6	5	4	3	2	1	0
1AH	N.A.		Reserved					
Default	-	-	0	1	1	0	1	1

25) 1BH--Reserved

Address	7	6	5	4	3	2	1	0
1BH	Reserved							
Default	0	1	0	1	0	0	1	0

26) 1CH--Reserved

Address	7	6	5	4	3	2	1	0
1CH	Reserved							
Default	1	1	1	1	1	1	1	1

27) 1DH--Temperature Sensor Readout (Read Only)

Address	7	6	5	4	3	2	1	0
1DH	Temp_Out							
Default	-							

Note: Temperature conversion formula is: $T = 0.47 \times \mathrm{Reg}(1\mathrm{DH}) - 40$

10.2.4 Gamma Correction Registers

28) 21H&20H--9 Bit Gamma Correction LUT0

Address	7	6	5	4	3	2	1	0
21H	N.A.							LUT0[8]
Default	-							0
20H	LUT0[7:0]							
Default	0	0	0	0	0	0	0	0

29) 23H&22H--9 Bit Gamma Correction LUT1

Address	7	6	5	4	3	2	1	0
23H	N.A.							LUT1[8]
Default	-							0
22H	LUT1[7:0]							
Default	0	0	1	0	0	0	0	0

30) 25H&24H--9 Bit Gamma Correction LUT2

Address	7	6	5	4	3	2	1	0
25H	N.A.							LUT2[8]
Default	-							0
24H	LUT2[7:0]							
Default	0	1	0	0	0	0	0	0

31) 27H&26H--9 Bit Gamma Correction LUT3

Address	7	6	5	4	3	2	1	0
27H	N.A.							LUT3[8]
Default	-							0
26H	LUT3[7:0]							
Default	0	1	1	0	0	0	0	0

32) 29H&28H--Bit Gamma Correction LUT4

Address	7	6	5	4	3	2	1	0
29H	N.A.							LUT4[8]
Default	-							0
28H	LUT4[7:0]							
Default	1	0	0	0	0	0	0	0

33) 2BH&2ABH--Bit Gamma Correction LUT5

Address	7	6	5	4	3	2	1	0
2BH	N.A.							LUT5[8]
Default	-							0
2AH	LUT5[7:0]							
Default	1	0	1	0	0	0	0	0

34) 2DH&2CH--9 Bit Gamma Correction LUT6

Address	7	6	5	4	3	2	1	0
2DH	N.A.							LUT6[8]
Default	-							0
2CH	LUT6[7:0]							
Default	1	1	0	0	0	0	0	0

35) 2FH&2EH--9 Bit Gamma CorrectionLUT7

Address	7	6	5	4	3	2	1	0
2FH	N.A.							LUT7[8]
Default	-							0
2EH	LUT7[7:0]							
Default	1	1	1	0	0	0	0	0

36) 31H&30H--9 Bit Gamma Correction LUT8

Address	7	6	5	4	3	2	1	0
31H	N.A.							LUT8[8]
Default	-							1
30H	LUT8[7:0]							
Default	0	0	0	0	0	0	0	0

37) 33H&32H--9 Bit Gamma Correction LUT9

Address	7	6	5	4	3	2	1	0
33H	N.A.							LUT9[8]
Default	-							1
32H	LUT9[7:0]							
Default	0	0	1	0	0	0	0	0

38) 35H&34H--9 Bit Gamma Correction LUT10

Address	7	6	5	4	3	2	1	0
35H	N.A.							LUT10[8]
Default	-							1
34H	LUT10[7:0]							
Default	0	1	0	0	0	0	0	0

39) 37H&36H--9 Bit Gamma Correction LUT11

Address	7	6	5	4	3	2	1	0
37H	N.A.							LUT11[8]
Default	-							1
36H	LUT11[7:0]							
Default	0	1	1	0	0	0	0	0

40) 39H&38H--9 Bit Gamma Correction LUT12

Address	7	6	5	4	3	2	1	0
39H	N.A.							LUT12[8]
Default	-							1
38H	LUT12[7:0]							
Default	1	0	0	0	0	0	0	0

41) 3BH&3AH--9 Bit Gamma Correction LUT13

Address	7	6	5	4	3	2	1	0
3BH	N.A.							LUT13[8]
Default	-							1
3AH	LUT13[7:0]							
Default	1	0	1	0	0	0	0	0

42) 3DH&3CH--9 Bit Gamma Correction LUT14

Address	7	6	5	4	3	2	1	0
3DH	N.A.							LUT14[8]
Default	-							1
3CH	LUT14[7:0]							
Default	1	1	0	0	0	0	0	0

43) 3FH&3EH--9 Bit Gamma Correction LUT15

Address	7	6	5	4	3	2	1	0
3FH	N.A.							LUT15[8]
Default	-							1
3EH	LUT15[7:0]							
Default	1	1	1	0	0	0	0	0

44) 41H&40H--10 Bit Gamma Correction LUT16

Address	7	6	5	4	3	2	1	0
41H	N.A.						LUT16[9:8]	
Default	-						1	0
40H	LUT16[7:0]							
Default	0	0	0	0	0	0	0	0

10.2.5 Color Offset Control Registers

45) 45H&44H--9 Bit Red offset control

Address	7	6	5	4	3	2	1	0
45H	N.A.							R_Offset[8]
Default	-							1
44H	R_Offset[7:0]							
Default	0	0	0	0	0	0	0	0

46) 47H&46H--9 Bit Green offset control

Address	7	6	5	4	3	2	1	0
47H	N.A.							G_Offset[8]
Default	-							1
46H	G_Offset[7:0]							
Default	0	0	0	0	0	0	0	0

47) 49H&48H--Blue Offset Control

Address	7	6	5	4	3	2	1	0
49H	N.A.							B_offset[8]
Default	-							1
48H	B_Offset[7:0]							
Default	0	0	0	0	0	0	0	0

10.2.6 Test Pattern Generator Registers

48) 4AH--Select Test Pattern

Address	7	6	5	4	3	2	1	0
4AH	N.A.					PatternMode		
Default	-					0	0	0

PatternMode: Select Test Pattern

PatternMode	Test Pattern
000	Pattern Generator Off (Normal)
001	Color Bar
010	Gray Scale
011	Tile
100	Vertical Lines
101	Horizontal Lines
110	Ver. & Hor. Lines
111	Do not use

49) 4BH--Set line width for lines pattern (Patterns = 100 ~110)

Address	7	6	5	4	3	2	1	0
4BH	LineWidth							
Default	0	0	0	0	0	0	1	0

50) 4CH--Set line space for line pattern (Patterns = 100 ~ 110)

Address	7	6	5	4	3	2	1	0
4CH	LineSpace							
Default	0	0	0	0	0	0	1	1

51) 4DH--Set Foreground & Background RGB color for lines pattern (Patterns = 100 ~ 110)

Address	7	6	5	4	3	2	1	0
4CH	N.A.	BGCOLOR			N.A.	FGCOLOR		
Default	-	0	0	0	-	0	1	1

BGCOLOR: Background Color

BGCOLOR	Color
000	Black
001	Blue
010	Green
100	Red
111	White

FGCOLOR: Foreground Color

FGCOLOR	Color
000	Black
001	Blue
010	Green
100	Red
111	White

10.3Register Setting Example

Table 10-2 Register Setting Example

Video Mode				Register Setting					
Mode	Scan	Input	Display	Reg01H	Reg07H	Reg11H	Reg12H	Reg13H	Reg14H
SVGA	Progressive	800×600	800×600	3CH	00H	02H	02H	02H	02H
VGA	Progressive	640×480	640×480	3CH	00H	52H	52H	3EH	3EH
SMPTE-170M-1	Interlaced	640×480	640×480	21H	00H	52H	52H	3EH	3EH
SMPTE-170M-2	Interlaced	800×600	800×600	3DH	00H	02H	02H	02H	02H
NTSC	Interlaced	720×480	640×480	41H	04h	52H	52H	3EH	3EH
PAL	Interlaced	720×480	640×480	41H	05H	52H	52H	3EH	3EH
NTSC (Square)	Interlaced	640×480	640×480	41H	00H	52H	52H	3EH	3EH
PAL (Square)	Interlaced	768×676	768×576	41H	00H	12H	12H	14H	14H

11. Optical Characteristics

Table 11-1 Photic Properties

Item			Remark		Min	Typ	Max
Contrast Ratio			Highest gray: Minimum gray		10000:1	-	-
Luminance		Full Color	Using Built-in test pattern under typical test conditions and all pixels are fully on		100	200	300
Luminance Uniformity			The average of five test points		85	95	100
Chromaticity	W	CIEx	all pixels are fully on	Using built-in test pattern under typical test conditions and all pixels are fully on.	0.25	0.30	0.35
		CIEy			0.30	0.35	0.40
	R	CIEx	all red sub-pixels are on		0.48	0.61	0.66
		CIEy			0.32	0.34	0.37
	G	CIEx	all green sub-pixels are on		0.15	0.25	0.30
		CIEy			0.58	0.62	0.66
	B	CIEx	all blue sub-pixels are on		0.10	0.13	0.18
		CIEy			0.07	0.09	0.14

12. Pixel Alignment

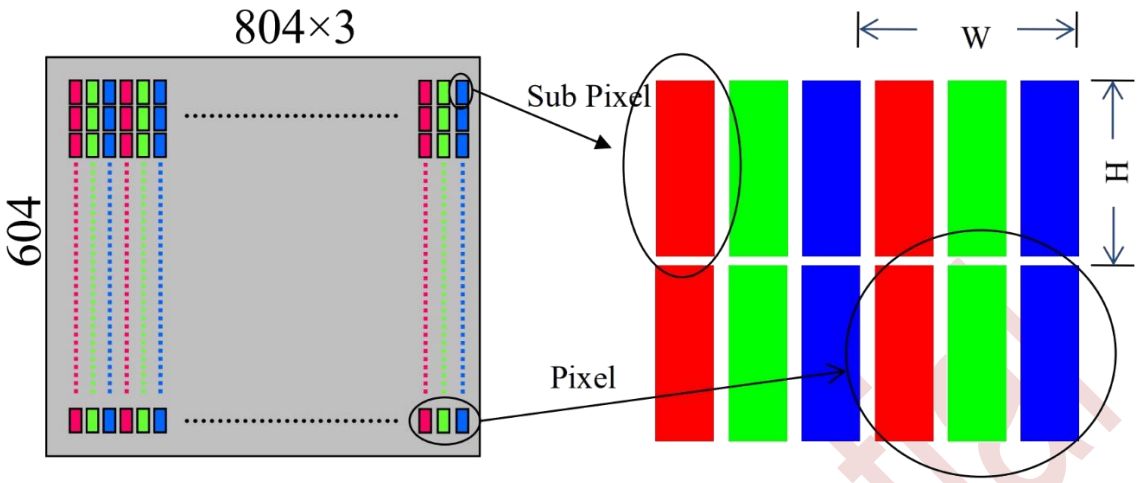
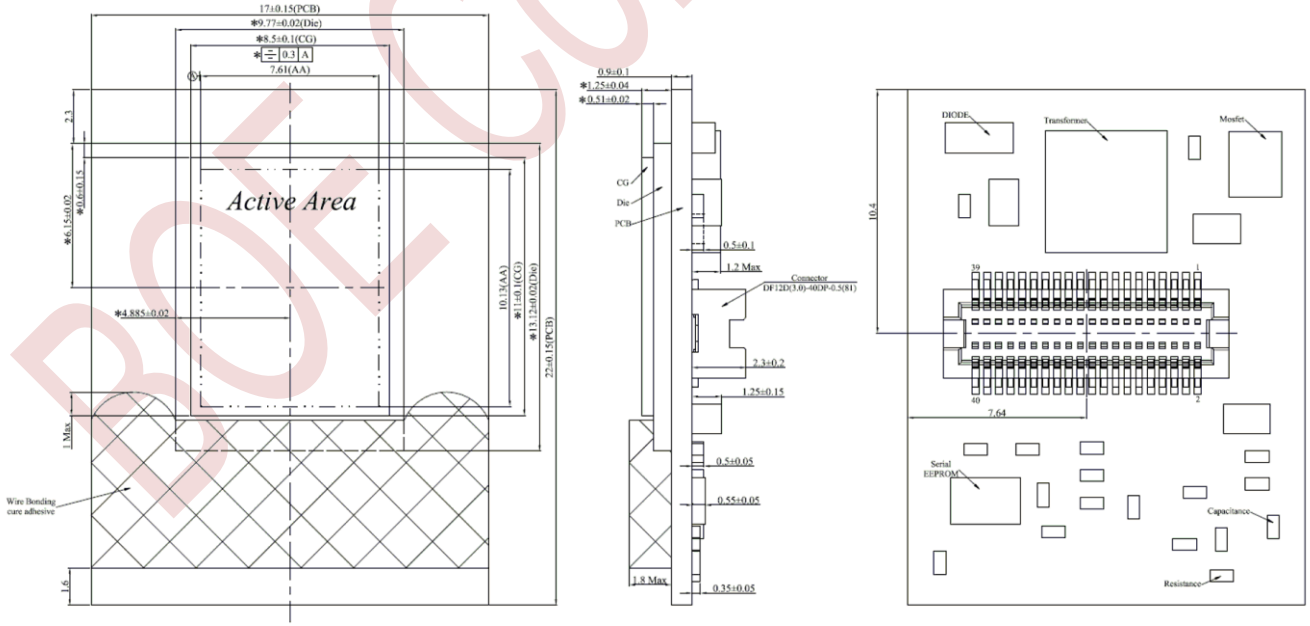


Figure 1 Pixel and Sub-Pixel Array

Each sub-pixel of colorful display emits white light, and full-color display is fulfilled through the RGB color filter. Each pixel of SVGA050 AMOLED micro-display is formed by three sub-pixels (Figure 12-1). The pixel's related parameters are shown below:

Model	Pixel Size		Duty Cycle	View Area	
	Width(W)	Height (H)		Width (804*W)	Height (604*H)
SVGA050	12.6mm	12.6mm	70%	10.13mm	7.61mm

13. Package Outline



Notes: 1. Display: 050 SVGA Micro OLED

2. Positioning by the edge of die is recommended

3. Undeclared tolerance: ±0.1mm

4. PCB module connector model: DF12NC (3.0)-40DS-0.5V (51)

5. Corresponding connector model: DF12NC (3.0)-40DS-0.5V (51)

6. "*" key dimension

14. Recommended Items

Temperature of organic EL panel tends to rise due to power consumption (heat generation) by the EL emission layer and the integrated silicon drive circuit. The temperature rise may cause luminance rise at initial state, or luminance drop by over time.

The temperature change in panel can be suppressed by establishing a thermal connection between panel rear surface (silicon substrate surface) and metal (chassis, frame, metal structure, etc.) at panel mount area, and the heat conducting sheet size can be changed, So highly recommend the heat conductive sheet between them as show in below. In order to ensure the normal operation of the screen, heat dissipation must be done to ensure that the screen temperature $< 60℃$.

15. Notes on Handling

15.1 Static charge prevention

Be sure to take the following protective measures. Organic EL panels are easily damaged by static charges.

1) Use non-chargeable gloves or handle with bare hands.
2) Use a wrist strap connecting ground when handling.
3) Do not touch any electrodes on the panel.
4) Wear non-chargeable clothes and conductive shoes.
5) Install grounded conductive mats on the working floor and working table.
6) Keep the panel away from any charged materials.

15.2 Protection from dust and dirt

7) Operate in a clean environment.
8) Do not touch the panel surface. The surface is easily scratched.
9) When cleaning on panel surface, use a clean-room wiper with isopropyl alcohol. Be careful not to leave stains on the surface.
10) Use ionized air to blow dust off the panel surface.

15.3 Others

11) Not hold FPC (Flexible Printed Circuit), not twist the FPC, and not bend FPC because connection area between the FPC and panel is easily broken by mechanical stress.
12) The minimum fold radius of the FPC is 1.0 mm. So, do not fold the FPC less than 1.0mm radius.
13) Do not drop the module.
14) Do not twist or bend the module.
15) Keep the module away from heat sources.
16) Not be close the module to water or other solvents.
17) Do not store or use the module at high temperatures or high humidity circumstance, as the

circumstance may affect module specifications.

18) When disposing of this, regard it as industrial waste and please comply with related regulations.

19) Do not store or use the panel in reactive chemical substance (including alcohol) environments, as these may affect the specifications.