MAX17783C

4.5V to 60V, 2.5A, High Efficiency, Step-Down DC-DC Converter

General Description

The *Himalaya* series of voltage regulator ICs, power modules, and chargers enable cooler, smaller, and simpler power supply solutions. The MAX17783C is a high-efficiency, high-voltage, Himalaya step-down DC-DC converter with an integrated high-side MOSFET operating over a wide input-voltage range of 4.5V to 60V. It can deliver up to 2.5A current, and generate output voltages from 0.9V up to 90% of V_{IN}. The device features internal compensation.

The MAX17783C device uses peak current-mode control architecture. The device operates in Low I_q mode at light loads to enable high efficiency. The MAX17783C offers a low minimum on-time that allows high switching frequencies and smaller solution sizes.

The feedback-voltage regulation accuracy is ±1.6% over -40°C to +125°C. The MAX17783C is available in a compact 10-pin (3mm x 3mm) TDFN package. Simulation models are available.

Applications

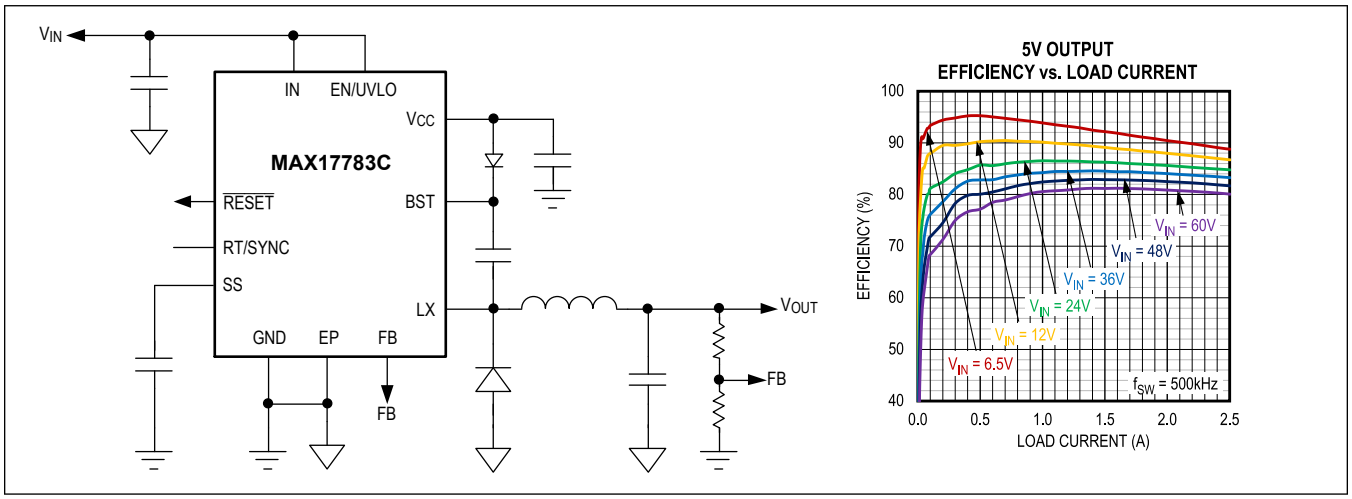
- Industrial and Commercial Power Distribution
- General Purpose Point-of-Load
- Distributed Supply Regulation
- Base-Station Power Supplies
- Wall Transformer Regulation
- High-Voltage, Single-Board Systems
- Set Top Boxes
- Audio Power Supplies
- LED Displays

Benefits and Features

- Reduces External Components and Total Cost
  - Internal Compensation Components
  - All-Ceramic Capacitors, Compact Layout
- Reduces Number of DC-DC Regulators to Stock
  - Wide 4.5V to 60V Input-Voltage Range
  - Adjustable Output Range from 0.9V up to 90% of V_{IN}
  - Delivers up to 2.5A Over the Temperature Range
  - 400kHz to 2.2MHz Adjustable Frequency with External Clock Synchronization
- Reduces Power Dissipation
  - 90.4% Peak Efficiency
  - 3.01µA Shutdown Current
  - Low I_q Mode for Enhanced Light-Load Efficiency
- Operates Reliably in Adverse Industrial Environments
  - Hiccup-Mode Overload Protection
  - Adjustable and Monotonic Startup with Prebiased Output Voltage
  - Built-In Output-Voltage Monitoring with $\overline{RESET}$
  - Programmable EN/UVLO Threshold
  - Overtemperature Protection
  - Wide -40°C to +125°C Ambient Operating Temperature Range/ -40°C to +150°C Junction Temperature Range

***Ordering Information* appears at end of data sheet.**

Simplified Application Circuit



19-100843; Rev 0; 11/20

Absolute Maximum Ratings

IN to GND ..... -0.3V to +65V
EN/UVLO to GND ..... -0.3V to V_{IN} + 0.3V
V_{CC}, SS, RT/SYNC, FB, $\overline{RESET}$ to GND ..... -0.3V to +6.5V
LX to GND ..... -0.3V to V_{IN} + 0.3V
BST to GND ..... -0.3V to +70V
BST to LX ..... -0.3V to +6V
BST to V_{CC} ..... -0.3V to +65V
LX Total RMS Current 2.7A

Continuous Power Dissipation (Multilayer Board, 10-Pin TDFN) (T_A = +70°C, derate 24.4mW/°C above +70°C) 1951.2mW
Output Short-Circuit Duration ..... Continuous
Operating Temperature Range (Note 1) ..... -40°C to 125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Note 1: Junction temperature greater than +125°C degrades operating lifetimes.

Note 2: Package thermal resistance was obtained using the MAX17783C evaluation kit with no airflow.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

10-PIN TDFN-CU

Package Code	T1033+1C
Outline Number	21-0137
Land Pattern Number	90-0003
THERMAL RESISTANCE, FOUR-LAYER BOARD (Note 2)	
Junction-to-Ambient (θ_{JA})	34ºC/W
Junction-to-Case Thermal Resistance (θ_{JC})	9ºC/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Electrical Characteristics

(V_{IN} = $V_{EN/UVLO}$ = 24V, C_{VCC} = 2.2µF, V_{GND} = 0V, V_{FB} = 1V, RT/SYNC = LX = SS = $\overline{RESET}$ = Open, V_{BST} to V_{LX} = 5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND.) (*Note 3*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY (IN)						
Input-Voltage Range	V_{IN}		4.5		60	V
Input-Shutdown Current	I_{IN_SH}	$V_{EN/UVLO}$ = 0V (shutdown mode)		3.01	6	µA
Input-Quiescent Current	I_{Low_Iq}	Not switching		205	350	µA
	I_{CCM}	Normal Switching mode, f_{SW} = 500kHz		1.6	3	mA
ENABLE/UVLO (EN/UVLO)						
EN/UVLO Threshold	V_{ENR}	$V_{EN/UVLO}$ rising	1.192	1.218	1.238	V
	V_{ENF}	$V_{EN/UVLO}$ falling	1.068	1.088	1.111	
EN/UVLO Input-Leakage Current	I_{ENLKG}	$V_{EN/UVLO}$ = 1.25V, T_A = +25ºC	-100	0	+100	nA
V_{CC} (LDO)						
V_{CC} Output-Voltage Range	V_{CC}	1mA ≤ I_{VCC} ≤ 15mA	4.75	5	5.25	V
		6V ≤ V_{IN} ≤ 60V, I_{VCC} = 1mA	4.75	5	5.25	

Electrical Characteristics (continued)

(V_{IN} = $V_{EN/UVLO}$ = 24V, C_{VCC} = 2.2µF, V_{GND} = 0V, V_{FB} = 1V, RT/SYNC = LX = SS = $\overline{RESET}$ = Open, V_{BST} to V_{LX} = 5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND.) (*Note 3*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} Current Limit	I_{VCC_MAX}	V_{CC} = 4.3V, V_{IN} = 6V	25	52.9	100	mA
V_{CC} Dropout	V_{CC_DO}	V_{IN} = 4.5V, I_{VCC} = 15mA			400	mV
V_{CC} UVLO	V_{CC_UVR}	V_{CC} rising	4.05	4.17	4.3	V
	V_{CC_UVF}	V_{CC} falling	3.65	3.77	3.9	
HIGH-SIDE MOSFET						
High-Side nMOSFET On-Resistance	R_{DS-ONH}	I_{LX} = 0.3A		158	365	mΩ
LX Leakage Current	I_{LXLKG}	V_{BST} = V_{LX} = 1V, $V_{EN/UVLO}$ = 0, T_A = +25°C			2	µA
SOFT-START (SS)						
Soft-Start Current	I_{SS}	V_{SS} = 0.5V	4.7	5	5.3	µA
FEEDBACK (FB)						
FB Regulation Voltage	V_{FB-REG}		0.886	0.9	0.9145	V
Low I_q Mode FB Falling Threshold	V_{FB_L}	Low I_q Mode	98	99	100	% of V_{FB-REG}
FB Input Bias Current	I_{FB}	0 ≤ V_{FB} ≤ 1V, T_A = 25ºC	-100	0	+100	nA
CURRENT LIMIT						
Peak Current-Limit Threshold	$I_{PEAK-LIMIT}$		3.4	4	4.6	A
Runaway Current-Limit Threshold	$I_{RUNAWAY-LIMIT}$		4.08	4.77	5.52	A
Low I_q Mode Peak-Current Threshold	I_{MIN_PK}			0.621		A
RT/SYNC						
Switching Frequency	f_{SW}	$R_{RT/SYNC}$ = 52kΩ	370	400	430	kHz
		$R_{RT/SYNC}$ = 40.2kΩ	475	500	525	
		$R_{RT/SYNC}$ = 8.06kΩ	1950	2200	2450	
		$R_{RT/SYNC}$ = Open	440	500	550	
Feedback Undervoltage Trip-Level to Cause HICCUP	$V_{FB-HICF}$		0.55	0.58	0.6	V
HICCUP Timeout		(*Note 4*)		32768		Cycles
Minimum On-Time	t_{ON_MIN}			63	100	ns
Minimum Off-Time	t_{OFF_MIN}		140	150	160	ns
SYNC Frequency-Capture Range		f_{SW} set by $R_{RT/SYNC}$	1.1 x f_{SW}		1.4 x f_{SW}	
SYNC Pulse-Width			50			ns
SYNC Threshold	V_{IH}		2.1			V
	V_{IL}				0.8	

Electrical Characteristics (continued)

(V_{IN} = $V_{EN/UVLO}$ = 24V, C_{VCC} = 2.2µF, V_{GND} = 0V, V_{FB} = 1V, RT/SYNC = LX = SS = $\overline{RESET}$ = Open, V_{BST} to V_{LX} = 5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND.) (*Note 3*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{RESET}$						
$\overline{RESET}$ Output-Level Low		$I_{\overline{RESET}}$ = 10mA			200	mV
$\overline{RESET}$ Output-Leakage Current		T_A = T_J = +25°C, $V_{\overline{RESET}}$ = 5.5V	-100		+100	nA
FB Threshold for $\overline{RESET}$ Assertion	V_{FB-OKF}	V_{FB} Falling	90.5	92.1	94	%
FB Threshold for $\overline{RESET}$ Deassertion	V_{FB-OKR}	V_{FB} Rising	93.8	95.4	97.2	%
$\overline{RESET}$ Delay after FB Reaches 95% Regulation				1024		Cycles
THERMAL SHUTDOWN						
Thermal Shutdown Rising Threshold	T_{SHDNR}			154		°C
Thermal Shutdown Hysteresis	T_{SHDNHY}			15		°C

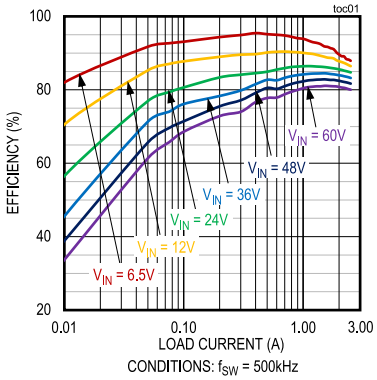
Note 3: Electrical specifications are production tested at T_A = +25ºC. Specifications over the entire operating temperature range are guaranteed by design and characterization.

Note 4: See the *Overcurrent Protection (OCP)/Hiccup Mode* section for more details.

Typical Operating Characteristics

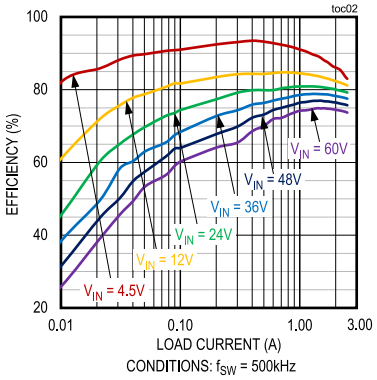
($V_{EN/UVLO}$ = V_{IN} = 24V, V_{GND} = 0V, C_{VCC} = 2.2µF, C_{BST} = 0.1µF, C_{SS} = 5600pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.)

5V OUTPUT, EFFICIENCY vs. LOAD CURRENT
FIGURE 5 CIRCUIT



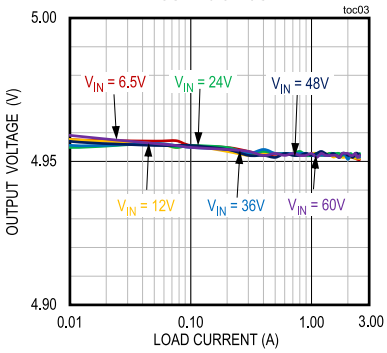
CONDITIONS: f_{SW} = 500kHz

3.3V OUTPUT, EFFICIENCY vs. LOAD CURRENT
FIGURE 6 CIRCUIT



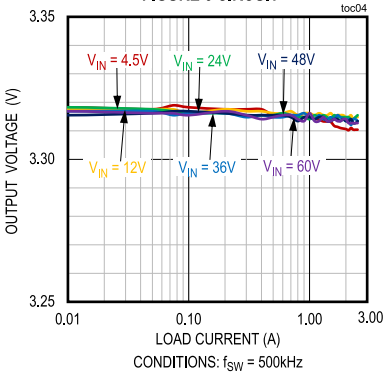
CONDITIONS: f_{SW} = 500kHz

5V OUTPUT, LOAD AND LINE REGULATION
FIGURE 5 CIRCUIT



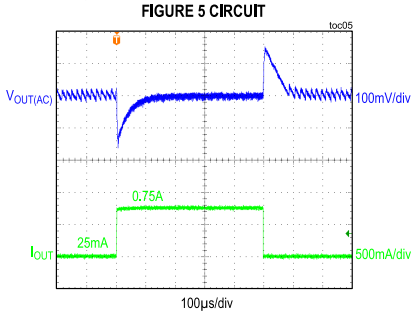
CONDITIONS: f_{SW} = 500kHz

3.3V OUTPUT, LOAD AND LINE REGULATION
FIGURE 6 CIRCUIT



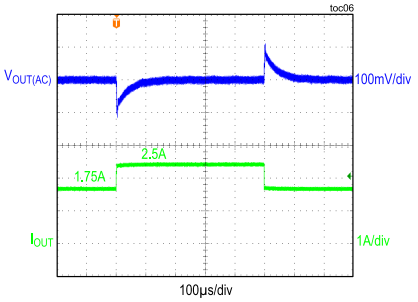
CONDITIONS: f_{SW} = 500kHz

5V OUTPUT, LOAD TRANSIENT BETWEEN 25mA AND 0.75A
FIGURE 5 CIRCUIT



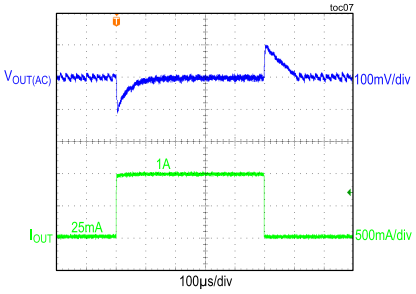
CONDITIONS: f_{SW} = 500kHz

5V OUTPUT, LOAD TRANSIENT BETWEEN 1.75A AND 2.5A
FIGURE 5 CIRCUIT



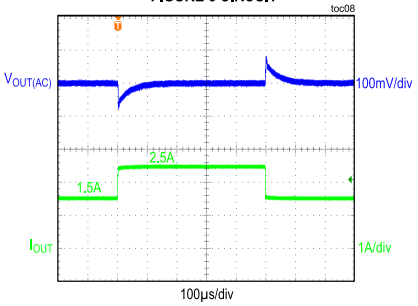
CONDITIONS: f_{SW} = 500kHz

3.3V OUTPUT, LOAD TRANSIENT BETWEEN 25mA AND 1A
FIGURE 6 CIRCUIT



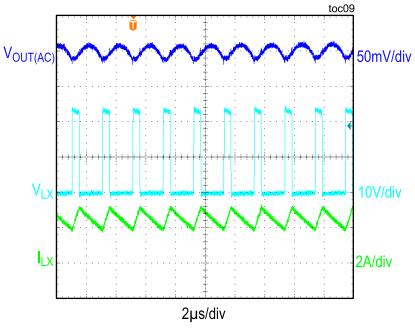
CONDITIONS: f_{SW} = 500kHz

3.3V OUTPUT, LOAD TRANSIENT BETWEEN 1.5A AND 2.5A
FIGURE 6 CIRCUIT



CONDITIONS: f_{SW} = 500kHz

5V OUTPUT, STEADY-STATE AT 2.5A LOAD
FIGURE 5 CIRCUIT

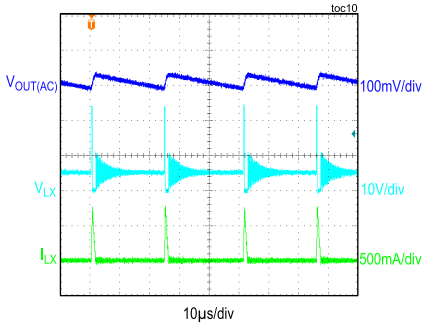


CONDITIONS: f_{SW} = 500kHz

Typical Operating Characteristics (continued)

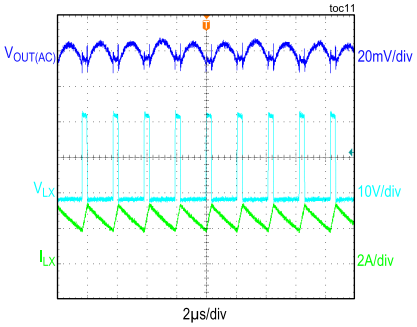
($V_{EN/UVLO}$ = V_{IN} = 24V, V_{GND} = 0V, C_{VCC} = 2.2µF, C_{BST} = 0.1µF, C_{SS} = 5600pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.)

5V OUTPUT, STEADY-STATE AT 25mA LOAD
FIGURE 5 CIRCUIT



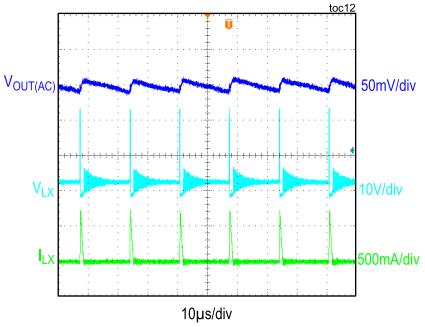
CONDITIONS: f_{SW} = 500kHz

3.3V OUTPUT, STEADY-STATE AT 2.5A LOAD
FIGURE 6 CIRCUIT



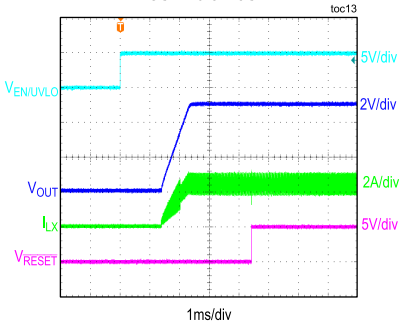
CONDITIONS: f_{SW} = 500kHz

3.3V OUTPUT, STEADY-STATE AT 25mA LOAD
FIGURE 6 CIRCUIT



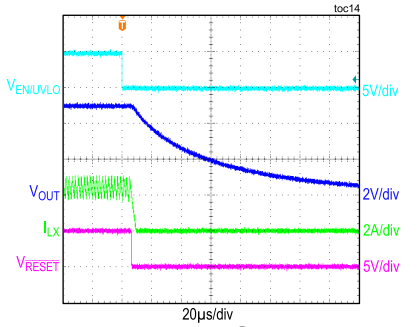
CONDITIONS: f_{SW} = 500kHz

5V OUTPUT, SOFT-START THROUGH EN/UVLO
FIGURE 5 CIRCUIT



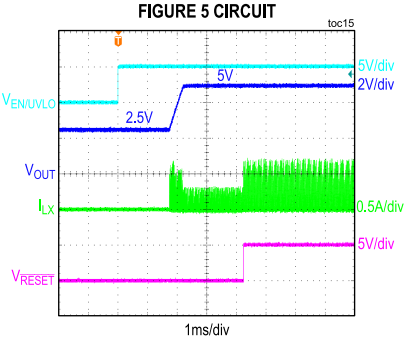
CONDITIONS: f_{SW} = 500kHz, 2Ω RESISTIVE LOAD, $\overline{RESET}$ IS PULLED UP TO V_{CC} WITH A 10kΩ RESISTOR

5V OUTPUT, SHUTDOWN FROM EN/UVLO
FIGURE 5 CIRCUIT



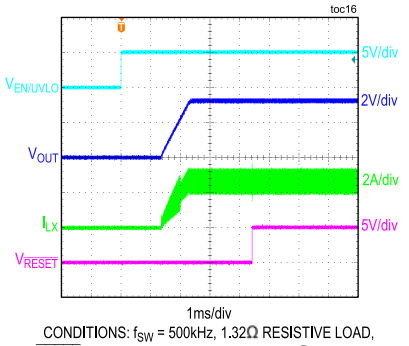
CONDITIONS: f_{SW} = 500kHz, 2Ω RESISTIVE LOAD, $\overline{RESET}$ IS PULLED UP TO V_{CC} WITH A 10kΩ RESISTOR

5V OUTPUT, SOFT-START WITH
PREBIAS VOLTAGE OF 2.5V
FIGURE 5 CIRCUIT



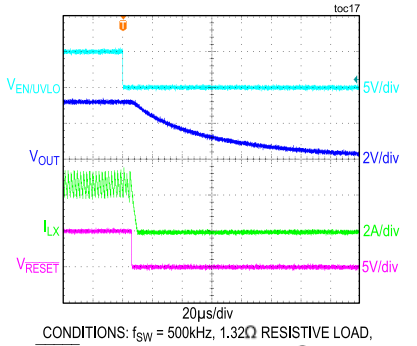
CONDITIONS: f_{SW} = 500kHz, 200Ω RESISTIVE LOAD, $\overline{RESET}$ IS PULLED UP TO V_{CC} WITH A 10kΩ RESISTOR

3.3V OUTPUT, SOFT-START THROUGH EN/UVLO
FIGURE 6 CIRCUIT



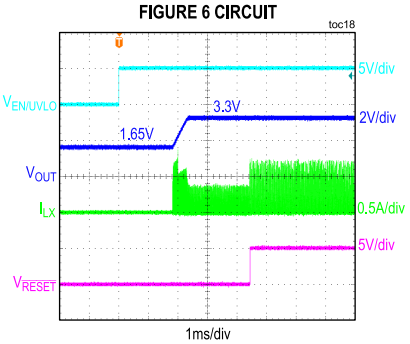
CONDITIONS: f_{SW} = 500kHz, 1.32Ω RESISTIVE LOAD, $\overline{RESET}$ IS PULLED UP TO V_{CC} WITH A 10kΩ RESISTOR

3.3V OUTPUT, SHUTDOWN FROM EN/UVLO
FIGURE 6 CIRCUIT



CONDITIONS: f_{SW} = 500kHz, 1.32Ω RESISTIVE LOAD, $\overline{RESET}$ IS PULLED UP TO V_{CC} WITH A 10kΩ RESISTOR

3.3V OUTPUT, SOFT-START WITH
PREBIAS VOLTAGE OF 1.65V
FIGURE 6 CIRCUIT

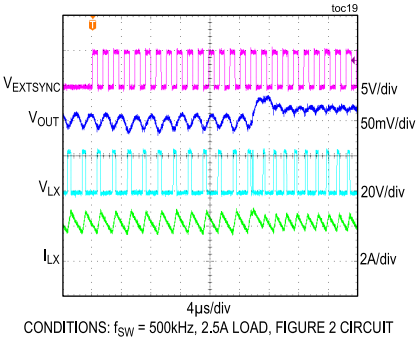


CONDITIONS: f_{SW} = 500kHz, 132Ω RESISTIVE LOAD, $\overline{RESET}$ IS PULLED UP TO V_{CC} WITH A 10kΩ RESISTOR

Typical Operating Characteristics (continued)

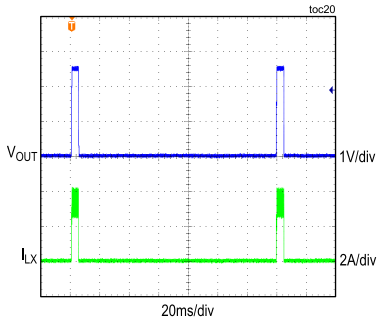
($V_{EN/UVLO}$ = V_{IN} = 24V, V_{GND} = 0V, C_{VCC} = 2.2µF, C_{BST} = 0.1µF, C_{SS} = 5600pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.)

5V OUTPUT, EXTERNAL CLOCK SYNCHRONIZATION WITH 700kHz, FIGURE 5 CIRCUIT



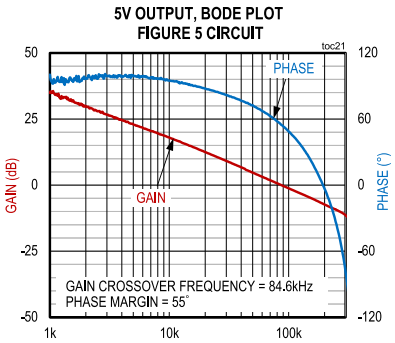
CONDITIONS: f_{SW} = 500kHz, 2.5A LOAD, FIGURE 2 CIRCUIT

5V OUTPUT, OVERLOAD PROTECTION FIGURE 5 CIRCUIT



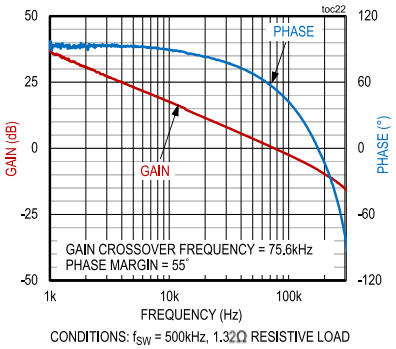
CONDITIONS: f_{SW} = 500kHz, 1Ω RESISTIVE LOAD

5V OUTPUT, BODE PLOT FIGURE 5 CIRCUIT



CONDITIONS: f_{SW} = 500kHz, 2Ω RESISTIVE LOAD

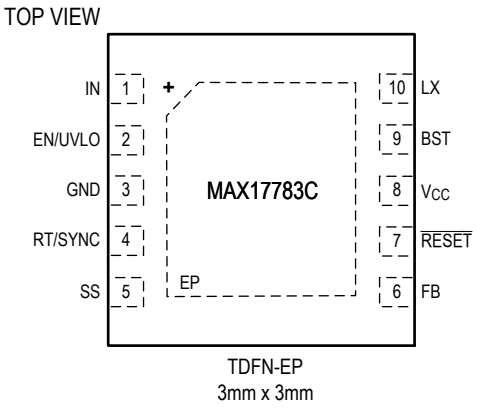
3.3V OUTPUT, BODE PLOT FIGURE 6 CIRCUIT



CONDITIONS: f_{SW} = 500kHz, 1.32Ω RESISTIVE LOAD

Pin Configuration

MAX17783C

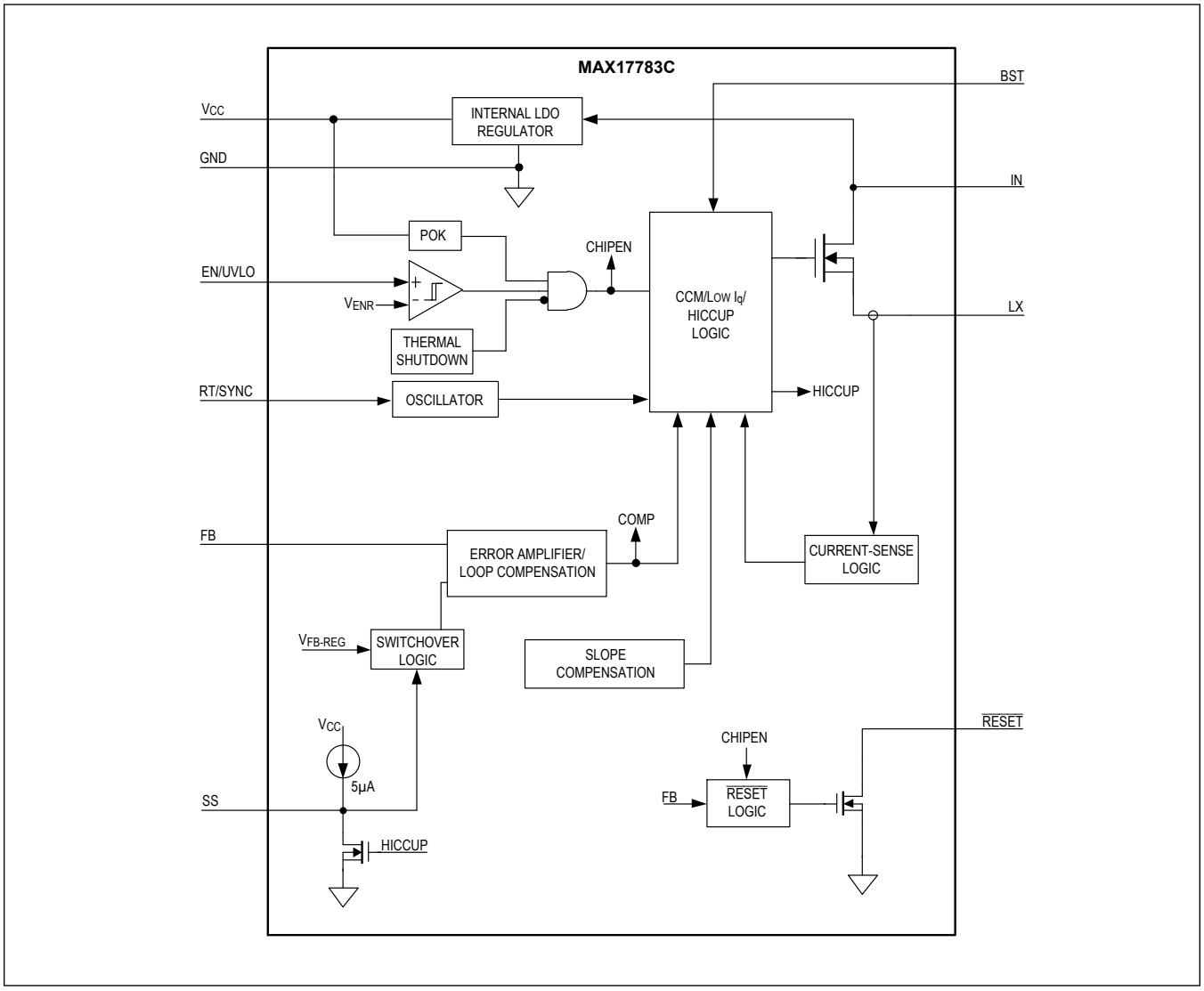


Pin Description

PIN	NAME	FUNCTION
1	IN	Power-Supply Input Pin. Decouple the IN pin to GND with a minimum of 2.2µF X7R ceramic capacitor. Place the capacitor close to the IN and GND pins.
2	EN/UVLO	Enable/Undervoltage Lockout Input Pin. Drive EN/UVLO high to enable the converter. Connect to the midpoint of a resistor divider from IN to GND to set the input voltage at which the device turns on/off. Connect to IN pin for always on operation. Pull low to GND to disable the device.
3	GND	Ground Pin. Connect GND to the power ground plane. Connect all the circuit ground connections together at a single point. Refer to the MAX17783C evaluation kit data sheet for a layout example.
4	RT/SYNC	Switching Frequency Programming Input/External Clock Synchronization Input Pin. Connect a resistor from RT/SYNC to GND to set the internal clock frequency between 400kHz and 2200kHz. Leave RT/SYNC open for the default 500kHz switching frequency. The RT/SYNC pin can also be used to synchronize the converter to an external clock. See the *Switching Frequency and External Clock Synchronization (RT/SYNC)* section for more details.
5	SS	Soft-Start Input Pin. Connect a capacitor from the SS pin to the GND node to set the soft-start time.
6	FB	Feedback Input Pin. Connect the FB pin to the center node of a resistor-divider between the output voltage node and GND. See the *Adjusting Output Voltage* section for details.
7	$\overline{\text{RESET}}$	Open-Drain $\overline{\text{RESET}}$ Output Pin. The $\overline{\text{RESET}}$ output is driven low if FB drops below 92.1% of its set value. $\overline{\text{RESET}}$ goes high 1024 cycles after FB rises above 95.4% of its set value.
8	V_{CC}	5V LDO Output Pin. Bypass V_{CC} with a 2.2µF ceramic capacitor to GND. LDO does not support the external loading on V_{CC}.
9	BST	Bootstrap Capacitor Pin. Connect a minimum of 0.1µF ceramic capacitor between BST and LX, and a diode from V_{CC} to BST.
10	LX	Switching Node. Connect the LX pin to the switching side of the inductor.
—	EP	Exposed Pad. Always connect EP to the GND pin of the IC. Also, connect EP to a large GND plane with several thermal vias for best thermal performance. Refer to the MAX17783C evaluation kit data sheet for an example of the correct method for EP connection and thermal vias.

Functional Diagrams

Block Diagram



Detailed Description

The MAX17783C is a high-efficiency, high-input step-down DC-DC converter with an integrated high-side MOSFET operating over a 4.5V to 60V input-voltage range. It can deliver up to 2.5A current and generate output voltages ranging from 0.9V to 90% of V_{IN}. The device offers internal compensation across the operating range of input voltages, output voltage settings and load currents. The feedback-voltage regulation accuracy is ±1.6% over -40°C to +125°C. The device operates in Low I_q mode at light loads to improve efficiency.

The MAX17783C features a peak current-mode control architecture. At the rising edge of each clock, the high-side MOSFET turns on. During the on-state, the inductor current ramps up. The internal error amplifier sets the duty cycle using a comparator. The high-side MOSFET remains in on-state until either the appropriate duty cycle is reached, or the inductor current reaches the peak current limit. After the duty cycle is reached, the high-side MOSFET turns off and the external freewheeling diode conducts inductor current. During the rest of the switching cycle, the inductor releases the stored energy as its current ramps down and provides current to the output.

The MAX17783C features a RT/SYNC pin that can be used to program the switching frequency and to synchronize the internal clock to an external clock. The device offers an adjustable input enable/undervoltage lockout pin to program the desired input voltage at which the converter turns on/off. The device also has a soft-start pin to reduce inrush currents during startup. In addition, the device features an open-drain $\overline{RESET}$ pin to monitor the output voltage. The MAX17783C offers a low minimum on-time that allows high switching frequencies and smaller solution sizes.

Low I_q Mode

The MAX17783C works in Low I_q mode to improve the light load efficiency. At light loads, the device forces the inductor current to a minimum peak of I_{MIN_PK} (0.621A) every clock cycle until the output voltage rises above its set point. If the output voltage stays above its set point, further high-side MOSFET switching cycles are skipped. When the MOSFET switching is skipped for 64 consecutive clock cycles, the device enters Low I_q mode. In Low I_q mode, the device consumes approximately I_{Low_Iq} (205µA) from the input supply. The device stays in Low I_q mode until the load current discharges the output voltage to V_{FB_L} (99%) of its set value. The high-side MOSFET is turned on in the next clock cycle, and I_{MIN_PK} inductor current is forced, and the cycle continues. The advantage of Low I_q mode is higher efficiency at light loads due to lower quiescent current. Figure 1 shows the Low I_q mode operation, where V_{OUT} is the output voltage and I_{IND} is the inductor current.

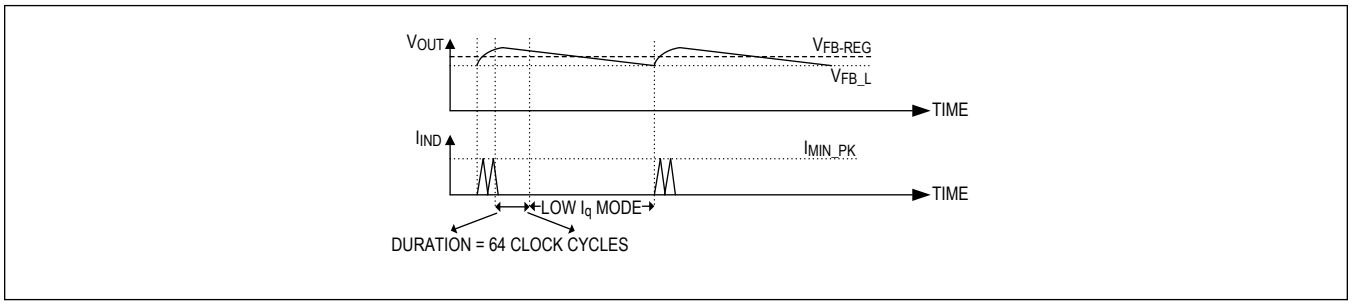


Figure 1. Low I_q Mode Operation

Switching Frequency and External Clock Synchronization (RT/SYNC)

The switching frequency of the device can be programmed from 400kHz to 2.2MHz by using a resistor connected from the RT/SYNC pin to GND. Calculate the value of the resistor at RT/SYNC pin ($R_{RT/SYNC}$) for a desired switching frequency (f_{SW}) using the following equation.

$$R_{RT/SYNC} = \frac{21000}{f_{SW}} - 1.7$$

Where $R_{RT/SYNC}$ is in kΩ and f_{SW} is in kHz. Leave the RT/SYNC pin open for a default f_{SW} of 500kHz. See Table 1 for $R_{RT/SYNC}$ resistor values for a few common switching frequencies.

Table 1. Switching Frequency vs. RT/SYNC Resistor

SWITCHING FREQUENCY (kHz)	$R_{RT/SYNC}$ RESISTOR (kΩ)
500	Open
500	40.2
400	52
2200	8.06

The RT/SYNC pin can be used to synchronize the internal oscillator of the device to an external clock. Use the network shown in Figure 2 to use the external clock synchronization feature. Note that $R_{RT/SYNC}$ cannot be open to utilize this feature. The external synchronization clock frequency must be between 1.1 x f_{SW} and 1.4 x f_{SW}, where f_{SW} is the switching frequency programmed by the resistor connected to the RT/SYNC pin. When an external clock is applied to the RT/SYNC pin, the internal oscillator frequency changes to external clock frequency (from original frequency based on the RT/SYNC setting) after detecting 18 external consecutive clock edges. The external clock logic-high level should be higher than V_{IH}, the logic-low level lower than V_{IL}, and the pulse-width of the external clock should be more than 50ns.

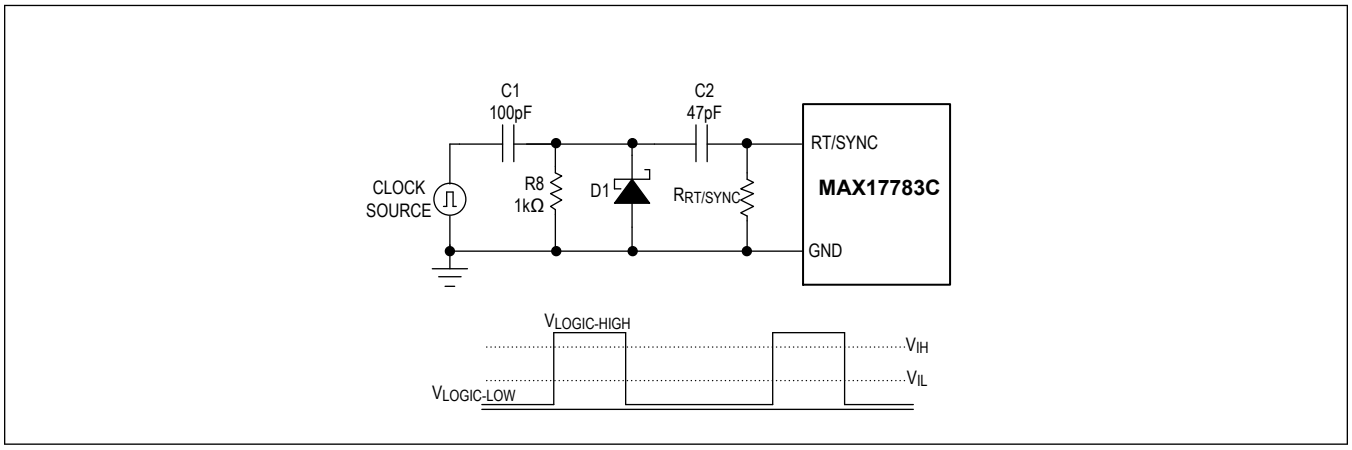


Figure 2. Synchronization to an External Clock

Linear Regulator (V_{CC})

The MAX17783C has an internal low dropout (LDO) regulator that powers V_{CC} from V_{IN}. This LDO is enabled during power-up or when EN/UVLO is above 0.7V (typ). The typical V_{CC} output voltage is 5V. Bypass V_{CC} to GND with a 2.2µF low-ESR ceramic capacitor. V_{CC} powers the internal blocks and recharges the external bootstrap capacitor.

The device is enabled when $V_{CC} > V_{CC\_UVR}$ (4.17V). The device employs an undervoltage-lockout circuit that forces the device off when $V_{CC} < V_{CC\_UVF}$ (3.77V).

Operating Input-Voltage Range

The minimum and maximum operating input voltages for a given output-voltage setting is calculated using the following equation.

$$V_{IN(MIN)} = \frac{V_{OUT} + I_{OUT(MAX)} \times R_{DCR(MAX)} + V_D}{1 - \left(f_{SW} \times t_{OFF\_MIN(MAX)}\right)} + I_{OUT(MAX)} \times R_{DS\text{-}ONH(MAX)} - V_D$$

$$V_{IN(MAX)} = \frac{V_{OUT}}{f_{SW} \times t_{ON\_MIN(MAX)}}$$

where:

V_{OUT} = Steady-state output voltage (V).

$I_{OUT(MAX)}$ = Maximum load current (A).

$R_{DCR(MAX)}$ = Worst-case maximum DC resistance of the inductor (Ω).

f_{SW} = Operating switching frequency (Hz).

$t_{OFF\_MIN(MAX)}$ = Worst-case minimum switch off-time (160ns).

$t_{ON\_MIN(MAX)}$ = Worst-case minimum switch on-time (100ns).

$R_{DS-ONH(MAX)}$ = Worst-case on-state resistance of the high-side internal MOSFET (Ω).

V_D = Worst-case forward voltage drop across the external free-wheeling diode (V).

Overcurrent Protection (OCP)/Hiccup Mode

The MAX17783C provides a robust overcurrent protection (OCP) scheme that protects the converter under overload and output short-circuit conditions. A cycle-by-cycle peak current limit turns off the high-side MOSFET when the high-side switch current exceeds an internal limit of $I_{PEAK-LIMIT}$ (4A). A runaway current limit on the high-side switch current at $I_{RUNAWAY-LIMIT}$ (4.77A) protects the device under output short-circuit conditions at high input voltages when there is insufficient output voltage available to restore the inductor current that built up during the on period of the step-down converter. One occurrence of the runaway current limit triggers a hiccup mode. Additionally, if the feedback voltage drops to $V_{FB-HICF}$ anytime after soft-start is complete, hiccup mode is triggered. In hiccup mode, the converter is protected by suspending switching for a hiccup timeout period of 32768 clock cycles of half the programmed switching frequency. Once the hiccup timeout period expires, soft-start is attempted again. Note that when soft-start is attempted under overload condition, if feedback voltage does not exceed $V_{FB-HICF}$, the device switches at half the programmed switching frequency for the time duration of the programmed soft-start time and the subsequent 1024 clock cycles. Hiccup mode of operation ensures low power dissipation under output short-circuit conditions.

$\overline{\text{RESET}}$ Output

The MAX17783C includes a $\overline{\text{RESET}}$ comparator to monitor the output voltage. The open-drain $\overline{\text{RESET}}$ output requires an external pullup resistor. $\overline{\text{RESET}}$ goes high (high impedance) 1024 switching cycles after the feedback voltage (V_{FB}) increases above 95.4% of the V_{FB-REG}. $\overline{\text{RESET}}$ goes low when the V_{FB} drops to below 92.1% of the V_{FB-REG}. $\overline{\text{RESET}}$ also goes low during thermal shutdown or when the EN/UVLO pin goes below V_{ENF}.

Prebiased Output

When the MAX17783C starts into a prebiased output, the high-side MOSFET is turned off so that the converter does not sink current from the output. The switching of the high-side MOSFET commences only after the voltage at the SS pin (V_{SS}) crosses the voltage at the feedback pin (V_{FB}). V_{FB} then smoothly ramps up to V_{FB-REG} in alignment with the V_{SS} and the output voltage reaches its target value.

Thermal-Shutdown Protection

The MAX17783C offers thermal shutdown protection to limit the junction temperature. When the junction temperature of the device exceeds +154ºC, an on-chip thermal sensor shuts down the device, allowing the device to cool. The thermal sensor turns the device on again after the junction temperature cools by 15ºC. Soft-start is deasserted during thermal shutdown and it initiates the startup operation when the device recovers from thermal shutdown. Carefully evaluate the total power dissipation (see *Power Dissipation*) to avoid undesired triggering of the thermal shutdown during normal operation.

Applications Information

Input Capacitor Selection

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the converter switching. The input capacitor RMS current requirement (I_{RMS}) is defined by the following equation:

$$I_{RMS} = I_{OUT(MAX)} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

where, $I_{OUT(MAX)}$ is the maximum load current. I_{RMS} has a maximum value when the input voltage equals twice the output voltage (V_{IN} = 2 x V_{OUT}), so

$$I_{RMS(MAX)} = \frac{I_{OUT(MAX)}}{2}.$$

Choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current for optimal long-term reliability. Use low-ESR ceramic capacitors with high-ripple-current capability at the input. X7R capacitors are recommended in industrial applications for their temperature stability.

Calculate the input capacitance using the following equation.

$$C_{IN} = \frac{I_{OUT(MAX)} \times D \times (1 - D)}{\eta \times f_{SW} \times \Delta V_{IN}}$$

where:

D = V_{OUT}/V_{IN} is the duty ratio of the converter

f_{SW} = Switching frequency (Hz)

ΔV_{IN} = Allowable input-voltage ripple (V)

η = Efficiency

In applications where the source is located distant from the device input, an appropriate electrolytic capacitor should be added in parallel to the ceramic capacitor to provide necessary damping for potential oscillations caused by the inductance of the longer input cables and the input ceramic capacitor. Actual derating of ceramic capacitors with DC-bias voltage must be considered while selecting the input capacitor. Derating curves are available from all major ceramic capacitor manufacturers.

Inductor Selection

Three key inductor parameters must be specified for operation with the device: inductance value (L), inductor saturation current (I_{SAT}) and DC resistance (R_{DCR}). Calculate the inductor value for a given output voltage and switching frequency using the following equation.

$$L = \frac{V_{OUT} \times 0.8}{f_{SW}}$$

where V_{OUT} and f_{SW} are nominal values and f_{SW} is in Hz. Select an inductor whose value is nearest to the value calculated by the above formula. Select a low-loss inductor with acceptable dimensions, having the lowest possible DC resistance. The saturation current rating (I_{SAT}) of the inductor must be high enough to ensure that saturation occurs only above $I_{PEAK-LIMIT}$.

Output-Capacitor Selection

X7R ceramic output capacitors are preferred due to their stability over temperature in industrial applications. The output capacitors are sized to support a step load of 40% (1A) of the maximum output current in the application, so the output-voltage deviation is contained to 3% of the output-voltage change. The minimum required output capacitance can be

calculated as follows:

$$C_{OUT} = \frac{1}{2} \times \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_{OUT}}$$

$$t_{RESPONSE} \cong \frac{0.35}{f_C}$$

where:

I_{STEP} = Load current step (A),

$t_{RESPONSE}$ = Response time of the controller (s),

ΔV_{OUT} = Allowable output-voltage deviation (V),

f_C = Target closed-loop crossover frequency (Hz),

f_{SW} = Switching frequency (kHz)

Select f_C to be 1/10th of f_{SW} if the switching frequency is less than or equal to 800kHz. If the switching frequency is more than 800kHz, select f_C to be 80kHz. Actual derating of ceramic capacitors with DC-bias voltage must be considered while selecting the output capacitor. Derating curves are available from all major ceramic capacitor manufacturers.

Adjusting Output Voltage

Set the output voltage using a resistive voltage-divider connected from the output-voltage node (V_{OUT}) to GND (see Figure 3). Connect the center node of the divider to the FB pin. Use the following procedure to choose the resistive voltage-divider values:

Calculate resistor R_{FB_TOP} from the output to the FB pin as follows:

$$R_{FB\_TOP} = \frac{216}{\left(f_C \times C_{OUT\_SEL}\right)}$$

where:

R_{FB_TOP} is in kΩ

f_C = Crossover frequency (Hz)

C_{OUT_SEL} = Actual capacitance of output capacitor at DC-bias voltage (F).

Calculate resistor R_{FB_BOT} from the FB pin to GND as follows:

$$R_{FB\_BOT} = \frac{R_{FB\_TOP} \times 0.9}{\left(V_{OUT} - 0.9\right)}$$

where R_{FB_BOT} is in kΩ.

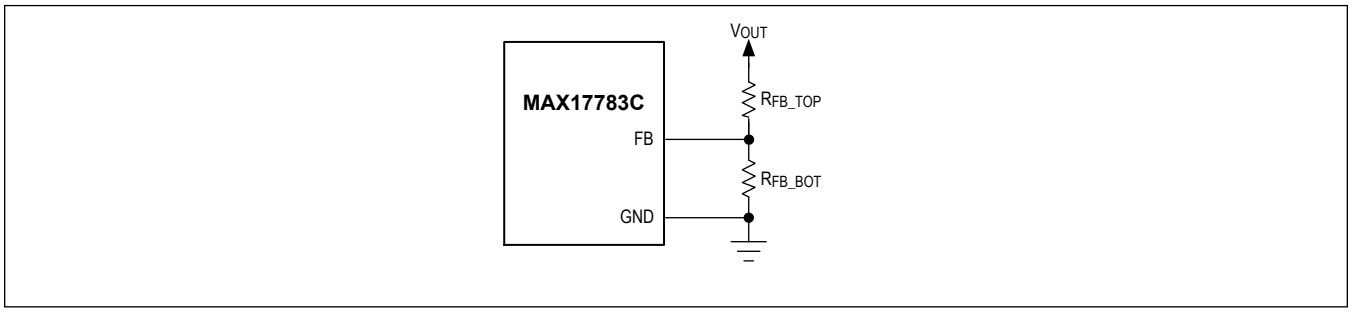


Figure 3. Setting the Output Voltage

Soft-Start Capacitor Selection

The MAX17783C offers an adjustable soft-start operation to reduce inrush current. A capacitor connected from the SS pin to GND programs the soft-start time. The selected output capacitance (C_{OUT_SEL}) and the output voltage (V_{OUT}) determine the minimum required soft-start capacitor as follows:

$$C_{SS} \geq 28 \times 10^{-6} \times C_{OUT\_SEL} \times V_{OUT}$$

The soft-start time (t_{SS}) is related to the capacitor connected at SS (C_{SS}) by the following equation:

$$t_{SS} = \frac{C_{SS}}{5.55 \times 10^{-6}}$$

For example, to program a 1ms soft-start time, a 5.6nF capacitor should be connected from the SS pin to GND. Note that during start-up, the device operates at half the programmed switching frequency until the feedback (FB) voltage reaches $V_{FB-HICF}$ (0.58V).

Setting the Input Undervoltage-Lockout Level

The device offers an adjustable input undervoltage-lockout level. Set the voltage above which the device turns on/off with a resistive voltage-divider connected from IN to GND as shown in Figure 4. Connect the center node of the divider to the EN/UVLO pin. Choose R_{UVL_TOP} to be 3.32MΩ and then calculate R_{UVL_BOT} as follows:

$$R_{UVL\_BOT} = \frac{R_{UVL\_TOP} \times 1.218}{\left(V_{INU} - 1.218\right)}$$

where V_{INU} is the input-voltage level at which the device is required to turn on. Ensure that V_{INU} is higher than 0.8 x V_{OUT}. If the EN/UVLO pin is driven from an external signal source, a series resistance of minimum 1kΩ is recommended to be placed between the output pin of signal source and the EN/UVLO pin to reduce voltage ringing on the line.

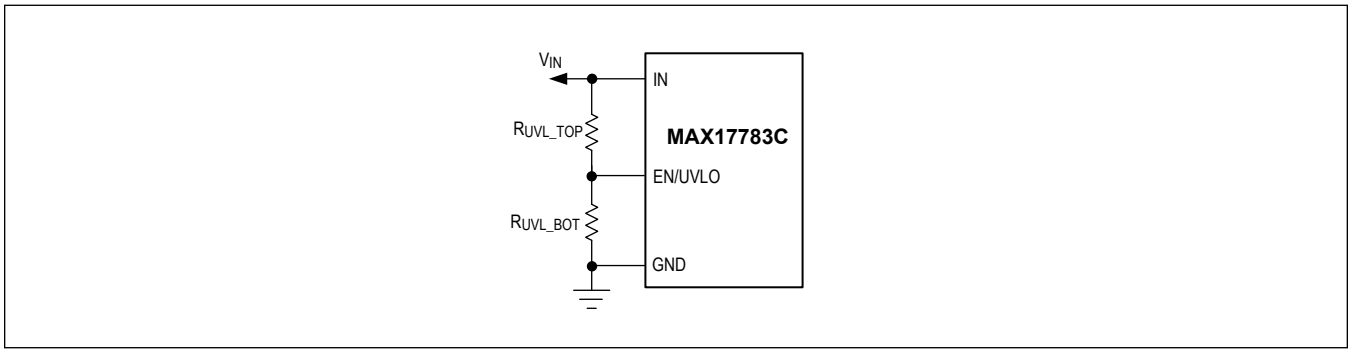


Figure 4. Setting the Input Undervoltage Lockout

Power Dissipation

At a given operating condition, the power losses that lead to temperature rises of the part are estimated as follows:

$$P_{LOSS} = \left(P_{OUT} \times \left(\frac{1}{\eta} - 1\right)\right) - \left(I_{OUT}^{2} \times R_{DCR}\right) - (V_D \times I_{OUT} \times (1 - D))$$

$$P_{OUT} = V_{OUT} \times I_{OUT}$$

where:

P_{OUT} = Output power

η = Efficiency of the converter

D = Operating duty cycle

R_{DCR} = DC resistance of the inductor

(see the *Typical Operating Characteristics* for more information on efficiency at typical operating conditions).

The junction temperature of the device can be estimated at any given maximum ambient temperature (T_A) using the following equation.

$$T_J = T_A + (\theta_{JA} \times P_{LOSS})$$

PCB Layout Guidelines

All connections carrying pulsed currents must be very short and as wide as possible. The inductance of these connections must be kept to an absolute minimum due to the high di/dt of the currents. Since inductance of a current-carrying loop is proportional to the area enclosed by the loop, if the loop area is made very small, inductance is reduced. Additionally, small-current loop areas reduce radiated EMI.

A ceramic input filter capacitor should be placed close to the IN pin of the device. This eliminates as much trace inductance effects as possible and gives the device a cleaner voltage supply. A bypass capacitor for the V_{CC} pin should also be placed close to the pin to reduce the effects of trace impedance.

When routing the circuitry around the device, the analog small signal ground and the power ground for switching currents must be kept separate. They should be connected together at a point where switching activity is minimum. This helps keep the analog ground quiet. The ground plane should be kept continuous (unbroken) as far as possible. No trace carrying high-switching current should be placed directly over any ground plane discontinuity.

PCB layout also affects the thermal performance of the design. A number of thermal throughputs that connect to a large ground plane should be provided under the exposed pad of the part for efficient heat dissipation.

For a sample layout that ensures first pass success, refer to the MAX17783C evaluation kit layout available at www.maximintegrated.com.

Typical Application Circuits

MAX17783C 5V Application Circuit

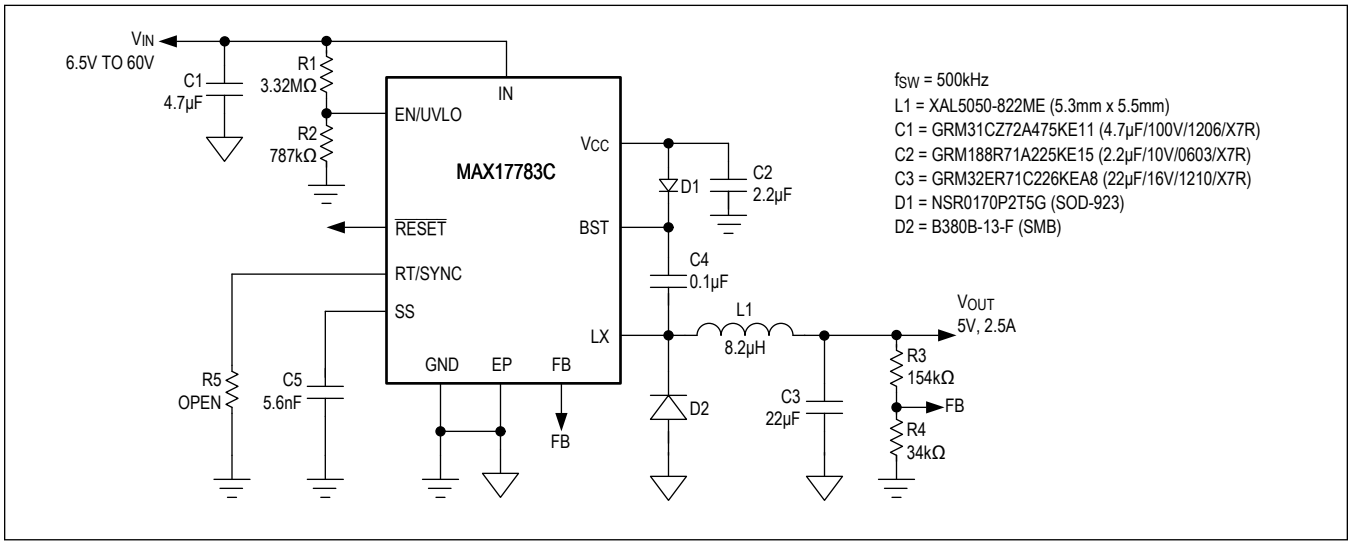


Figure 5. 5V Step-Down DC-DC Converter at 500kHz Switching Frequency

Typical Application Circuits (continued)

MAX17783C 3.3V Application Circuit

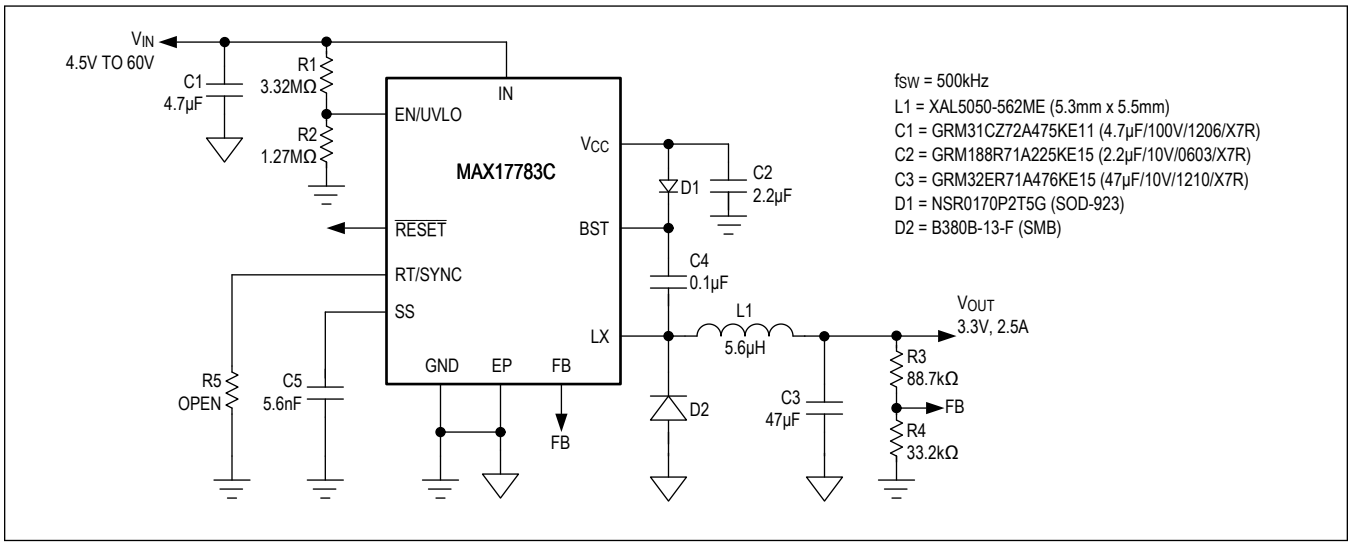


Figure 6. 3.3V Step-Down DC-DC Converter at 500kHz Switching Frequency

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PIN-PACKAGE
MAX17783CATB+	-40°C to +125°C	10 TDFN 3mm x 3mm
MAX17783CATB+T	-40°C to +125°C	10 TDFN 3mm x 3mm

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	11/20	Initial release	—