Doc. Number :

☐ Tentative Specification
☐ Preliminary Specification
■ Approval Specification

MODEL NO.: R213RFE
SUFFIX: L01

Customer: general customer

APPROVED BY **SIGNATURE**

Name / Title
Note

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By
陳立錚	張喻翔	郭榮欽

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REVISION HISTORY

Version	Date	Page	Description
1.0	06, Nov,2014	ALL	Spec Ver.1.0 was first issued.
1.1	12, Aug,2015	5	Section 1.3，Power Consumption modified
	12, Aug,2015	7	Section3.2.2，LED forward current modified
	12, Aug.,2015	15	Section4.3.3，LED light bar current modified
	12, Aug.,2015	22	New add NOTE：Tv(Tvd+Tvb) must be integer, otherwise, this module would operate abnormally.
	12, Aug.,2015	25	Color point spec modify
2.0	12, Nov. 2015	ALL	Spec Ver.2.0 first issued
2.1	18, Oct. 2016	37	Outline Drawing modify (two converter)
2.2	10, Mar. 2017	5	Outline Drawing modify (thickness is 22.67mm)
2.3	2, Nov. 2017	5	Section 1.3 General Specifications modify
		15	Section 4.3.4 Converter electrical charateristics modify
		25	Section 5.2 Optical Specifications & Note6 modify
2.4	13, Jul. 2018	5	Section 2. MECHANICAL SPECIFICATIONS modify
		22	Section 4.5 DISPLAY TIMING SPECIFICATIONS modify
		33	Section 8. INX MODULE LABEL modify
		36	Section Appendix. OUTLINE DRAWING modify
2.5	13, Jul. 2018	36	Section Appendix. OUTLINE DRAWING modify
2.6	13,May.2020	37,38	Appendix. OUTLINE DRAWING modify

1. GENERAL DESCRIPTION

1.1 OVERVIEW

R213RFE-L01 is a 21.3" TFT Liquid Crystal Display module with LED Backlight unit and one 41-pin LVDS port and one 51-pin LVDS port each port has 2ch-LVDS interface. This module supports 2048 x 1536 QXGA mode and can display color driven by 10bit drivers. The LCD module includes built-in converter for Backlight.

1.2 FEATURES

This specification applies to the Type 21.3" color TFT LCD Module, Model R213RFE-L01

This module includes a converter card for the LED backlight unit.

The screen format is intended to support 2048(H) x 1536(V) resolution.

All input signals are LVDS (Low Voltage Differential Signaling) interface.

This module is UL approved and RoHs compliant

This module is 8/10bit compatible (default is 10bit)

1.3 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Screen Size	21.3" real diagonal		
Driver Element	a-si TFT active matrix	-	-
Pixel Number	2048(x3) x 1536	Pixel	-
Pixel Pitch	0.2115 (H) x 0.2115 (V)	Mm	-
Pixel Arrangement	Sub-pixel Vertical stripe	-	-
Display Colors	1.07G	-	-
Transmissive Mode	Dual domain IPS, Normally Black	-	-
Surface Treatment	Anti-glare, Hardness: 3H	-	-
Luminance, White	1000	Cd/m2	-
Power Consumption	Total 65W (typ.) @ cell 10 W (typ.), BL 55W (typ.)		(1)

Note (1) The specified power consumption: Total= cell (reference 4.3.1)+BL (reference 4.3.3)

2. MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	456.5	457	457.5	mm	(1)
	Vertical (V)	349.5	350	350.5	mm	
	Thickness (T)	22.17	22.67	23.17	mm	
Bezel Area	Horizontal	437.7	438.2	438.7	mm	
	Vertical	329.5	330	330.5	mm	
Active Area	Horizontal		433.15		mm	
	Vertical		324.86		mm	
Weight		2888	3040	3192	g	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

3. ABSOLUTE MAXIMUM RATINGS

3.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	TST	-20	60	ºC	(1)
Operating Ambient Temperature	TOP	0	50	ºC	(1), (2)

Note (1)

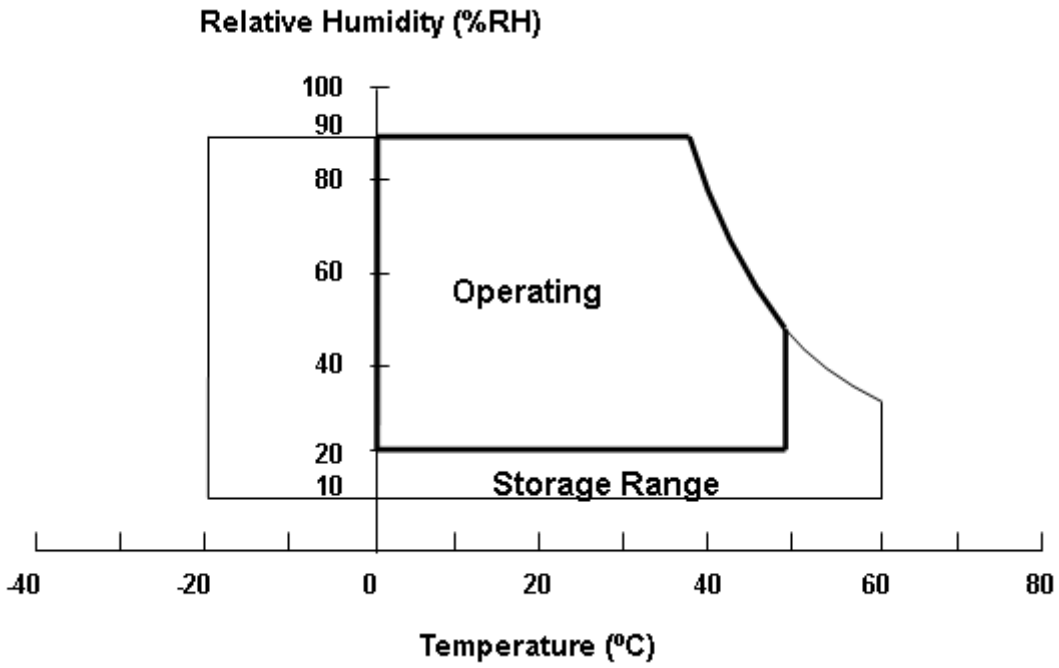
(a) 90 %RH Max. (Ta < 40 ºC).

(b) Wet-bulb temperature should be 39^0 C Max.

(c) No condensation.

Note (2)

The temperature of panel surface should be 0^0C min. and 60 ºC max



3.2 ELECTRICAL ABSOLUTE RATINGS

3.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCCS	-0.3	13.2	V	(1)
Logic Input Voltage	V_{IN}	-0.3	3.6	V	

3.2.2 BACKLIGHT UNIT

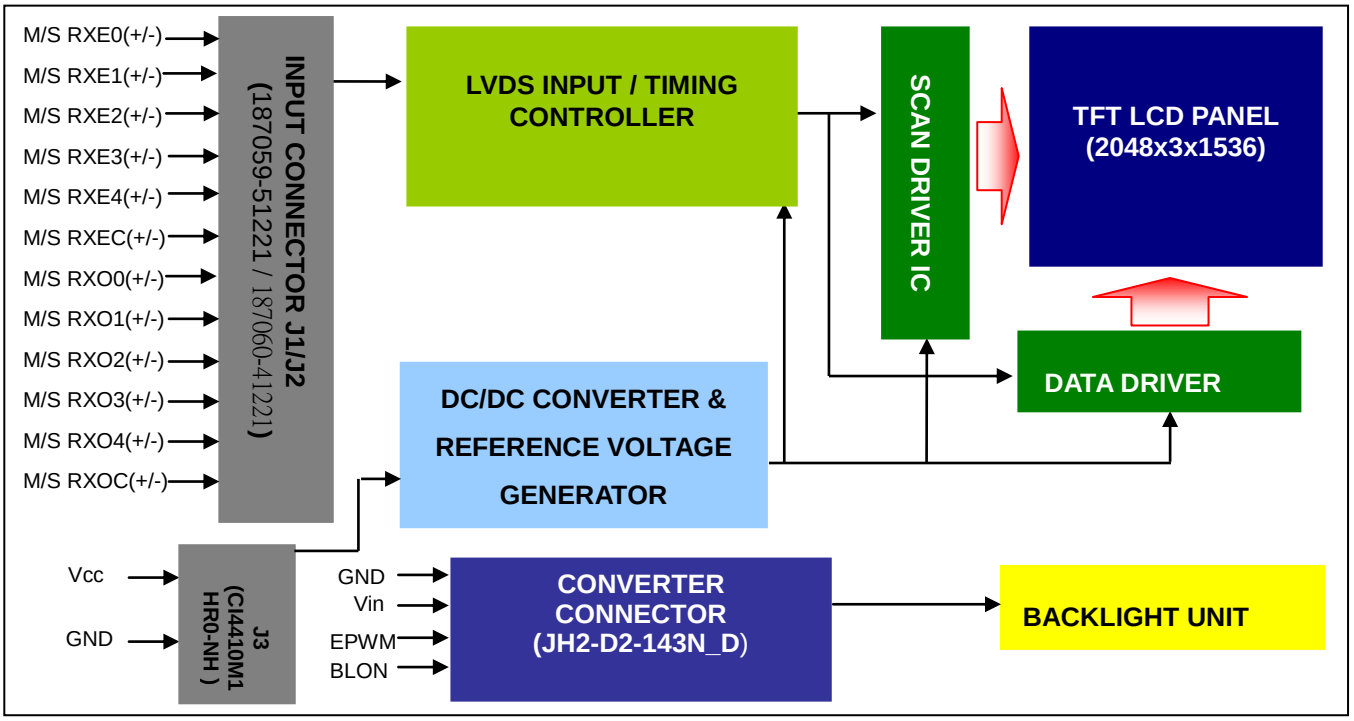
Item	Symbol	Value			Unit	Note
		Min.	Typ	Max.		
LED Forward Current Per Input Pin	I_F	---	130	280	mA	(1), (2) Duty=100%
LED Reverse Voltage Per Input Pin	V_R	---	---	60	V	
LED Pulse Forward Current Per Input Pin	I_P	---	---	500	mA	(1), (2) Pulse Width≦10μsec. and Duty≦0.5%

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) Specified values are for input pin of LED light bar at Ta=25±2 ℃ (Refer to 4.3.3 and 4.3.4 for further information).

4. ELECTRICAL SPECIFICATIONS

4.1 FUNCTION BLOCK DIAGRAM



4.2. INPUT INTERFACE CONNECTIONS

4.2.1 J1 (MASTER) : LEFT SIDE(FRONT VIEW)

Pin	Name	Description
1	GND	LVDS Ground
2	GND	LVDS Ground
3	GND	LVDS Ground
4	MRXE0-	Negative LVDS differential data input. Channel E0 (even)
5	MRXE0+	Positive LVDS differential data input. Channel E0 (even)
6	GND	LVDS Ground
7	MRXE1-	Negative LVDS differential data input. Channel E1 (even)
8	MRXE1+	Positive LVDS differential data input. Channel E1 (even)
9	GND	LVDS Ground
10	MRXE2-	Negative LVDS differential data input. Channel E2 (even)
11	MRXE2+	Positive LVDS differential data input. Channel E2 (even)
12	GND	LVDS Ground
13	MRXEC-	Negative LVDS differential clock input. (even)
14	MRXEC+	Positive LVDS differential clock input. (even)
15	GND	LVDS Ground
16	MRXE3-	Negative LVDS differential data input. Channel E3 (even)
17	MRXE3+	Positive LVDS differential data input. Channel E3 (even)
18	GND	LVDS Ground
19	MRXE4-	Negative LVDS differential data input. Channel E4 (even)
20	MRXE4+	Positive LVDS differential data input. Channel E4 (even)
21	GND	LVDS Ground
22	MRXO0-	Negative LVDS differential data input. Channel O0 (odd)
23	MRXO0+	Positive LVDS differential data input. Channel O0 (odd)
24	GND	LVDS Ground
25	MRXO1-	Negative LVDS differential data input. Channel O1 (odd)
26	MRXO1+	Positive LVDS differential data input. Channel O1 (odd)
27	GND	LVDS Ground
28	MRXO2-	Negative LVDS differential data input. Channel O2 (odd)
29	MRXO2+	Positive LVDS differential data input. Channel O2 (odd)
30	GND	LVDS Ground
31	MRXOC-	Negative LVDS differential clock input. (odd)
32	MRXOC+	Positive LVDS differential clock input. (odd)
33	GND	LVDS Ground
34	MRXO3-	Negative LVDS differential data input. Channel O3 (odd)
35	MRXO3+	Positive LVDS differential data input. Channel O3 (odd)
36	GND	LVDS Ground
37	MRXO4-	Negative LVDS differential data input. Channel O4 (odd)
38	MRXO4+	Positive LVDS differential data input. Channel O4 (odd)
39	GND	LVDS Ground
40	GND	LVDS Ground
41	BIT_SEL	Bit mode selection pin; 0: 10bit (default), 1: 8bit Note (5)
42	NC	Not connection, this pin should be open
43	LVDS_SEL	LVDS Format mode selection pin; 0: VESA (default), 1: JEITA Note (6)
44	NC	Not connection, this pin should be open
45	GND	LVDS Ground
46	GND	LVDS Ground
47	GND	LVDS Ground
48	NC	Not connection, this pin should be open

49	NC	Not connection, this pin should be open
50	NC	Not connection, this pin should be open
51	GND	LVDS Ground

4.2.2 J2 (SLAVE): RIGHT SIDE(FRONT VIEW)

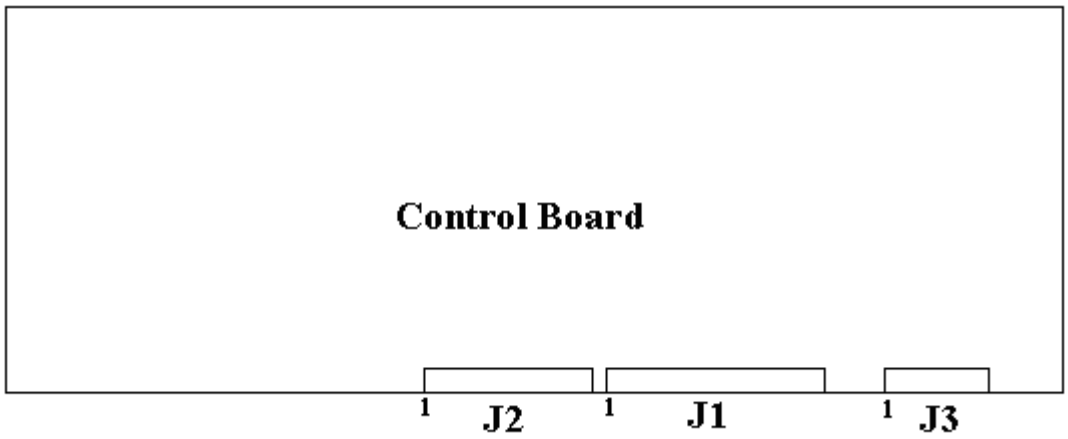
Pin	Name	Description
1	GND	LVDS Ground
2	GND	LVDS Ground
3	GND	LVDS Ground
4	SRXE0-	Negative LVDS differential data input. Channel E0 (even)
5	SRXE0+	Positive LVDS differential data input. Channel E0 (even)
6	GND	LVDS Ground
7	SRXE1-	Negative LVDS differential data input. Channel E1 (even)
8	SRXE1+	Positive LVDS differential data input. Channel E1 (even)
9	GND	LVDS Ground
10	SRXE2-	Negative LVDS differential data input. Channel E2 (even)
11	SRXE2+	Positive LVDS differential data input. Channel E2 (even)
12	GND	LVDS Ground
13	SRXEC-	Negative LVDS differential clock input. (even)
14	SRXEC+	Positive LVDS differential clock input. (even)
15	GND	LVDS Ground
16	SRXE3-	Negative LVDS differential data input. Channel E3 (even)
17	SRXE3+	Positive LVDS differential data input. Channel E3 (even)
18	GND	LVDS Ground
19	SRXE4-	Negative LVDS differential data input. Channel E4 (even)
20	SRXE4+	Positive LVDS differential data input. Channel E4 (even)
21	GND	LVDS Ground
22	SRXO0-	Negative LVDS differential data input. Channel O0 (odd)
23	SRXO0+	Positive LVDS differential data input. Channel O0 (odd)
24	GND	LVDS Ground
25	SRXO1-	Negative LVDS differential data input. Channel O1 (odd)
26	SRXO1+	Positive LVDS differential data input. Channel O1 (odd)
27	GND	LVDS Ground
28	SRXO2-	Negative LVDS differential data input. Channel O2 (odd)
29	SRXO2+	Positive LVDS differential data input. Channel O2 (odd)
30	GND	LVDS Ground
31	SRXOC-	Negative LVDS differential clock input. (odd)
32	SRXOC+	Positive LVDS differential clock input. (odd)
33	GND	LVDS Ground
34	SRXO3-	Negative LVDS differential data input. Channel O3 (odd)
35	SRXO3+	Positive LVDS differential data input. Channel O3 (odd)
36	GND	LVDS Ground
37	SRXO4-	Negative LVDS differential data input. Channel O4 (odd)
38	SRXO4+	Positive LVDS differential data input. Channel O4 (odd)
39	GND	LVDS Ground
40	GND	LVDS Ground
41	GND	LVDS Ground

Note (1) the first pixel is even.

Note (2) Input signal of even and odd clock should be the same timing.

Note (3) the module uses a 100-ohm resistor between positive and negative data lines of each receiver input

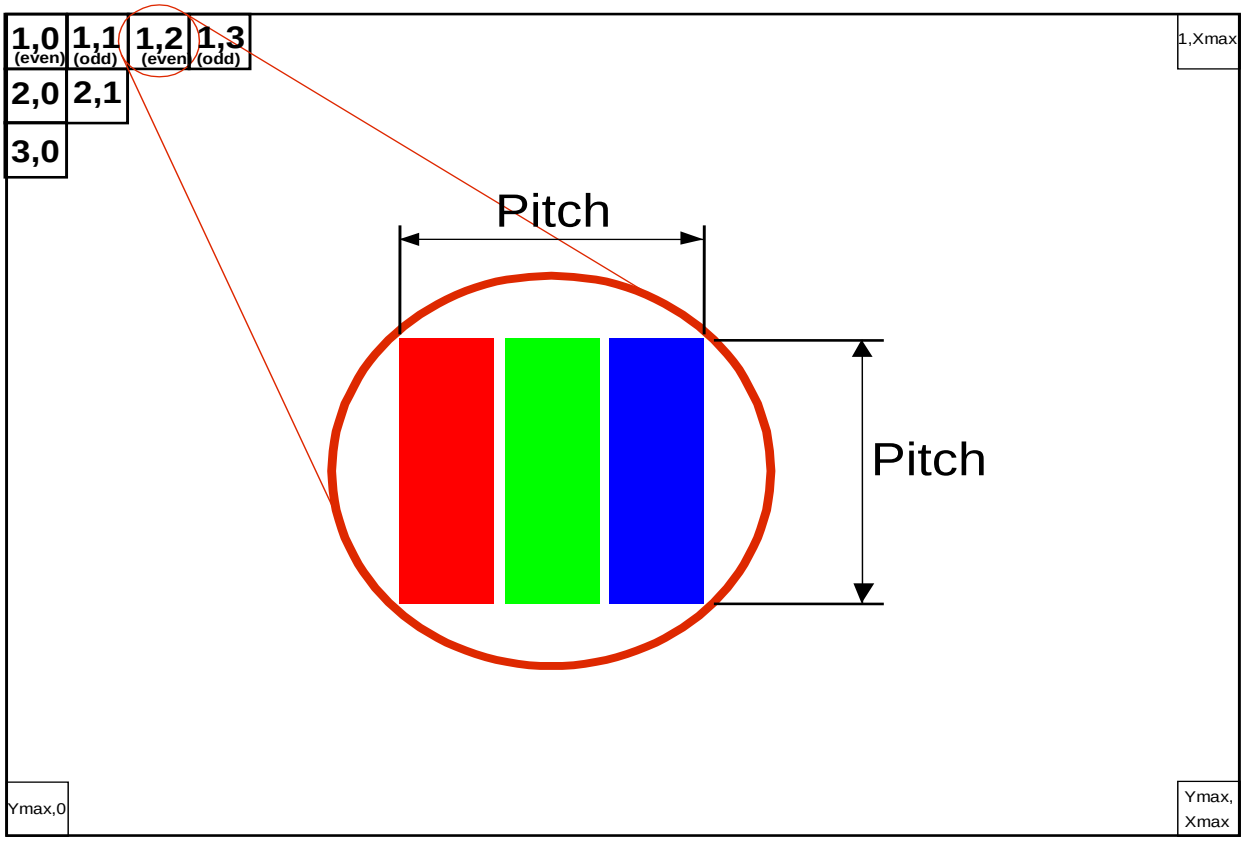
Note (4) Control board front view



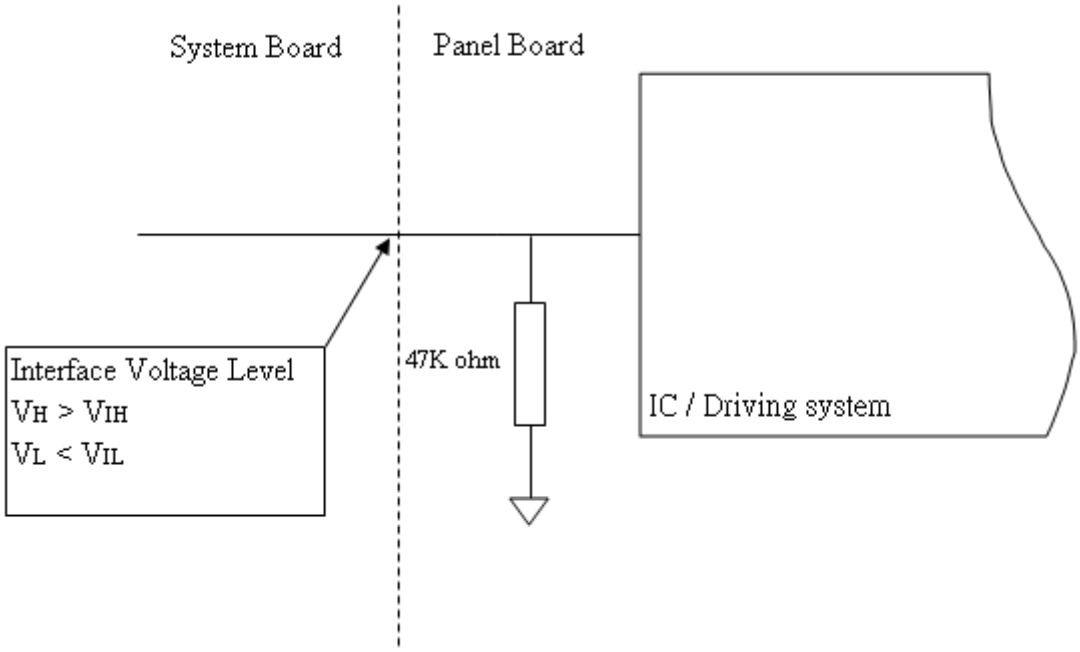
J1: 187059-51221 (P-two) or equivalent; LVDS input for LEFT half screen

J2: 187060-41221 (P-two) or equivalent; LVDS input for RIGHT half screen

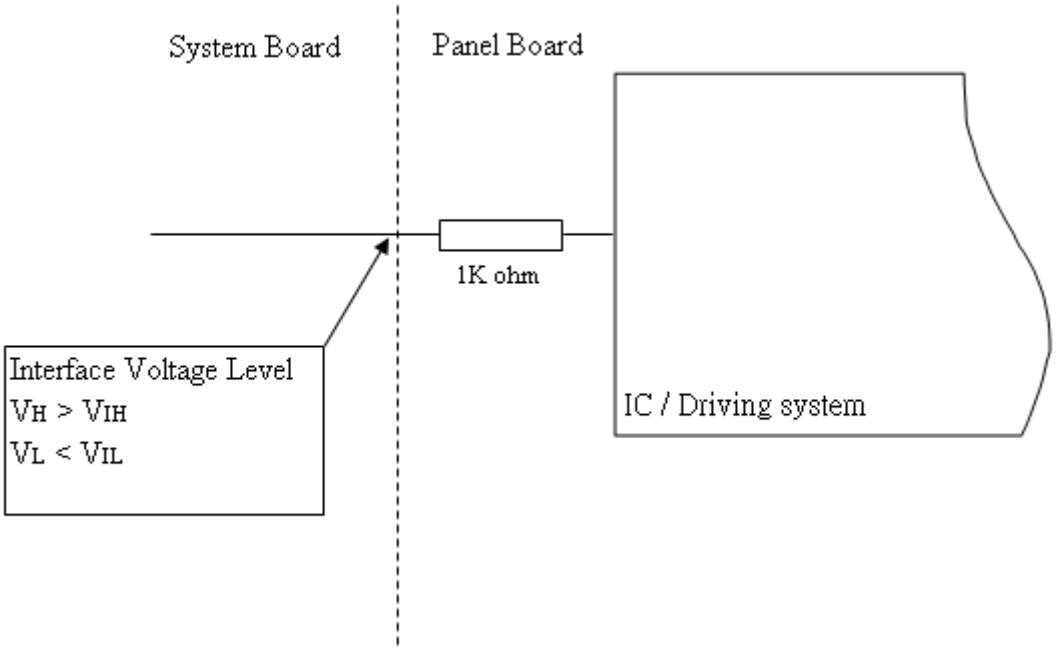
J3: CI4410M1HR0-NH (Cvilux): Power input (+12V) ;



Note (5) Interface optional pin has internal scheme as following diagram, Customer should keep the interface voltage level requirement which including panel board loading as below.



Note (6) Interface optional pin has internal scheme as following diagram, Customer should keep the interface voltage level requirement which including panel board loading as below.



4.2.3 J3 DC INPUT PIN ASSIGNMENT

Pin	Name	Description
1	Vcc	+12.0V Power Supply for Control board
2	Vcc	+12.0V Power Supply for Control board
3	Vcc	+12.0V Power Supply for Control board
4	Vcc	+12.0V Power Supply for Control board
5	Vcc	+12.0V Power Supply for Control board
6	GND	Ground for Vcc
7	GND	Ground for Vcc
8	GND	Ground for Vcc
9	GND	Ground for Vcc
10	GND	Ground for Vcc

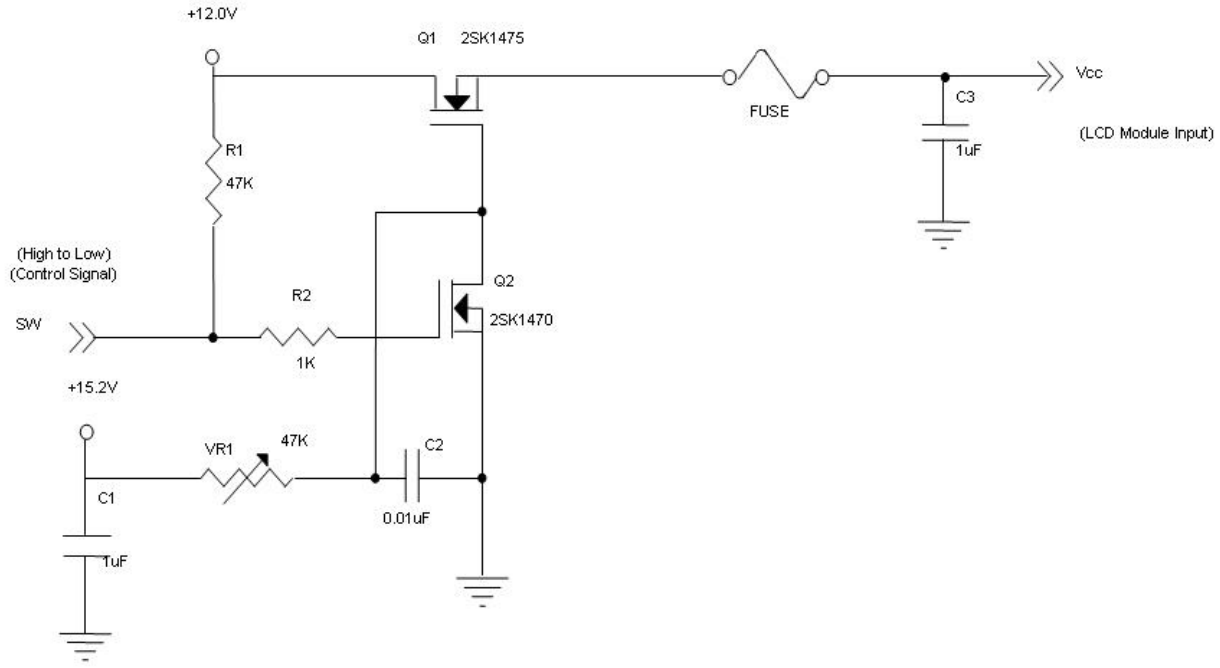
4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD ELETRONICS SPECIFICATION

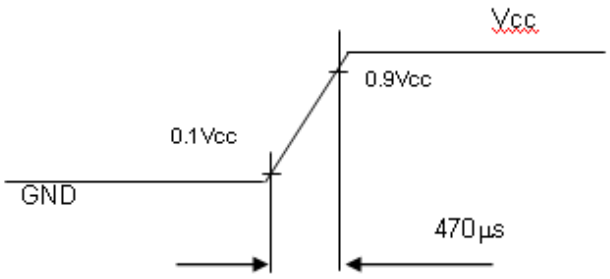
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		Vcc	11.4	12	12.6	V	-
Ripple Voltage		V_{RP}	-	-	300	mV	-
Rush Current		I_{RUSH}	-	-	2	A	(2)
Power Supply Current	White		-	0.82	1	A	(3)a
	Black		-	0.44	0.53	A	(3)b
	Vertical Stripe		-	0.7	0.84	A	(3)c
Power Consumption		PLCD	-	10	12	Watt	(4)
LVDS differential input voltage		Vid	200	-	600	mV	(5)
LVDS common input voltage		Vic	1.0	1.2	1.4	V	
Logic High Input Voltage		VIH	2.31	-	3.3	V	
Logic Low Input Voltage		VIL	0	-	1	V	

Note (1) The ambient temperature is Ta = 25 ± 2 ºC.

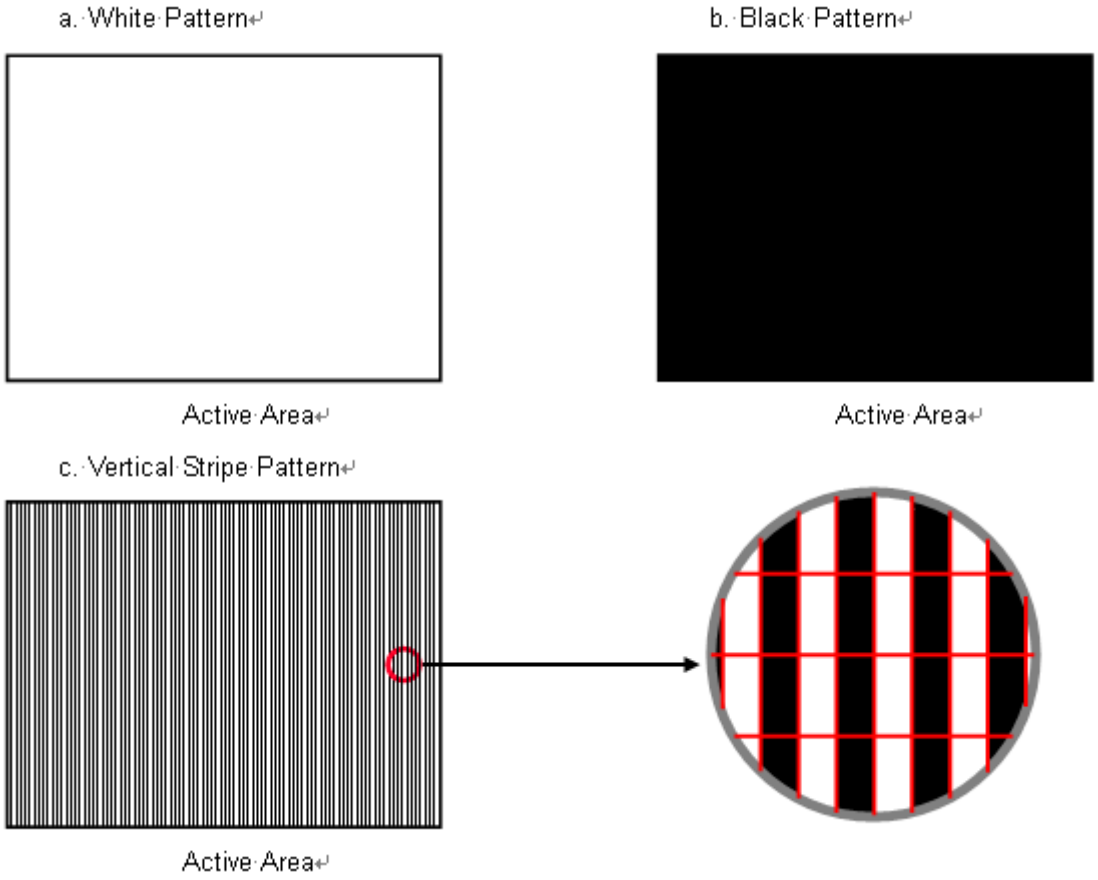
Note (2) Measurement Conditions:



Vcc rising time is 470µs

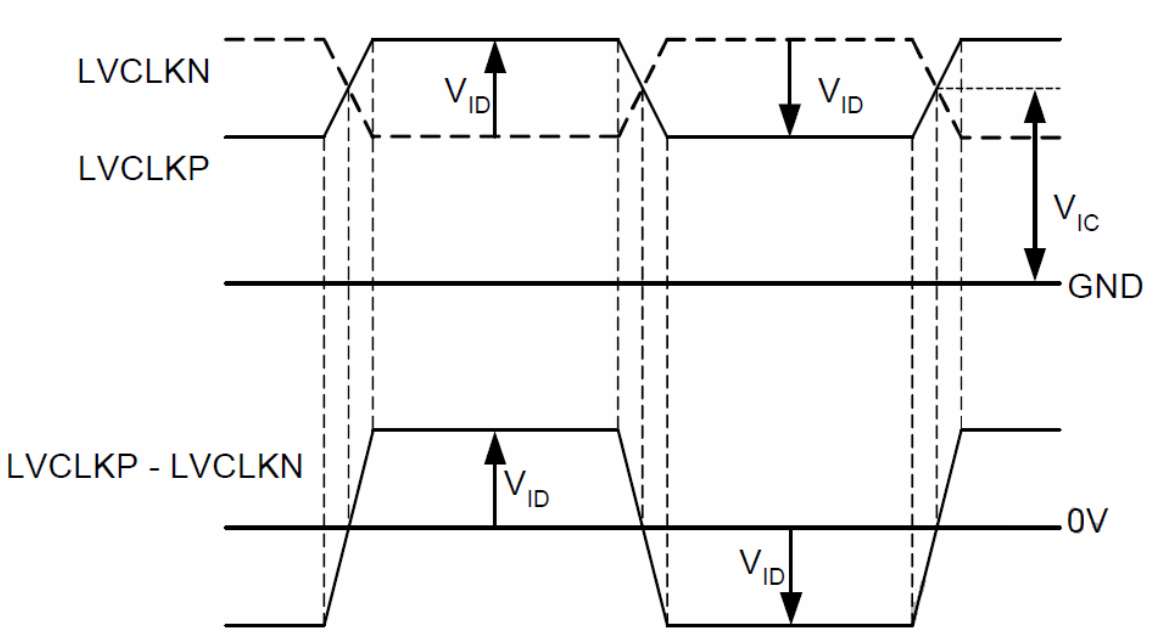


Note (3) The specified power supply current is under the conditions at Vcc = 12.0 V, Ta = 25 ± 2 ºC, Fr = 50Hz, whereas a power dissipation check pattern below is displayed.

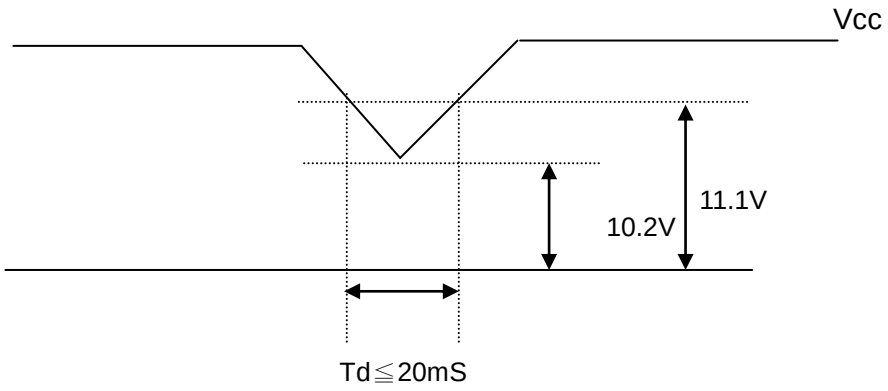


Note (4) The power consumption is specified at the pattern with the maximum current.

Note (5) VID waveform condition



4.3.2 Vcc Power Dip Condition



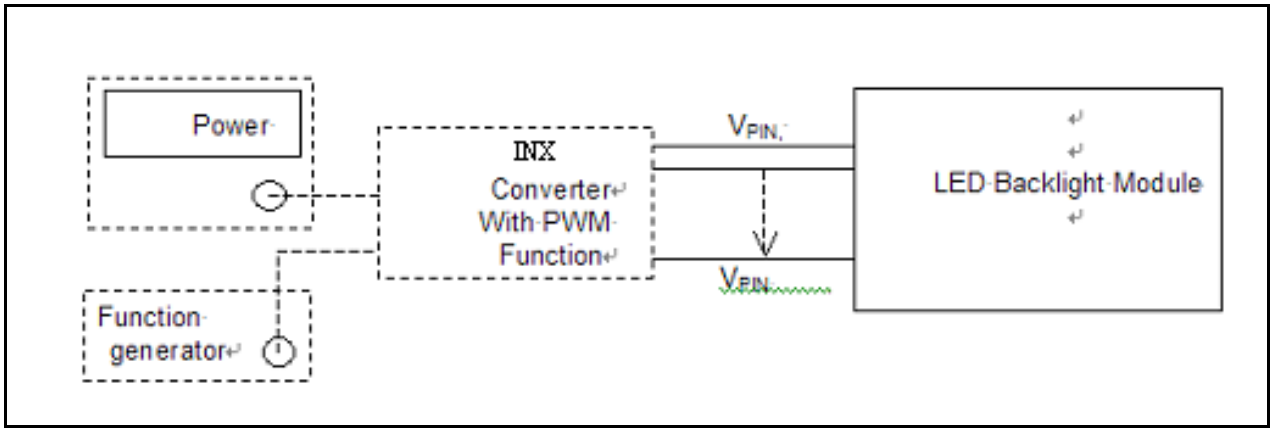
4.3.3 BACKLIGHT UNIT

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
LED Light Bar Input Voltage Per Input Pin	VPIN	29	32	35	V	(1), Duty=100%, IPIN=130mA
LED Light Bar Current Per Input Pin	IPIN	0	130	280	mA	(1), (2) Duty=100%
LED Life Time	LLED	50000			Hrs	(3)
Power Consumption	PBL	---	55	60	W	(1) Duty=100%, IPIN=130mA

Note (1) LED light bar input voltage and current are measured by utilizing a true RMS multi-meter as shown below:

Note (2) PBL = IPIN × VPIN × input pins

Note (3) The lifetime of LED is estimated and defined as the time when LED packages continue to operate under the conditions at Ta = 25 ±2 ℃ and I= 130 mA (per chip) until the brightness becomes ≦ 50% of its original value.



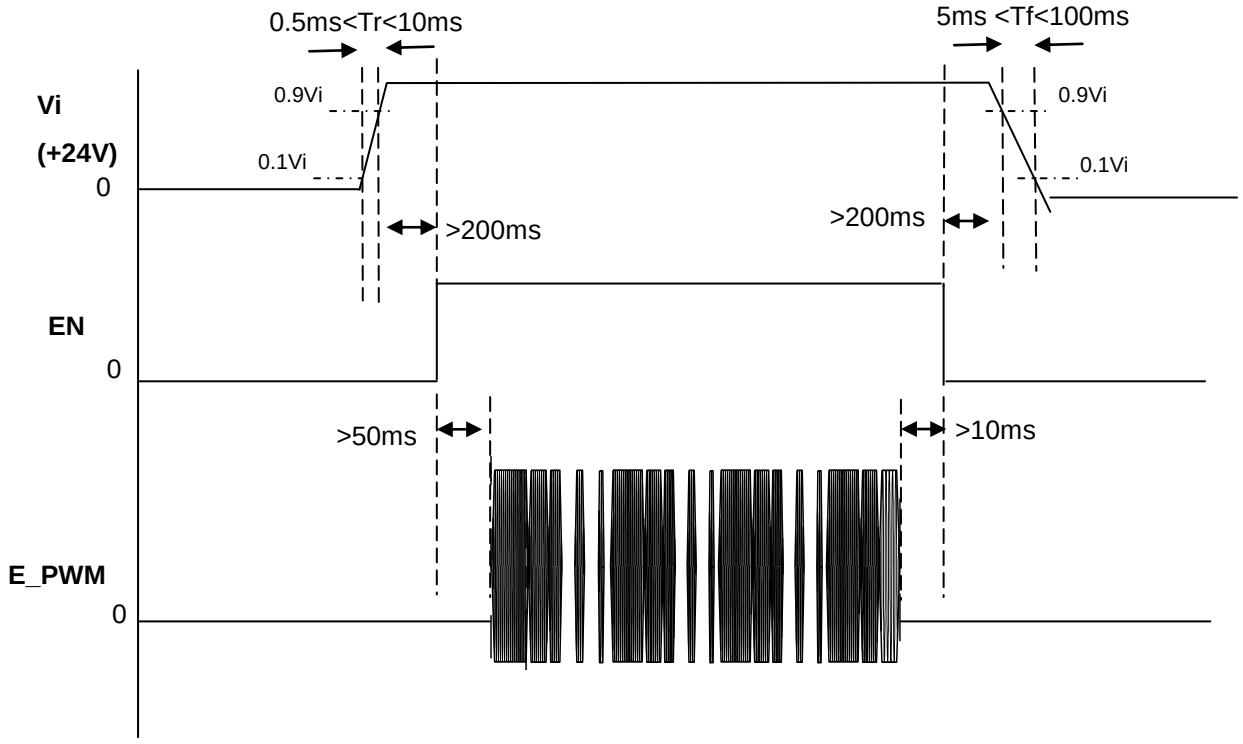
4.3.4 CONVERTER ELECTRICAL CHARATERISTICS

Ta = 25 ± 2 ºC

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Converter Power Supply Voltage		V_i	21.6	24.0	26.4	V	(Duty 100%)
Converter Power Supply Current		I_i	---	2.3	2.8	A	@ Vi = 24V (Duty 100%)
Input Power Consumption		P_O	---	55	60	W	@ Vi = 24V (Duty 100%)
BL Control Level	Backlight on	BLON	2.5	3.3	5.0	V	
	Backlight off		0	0	0.2	V	
PWM Control Level	PWM High Level	E_PWM	2.5	3.3	5.0	V	
	PWM Low Level		0	0	0.2	V	
PWM Control Duty Ratio			5		99.8	%	@200Hz,(1)
PWM Control Frequency		f_{PWM}	100	200	1000	Hz	(1)

Note (1) At 200 Hz PWM control frequency, duty ratio range is restricted from 1% to 99.8%,
When PWM control frequency is 1000Hz, duty ratio range is restricted from 5% to 99.8%.

Power sequence and control signal timing are shown in the following figure



Note： While system is turned ON or OFF, the power sequences must follow as below descriptions

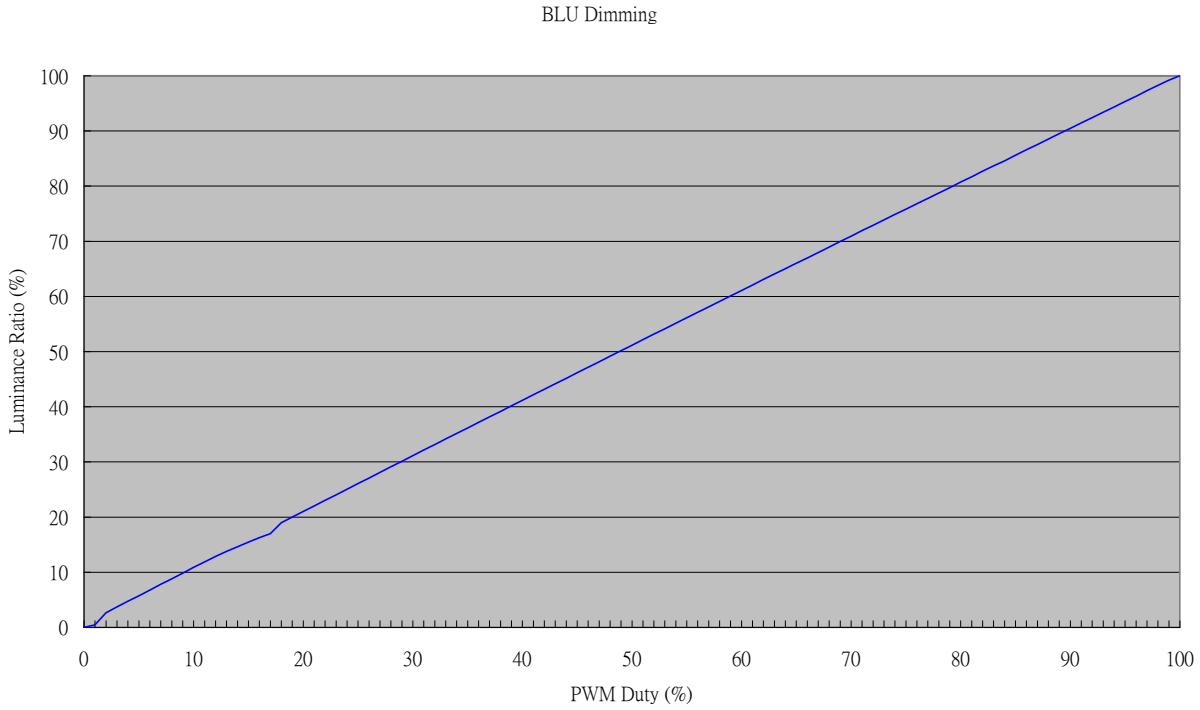
Turn ON sequence: Vi(+24V) → BLON → E_PWM signal

Turn OFF sequence: E_PWM signal → BLON → Vi(+24V)

The definition of T_r : the time period of 10%*V_i to 90%*V_i

The definition of T_f : the time period of 90%*V_i to 10%*V_i

The following chart is the BLU Dimming for your reference.



4.3.5 CONVERTER INPUT CONNECTOR PIN ASSIGNMENT

Connector: FCN JH2-D2-143N_D or equivalent

Pin №	Signal name	Feature
1	V_{BL}	+24 V
2		
3		
4		
5		
6	GND	GND
7		
8		
9		
10		
11	NC	NC
12	BLON	BL ON/OFF (ON:5V, OFF:0V)
13	NC	NC
14	E_PWM	External PWM Control (Hi Level: 5V, Lo Level: 0V)

4.4 LVDS INPUT SIGNAL SPECIFICATIONS

4.4.1 LVDS DATA INPUT DATA ORDER (VESA Mode)

VESA mode: LVDS_SEL= L (0V)

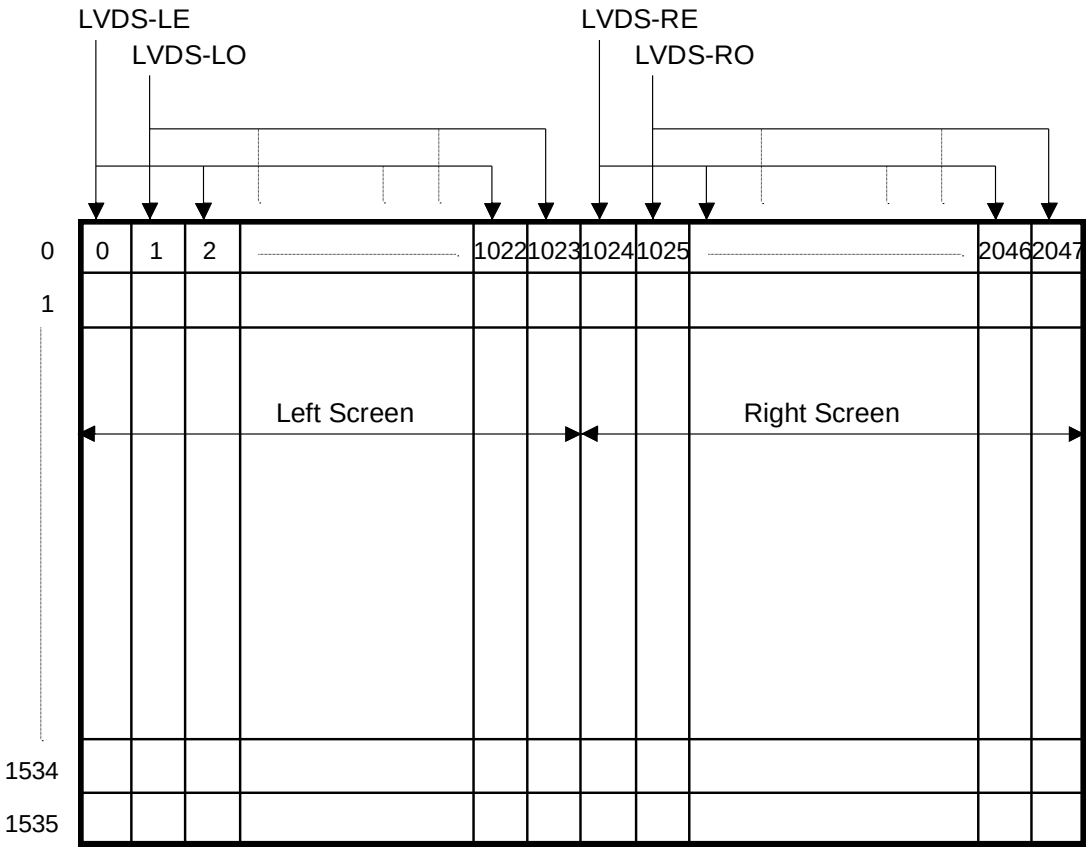
LVDS interface receiver required input data mapping table								
LVDS Channel E0	LVDS output	TA6	TA5	TA4	TA3	TA2	TA1	TA0
	Data order	EB0	EA5	EA4	EA3	EA2	EA1	EA0
LVDS Channel E1	LVDS output	TB6	TB5	TB4	TB3	TB2	TB1	TB0
	Data order	EC1	EC0	EB5	EB4	EB3	EB2	EB1
LVDS Channel E2	LVDS output	TC6	TC5	TC4	TC3	TC2	TC1	TC0
	Data order	DE	VS	HS	EC5	EC4	EC3	EC2
LVDS Channel E3	LVDS output	TD6	TD5	TD4	TD3	TD2	TD1	TD0
	Data order	NA	EC7	EC6	EB7	EB6	EA7	EA6
LVDS Channel E4	LVDS output	TE6	TE5	TE4	TE3	TE2	TE1	TE0
	Data order	NA	EC9	EC8	EB9	EB8	EA9	EA8
LVDS Channel O0	LVDS output	TA6	TA5	TA4	TA3	TA2	TA1	TA0
	Data order	OB0	OA5	OA4	OA3	OA2	OA1	OA0
LVDS Channel O1	LVDS output	TB6	TB5	TB4	TB3	TB2	TB1	TB0
	Data order	OC1	OC0	OB5	OB4	OB3	OB2	OB1
LVDS Channel O2	LVDS output	TC6	TC5	TC4	TC3	TC2	TC1	TC0
	Data order	DE	VS	HS	OC5	OC4	OC3	OC2
LVDS Channel O3	LVDS output	TD6	TD5	TD4	TD3	TD2	TD1	TD0
	Data order	NA	OC7	OC6	OB7	OB6	OA7	OA6
LVDS Channel O4	LVDS output	TE6	TE5	TE4	TE3	TE2	TE1	TE0
	Data order	NA	OC9	OC8	OB9	OB8	OA9	OA8

4.4.2 LVDS DATA INPUT DAT ORDER (JEITA Mode)

JEITA mode: LVDS_SEL= H (3.3V)

LVDS interface receiver required input data mapping table								
LVDS Channel E0	LVDS output	TA6	TA5	TA4	TA3	TA2	TA1	TA0
	Data order	EB4	EA9	EA8	EA7	EA6	EA5	EA4
LVDS Channel E1	LVDS output	TB6	TB5	TB4	TB3	TB2	TB1	TB0
	Data order	EC5	EC4	EB9	EB8	EB7	EB6	EB5
LVDS Channel E2	LVDS output	TC6	TC5	TC4	TC3	TC2	TC1	TC0
	Data order	DE	VS	HS	EC9	EC8	EC7	EC6
LVDS Channel E3	LVDS output	TD6	TD5	TD4	TD3	TD2	TD1	TD0
	Data order	NA	EC3	EC2	EB3	EB2	EA3	EA2
LVDS Channel E4	LVDS output	TE6	TE5	TE4	TE3	TE2	TE1	TE0
	Data order	NA	EC1	EC0	EB1	EB0	EA1	EA0
LVDS Channel O0	LVDS output	TA6	TA5	TA4	TA3	TA2	TA1	TA0
	Data order	OB4	OA9	OA8	OA7	OA6	OA5	OA4
LVDS Channel O1	LVDS output	TB6	TB5	TB4	TB3	TB2	TB1	TB0
	Data order	OC5	OC4	OB9	OB8	OB7	OB6	OB5
LVDS Channel O2	LVDS output	TC6	TC5	TC4	TC3	TC2	TC1	TC0
	Data order	DE	NA	NA	OC9	OC8	OC7	OC6
LVDS Channel O3	LVDS output	TD6	TD5	TD4	TD3	TD2	TD1	TD0
	Data order	NA	OC3	OC2	OB3	OB2	OA3	OA2
LVDS Channel O4	LVDS output	TE6	TE5	TE4	TE3	TE2	TE1	TE0
	Data order	NA	OC1	OC0	OB1	OB0	OA1	OA0

4.4.3 PIXEL FORMAT IMAGE



4.4.4 COLOR DATA INPUT ASSIGNMENT

The brightness of each sub-pixel is based on the 10-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																													
		Red										Green										Blue									
		R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale of Subpixel1 (Dark)	Gray(0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Gray(1)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Gray(2)	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	.	.	.	.	.	.	.	.	.	.	.	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	.	.	.	.	.	.	.	.	.	.	.	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Gray(1021)	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Gray(1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Gray(1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale of Subpixel2 (Dark)	Gray(0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Gray(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	Gray(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	.	0	0	0	0	0	0	0	0	0	0	.	.	.	.	.	.	.	.	.	.	0	0	0	0	0	0	0	0	0	0
	.	0	0	0	0	0	0	0	0	0	0	.	.	.	.	.	.	.	.	.	.	0	0	0	0	0	0	0	0	0	0
	Gray(1021)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0
	Gray(1022)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	Gray(1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
Gray Scale of Subpixel3 (Dark)	Gray(0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Gray(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Gray(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	.	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	.	.	.	.	.	.	.	.	.	.
	.	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	.	.	.	.	.	.	.	.	.	.
	Gray(1021)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1
	Gray(1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0
	Gray(1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

4.5 DISPLAY TIMING SPECIFICATIONS

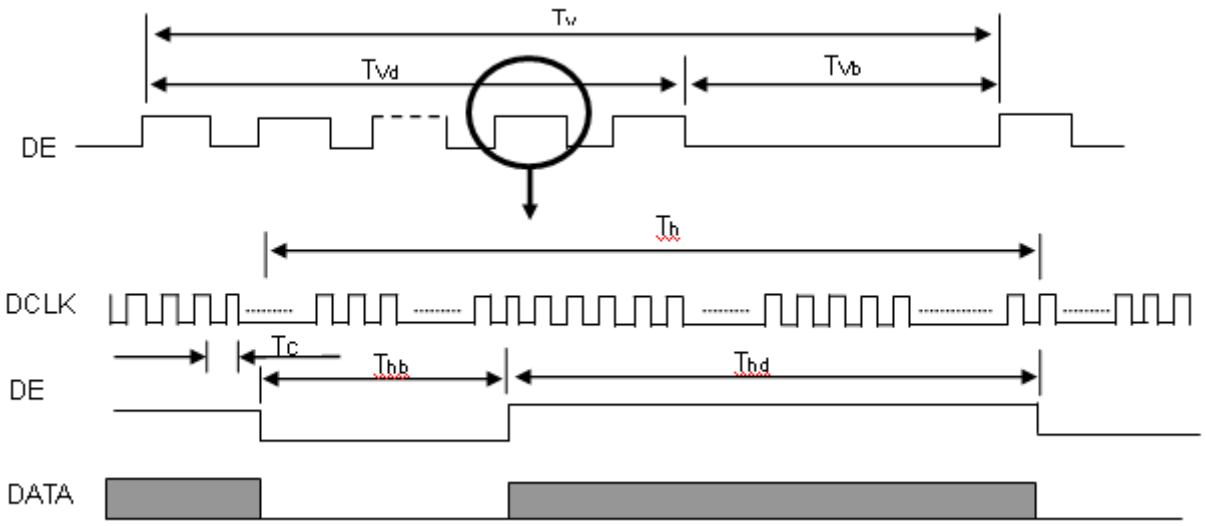
The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Clock	Frequency	F_c	57	65	66	MHz	-
	Period	T_c	15.15	15.4	17.54	ns	
	Input cycle to cycle jitter	T_{rcl}	---	---	250	ps	(1)
	Spread spectrum modulation range	F_{clkin_mod}	---	---	1.02*Fc	MHz	(2)
	Spread spectrum modulation frequency	F_{SSM}	---	---	200	KHz	(2)
	High Time	T_{ch}	---	4/7	---	Tc	
	Low Time	T_{cl}	---	3/7	---	Tc	
LVDS data	Setup Time	T_{lvs}	600	---	---	ps	(3)
	Hold Time	T_{lvh}	600	---	---	ps	
Vertical Display Term	Frame Rate	Fr	48	60	---	Hz	
	Total	T_v	1546	1612	1628	Th	$T_v=T_{vd}+T_{vb}$
	Active Display	T_{vd}	1536	1536	1536	Th	
	Sensor Line/frame	K	---		---	Th	
	Blank	T_{vb}	T_v-T_{vd}	76	T_v-T_{vd}	Th	
Horizontal Display Term	Total	T_h	640	672	752	Tc	$T_h=T_{hd}+T_{hb}$
	Active Display	T_{hd}	512	512	512	Tc	
	Blank	T_{hb}	T_h-T_{hd}	160	T_h-T_{hd}	Tc	

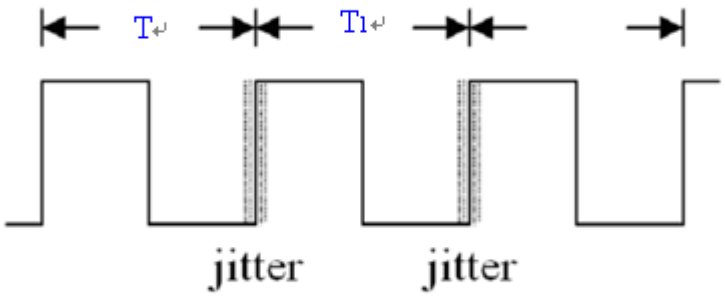
Note: Because this module is operated by DE only mode, H_{sync} and V_{sync} input signals should be set to low logic level or ground. Otherwise, this module would operate abnormally.

Note: The Tv(Tvd+Tvb) must be integer, otherwise, this module would operate abnormally.

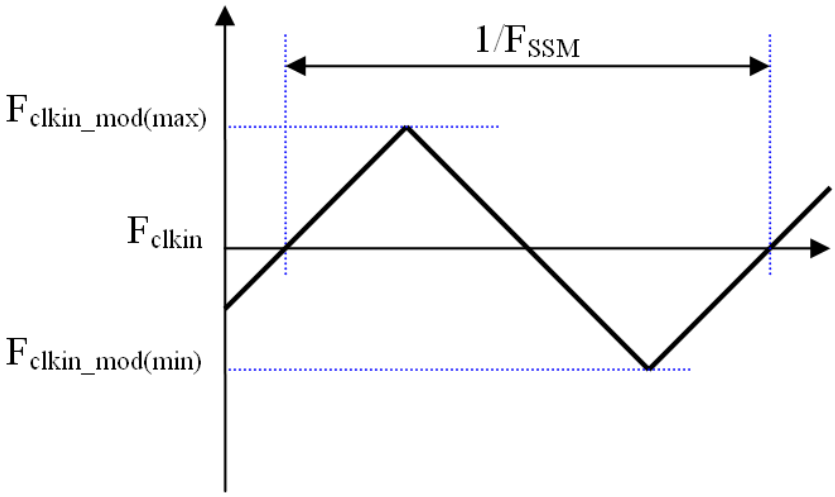
INPUT SIGNAL TIMING DIAGRAM



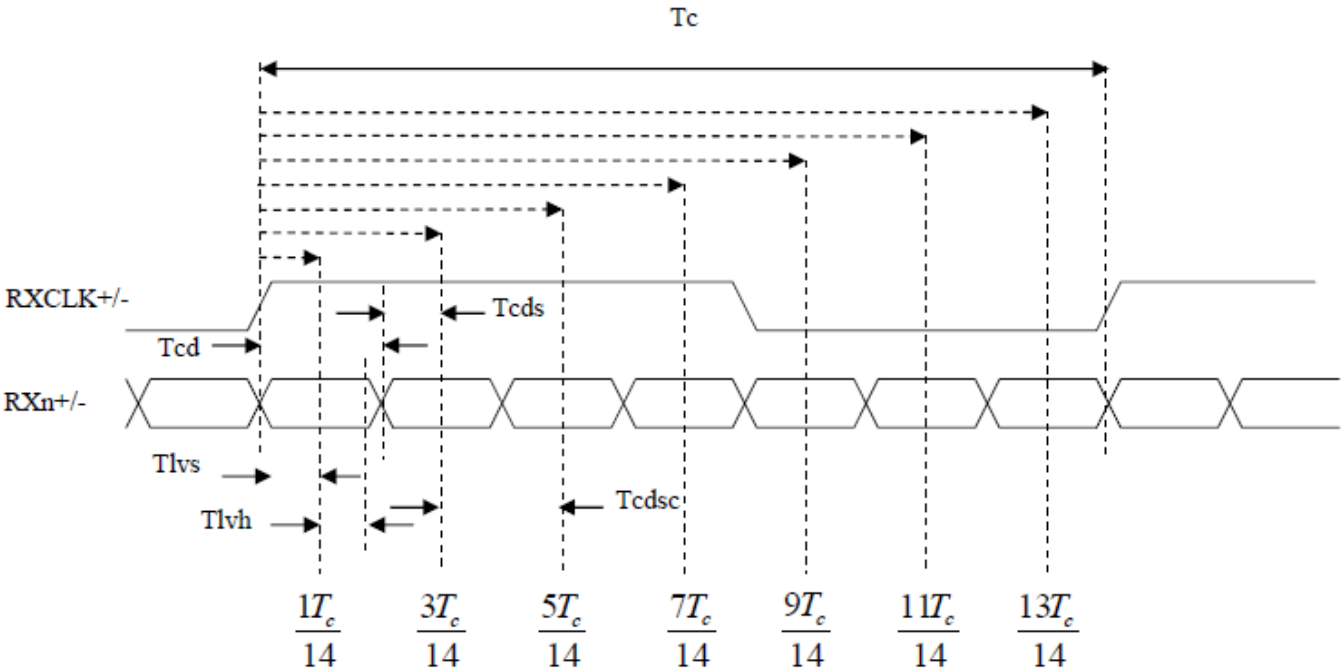
Note (1) The input clock cycle-to-cycle jitter is defined as below figures. Trcl = I T_1 – TI



Note (2) The SSCG (Spread spectrum clock generator) is defined as below figures.

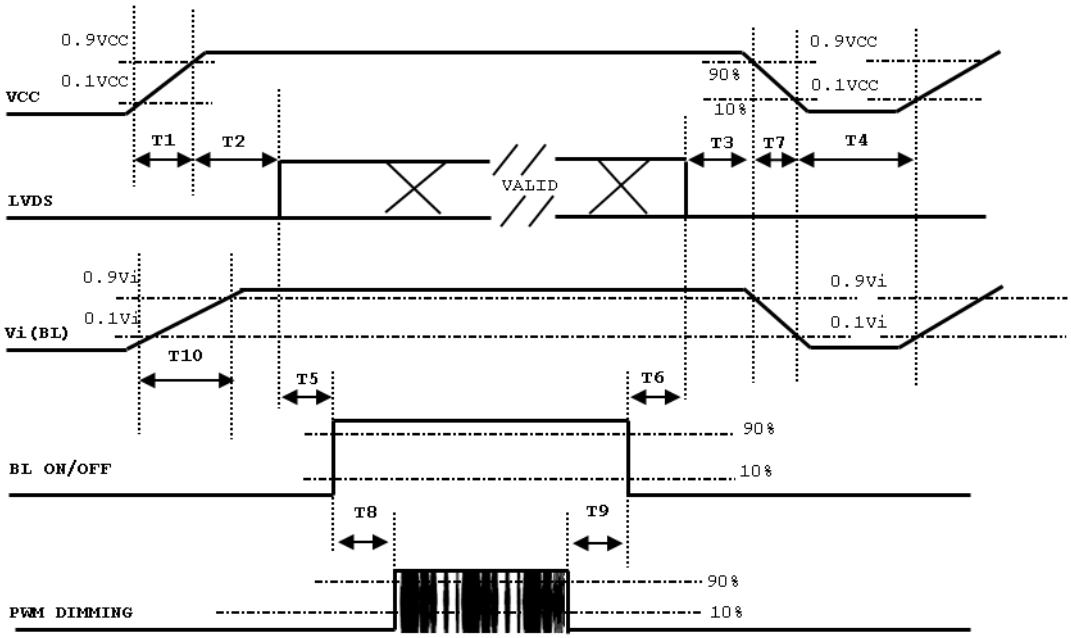


Note (3) Input Clock to Data timing is defined as below figures.



4.6 POWER ON/OFF SEQUENCE

The power sequence specifications are shown as the following table and diagram.



Timing Specifications:

Parameters	Values			Units
	Min	Typ.	Max	
T1	0.5	-	10	ms
T2	0	-	50	ms
T3	0	-	50	ms
T4	500	-	-	ms
T5	450	-	-	ms
T6	200	-	-	ms
T7	10	-	100	ms
T8	10	-	-	ms
T9	10	-	-	ms
T10	20	-	50	ms

Note

(1) The supply voltage of the external system for the module input should be the same as the definition of Vcc.

(2) When the backlight turns on before the LCD operation of the LCD turns off, the display may momentarily become abnormal screen.

(3) In case of VCC = off level, please keep the level of input signals on the low or keep a high impedance.

(4) T4 should be measured after the module has been fully discharged between power off and on period.

(5) Interface signal shall not be kept at high impedance when the power is on.

(6) INX won't take any responsibility for the products which are damaged by the customers not following the Power Sequence.

(7) There might be slight electronic noise when LCD is turned off (even backlight unit is also off). To avoid this symptom, we suggest "Vcc falling timing" to follow "T7 spec".

5. OPTICAL CHARACTERISTICS

5.1 TEST CONDITIONS

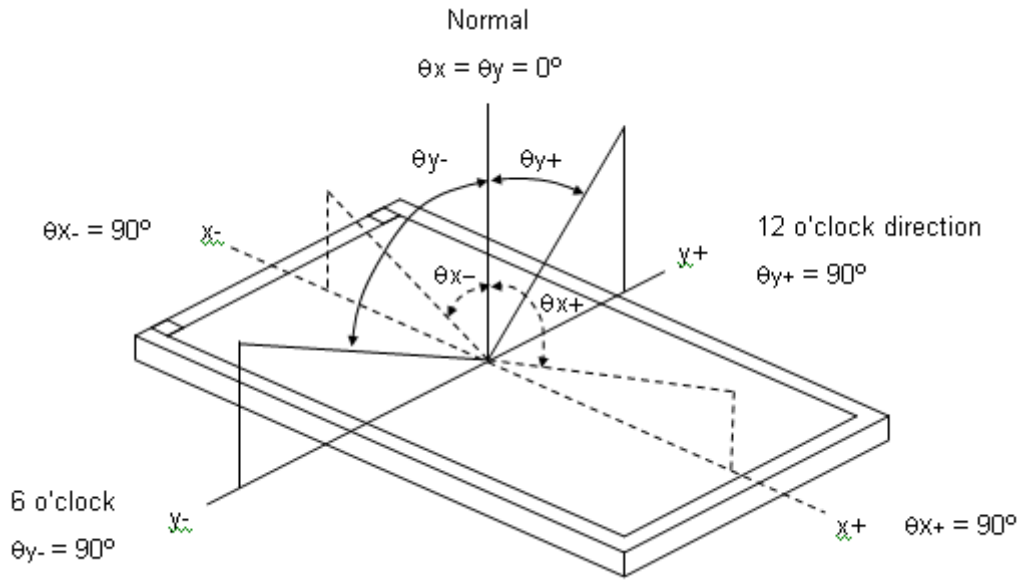
Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	According to typical value in "4.3. ELECTRICAL CHARACTERISTICS"		
Input Signal			
PWM Duty Ratio	D	100	%

5.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 5.2 and all items are measured at the center point of screen except white variation. The following items should be measured under the test conditions described in 5.1 and stable environment shown in Note (5).

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Color Chromaticity (CIE 1931)	White	W_x	θ_x=0°, θ_Y =0° CS-2000	Typ. -0.03	0.299	Typ. +0.03	-	(1), (5)
		W_y			0.315			
	Red	R_x			0.645			
		R_y			0.340			
	Green	G_x			0.315			
		G_y			0.606			
	Blue	B_x			0.155			
		B_y			0.050			
Center Luminance of White		L_C		800	1000	-	cd/m^2	(4), (5)
Contrast Ratio		CR		1200	1500	-	-	(2), (5)
Response Time		T_R	θ_x=0°, θ_Y =0°	-	15	25	ms	(3)
		T_F		-	10	15	ms	
White Variation(adjacent)		δW_a	θ_x=0°, θ_Y =0° USB2000	90	-	-	%	(5), (6)
White Variation(total)		δW_t	θ_x=0°, θ_Y =0° USB2000	75	-	-	%	(5), (6)
Viewing Angle		Θ_{y+}	CR ≧ 10 USB2000	80	89	-	Deg.	(1), (5)
		Θ_{y-}						
		Θ_{x+}						
		Θ_{x-}						

Note (1) Definition of Viewing Angle (θx, θy):



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L1023 / L0

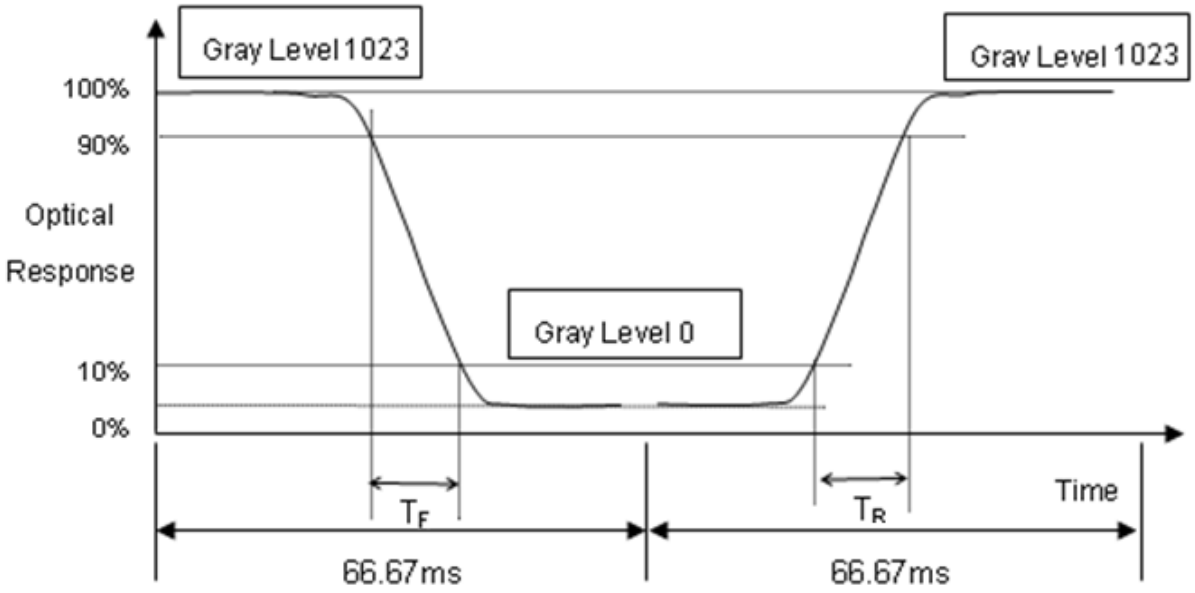
L1023: Luminance of gray level 1023

L 0: Luminance of gray level 0

CR = CR (5)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (4).

Note (3) Definition of Response Time (T_R, T_F):

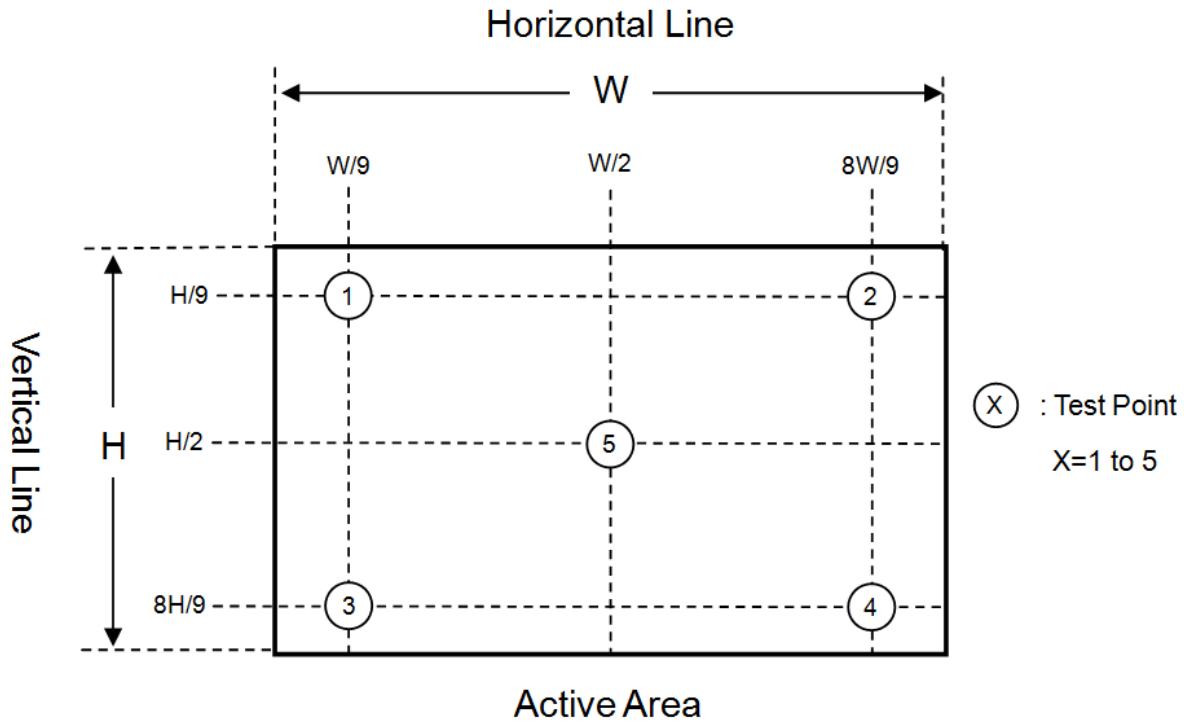


Note (4) Definition of Luminance of White (L_C):

Measure the luminance of gray level 1023 at center point

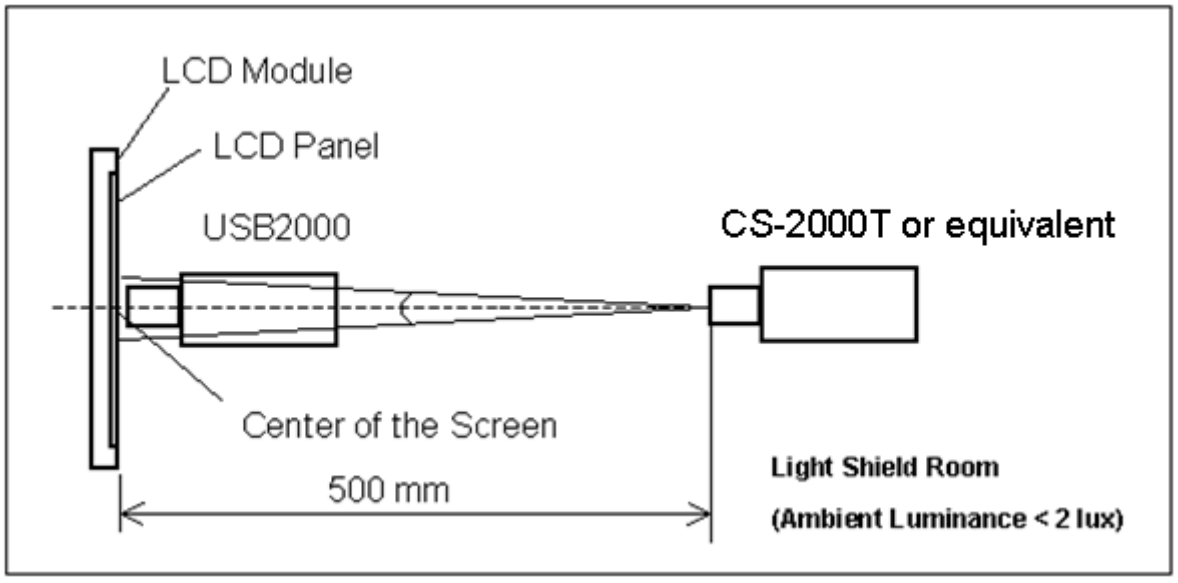
L_C = L (5)

L (x) is corresponding to the luminance of the point X at the following figure.



Note (5) Measurement Setup:

The LCD module should be stabilized at given temperature for 60 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 60 minutes in a windless room.

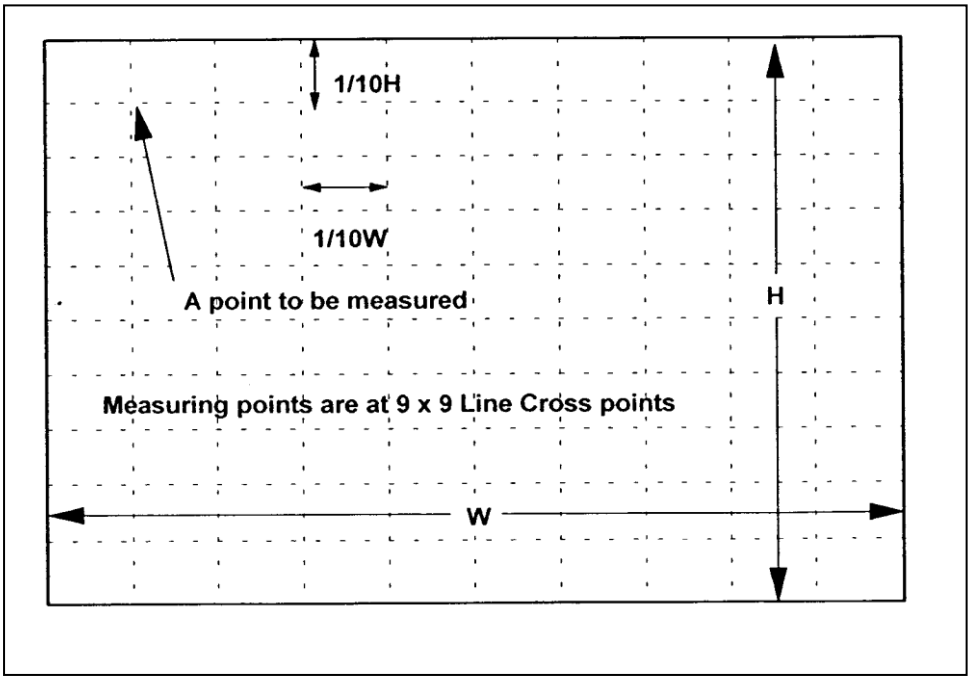


Note (6) There is the Uniformity Measurement below:

'L_{bright} ' represents the Luminance of the point that is brighter than the other point to be compared.

'L_{dark} ' represents the Luminance of the point that is darker than the other point to be compared.

Measuring points are shown in the following Fig.



When the backlight is on with all pixels in the white (maximum gray) level, the luminance uniformity is defined as follows;

Where:

L_{bright}: The luminance of the brightest part of the area

L_{dark}: The luminance of the darkest part of the area

1. Adjacent Area

$$\text{Luminance Uniformity} = \frac{L_{dark}}{L_{bright}} \geqq 0.90$$

over a circular area of 10mm diameter placed anywhere on the screen.

2. Screen Total

$$\text{Luminance Uniformity} = \frac{L_{dark}}{L_{bright}} \geqq 0.75$$

over the entire screen.

6. RELIABILITY TEST ITEM

Items	Required Condition	Note
Temperature Humidity Bias (THB)	Ta= 50℃ , 80%RH, 240hours	
High Temperature Operation (HTO)	Ta= 50℃ , 240hours	
Low Temperature Operation (LTO)	Ta= 0℃ , 240hours	
High Temperature Storage (HTS)	Ta= 60℃ , 240hours	
Low Temperature Storage (LTS)	Ta= -20℃ , 240hours	
Vibration Test (Non-operation)	Acceleration: 1.5 Grms Wave: Half-sine Frequency: 10 - 300 Hz Sweep: 30 Minutes each Axis (X, Y, Z)	
Shock Test (Non-operation)	Acceleration: 50 G Wave: Half-sine Active Time: 11 ms Direction : ± X, ± Y, ± Z.(one time for each Axis)	
Thermal Shock Test (TST)	-20℃/30min , 60℃ / 30min , 100 cycles	
On/Off Test	25℃ ,On/10sec , Off /10sec , 30,000 cycles	
ESD (Electro Static Discharge)	Contact Discharge: ± 8KV, 150pF(330Ω)	
	Air Discharge: ± 15KV, 150pF(330Ω)	
Altitude Test	Operation:10,000 ft / 24hours Non-Operation:30,000 ft / 24hours	
Carton packing Vibration	ISTA STANDARD Random, Frequency Range: 1 – 200 Hz Top & Bottom: 30 minutes (Z), Right & Left: 10 minutes (X) Back & Forth 10 minutes (Y)	Non Operation
Carton Packing Dropping Test	1 Corner , 3 Edge, 6 Face, 61cm	Non Operation

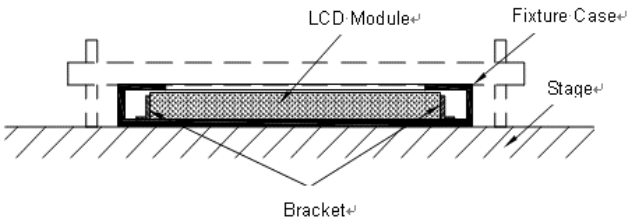
Note (1) criteria: Normal display image with no obvious non-uniformity and no line defect.

Note (2) Evaluation should be tested after storage at room temperature for more than two hour

Note (3) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

The fixing condition is shown as below:

At Room Temperature



7. PACKING

7.1 PACKING SPECIFICATIONS

(1) 5 LCD modules / 1 Box

(2) Box dimensions: 532(L) * 283(W) * 488(H) mm

(3) Weight: approximately: 13.7 kg (5 modules per box)

7.2 PACKING METHOD

Packaging method is shown as following figures.

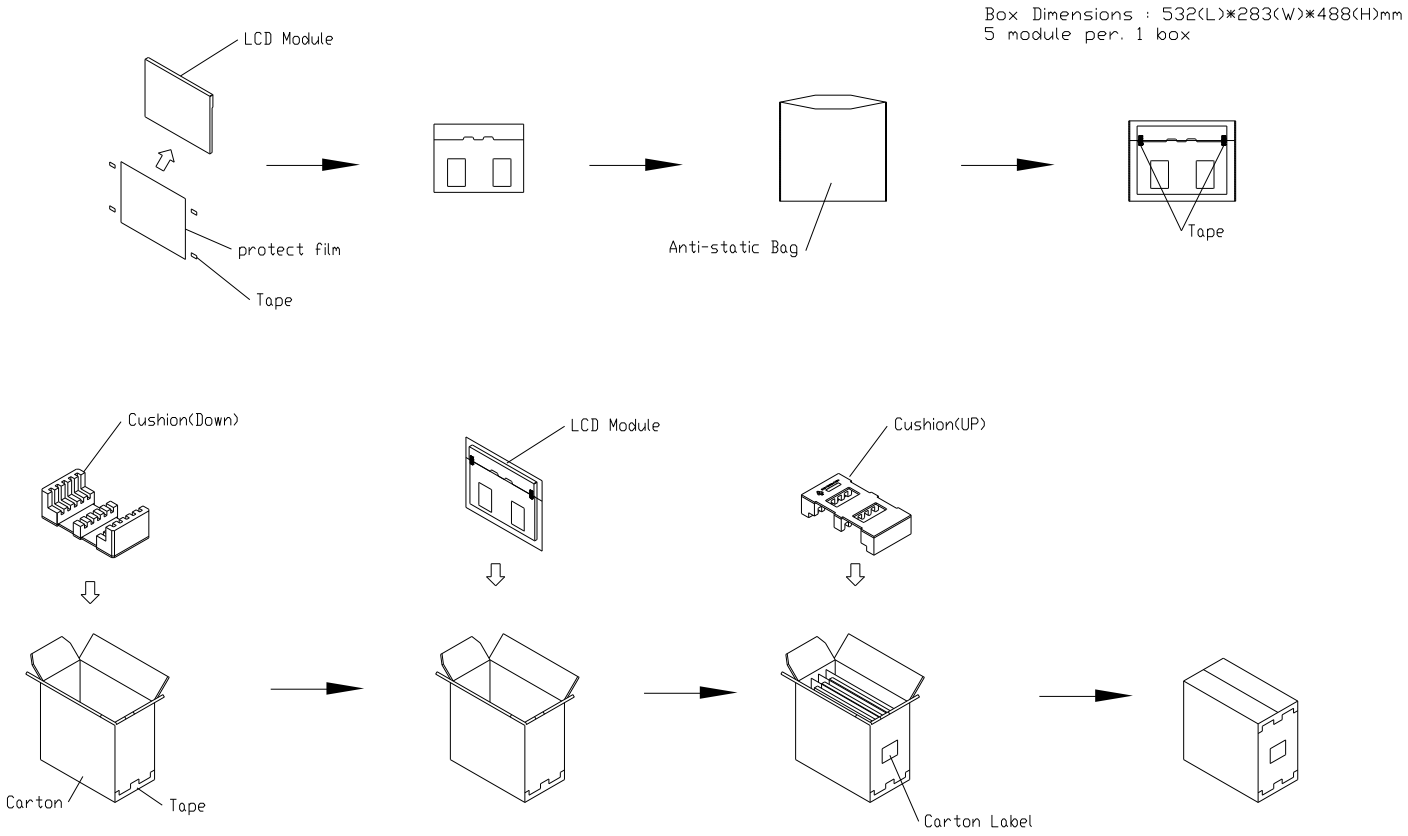
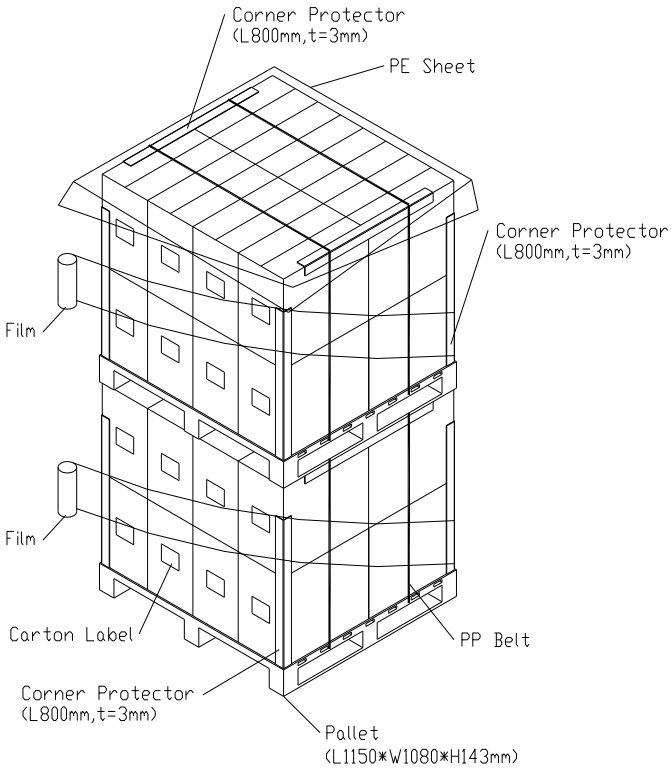


Figure. 7-1 Packing method

7.3 PALLET

Sea / Land Transportation
(40ft / 40ft HQ Container)



Air Transportation

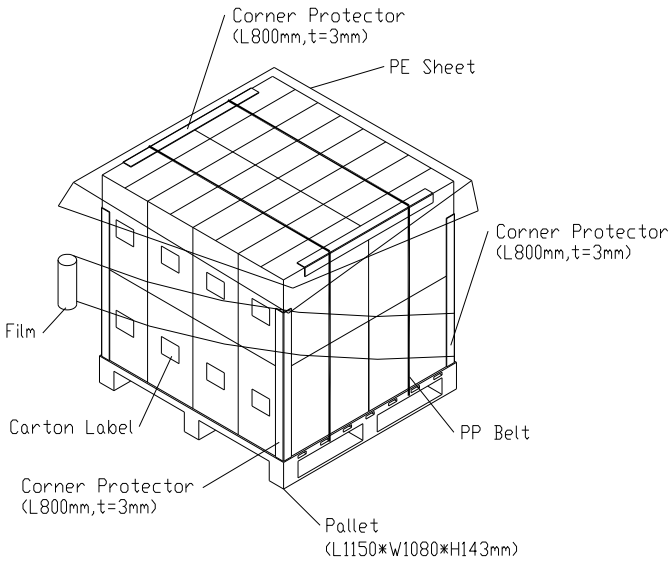


Figure 7-2 Packing method

7.4 UN-PACKING METHOD

UN-packaging method is shown as following figures.

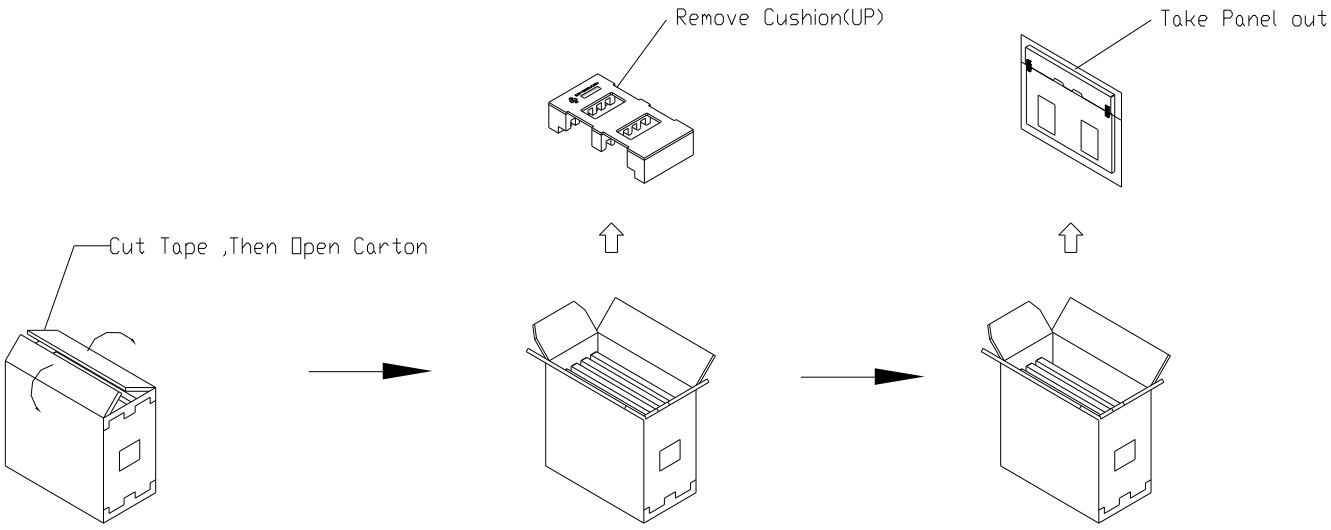
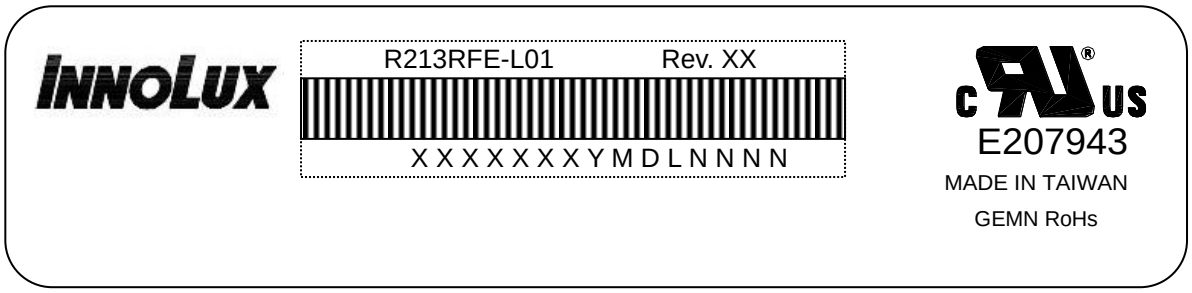


Figure 7-3 Un-packing method

8. INX MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



(a) Model Name: R213RFE-L01

(b) Revision: Rev. XX, for example: A0, A1… B1, B2… or C1, C2…etc.

(c) INX barcode definition:

Serial ID: XX-XX-X-XX-YMD-L-NNNN

Code	Meaning	Description
XX	Innolux internal use	-
XX	Revision	Cover all the change
X	Innolux internal use	-
XX	Innolux internal use	-
YMD	Year, month, day	Year: 0~9, 2001=1, 2002=2, 2003=3…2010=0, 2011=1, 2012=2… Month: 1~12=1, 2, 3, ~, 9, A, B, C Day: 1~31=1, 2, 3, ~, 9, A, B, C, ~, W, X, Y, exclude I, O, and U.
L	Product line #	Line 1=1, Line 2=2, Line 3=3, …
NNNN	Serial number	Manufacturing sequence of product

9. PRECAUTIONS

9.1 ASSEMBLY AND HANDLING PRECAUTIONS

(1) Do not apply rough force such as bending or twisting to the module during assembly.

(2) To assemble or install module into user's system can be only in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

(3) It's not permitted to have pressure or impulse on the module because the LCD panel and Backlight will be damaged.

(4) Always follow the correct power sequence when LCD module is connecting and operating. This can prevent damage to the CMOS LSI chips during latch-up.

(5) Do not pull the I/F connector in or out while the module is operating.

(6) Do not disassemble the module.

(7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

(8) It is dangerous that moisture come into or contacted the LCD module, because moisture may damage LCD module when it is operating.

(9) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.

(10)When ambient temperature is lower than 10ºC may reduce the display quality. For example, the response time will become slowly.

9.2 STORAGE PRECAUTIONS

(1) Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0℃ to 35℃ and relative humidity of less than 70%

(2) Do not store the TFT – LCD module in direct sunlight

(3) The module should be stored in dark place. It is prohibited to apply sunlight or fluorescent light in storing

9.3 OPERATION PRECAUTIONS

(1) The LCD product should be operated under normal condition.

Normal condition is defined as below:

Temperature : 20±15℃

Humidity: 65±20%

Display pattern : continually changing pattern(Not stationary)

(2) If the product will be used in extreme conditions such as high temperature, high humidity, high altitude ,display pattern or operation time etc…It is strongly recommended to contact CMO for application engineering advice . Otherwise, its reliability and function may not be guaranteed.

9.4 SAFETY PRECAUTIONS

(1) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

(2) After the module's end of life, it is not harmful in case of normal operation and storage.

9.5 SAFETY STANDARDS

The LCD module should be certified with safety regulations as follows:

(1) UL60950-1 or updated standard.

(2) IEC60950-1 or updated standard.

9.6 OTHER

When fixed patterns are displayed for a long time, remnant image is likely to occur.

Appendix. OUTLINE DRAWING