MODEL NO : TM041XDHC02

MODEL VERSION: 00

SPEC VERSION : 2.0

ISSUED DATE: 2018-12-24

□**Preliminary Specification**
■**Final Product Specification**

Customer :

Approved by	Notes

TIANMA Confirmed :

Prepared by	Checked by	Approved by
Junwen Du	Longping Deng	KimMin Hong

This technical specification is subjected to change without notice

Table of Contents

Record of Revision

Rev	Issued Date	Description	Editor
2.0	2018-12-24	Final Specification Release	Junwen Du

1 General Specifications

Feature		Spec
Display Spec.	Size	4.12inch
	Resolution	720（RGB）x720
	Technology Type	a-Si
	Pixel Configuration	R.G.B. Vertical Stripe
	Pixel pitch(um)	102.75×102.75
	Display Mode	Normally Black
	Surface Treatment	HC
	Viewing Direction	ALL
	Gray Scale Inversion Direction	NA
Mechanical Characteristics	LCM (W x H x D) (mm)	LCM:77.98x82.00x2.13
	Active Area(mm)	TFT LCD: 73.98×73.98
	CTP Touch Method	Finger
	Number of simultaneous touches	2
	Minimum Touch Area	Φ7
	CTP Structure	Incell (Without Cover Lens)
	With /Without TSP	With TSP
	Matching Connection Type	FH34SRJ-40S-0.5SH(50)
	LED Numbers	12 LEDs (3 series,4 parallel)
	Weight (g)	27.5
Electrical Characteristics	LCD Interface	MIPI
	CTP Interface	IIC
	Color Depth	16.7M
	Driver IC	ILI9881H
	IIC address	0X41

Note 1: Viewing direction for best image quality is different from TFT definition. There is a 180 degree shift.

Note 2: Requirements on Environmental Protection: Q/S0002

Note 3: LCM weight tolerance: ± 5%

2 Input/Output Terminals

Matching Connection Type:FH34SRJ-40S-0.5SH(50)

Pin No.	Symbol	I/O	Function	Remark
1	LEDK	P	LED cathode pin	
2	LEDA	P	LED anode pin	
3	NC	--	Not connect	
4	GND	P	Power Ground	
5	D2P	I	MIPI DSI DATA2 Positive	
6	D2N	I	MIPI DSI DATA2 Negative	
7	GND	P	Power Ground	
8	D1P	I	MIPI DSI DATA1 Positive	
9	D1N	I	MIPI DSI DATA1 Negative	
10	GND	P	Power Ground	
11	CLKP	I	MIPI DSI CLOCK Positive	
12	CLKN	I	MIPI DSI CLOCK Negative	
13	GND	P	Power Ground	
14	D0P	I	MIPI DSI DATA0 Positive	
15	D0N	I	MIPI DSI DATA0 Negative	
16	GND	P	Power Ground	
17	D3P	I	MIPI DSI DATA3 Positive	
18	D3N	I	MIPI DSI DATA3 Negative	
19	GND	P	Power Ground	
20	NC	--	Not connect	
21	IOVCC	P	Power supply to interface pins(1.8V)	
22	AVDD	P	Positive input analog power for driver IC use(6.0V)	
23	NC	--	Not connect	
24	AVEE	P	Negative input analog power for driver IC use(-6.0V)	
25	VCCB	P	Power supply to level shift IC(3.3V). If not used, please let it open.	
26	NC	--	Not connect	
27	GND	P	Power Ground	
28	NC	--	Not connect	
29	TE	O	Tearing effect output signal. If not used, please let this	

			pin open.	
30	RESET	I	LCM Reset pin, the LCD driver is initialized when RESET active low.	
31	NC	--	Not connect	
32	GND	P	Power Ground	
33	TP_RESET	I	Reset pin, the TP is initialized when RESET active low.	Note 2
34	GND	P	Power Ground	
35	TP_INT	O	Communication interrupt	Note 2
36	GND	P	Power Ground	
37	TP_SDA	I/O	I2C data	Note1,2
38	TP_SCL	I	I2C clock	Note1,2
39	GND	P	Power Ground	
40	GND	P	Power Ground	

Note1： It needs a pull-up resistor (suggest 4.7Kohm) on customer's main board.
Note2: ILI9881H only supports Long V mode (TP frequency must be 60Hz).

3 Absolute Maximum Ratings

GND=0V

Item	Symbol	MIN	MAX	Unit	Remark
Power Voltage	AVDD~AVSS	-0.3	6.3	V	Note1
Power Voltage	AVEE~AVSS	-6.3	0.3	V	
Power Voltage	VCCB	1.65	5.5	V	
Logic Power Supply	IOVCC	-0.3	1.95	V	
Input voltage	V_{IN}	-0.3	IOVCC+0.3	V	
Operating Temperature	Top	-20	70	℃	
Storage Temperature	Tst	-30	80	℃	
Relative Humidity Note2	RH	--	≤95	%	Ta≤40℃
		--	≤85	%	40℃＜Ta≤50℃
		--	≤55	%	50℃＜Ta≤60℃
		--	≤36	%	60℃＜Ta≤70℃
		--	≤24	%	70℃＜Ta≤80℃
Absolute Humidity	AH	--	≤70	g/m^3	Ta＞70℃

Table 3 Absolute Maximum Ratings

Note1: Input voltage include D0P/D0N,D1P/D1N,D2P/D2N,D3P/D3N,CLKP/CLKN,RESET, TP_RESET , TP_SDA , TP_SCL .

Note2: Ta means the ambient temperature.
It is necessary to limit the relative humidity to the specified temperature range.
Condensation on the module is not allowed.

4 Electrical Characteristics

4.1 Driving TFT LCD Panel

GND=0V, Ta=25℃

Item		Symbol	MIN	TYP	MAX	Unit	Remark
Logic operating Voltage		IOVCC	1.7	1.8	1.9	V	
operating Voltage		AVDD	5.9	6.0	6.1	V	
operating Voltage		AVEE	-6.1	-6.0	-5.9	V	
operating Voltage		VCCB	3.2	3.3	3.4	V	
Input Signal Voltage	Low Level	V_{IL}	0	-	0.3* IOVCC	V	IOVCC=1.8V
	High Level	V_{IH}	0.7* IOVCC	-	IOVCC	V	IOVCC=1.8V
Output Signal Voltage	Low Level	V_{OL}	0	-	0.2* IOVCC	V	I_{OL}=+1.0mA Note1
	High Level	V_{OH}	0.8* IOVCC	-	IOVCC	V	I_{OH}=-1.0mA Note1
(Panel+LSI) Power Consumption		White Mode (60Hz)	-	120	-	mW	IOVCC=1.8V, AVDD=6.0V,AVEE=-6.0V
		Sleeping Mode	-	5	-	mW	IOVCC=1.8V, AVDD=6.0V,AVEE=-6.0V

Table 4.1.1 LCD module electrical characteristics

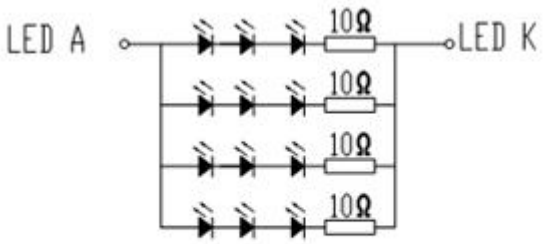
4.2 Backlight Unit

Ta=25℃

Item	Symbol	Min	Typ	Max	Unit	Remark
Forward Current	I_F	-	80	100	mA	
Forward Voltage	V_F	-	9.8	11.05	V	
Backlight Power Consumption	W_{BL}	-	784	1105	mW	3 series, 4 parallel
LED lifetime		20000	30,000		hrs	

Table 4.2.1 backlight unit electrical characteristics

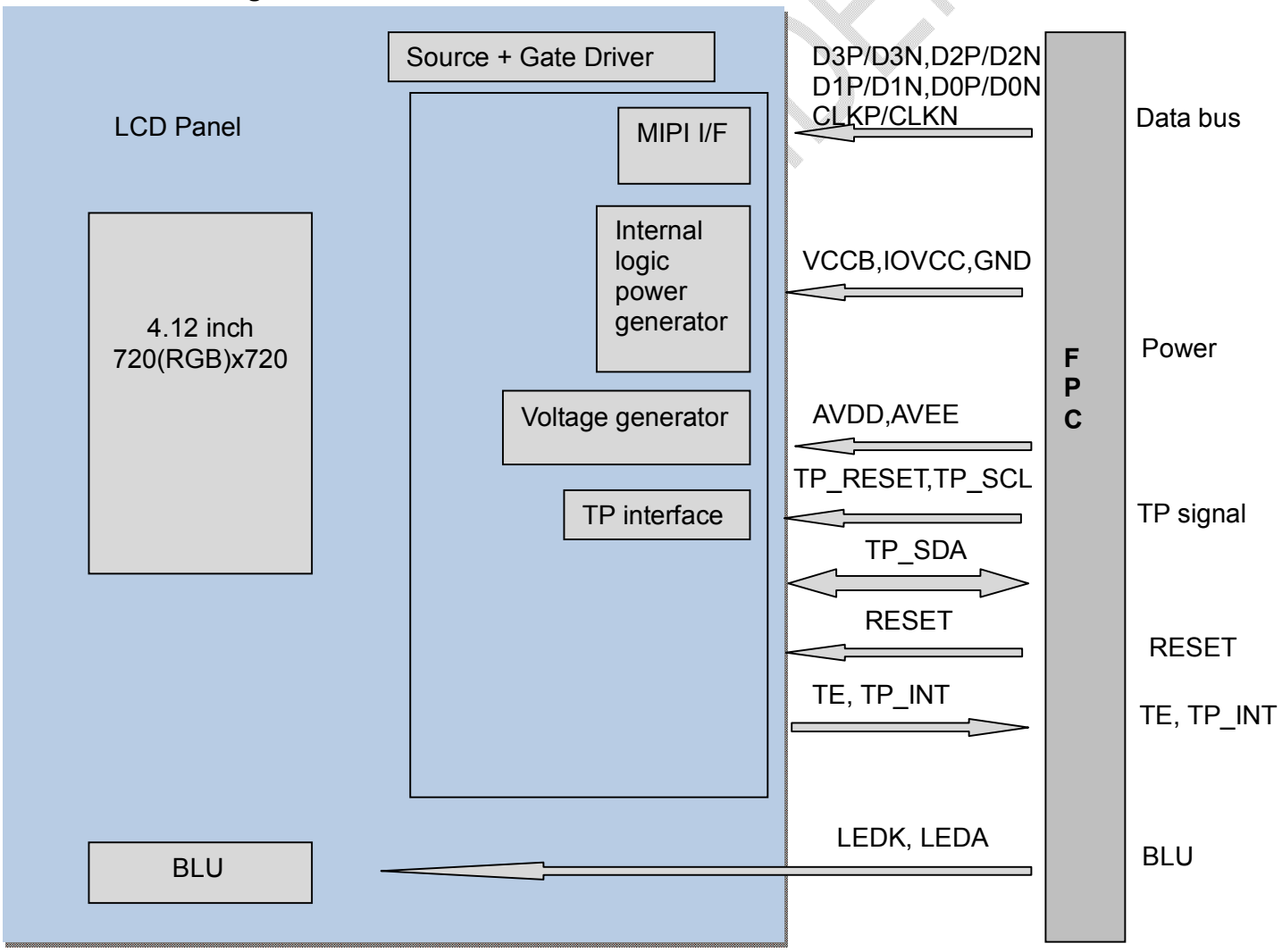
Note1: Figure below shows the connection of backlight LED.



LED circuit

Note 2: One LED: V_F =3.2V I_F =20mA
Note 3: : I_F is defined for one LED.
Optical performance should be evaluated at Ta=25℃ only.
If LED is driven by high current, high ambient temperature & humidity condition. The life time of LED will be reduced. Operating life means brightness goes down to 50% initial brightness. Typical operating life time is estimated data.

4.3 Block Diagram



5 Timing Chart

5.1 Power on/off sequence

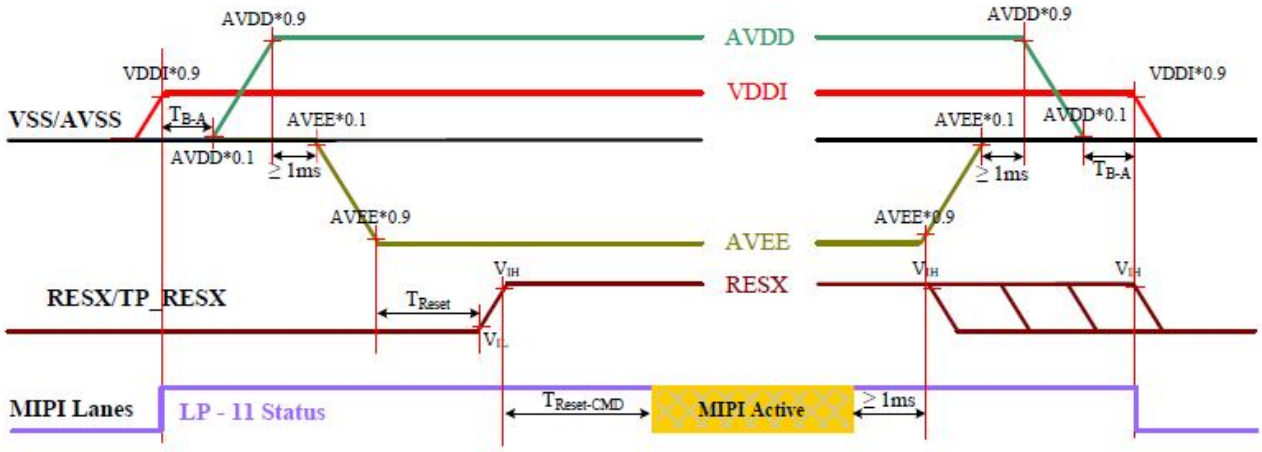


Figure 5.1 Power on/off sequence

Symbol	Characteristics	Min	Typ	Max	Units
T_{Rise}	External Power Rise Time	0.2	-	20	ms
T_{Fall}	External Power Fall Time	0.2	-	20	ms
T_{B-A}	Delay Time between Two External Power	2	5	-	ms
T_{Reset}	Delay Time between External Power and Reset	4	10	-	ms
$T_{Reset-CMD}$	Reset to First Command in Display Sleep In Mode	10	-	-	ms

Table 5.1 Timing relation of Power on/off sequence

5.2 DSI Timing characteristics

5.2.1 High Speed Mode – Clock Channel Timing

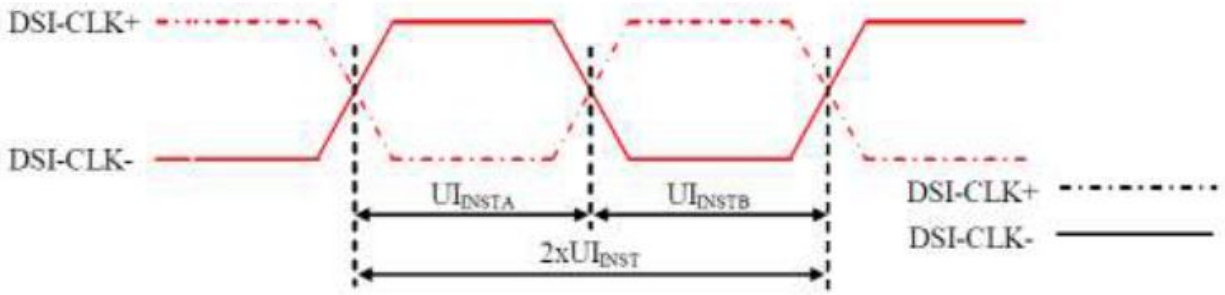


Figure 5.2.1 DSI Clock Channel Timing

Signal	Symbol	Parameter	Min.	Max.	Unit
DSI-CLK+/-	$2xUI_{INST}$	Double UI instantaneous	2	25	ns
DSI-CLK+/-	UI_{INSTA}, UI_{INSTB}	UI instantaneous Half	1	12.5	ns

Note: $UI_{INST} = UI_{INSTA} = UI_{INSTB}$

Table 5.2.1 DSI Clock Channel Timing

5.2.2 High Speed Mode – Data Clock Channel Timing

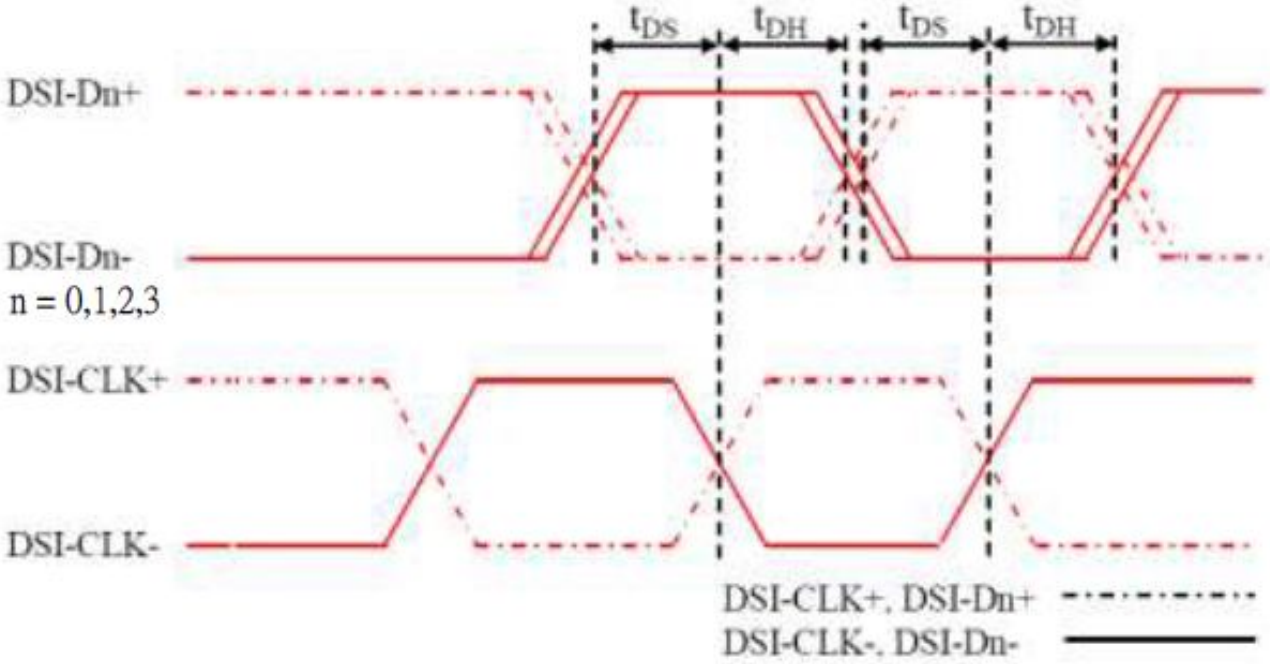


Figure 5.2.2 DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min.	Max.
DSI-Dn+/- (n=0,1,2,3)	t_{DS}	Data to Clock Setup time	0.15xUI	-
	t_{DH}	Clock to Data Hold Time	0.15xUI	-

Table 5.2.2 DSI Data to Clock Channel Timings

5.2.3 High Speed Mode – Rise and Fall Timings

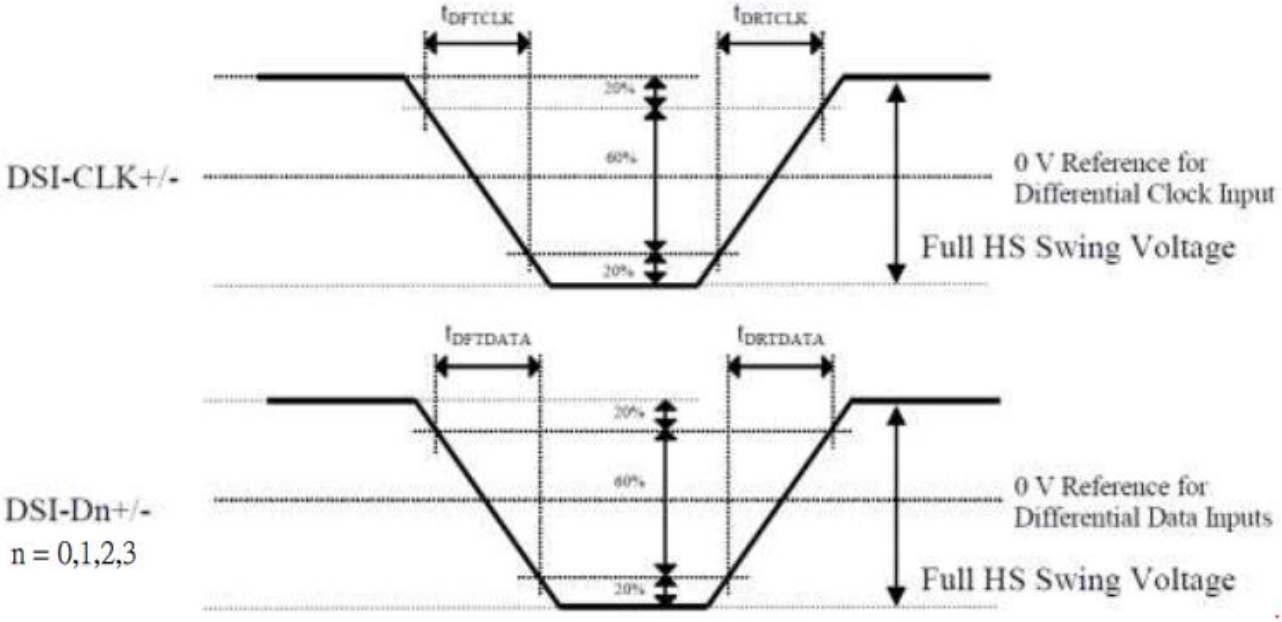


Figure 5.2.3 Rise and Fall Timings on Clock and Data Channels

Parameter	Symbol	Condition	Specification		
			Min.	Typ.	Max.
Differential Rise Time for Clock	t_{DRTCLK}	DSI-CLK+/-	150 ps	-	0.3UI
Differential Rise Time for Data	$t_{DRTDATA}$	DSI-Dn+/- (n=0,1,2,3)	150 ps	-	0.3UI
Differential Fall Time for Clock	t_{DFTCLK}	DSI-CLK+/-	150 ps	-	0.3UI
Differential Fall Time for Data	$t_{DFTDATA}$	DSI-Dn+/- (n=0,1,2,3)	150 ps	-	0.3UI

Table 5.2.3 Rise and Fall Timings on Clock and Data Channels

Note:
The display module has to meet timing requirements, what are defined for the transmitter(MCU)on MIPI D-Phy Standard.

5.2.4 Low Speed Mode – Bus Turn Around

Low Power Mode and its State Periods are illustrated for reference purposes on the Bus Turn Around(BTA) from the MCU to the Display Module(ILI9881H) sequence below.

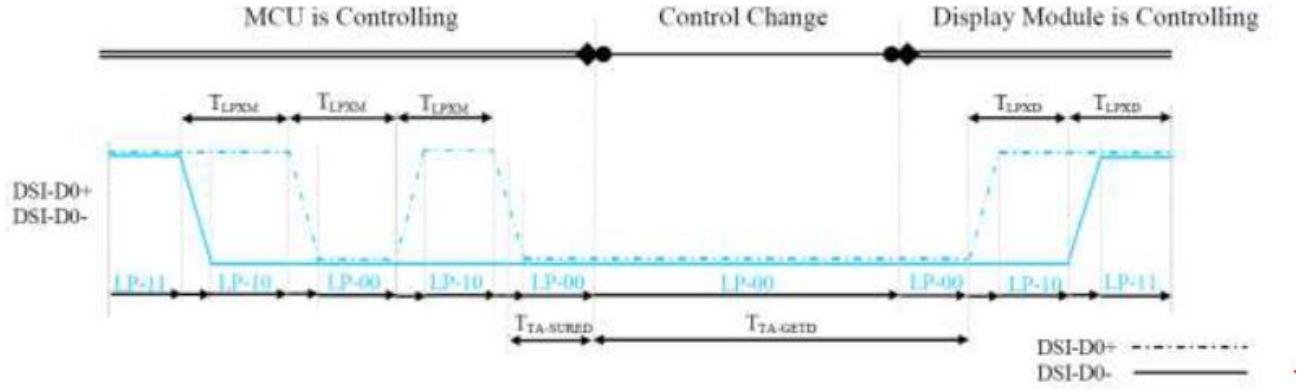


Figure 5.2.4 BTA from the MCU to the Display Module

Lower Power Mode and its State Periods are illustrated for reference purposes on the Bus Turn Around (BTA) from the Display Modue(ILI9881H) to the MCU sequence below.

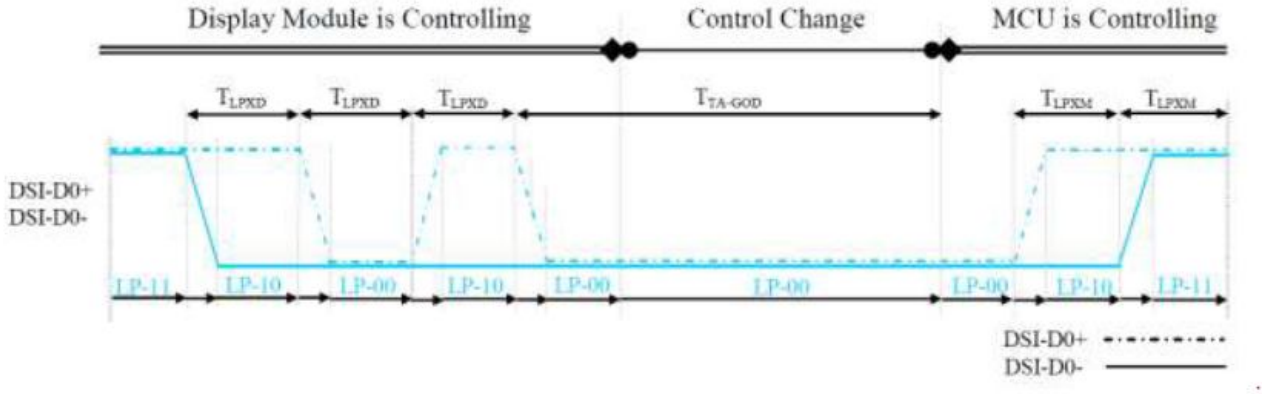


Figure 5.2.4 BTA from the Display Module to MCU

Signal	Symbol	Description	Min	Max	Unit
DSI-D0+/-	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MCU ➔ Display Module (ILI9881H)	50	75	ns
DSI-D0+/-	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module (ILI9881H) ➔ MCU	50	75	ns
DSI-D0+/-	$T_{TA-SURED}$	Time-out before the Display Module (ILI9881H) starts driving	T_{LPXD}	$2*T_{LPXD}$	ns

Table 5.2.4 Low Power State Period Timings –A

Signal	Symbol	Description	Time	Unit
DSI-D0+/-	$T_{TA-GETD}$	Time to drive LP-00 by Display Module (ILI9881H)	$5*T_{LPXD}$	ns
DSI-D0+/-	T_{TA-GOD}	Time to drive LP-00 after turnaround request – MCU	$4*T_{LPXD}$	ns

Table 5.2.4 Low Power State Period Timings –B

5.2.5 Data Lanes from Low Power Mode to High Speed Mode

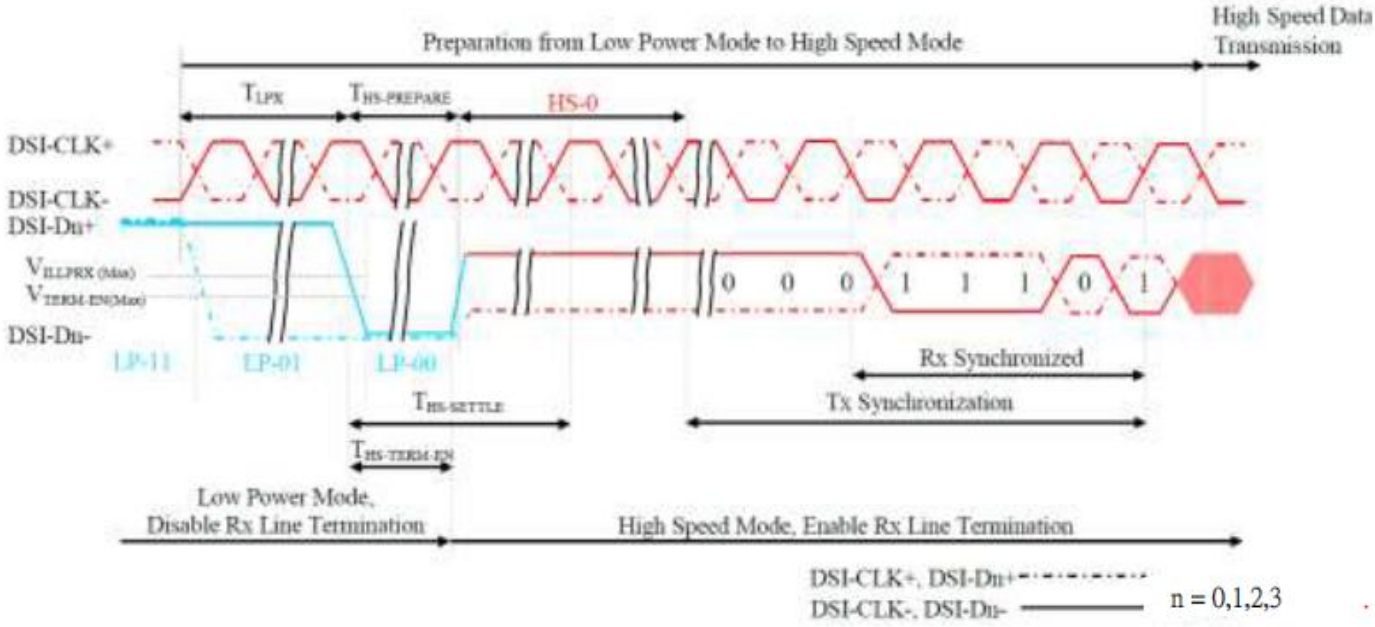


Figure 5.2.5 Data Lanes – Low Power Mode to High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DSI-Dn+/- (n=0,1,2,3)	T_{LPX}	Length of any Low Power State Period	50	-	ns
DSI-Dn+/- (n=0,1,2,3)	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
DSI-Dn+/- (n=0,1,2,3)	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX	-	35+4xUI	ns

Table 5.2.5 Data Lanes – Low Power Mode to High Speed Mode Timings

5.2.6 Data Lanes from High Speed Mode to Low Power Mode

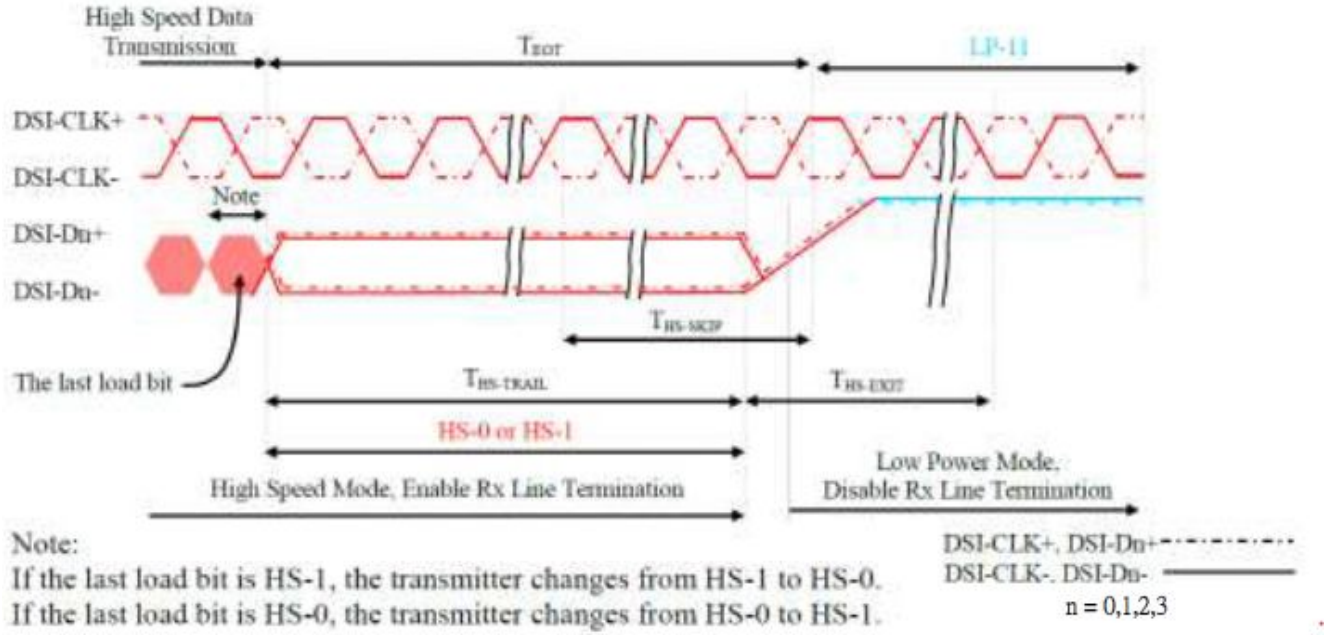


Figure 5.2.6 Data Lanes –High Speed Mode to Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DSI-Dn+/- (n=0,1,2,3)	$T_{HS-SKIP}$	Time-Out at Display Module (ILI9881H) to ignore transition period of EoT	40	55+4xUI	ns
DSI-Dn+/- (n=0,1,2,3)	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	ns
DSI-Dn+/- (n=0,1,2,3)	$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	max(8*UI, 60ns+ 4*UI)	-	ns

Table 5.2.6 Data Lanes –High Speed Mode to Low Power Mode Timings

5.2.7 DSI Clock Burst – High Speed Mode to/from Low Power Mode

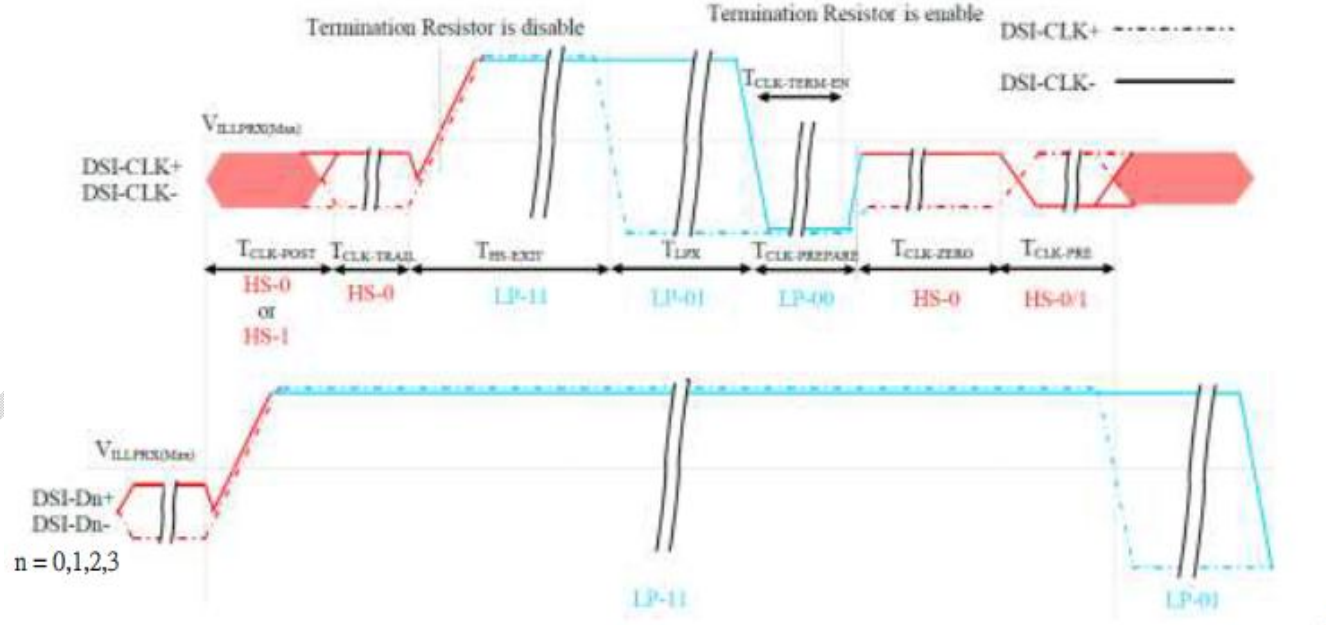
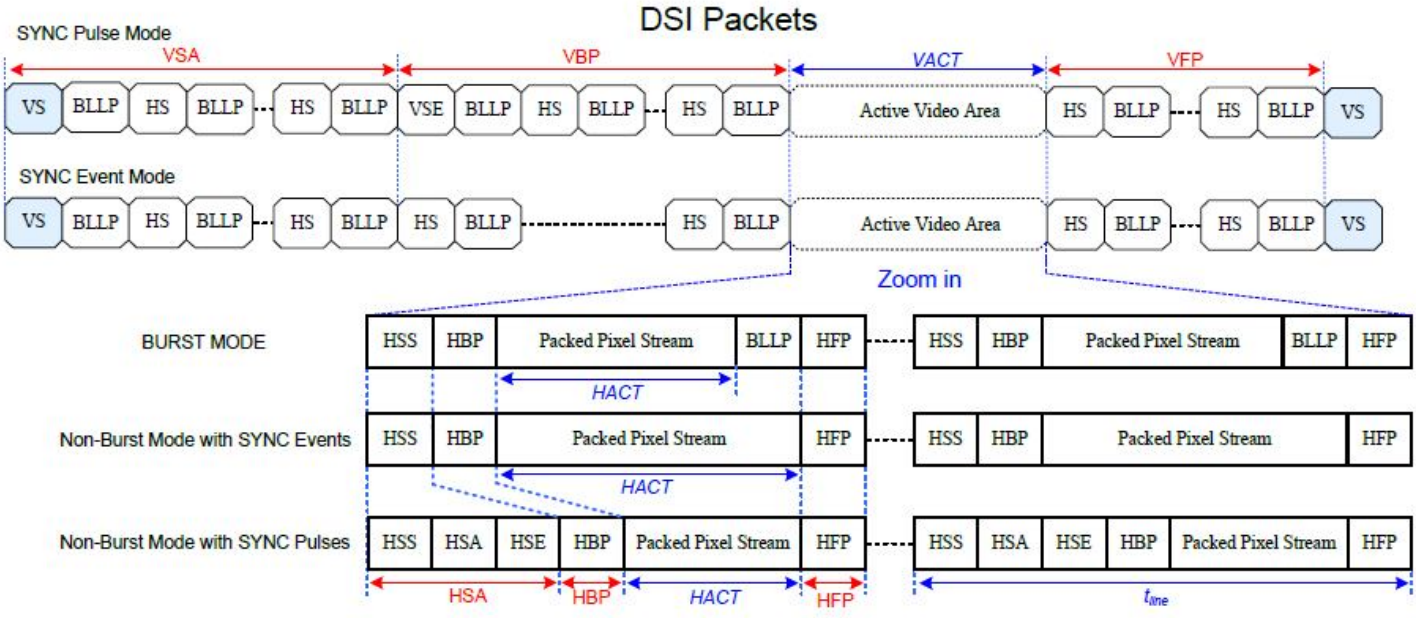


Figure 5.2.7 Clock Lanes –High Speed Mode to/from Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DSI-CLK+/-	$T_{CLK-POST}$	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52xUI	-	ns
DSI-CLK+/-	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
DSI-CLK+/-	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
DSI-CLK+/-	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
DSI-CLK+/-	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	-	38	ns
DSI-CLK+/-	$T_{CLK-PREPARE}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
DSI-CLK+/-	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI	-	ns

Table 5.2.7 Clock Lanes –High Speed Mode to/from Low Power Mode Timings

5.2.8 Timing for DSI video mode



VS → Packet V-sync. Start
VSE → Packet V-sync. End
HS → Packet H-sync.
BLLP → Non-restricted DSI packet or Low power mode including optional BTA

Packet Pixel Stream → Pixel stream and Null packets
HSS → H-sync. Start
HSA → H-sync. Active (No data)
HSE → H-sync. End
HBP → Horizontal Back Porch
HFP → Horizontal Front Porch
BLLP → Non-restricted DSI packet or Low power mode including optional BTA

Parameters	Symbols	Min.	Typ.	Max.	Units
Vertical sync. active	VSA Note 6, 7	2	-	-	Line
Vertical Back Porch	VBP Note 6, 7	16	-	-	Line
Vertical Front Porch	VFP Note 6, 7	20	-	-	Line
Active lines per frame	VACT	-	1280	-	Line
Horizontal sync. active	HSA	2	-	-	Pixel
Horizontal Porch	HSA + HBP+ HFP	1.2	-		us
Active pixels per line	HACT	-	720	-	Pixel
Bit Rate	BRbps	-	-	Note 5	Mbps/lane

1 UI = 1/Bit rate

HAS(pixel) = (tHSA*lane number) / (UI* pixel format)

HBP(pixel) = (tHBP*lane number) / (UI* pixel format)

HFP(pixel) = (tHFP*lane number) / (UI* pixel format)

$$\text{Frame Rate} = \frac{BR_{bps} \times Lane_{num}}{(VACT+VSA+VBP+VFP) \times (HACT+HSA+HBP+HFP) \times \text{Pixel Format}}$$

Example：BR_{bps} = 880Mbps/lane, 1UI=1.13ns, Frame rate=60.2Hz, VACT=1280, VSA=4, VBP=4, VFP=4, HACT=720, HSA=20, HBP=70, HFP=90, $Lane_{num}$=4(lane), Pixel Format=24(bit).

Note:

1. $Lane_{num}$: Date lane of MIPI-DSI.
2. Pixel Format: Please reference to “4.3 DSI System Interface”.
3. The formula exists slightly error because of the host-transmission way.
4. The best frame rate setting is 60 Hz.
5. Please reference to the following table.
6. The minimum values of this table mean the limitation of IC without considering the panel GIP.
7. The actual values of VSA, VBP and VFP will be changed by different panel GIP setting.

Data type	Two Lanes speed	Three Lanes speed	Four Lanes speed
Data Type = 00 1110 (0Eh), RGB 565, 16 UI per Pixel	566 Mbps	466 Mbps	366 Mbps
Data Type = 01 1110 (1Eh), RGB 666, 18 UI per Pixel	637 Mbps	525 Mbps	412 Mbps
Data Type = 10 1110 (2Eh), RGB 666 Loosely, 24 UI per Pixel	850 Mbps	700 Mbps	550 Mbps
Data Type = 11 1110 (3Eh), RGB 888, 24 UI per Pixel	850 Mbps	700 Mbps	550 Mbps

Table 5.2.8 Limited Clock Channel Speed

5.2.9 Reset Timings

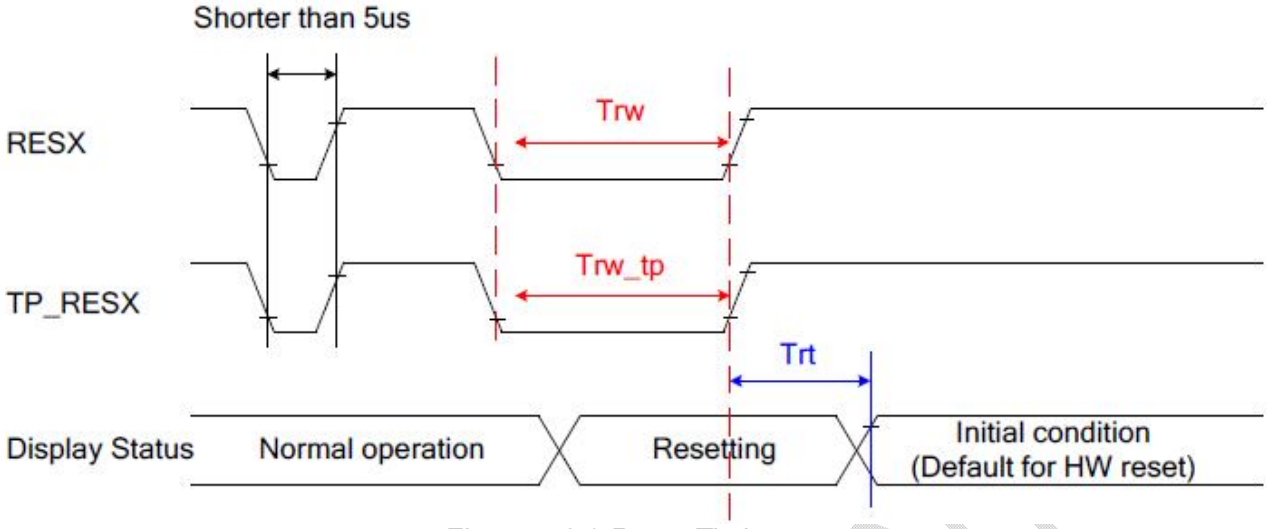


Figure 5.2.9 Reset Timing

Signal	Symbol	Parameter	Min	Max	Unit
RESX	Trw	Reset pulse duration	10	-	us
	Trt	Reset cancel	35 (Note 1,5)	-	ms
			150 (Note 1,6,7)	-	ms
TP_RESX	Trw_tp	Reset pulse duration	1	-	us

Table 5.2.9 Reset Timing

Note:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM to registers. This loading is done every time when there is H/W reset cancel time (Trt) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the following table.

RESX	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out mode. The display remains the blank state in Sleep In mode.) and return to default condition for Hardware Reset.
4. Spike Rejection also applies during a valid reset pulse as shown in following figure.

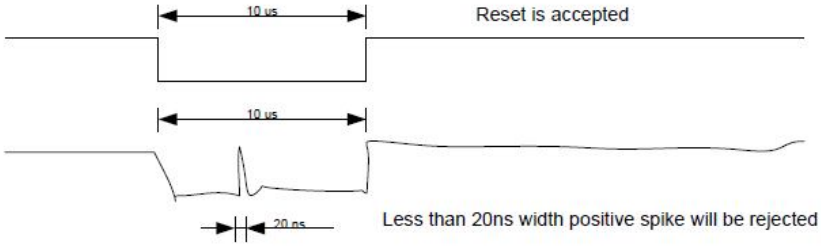


Figure 98. Positive Noise Pulse during Reset Low

5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending other commands. Also Sleep Out command (11h) cannot be sent for 120msec.

6 Optical Characteristics

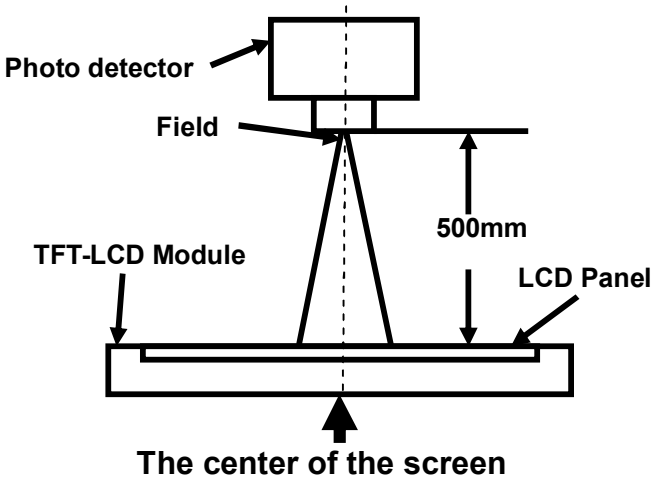
Item		Symbol	Condition	Min	Typ	Max	Unit	Remark
View Angles		θT	CR≧10	75	80		Degree	Note2,3
		θB		75	80			
		θL		75	80			
		θR		75	80			
Contrast Ratio		CR	θ=0°	1000	1200			Note 3
Response Time		T_{ON}	25℃	-	35	45	ms	Note 4
		T_{OFF}						
Chromaticity	White	x	Backlight is on	0.229	0.279	0.329		Note 1,5
		y		0.245	0.295	0.345		
	Red	x		0.568	0.618	0.668		Note 1,5
		y		0.275	0.325	0.375		
	Green	x		0.264	0.314	0.364		Note 1,5
		y		0.558	0.608	0.658		
	Blue	x		0.099	0.149	0.199		Note 1,5
		y		0.007	0.057	0.107		
Uniformity		U		70	80	-	%	Note 6
NTSC				65	70	-	%	Note 5
Luminance		L		300	350	-	cd/m^2	Note 7

Test Conditions:

1. I_F= 80 mA, and the ambient temperature is 25℃.
2. The test systems refer to Note 1 and Note 2.

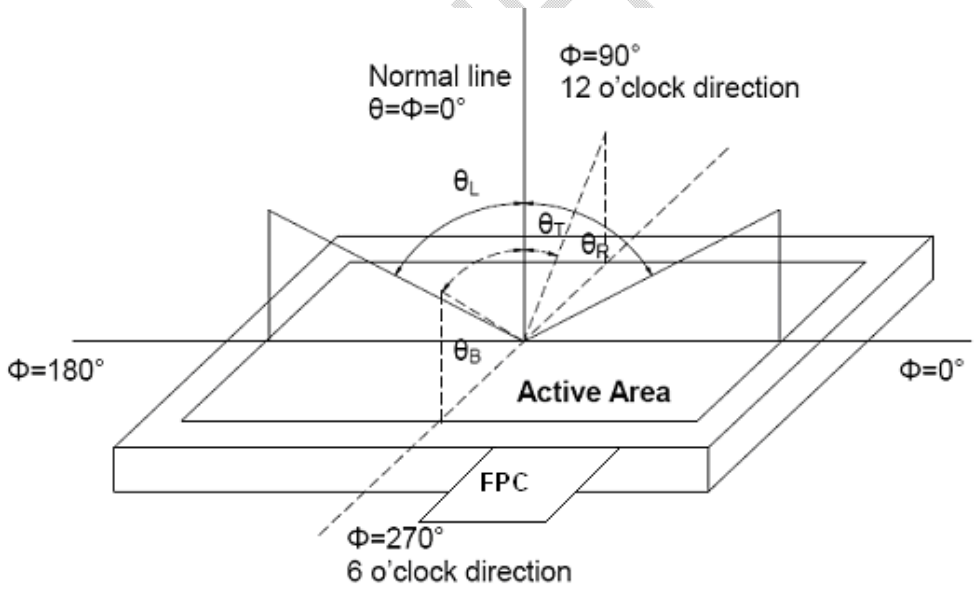
Note 1: Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 5 Minutes operation, the optical properties are measured at the center point of the LCD screen. All input terminals LCD panel must be ground when measuring the center area of the panel.



Note 2: Definition of viewing angle range and measurement system.

viewing angle is measured at the center point of the LCD .



Note 3: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD is on the "White" state}}{\text{Luminance measured when LCD is on the "Black" state}}$$

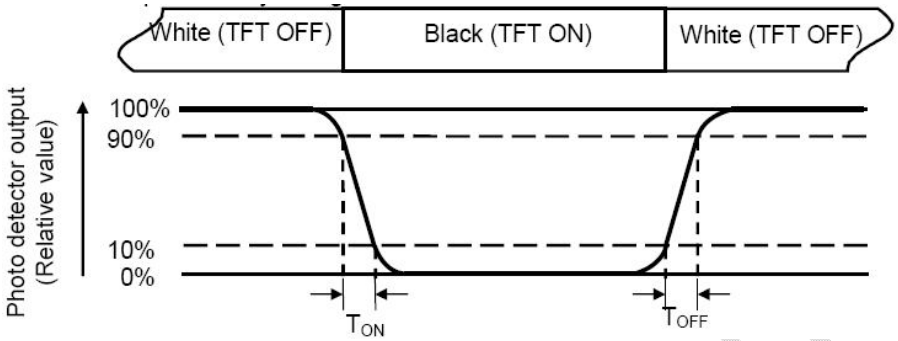
"White state ": The state is that the LCD should drive by Vwhite.

"Black state": The state is that the LCD should drive by Vblack.

Vwhite: To be determined Vblack: To be determined.

Note 4: Definition of Response time

The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time (T_{ON}) is the time between photo detector output intensity changed from 90% to 10%. And fall time (T_{OFF}) is the time between photo detector output intensity changed from 10% to 90%.



Note 5: Definition of color chromaticity (CIE1931)

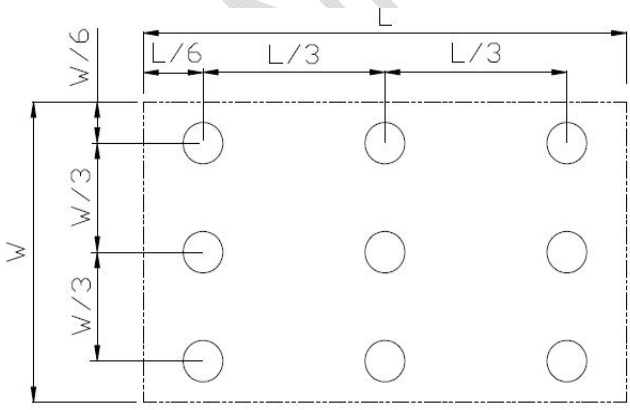
Color coordinates measured at center point of LCD.

Note 6: Definition of Luminance Uniformity

Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

Luminance Uniformity (U) = Lmin/ Lmax

L-------Active area length W----- Active area width



Lmax: The measured Maximum luminance of all measurement position.

Lmin: The measured Minimum luminance of all measurement position.

Note 7: Definition of Luminance:

Measure the luminance of white state at center point.

7 Environmental / Reliability Test

No	Test Item	Condition	Remarks
1	High Temperature Operation	+70℃，96Hrs	IEC60068-2-1:2007 GB2423.2-2008
2	Low Temperature Operation	-20℃，96Hrs	IEC60068-2-1:2007 GB2423.1-2008
3	High Temperature Storage	+80℃，96Hrs	IEC60068-2-1:2007 GB2423.2-2008
4	Low Temperature Storage	-30℃，96Hrs	IEC60068-2-1:2007 GB2423.1-2008
5	High Temperature and Humidity	+60℃，90%RH，96Hrs（Operation）	IEC60068-2-78 :2001 GB/T2423.3—2006
6	Thermal Shock (non-operation)	-30℃，30min~80℃，30min，change time：5min，100cycle	Start with cold temperature, End with high temperature, IEC60068-2-14:1984,GB2423.22-2002
7	ESD	C=150pF，R=330Ω，5point/panel Air：±8kv，5times； Contact：±4kv，5times； （Environment：15℃~35℃，30%~60%，86Kpa~106Kpa）	IEC61000-4-2:2001 GB/T17626.2-2006
8	Package Vibration	5-20-200HZ，PSD：0.01-0.01-0.001 Total:0.781g2/HZ,x/y/z every direction 30min）	
9	Package Drop Test	Height: 60cm,1 corner, 3edges, 6 surfaces	IEC60068-2-32:1990 GB/T2423.8—1995

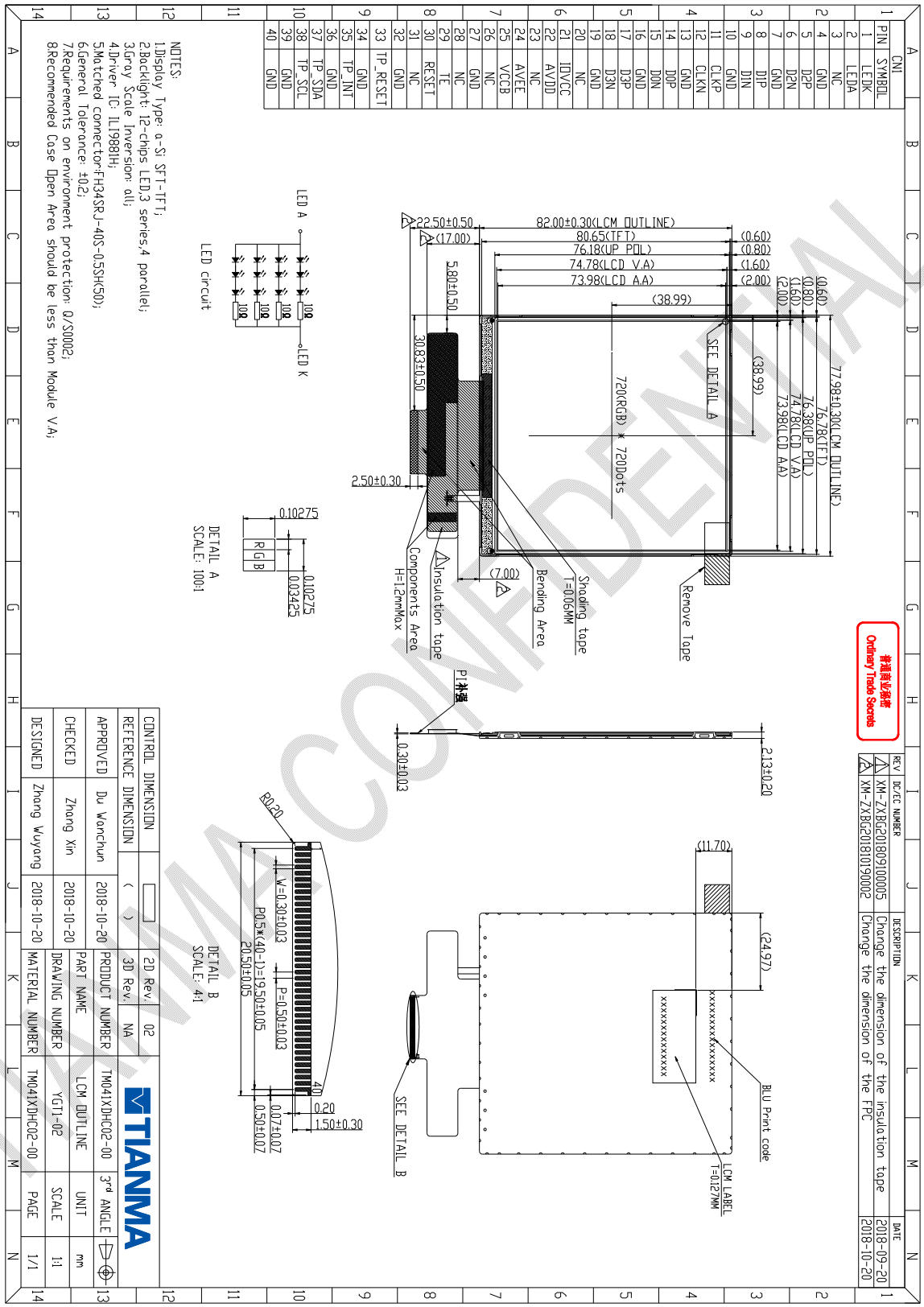
Note1: Ts is the temperature of panel's surface.

Note2: Ta is the ambient temperature of sample.

Note3: Before cosmetic and function test, the product must have enough recovery time, at least 2 hours at room temperature.

Note 4: In the standard condition, there shall be no practical problem that may affect the display function. After the reliability test, the product only guarantees operation, but don't guarantee all of the cosmetic specification.

8 Mechanical Drawing



9 Packing Drawing

9.1 Packaging Material

Per Carton

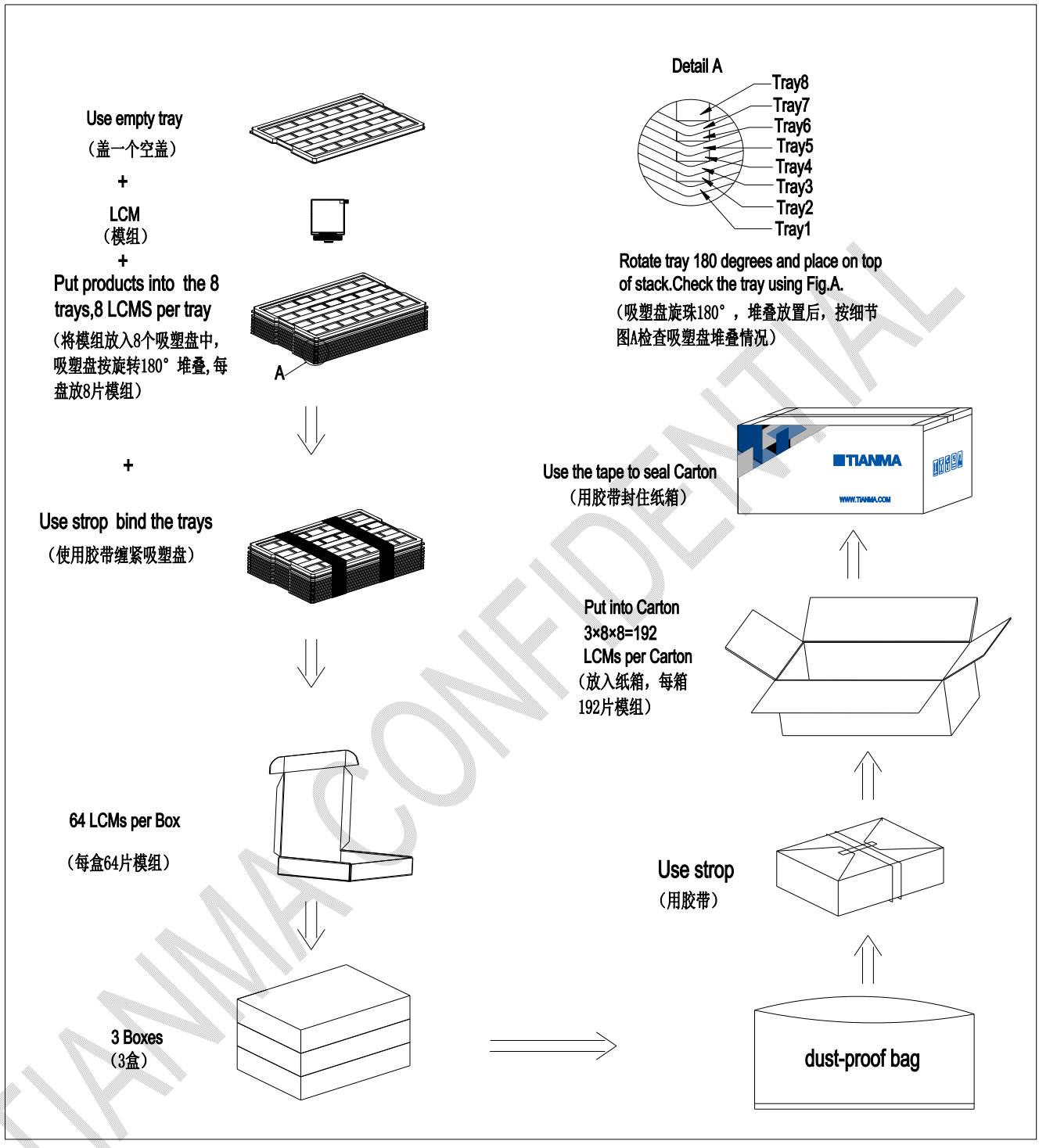
No	Item	Model (Material)	Dimensions(mm)	Unit Weight(Kg)	Quantity	Remark
1	LCM module	TM041XDHC02-00	77.98×82.00×2.13mm	0.0275	192	
2	Dust-Proof Bag	PE	700×545mm	0.03	1	
3	Tray	PET	485×330×13.8mm	0.16	27	
4	Carton	Corrugated Paper	544×365×250mm	0.76	1	
5	BOX	Corrugated Paper	520×345×74mm	0.35	3	
6	Label	Paper	100*52mm 2000PCS/Roll	0.001	1	
7	Total weight	11.44±5% Kg				

9.2 Packaging Specification and Quantity

(1) LCM quantity per tray: 8

(2) Total LCM quantity in Carton: quantity per tray 8 × 24 tray = 192

Note: Please refer to the data from “estimated report about the dimension and stack of Carton “ about stacking carton



10 Precautions for Use of LCD Modules

10.1 Handling Precautions

10.1.1 The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

10.1.2 If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

10.1.3 Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

10.1.4 The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

10.1.5 If the display surface is contaMinated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Water
- Ketone
- Aromatic solvents

10.1.6 Do not attempt to disassemble the LCD Module.

10.1.7 If the logic circuit power is off, do not apply the input signals.

10.1.8 To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

10.1.8.1 Be sure to ground the body when handling the LCD Modules.

10.1.8.2 Tools required for assembly, such as soldering irons, must be properly ground.

10.1.8.3 To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

10.1.8.4 The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

10.2 Storage precautions

10.2.1 When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

10.2.2 The LCD modules should be stored under the storage temperature range. If the LCD modules will be stored for a long time, the recommend condition is:

Temperature : 0℃ ～ 40℃ Relatively humidity: ≤80%

10.2.3 The LCD modules should be stored in the room without acid, alkali and harmful gas.

10.3 Transportation Precautions

10.3.1 The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.