

SPEC

Spec No.	Q-DS-1-S109-00
Date	2024.06.25

TYPE : A0260WV65484-NN-AA

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KYOCERA CORPORATION
DONGGUAN SHILONG KYOCERA Co., Ltd.
DISPLAY DIVISION

This specification is subject to change without notice.
Consult Kyocera before ordering.

Original Issue Date	Designed by: Design Development dept.			Confirmed by: QA dept.	
	Prepared	Checked	Approved	Checked	Approved
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Warning

This product has been manufactured to your company's specifications as a part for use in your company's general electronic products. It is guaranteed to perform according to delivery specifications. For any other use apart from general electronic equipment, we cannot take responsibility if the product is used in medical devices, nuclear power control equipment, aerospace equipment, fire and security systems, or any other applications in which there is a direct risk to human life and where extremely high levels of reliability are required. If the product is to be used in any of the above applications, we will need to enter into a separate product liability agreement.

- 1) We cannot accept responsibility for any defect, which may arise from additional manufacturing of the product (including disassembly and reassembly), after product delivery.**
- 2) We cannot accept responsibility for any defect, which may arise after the application of strong external force to the product.**
- 3) We cannot accept responsibility for any defect, which may arise due to the application of static electricity after the product has passed your company's acceptance inspection procedures.**
- 4) When the product is in CFL models, CFL service life and brightness will vary according to the performance of the inverter used, leaks, etc. We cannot accept responsibility for product performance, reliability, or defect, which may arise.**
- 5) We cannot accept responsibility for intellectual property of a third party, which may arise through the application of our product to your assembly with exception to those issues relating directly to the structure or method of manufacturing of our product.**
- 6) We will not be held responsible for any quality guarantee issue for defect products judged As KYOCERA-origin in two years from our production or one year from KYOCERA Group delivery whichever is shorter.
However, priority is given to the contents of the "part (product) basic contract document" concluded in both.**

Revision record

Date		Designed by : Design Development dept.			Confirmed by : QA dept.	
		Prepared	Checked	Approved	Checked	Approved
Rev. No.	Date	Page	Descriptions			

1. General specifications

Screen size	:	2.6 inches (Diagonal)
Active area	:	57.6(W) × 34.56(H) mm
Dot pixels	:	800(W) × 3[R.G.B] × 480(H)
Pixel pitch	:	0.024(W) × 3[R.G.B] × 0.072 (H) mm
Pixel arrangement	:	RGB stripe
Color depth	:	16.7M colors
LCD type	:	TFT / Normally black-mode / Transmissive
Surface treatment	:	Glare
Front polarization axis angle	:	0° (Horizontal direction)
Polarization withstand temperature	:	Max. 110°C
LC clearing temperature	:	Min. 119.8°C
Data transfer	:	LVDS (JEIDA Format) data transfer 8bit + GPU or SPI
Driver IC	:	PTC (Princeton Technology Corporation) PT16203J
Recommended connector	:	EVAFLEX5 - SE 30pin (DAI-ICHI SEIKO CO., LTD) 04 6810 630 020 846+T (Kyocera)
Backlight	:	None
About the backlight to be used	:	The brightness of the backlight is less than 2 million cd/m ² Please evaluate long-term reliability carefully in advance.
Drawings	:	Dimensional outline 121A9035300
Outline dimensions	:	65.10(W) x 44.66(H) x 1.29 (D) mm Without FPC
Weight	:	9.4 g Typ.
RoHS regulation and Europe ELV instructions	:	This product satisfies material Europe ELV requirement of Europe ELV instructions and RoHS regulation.

2. Operating conditions

Item	Conditions	Temperature range	Remark
Operating temperature range	Panel surface	-40~105°C	Note1,2
Storage temperature range	Panel surface	-40~105°C	Note2

Note1: Operating temperature range defines the operation only and the contrast, response time and other display optical characteristics are set at Ta=+25°C.

Note2: No dew condensation

3. Electrical specifications

3.1 Absolute maximum rating

Ta=-40~105°C, GND=0V

Parameter	Symbol	Conditions	Min.	Max.	Unit
Supply voltage	V _{DD}	-	-0.3	+6.5	V
Input voltage(Logic)	V _I	-	-0.3	V _{DD} +0.3	V

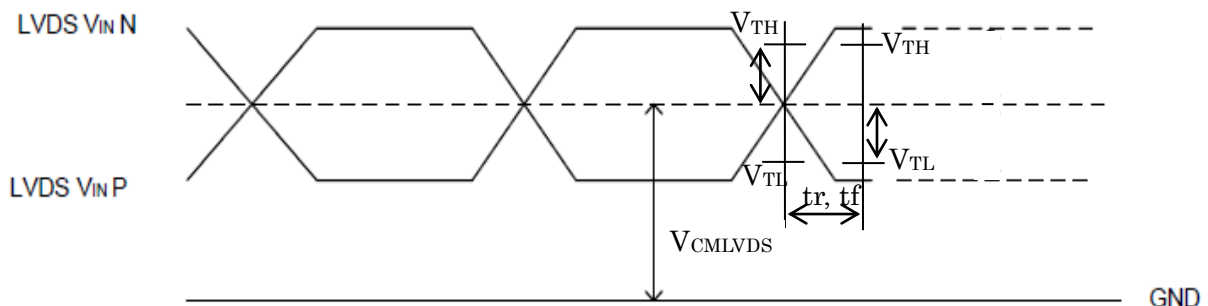
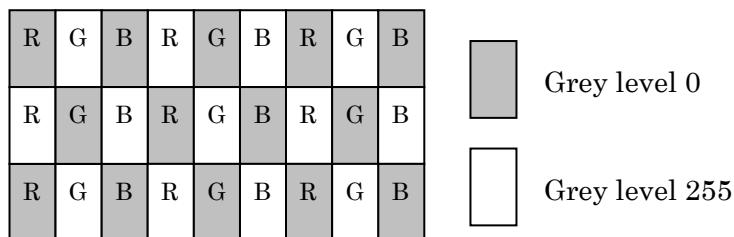
3.2 DC characteristics

Ta=-40~105°C, GND=0V

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V _{DD}	-	3.0 (Note1)	3.3	3.6	V
Supply current (Note2)	I _{DD}	V _{DD} -GND=3.3V	-	35	52.5	mA
"High" level input voltage	V _{IH}	-	0.7V _{DD}	-	V _{DD}	V
"Low" level input voltage	V _{IL}	-	0	-	0.3V _{DD}	V
High LVDS input threshold	V _{TH}	V _{CMLVDS} =1.25V	-	-	+100	mV
Low LVDS input threshold	V _{TL}	V _{CMLVDS} =1.25V	-100	-	-	mV
LVDS input signal rise time	t _r	V _{CMLVDS} =1.25V	-	-	1.5	ns
LVDS input signal fall time	t _f	V _{CMLVDS} =1.25V	-	-	1.5	ns
LVDS input common mode voltage	V _{CMLVDS}	-	0.3	1.25	2.2	V

Note1: If V_{DD} have dropped to less than 2.0V at any moment during the operation, display not appears.

Note2: Sub pixel checker pattern

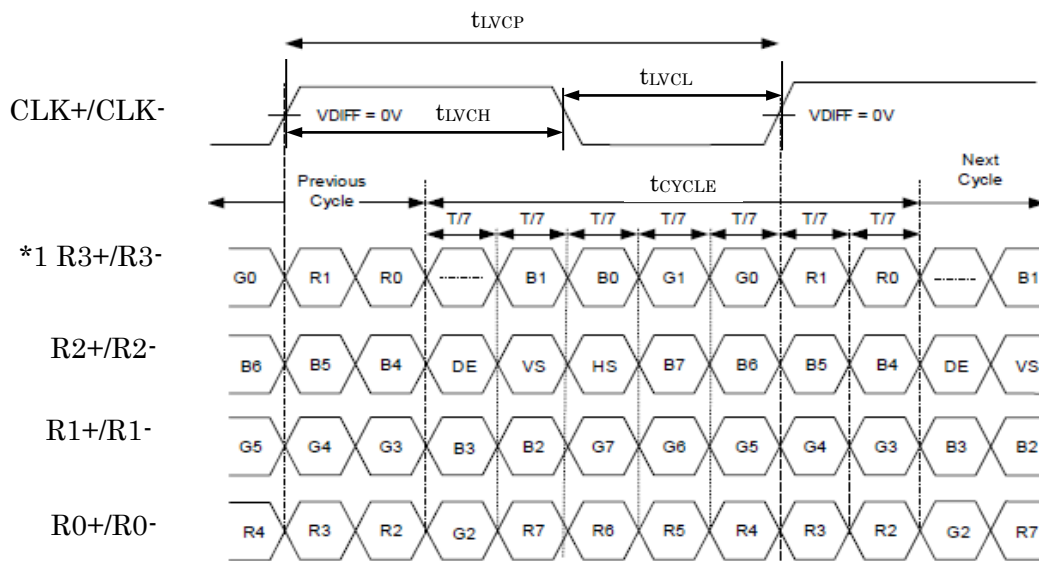
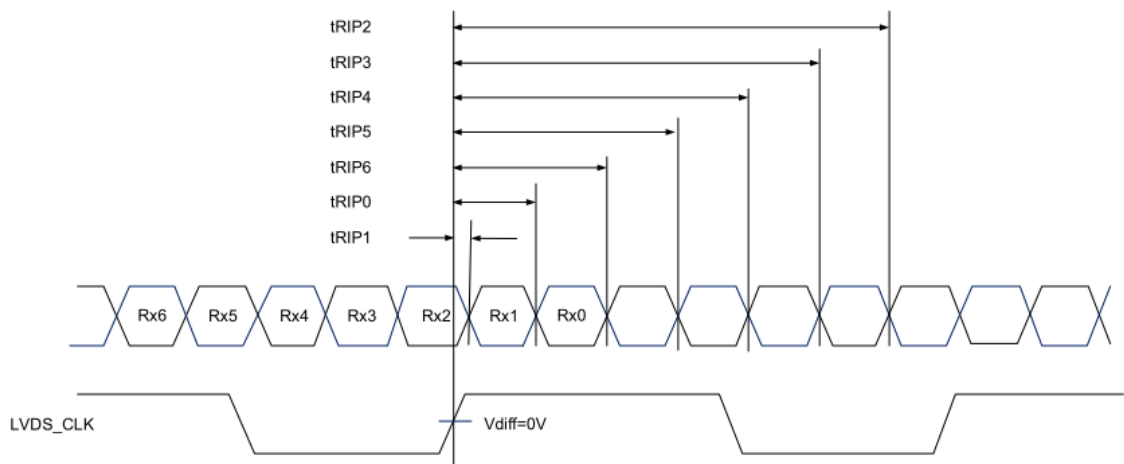
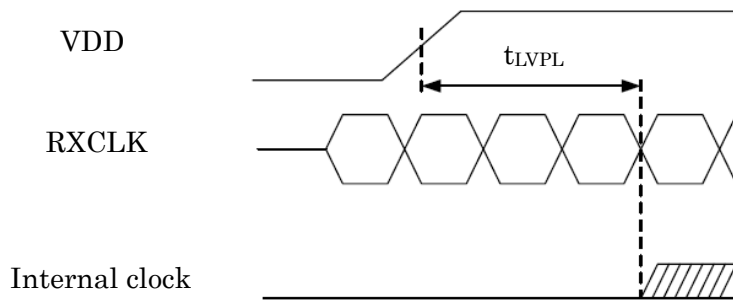


3.3 AC characteristics

3.3.1 LVDS interface timing characteristics

$T_a = -40 \sim 105^\circ\text{C}$, $V_{DD} = 3.0 \sim 3.6\text{V}$, $GND = 0\text{V}$

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock period	t_{LVCP}	31	T	42	ns
Clock high time	t_{LVCH}	-	$4T/7$	-	ns
Clock low time	t_{LVCL}	-	$3T/7$	-	ns
PLL wake-up time	t_{LVPLL}	-	-	10	ns
Input Data position 0	t_{RIP1}	-0.4	0	+0.4	ns
Input Data position 1	t_{RIP0}	$T/7-0.4$	$T/7$	$T/7+0.4$	ns
Input Data position 2	t_{RIP6}	$2T/7-0.4$	$2T/7$	$2T/7+0.4$	ns
Input Data position 3	t_{RIP5}	$3T/7-0.4$	$3T/7$	$3T/7+0.4$	ns
Input Data position 4	t_{RIP4}	$4T/7-0.4$	$4T/7$	$4T/7+0.4$	ns
Input Data position 5	t_{RIP3}	$5T/7-0.4$	$5T/7$	$5T/7+0.4$	ns
Input Data position 6	t_{RIP2}	$6T/7-0.4$	$6T/7$	$6T/7+0.4$	ns

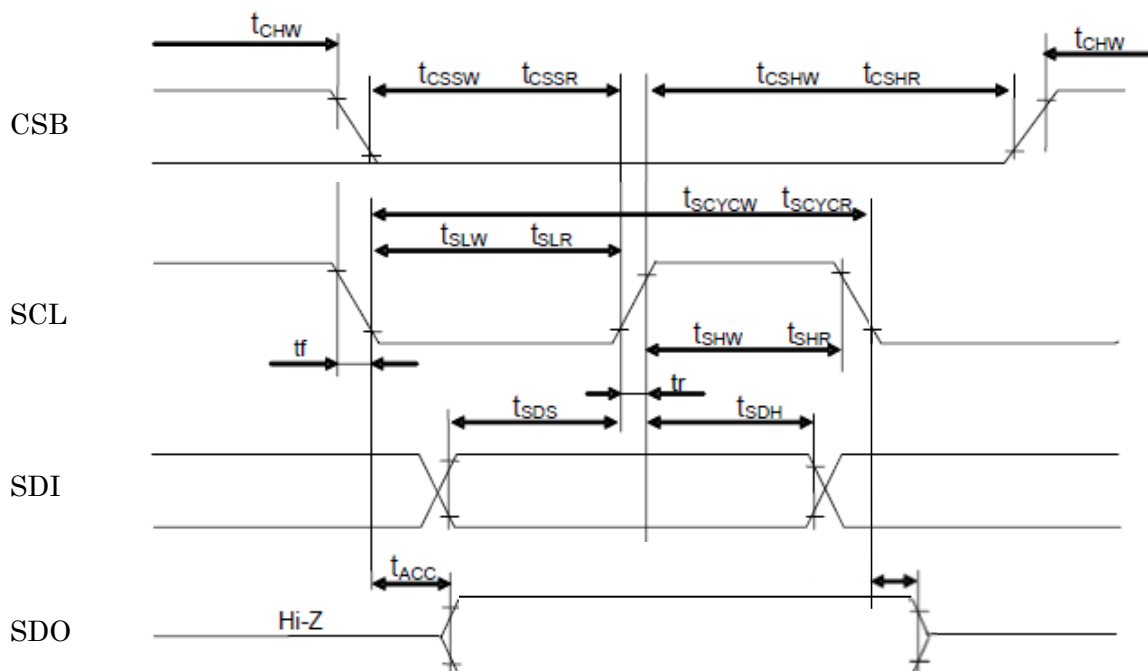


*1. In 6bit input mode (IM=L), LVDS input to R3+/R3- will be ignored.

3.3.2 Serial interface timing characteristics

$T_a = -40 \sim 105^\circ\text{C}$, $V_{DD} = 3.0 \sim 3.6\text{V}$, $GND = 0\text{V}$, $t_r = t_f = 6\text{ns}$

Parameter	Symbol	Min.	Typ.	Max.	Unit
CSB high pulse period	t_{CHW}	40	-	-	ns
CSB-SCL time (write)	t_{CSSW}	15	-	-	ns
	t_{CSHW}	15	-	-	ns
CSB-SCL time (read)	t_{CSSR}	60	-	-	ns
	t_{CSHR}	60	-	-	ns
Serial clock cycle (write)	t_{SCYCW}	66	-	-	ns
SCL high pulse width (write)	t_{SHW}	15	-	-	ns
SCL low pulse width (write)	t_{SLW}	15	-	-	ns
Serial clock cycle (read)	t_{SCYCR}	180	-	-	ns
SCL high pulse width (read)	t_{SHR}	80	-	-	ns
SCL low pulse width (read)	t_{SLR}	80	-	-	ns
Data setup time	t_{SDS}	10	-	-	ns
Data hold time	t_{SDH}	10	-	-	ns
Access time	t_{ACC}	-	-	60	ns
Output disable time	t_{OD}	-	-	50	ns
Input signal rise time	t_r	-	-	15	ns
Input signal fall time	t_f	-	-	15	ns



3.3.3 Data transfer timing

a) Vertical timing

The following figure illustrates vertical timing.

$T_a = -40 \sim 105^\circ\text{C}$, $V_{DD} = 3.0 \sim 3.6\text{V}$, $GND = 0\text{V}$

Parameter	Symbol	Min.	Typ.	Max.	Unit
Vertical cycle (Note1)	t_{VP}	486	488	490	Line
Vertical low pulse width (Note2)	t_{VS}	2	2	4	Line
Vertical front porch (Note2)	t_{VFP}	2	4	4	Line
Vertical back porch (Note2)	t_{VBP}	2	2	4	Line
Vertical data start point (Note2)	$t_{VS} + t_{VBP}$	4	4	8	Line
Vertical blanking period	t_{VBLK}	6	8	10	Line
Vertical display area	t_{VDISP}	480	480	480	Line
Vertical refresh rate (Note1)	f_{VRR}	59.5	60	60.5	Hz

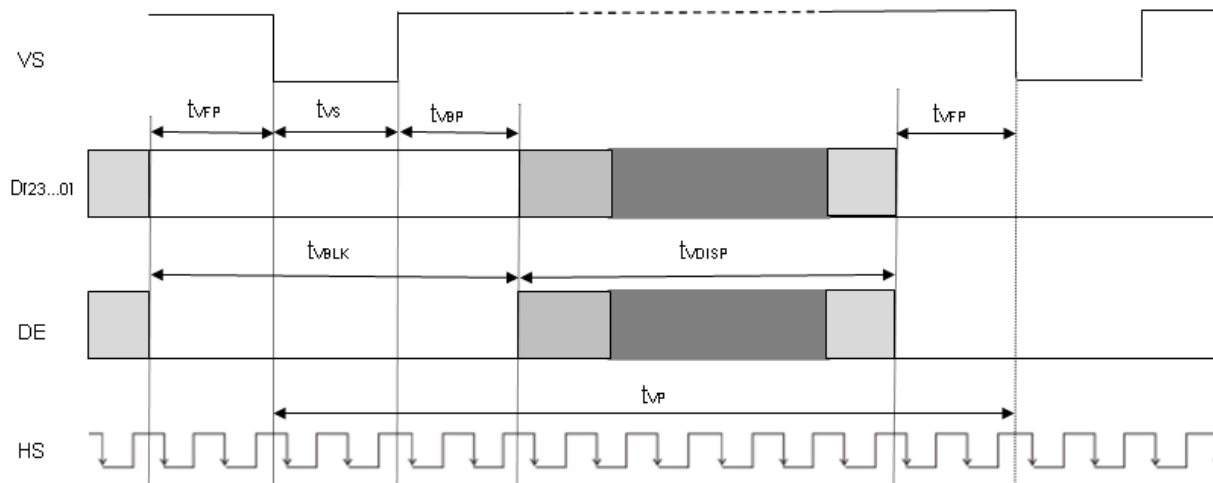
Note1: This value is also constrained by: $N_{HP} * N_{VP} * f_{VRR} = f_{PCLK}$

N_{HP} : PCLK count of t_{HP} period, N_{VP} : Line count of t_{VP} period

Note2: This value combined with other values may have limits.

For example, Max. of $t_{VS} = t_{VFP} = t_{VBP} = 4$, but also $t_{VBLK} (t_{VS} + t_{VFP} + t_{VBP}) \leq 10$

Note3: Line= t_{HP} (Horizontal cycle)



b) Horizontal timing

The following figure illustrates horizontal timing.

$T_a = -40 \sim 105^\circ\text{C}$, $V_{DD} = 3.0 \sim 3.6\text{V}$, $GND = 0\text{V}$

Parameter	Symbol	Min.	Typ.	Max.	Unit
Horizontal period in time (Note2)	1Hperiod	34.0	34.15	34.3	μs
Horizontal cycle (Note1,2)	t_{HP}	832	896	1200	PCLK
Horizontal low pulse width (Note3)	t_{HS}	2	16	226	PCLK
Horizontal front porch (Note3)	t_{HFP}	2	32	226	PCLK
Horizontal back porch (Note3)	t_{HBP}	2	48	226	PCLK
Horizontal data start point (Note3)	$t_{HS} + t_{HBP}$	30	64	228	PCLK
Horizontal blanking period	t_{HBLK}	32	96	230	PCLK
Horizontal display area	t_{HDISP}	800	800	800	PCLK
Pixel clock frequency (Note1,2)	f_{PCLK}	24.5	26.2	35	MHz

Note1: This value is also constrained by: $N_{HP} * N_{VP} * f_{VRR} = f_{PCLK}$

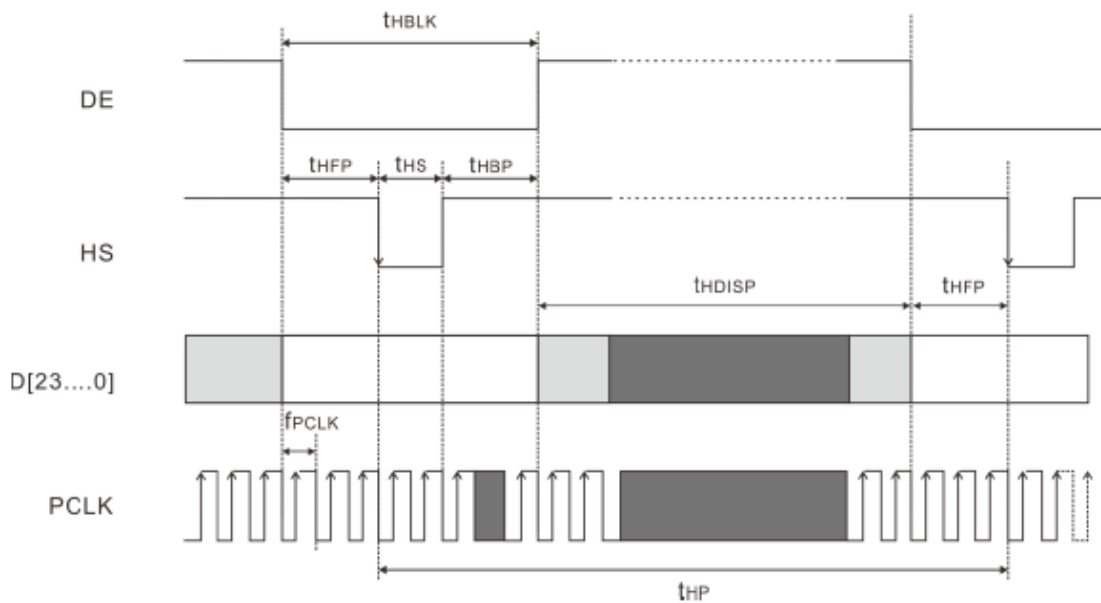
N_{HP} : PCLK count of t_{HP} period, N_{VP} : Line count of t_{VP} period

Note2: This value is also constrained by $1/f_{PCLK} * t_{HP} = 1\text{Hperiod}$

Note3: This value combined with other values may have limits.

For example, Max. of $t_{HS} = t_{HFP} = t_{HBP} = 226$, but also $t_{HBLK} (t_{HS} + t_{HFP} + t_{HBP}) \leq 230$.

Note4: $PCLK = 1 / f_{PCLK}$

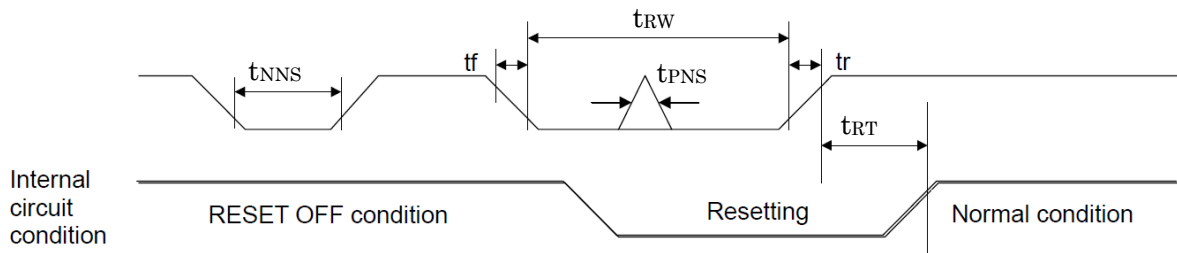


3.3.4. Reset characteristics

$T_a = -40 \sim 105^\circ\text{C}$, $V_{DD} = 3.0 \sim 3.6\text{V}$, $\text{GND} = 0\text{V}$

Parameter	Symbol	Min.	Typ.	Max.	Unit
Reset pulse duration	t_{RW}	10	-	-	μs
Reset cancel	t_{RT}	1	-	-	ms
Pulse width not to be sense as low level	t_{NNS}	-	-	5	μs
Pulse width not to be sense as noise	t_{PNS}	-	-	20	ns
RES rise time	t_r	-	-	15	ns
RES fall time	t_f	-	-	15	ns

- * Rise time and fall time of input signals (t_r, t_f) are less than 15ns.
- * Time duration is between 30% and 70% of $V_{DD} - \text{GND}$ amplitude.
- * This IC will not respond to a negative input pulse (t_{NNS}) to RES terminal with width up to 5 μs . It is considered as noise.
- * This IC will not respond to a positive input pulse (t_{PNS}) to RES terminal with width up to 20ns. It is considered as noise.
- * If RES pulse is between 5 $\mu\text{s} \sim 9\mu\text{s}$, the reset operation is abnormal.

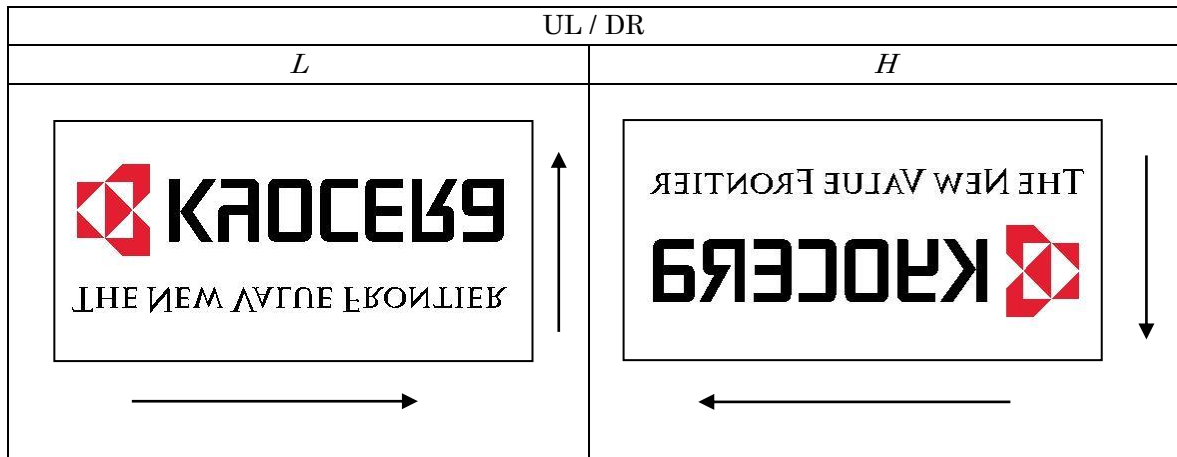


3.4 Interface

3.4.1 GPU interface

Display state of the panel is determined by the logic UL / DR as shown below in the GPU I/F mode.

Original data to transfer



→ Writing direction to the LCD

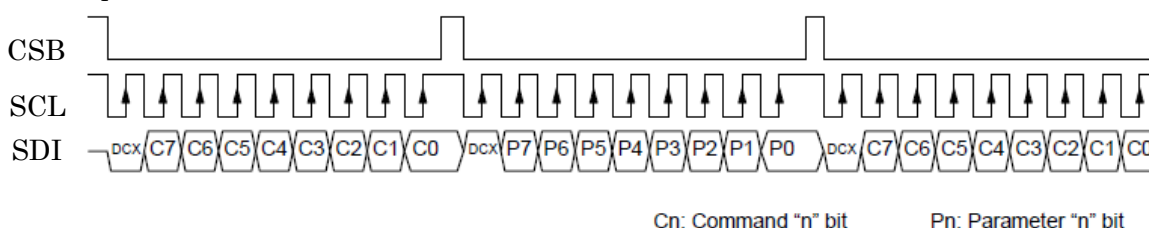
3.4.2 Serial interface mode

Even in GPU I/F mode, SPI commands can still be accessed by using the EXTCTL1 command. In serial interface mode, the use of external input pins CSB, SCL, SDI, SDO are described in the bellow table. If the serial interface mode is not used, please set CSB, SCL and SDI to GND.

Pin name	I/O	Description
CSB	I	Chip select signal
SCL	I	Serial clock
SDI	I	Serial data input
SDO	O	Serial data output

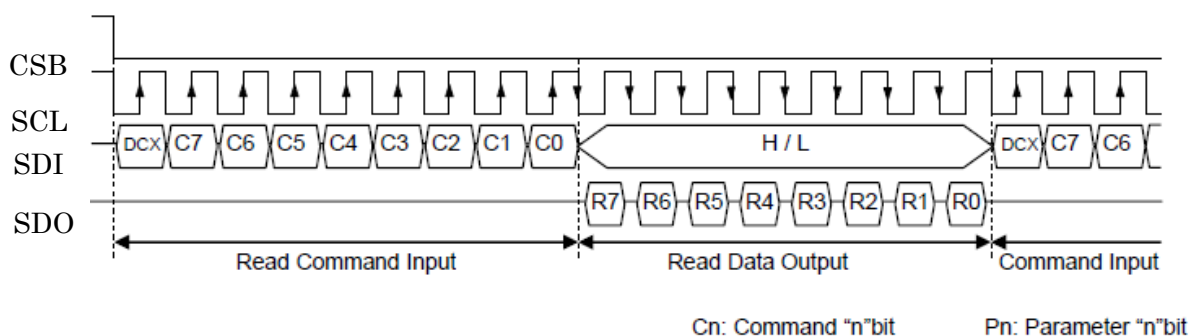
The following figures illustrate the usage of serial interface.

Write operation



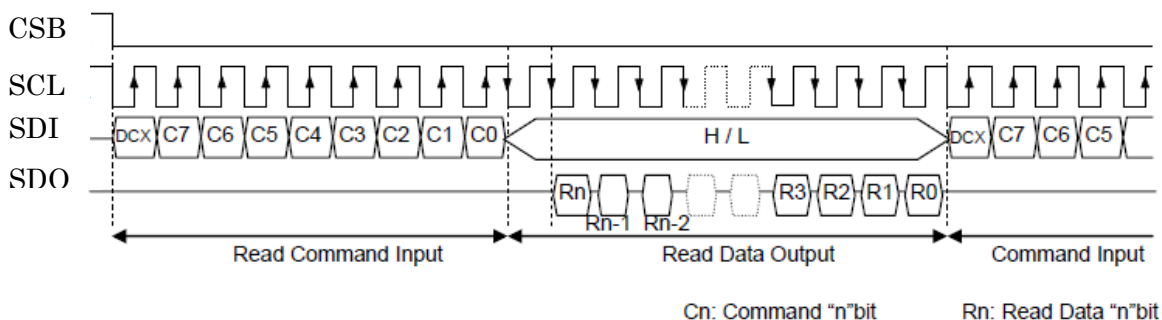
1-byte read operation

The following figure illustrates the 1-byte read operation. After read command input, the 8-bit read data will be shifted out and the read operation is finished. Then the IC will return to command Input mode.



Multi-byte read operation

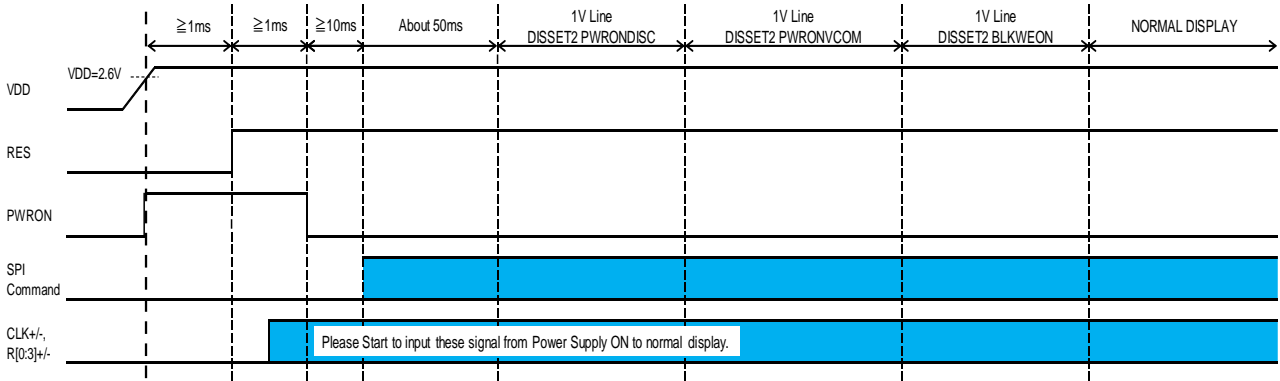
The following figure illustrates the multi-byte read operation. If the last byte is transmitted the IC will return to Command Input mode from Read Mode. Moreover, the read data output will be a leading dummy bit followed by the normal data.



3.5 Power ON procedure

*To keep the below condition

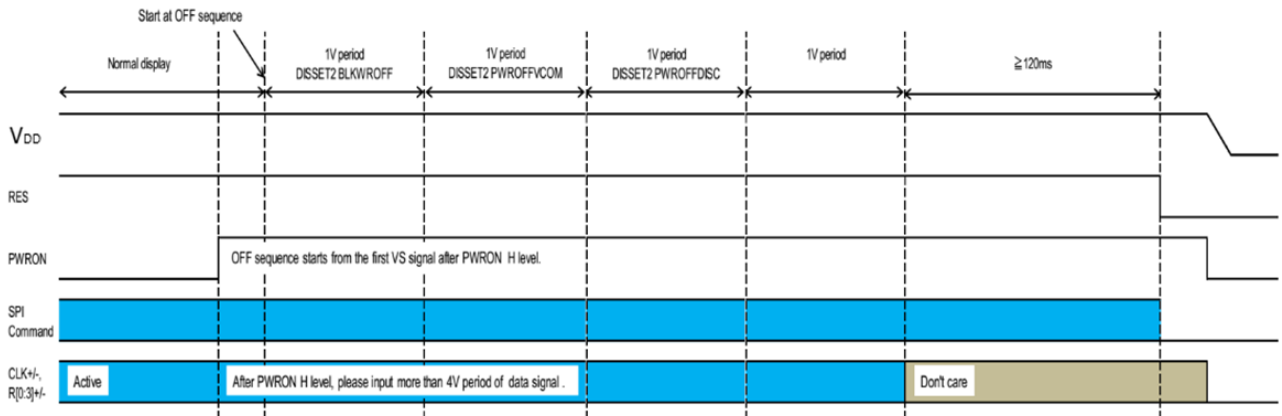
(GPU I/F mode)



3.6 Power OFF procedure

*To keep the below condition

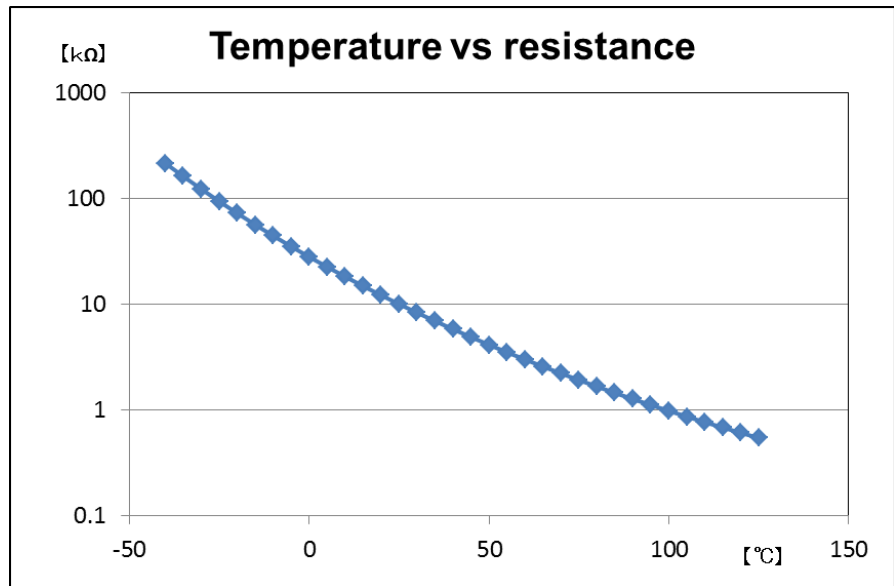
(GPU I/F mode)



3.7.Thermistor characteristic :Reference

Thermistor: TCT3GH103F3435V (TATEYAMA KAGAKU IND. CO., LTD)

°C	kΩ
-40	214.3
-35	160.8
-30	121.9
-25	93.29
-20	72.08
-15	56.18
-10	44.15
-5	34.98
0	27.91
5	22.44
10	18.16
15	14.79
20	12.13
25	10
30	8.293
35	6.914
40	5.795
45	4.882
50	4.132
55	3.514
60	3.002
65	2.575
70	2.218
75	1.918
80	1.665
85	1.451
90	1.269
95	1.114
100	0.981
105	0.866
110	0.768
115	0.683
120	0.609
125	0.544
$B_{25/85}$	3435K



4. Optical specifications

4.1. Optical characteristic

Item	Symbol	Conditions		Standard value			Unit	Method of measure	Remark	
		θ	ϕ	Min.	Typ.	Max.				
Transmittance	T	0°	0°	5.8	7.0	-	%	(Fig.1)	Note1	
Contrast	25°C	CR	0°	0°	900	1500	-			
Color coordinates	Red	Rx	0°	0°	0.582	0.612	0.642			-
		Ry	0°	0°	0.316	0.346	0.376			-
	Green	Gx	0°	0°	0.265	0.295	0.325			-
		Gy	0°	0°	0.518	0.548	0.578			-
	Blue	Bx	0°	0°	0.113	0.143	0.173			-
		By	0°	0°	0.192	0.222	0.252			-
White	Wx	0°	0°	0.299	0.329	0.359	-			
	Wy	0°	0°	0.360	0.390	0.420	-			
Response time Tr + Td	Black ⇔ White	-30°C	θ	0°	0°	-	650	980	ms	(Fig.2)
	0°C	-				85	130			
	25°C	-				30	45			

Note1: Under the condition of light source (5000cd/m² x , y : 0.285 , 0.265).

◆ Conditions for measuring.

- ◇ Environment : Dark room with no light or close to no light.
- ◇ Temperature : 25±5°C
- ◇ Humidity : 40~70%RH

◆ Method of measurement of contrast and transmittance
(Fig.1)

(1) Measuring device

SR-LEDW-5N, Measuring Field: 1°

(2) Measuring point

Center of display, Vertical direction.

(3) Method of measuring

The distance between SR-LEDW-5N's front lens to panel surface is 500mm.

- Brightness of light source L1
- Maximum brightness: All white pattern Y1, Minimum brightness: All black pattern Y2
- Contrast is derived from $CR=Y1/Y2$.
- Transmittance derived from $T= Y1/L1 *100$

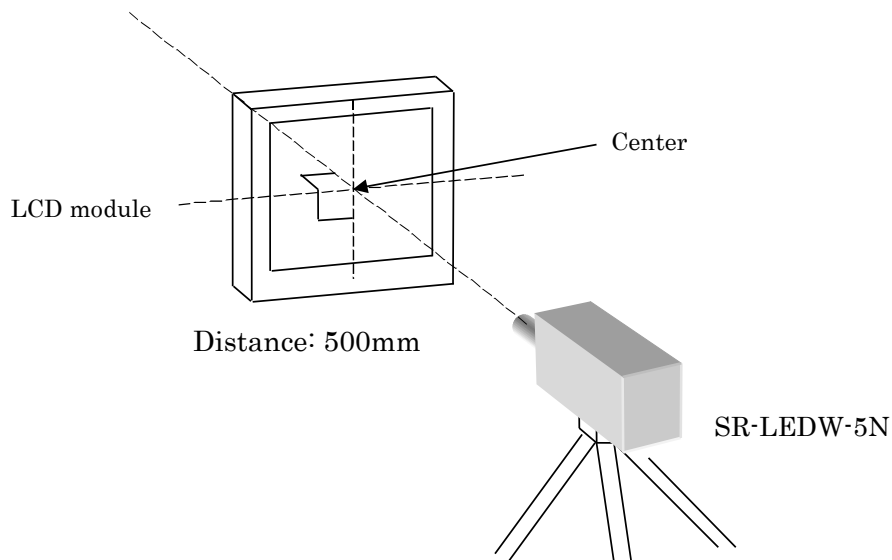


Fig. 1

◆ Method of color measurement (Fig1.)

- (1) Measuring device
SR-LEDW-5N, Measuring Field: 1 °
- (2) Measuring point
Center of display, Vertical direction.

◆ Measuring response time (Fig.2)

- (1) Measuring device
LCD-5200, Measuring Field: 1°
TFT Response program

- (2) Measuring point
Center of display, Vertical direction.

(3) Method of measuring

* Black ↔ White response time

- Input black→white→black to display by switching signal voltage.
- If brightness of black and white are set to 0% and 100%, changing time of optical response from 10% to 90% just after changing signal voltage is defined as "Tr" and from 90% to 10% is "Td".

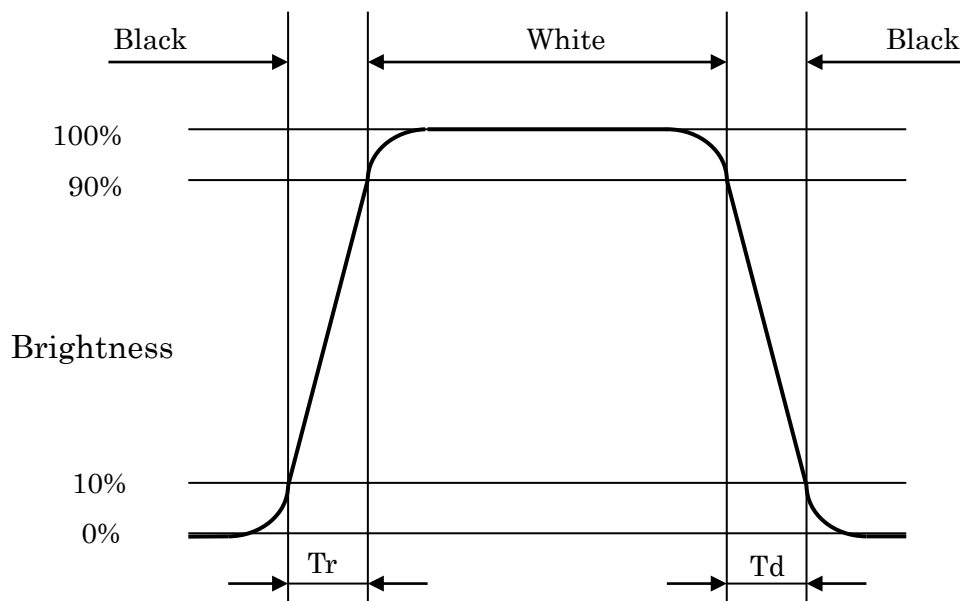


Fig. 2

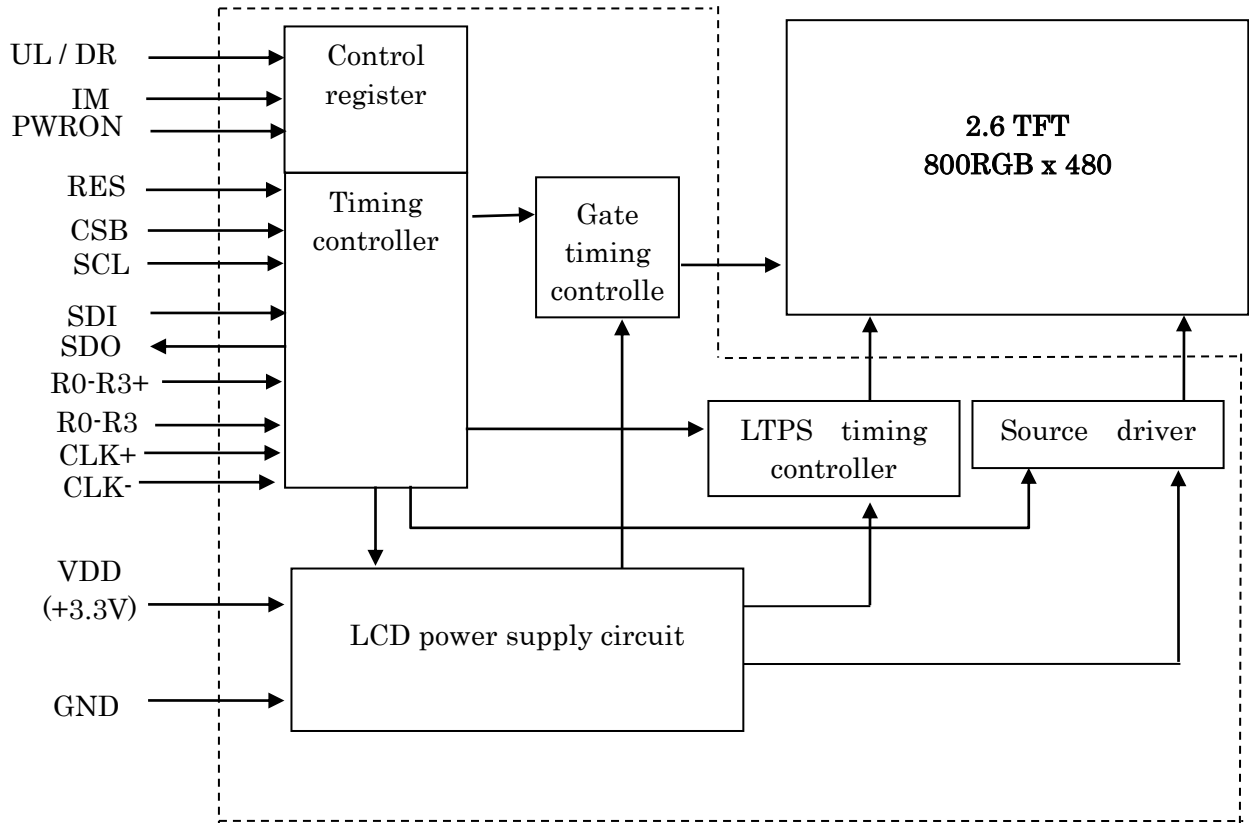
5. I/O terminal

5.1 Pin assignment

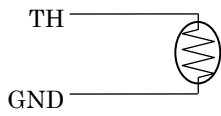
I : input, O : output, P : power

No.	Symbol	Functional Description	I/O
1	GND	0V, GND	P
2	UL / DR	Display flip control input	I
3	IM	6/8 bit (JEIDA Format) IM=L : 6bit, IM=H : 8bit	I
4	SCL	SPI serial clock SPI If the serial interface mode is not used,connect to GND.	I
5	CSB	SPI chip select SPI If the serial interface mode is not used,connect to GND or VDD.	I
6	SDI	Serial data Input If the serial interface mode is not used,connect to GND.	I
7	SDO	Serial data output If the serial interface mode is not used,open.	O
8	GND	0V, GND	P
9	R0-	Data signal 0-	I
10	R0+	Data signal 0+	I
11	GND	0V, GND	P
12	R1-	Data signal 1-	I
13	R1+	Data signal 1+	I
14	GND	0V, GND	P
15	R2-	Data signal 2-	I
16	R2+	Data signal 2+	I
17	GND	0V, GND	P
18	CLK-	Clock signal-	I
19	CLK+	Clock signal+	I
20	GND	0V, GND	P
21	R3-	Data signal 3-	I
22	R3+	Data signal 3+	I
23	GND	0V, GND	P
24	PWRON	Display ON/OFF select PWRON=L : Display ON, PWRON=H : Display OFF	I
25	VDD	Power Supply	P
26	VDD	Power Supply	P
27	VDD	Power Supply	P
28	TH	Thermistor If thermistor is not used, open.	-
29	GND	0V, GND	P
30	RES	Reset input (active L)	I

6. Block diagram



Customer I/F ↔ KYOCERA module



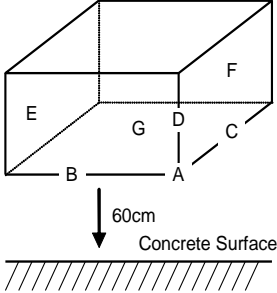
7. Test

No abnormal function and appearance are found after the following tests.

Conditions: Unless otherwise specified, tests will be conducted under the following condition.

Temperature: $20\pm 5^{\circ}\text{C}$ Humidity: $65\pm 5\%\text{RH}$

Tests will be not conducted under operating state.

No.	Parameter	Conditions	Remark
1	High temperature Operating	$105\pm 2^{\circ}\text{C}$, 500 hrs. (Operation state)	
2	Low temperature Operating	$-40\pm 2^{\circ}\text{C}$, 500 hrs. (Operation state)	1
3	High temperature Storage	$105\pm 2^{\circ}\text{C}$, 500 hrs. (Storage)	2
4	Low temperature Storage	$-40\pm 2^{\circ}\text{C}$, 500 hrs. (Storage)	1,2
5	Damp proof test	$60\pm 2^{\circ}\text{C}$, 85~90%RH, 500 hrs. (Operation state)	1,2
6	Heat shock test	$-40\pm 2^{\circ}\text{C} \leftrightarrow 85\pm 2^{\circ}\text{C}$ (30min each), 100cycle	2
7	Vibration test	Total fixed amplitude : 1.5mm Vibration frequency : 10~55Hz Sweep time is 1 minute, X, Y, Z 3 directions for 15 minutes each performed.	3
8	Shock Test	To be measured after dropping from 60cm height on the concrete surface in packing state.  <p>Dropping method corner dropping A corner : once Edge dropping B,C,D edge : once Face dropping E,F,G face : once</p>	

Note1: No dew condensation to be observed.

Note2: The function test shall be conducted after 4 hours storage at the normal temperature and humidity after removed from the test chamber.

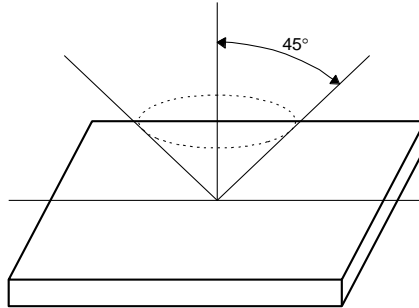
Note3: Vibration test will be conducted to the product itself without putting it in a container.

8. Appearance standards

8.1 Appearance inspection conditions.

The distance between the eyes and the sample shall be 30cm.

All directions for inspecting the sample should be within 45° against perpendicular line.



(a) Operating inspection

Functional operating and appearance inspection are used operating inspection tester.
The inspection environment is under condition of backlight unit of 600 ± 100 cd/m² of Surface of panel.

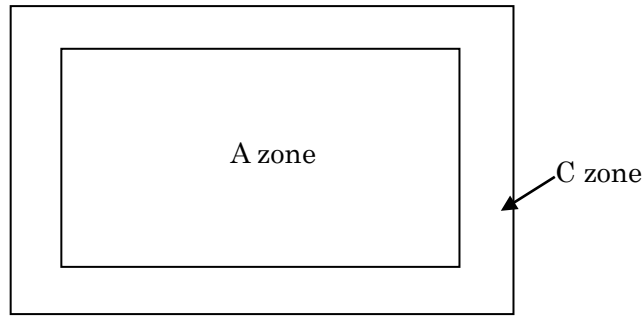
(b) Inspection environment

Functional operating inspection environment is 50 [lx] or less.

(c) Appearance inspection

Environment is under condition of 1000 ± 500 [lx] of surface of LCD.

8.2 Definition of applicable zones



A zone: Active display area
C zone: Rest parts

8.3 Inspection parameter and criteria

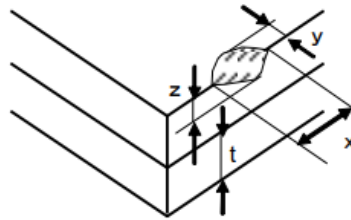
No.	Parameter	Criteria																										
1	G-Line	Not allowed.																										
2	S-Line	Not allowed.																										
3	Leak	Not allowed.																										
4	Bright spot and dark dot	<p>Definition</p> <ul style="list-style-type: none"> •Bright spot: Dot / spot appear bright in black ,red, green and blue display pattern. (Including bright spots caused by foreign material) •Level to be counted as a bright spot shall brighter than the limit sample. (Artificial bright spot BMP data). No count, in case of invisible through ND5% filters at R/G/B pattern. •Dark dot: Sub-pixel appear dark in R/G/B display pattern. <table border="1" style="margin-left: 40px;"> <thead> <tr> <th>Zone</th> <th colspan="3">Acceptable gray level, number</th> </tr> </thead> <tbody> <tr> <td rowspan="4">A</td> <td rowspan="4">Bright spot</td> <td rowspan="4">0</td> <td>W</td> <td>12/63</td> </tr> <tr> <td>R</td> <td>24/63</td> </tr> <tr> <td>G</td> <td>14/63</td> </tr> <tr> <td>B</td> <td>22/63</td> </tr> <tr> <td></td> <td>Dark dot</td> <td colspan="2">3</td> </tr> <tr> <td rowspan="2">C</td> <td>Bright spot</td> <td colspan="2">Disregard</td> </tr> <tr> <td>Dark dot</td> <td colspan="2">Disregard</td> </tr> </tbody> </table> <p>Defect must be away from each other more than 5mm.</p>	Zone	Acceptable gray level, number			A	Bright spot	0	W	12/63	R	24/63	G	14/63	B	22/63		Dark dot	3		C	Bright spot	Disregard		Dark dot	Disregard	
Zone	Acceptable gray level, number																											
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C	Bright spot	Disregard																										
	Dark dot	Disregard																										

No.	Parameter	Criteria																																																
5	Black dot, Round foreign particle, Line foreign particle Others foreign particle	<p>(1) Round shape</p> <table border="1"> <thead> <tr> <th colspan="2">Zone</th> <th colspan="2">Acceptable number</th> </tr> <tr> <th colspan="2">Dimension(mm)</th> <th>A</th> <th>C</th> </tr> </thead> <tbody> <tr> <td colspan="2">D ≤ 0.10</td> <td colspan="2">Disregard</td> </tr> <tr> <td colspan="2">0.10 < D ≤ 0.15</td> <td>2</td> <td rowspan="3">Disregard</td> </tr> <tr> <td colspan="2">0.15 < D ≤ 0.20</td> <td>1</td> </tr> <tr> <td colspan="2">0.20 < D</td> <td>0</td> </tr> </tbody> </table> <p>D = (Long + Short) / 2</p> <p>(2) Line shape</p> <table border="1"> <thead> <tr> <th colspan="2">Zone</th> <th colspan="2">Acceptable number</th> </tr> <tr> <th>L(mm)</th> <th>W(mm)</th> <th>A</th> <th>C</th> </tr> </thead> <tbody> <tr> <td>-</td> <td>W ≤ 0.01</td> <td colspan="2">Disregard</td> </tr> <tr> <td>L ≤ 2.0</td> <td>W ≤ 0.02</td> <td>2</td> <td rowspan="3">Disregard</td> </tr> <tr> <td>L ≤ 1.0</td> <td>W ≤ 0.03</td> <td>1</td> </tr> <tr> <td>L > 2.0</td> <td>-</td> <td>0</td> </tr> <tr> <td>-</td> <td>W > 0.03</td> <td>0</td> <td></td> </tr> </tbody> </table> <p>L : Length W : Width</p> <p>Total defects of (1) and (2) shall not exceed 5.</p>	Zone		Acceptable number		Dimension(mm)		A	C	D ≤ 0.10		Disregard		0.10 < D ≤ 0.15		2	Disregard	0.15 < D ≤ 0.20		1	0.20 < D		0	Zone		Acceptable number		L(mm)	W(mm)	A	C	-	W ≤ 0.01	Disregard		L ≤ 2.0	W ≤ 0.02	2	Disregard	L ≤ 1.0	W ≤ 0.03	1	L > 2.0	-	0	-	W > 0.03	0	
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L ≤ 1.0	W ≤ 0.03	1																																																
L > 2.0	-	0																																																
-	W > 0.03	0																																																
6	Uneven contrast Mura	No object, in case of not visible through ND5% filter.																																																
7	Air bubbles (Between glass and polarizer)	<table border="1"> <thead> <tr> <th colspan="2">Zone</th> <th colspan="2">Acceptable number</th> </tr> <tr> <th colspan="2">Dimension(mm)</th> <th>A</th> <th>C</th> </tr> </thead> <tbody> <tr> <td colspan="2">D ≤ 0.10</td> <td colspan="2">Disregard</td> </tr> <tr> <td colspan="2">0.10 < D ≤ 0.15</td> <td>1</td> <td rowspan="3">Disregard</td> </tr> <tr> <td colspan="2">0.15 < D ≤ 0.20</td> <td>1</td> </tr> <tr> <td colspan="2">0.20 < D</td> <td>0</td> </tr> </tbody> </table>	Zone		Acceptable number		Dimension(mm)		A	C	D ≤ 0.10		Disregard		0.10 < D ≤ 0.15		1	Disregard	0.15 < D ≤ 0.20		1	0.20 < D		0																										
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0.15 < D ≤ 0.20		1																																																
0.20 < D		0																																																
8	Polarizer scratches, dent	No object, in case of not visible through ND5% filter.																																																
9	Polarizer dirt	Stains should be removed easily from LCDP surface.																																																

10 Glass chips

(1) At area except terminal and corner area.

t : glass thickness



(mm)		
X	Y	Z
≤ 5.0	≤ 1.0	≤ t

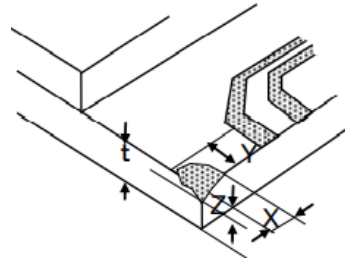
•Rear side is disregarded if the crack don't affect reliability or it's not progressive crack.

•It is disapproval if glass crack reaches sealing area, wiring, terminal, and polarizer.

(2) At corner of glass

•It is disapproval if glass crack reaches wiring and terminal area.

① At terminal area

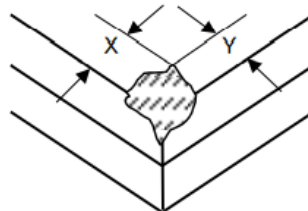


(mm)		
X	X	X
< 1.0	< 1.0	< 1.0

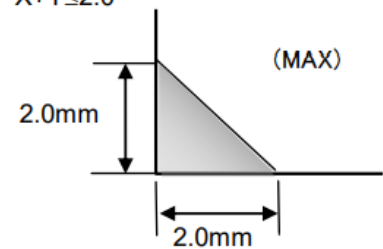
•As for $Z > t$, when it is only one place, it is no object.

•When they are more than two places, $Z \leq 1/2$

② At other area except terminal area



$$X+Y \leq 2.0$$

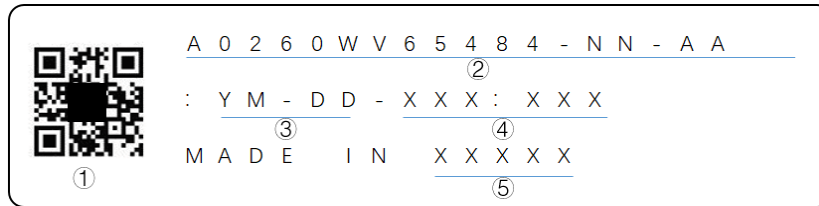


•Not to expose sealing member at glass thickness direction.

•It is disapproval if glass crack reaches polarizer.

9. Lot number identification

The lot number shall be indicated on the FPC of each LCD.



No①. - No⑤. above indicate

- ①Data matrix(For internal control purpose only)
(The item from parts No. to Version No. is included in data matrix.)
- ②Module product name
- ③Manufacturing Date
- ④Version Number
- ⑤Country of origin (Japan or China)

③Manufacturing Date :

Year 0~9,for 2020~2029
 Month 1~9, X~Z, for Jan. ~ Dec.
 Day 01~31,for 1st to 31th

10.Applying precautions

Shall be determined by mutual discuss when questions and new problems not specified in this specification arise.

11. Precautions relating product handling

The Following precautions will guide you in handling our product correctly.

- 1) Liquid crystal display devices
 - (1) The liquid crystal display panel used in the liquid crystal display module is made of plate glass. Avoid any strong mechanical shock. Should the glass break handle it with care.
 - (2) The polarizer adhering to the surface of the LCD is made of a soft material. Guard against scratching it.
- 2) Care of the liquid crystal display module against static electricity discharge.
 - (1) When working with the module, be sure to ground your body and any electrical equipment you may be using. We strongly recommend the use of anti-static mats (made of rubber), to protect worktables against the hazards of electrical shock.
 - (2) Avoid the use of work clothing made of synthetic fibers. We recommend cotton clothing or other conductivity-treated fibers.
 - (3) Slowly and carefully remove the protective film from the LCD module, since this operation can generate static electricity.
- 3) When the LCD module must be stored for long periods of time.
 - (1) Protect the modules from high temperature and humidity.

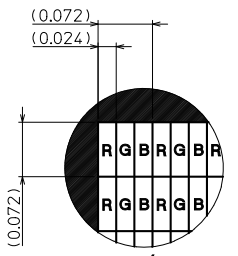
"Recommended storage conditions"

Temperature : 15~25°C
Humidity : 60~70%RH
No dew condensation to be observed.
 - (2) Keep the modules out of direct sunlight or direct exposure to ultraviolet rays.
 - (3) Protect the modules from excessive external forces.
- 4) Use the module with a power supply that is equipped with an overcurrent protector circuit, since the module is not provided with this protective feature.
- 5) Do not ingest the LC fluid itself should it leak out of a damaged LCD module. Should hands or clothing come in contact with LC fluid, wash immediately with soap.
- 6) Conductivity is not guaranteed for models that use metal holders where solder connections between the metal holder and the PCB are not used. Please contact us to discuss appropriate ways to assure conductivity.
- 7) For models which use touch panels:
 - (1) Do not stack up modules since they can be damaged by components on neighboring modules.
 - (2) Do not place heavy objects on top of the product. This could cause glass breakage.
- 8) For models which use COG, TAB, or COF:
 - (1) The mechanical strength of the product is low since the IC chip faces out unprotected from the rear. Be sure to protect the rear of the IC chip from external forces.
 - (2) Given the fact that the rear of the IC chip is left exposed, in order to protect the unit from electrical damage, avoid installation configurations in which the rear of the IC chip runs the risk of making any electrical contact.
- 9) Models which use flexible cable, heat seal, or TAB:
 - (1) In order to maintain reliability, do not touch or hold by the connector area.
 - (2) Avoid any bending, pulling, or other excessive force, which can result in broken connections.

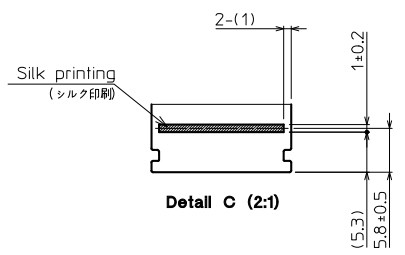
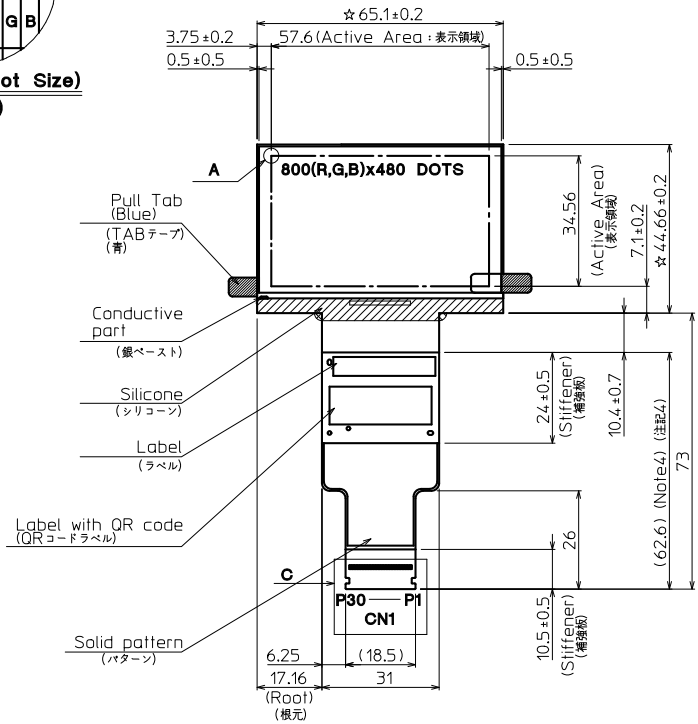
Spec No. Q-DS-1-S109-00	Part No. A0260WV65484-NN-AA	Page 29
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- 10) In case of buffer material such as cushion / gasket is assembled into LCD module, it may have an adverse effect on connecting parts (LCD panel-TCP / HEAT SEAL / FPC / etc., PCB-TCP / HEAT SEAL / FPC etc., TCP-HEAT SEAL, TCP-FPC, HEAT SEAL-FPC,etc.) depending on its materials.
Please check and evaluate these materials carefully before use.
- 11) In case of acrylic plate is attached to front side of LCD panel, cloudiness (very small cracks) can occur on acrylic plate, being influenced by some components generated from polarizer film.
Please check and evaluate those acrylic materials carefully before use.
- 12) Flickering due to optical interference may occur by combination of LCD driving frame frequency decided by either internal oscillator in driver IC or external clock input by the customer and lighting frequency of either backlight or other light sources.
Please evaluate enough at the environment of actual use, and decide the driving condition that does not cause flickering.
- 13) Please be advised that do not apply DC voltage to the LCD.
If DC voltage is applied to the LCD, then it may cause poor display quality.
- 14) About disposal: Please dispose of the product following to rule and regulation in that land, region, country and area.

No	Description	Drawn	Checked	Checked	Approved
△	FPC外形修正	'24.06.19 黄俊諭	'24.06.19 李威		'24.06.20 李威



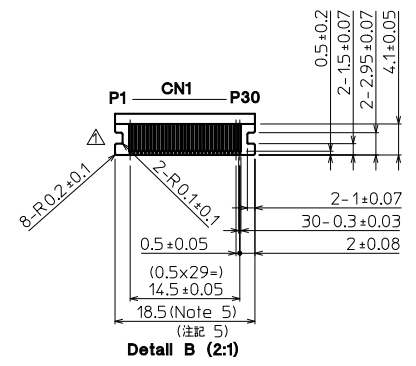
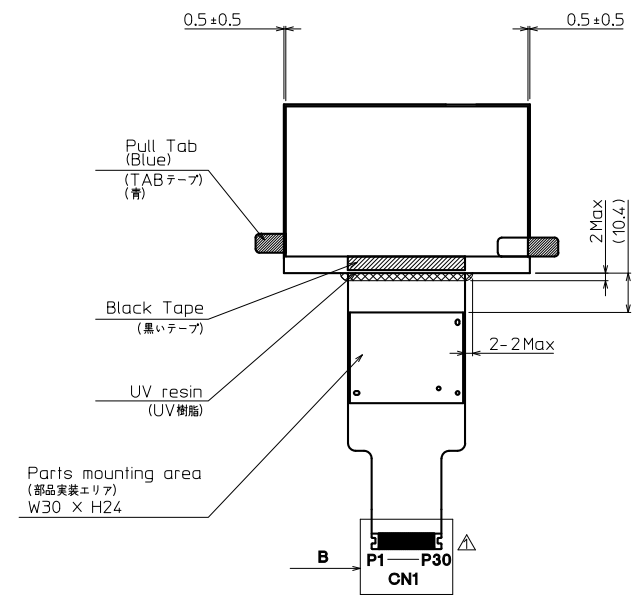
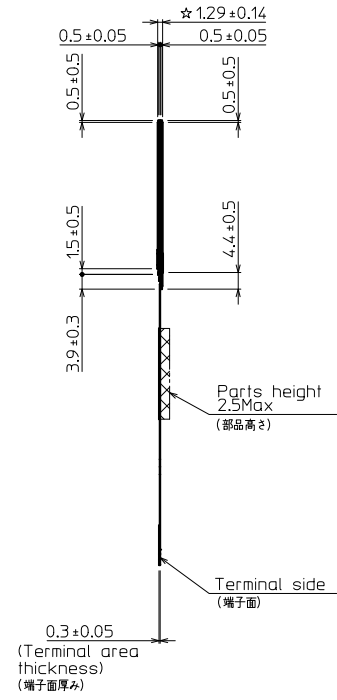
DETAIL A (Dot Size)
(NTS)



Detail C (2:1)

Notes (注記)

- The dimensions with the mark (☆) are controlled as a important characteristic. (☆マーク付ける寸法を重要管理寸法とする.)
- The area of shows silicone coating.(MAX.) The silicone should not protrude from the edge of LCDP. And the total thickness with silicone should not exceed maximum module thickness. (このシリコン塗布エリアとする (MAX)) (シリコンはLCDP端からはみ出さ無きこと.) (シリコン厚みはモジュール一番高いエリアを超え無きこと.)
- Cross-Hatched area shows maximum area of UV resin. (ハッチングエリアはUV樹脂の最大面積とする)
- FPC bending prohibition area is shown. (FPC折り曲げ禁止エリアとする)
- Tolerance(公差)
Terminal area(端子面エリア):±0.07
The others(その他):±0.3
- Outside of Active Area apply to C zone of appearance standard. (アクティブエリア以外はCゾーン検査規格に適用すること.)



Detail B (2:1)

Ref(参考)
Mating Connector(適合コネクタ):
EVAFLEX5-SE 30Pin (DAI-ICHI SEIKO)

TOLERANCE(公差)			
MEASURE(量尺)	A	B	C
L≤16	±0.1	±0.3	±1
16<L≤63	±0.2	±0.5	±1.5
63<L≤250	±0.3	±0.8	±2
250<L≤500	±0.5	±1.2	±3
500<L	±0.8	±2	±4
ANGLE	±5°	±5°	±10°

Material 材質	Treatment 処理	Approved '24.04.24	Checked '24.04.22	Checked '24.04.22	Drawn 黄俊諭	Scale 1:1(2:1,NTS)	Title 365484AA	KYOCERA	Year-Month-Day '24.01.17	Size 2
Quantity 製作数	Description 備考	李威	鄭海銘				Outline Dimensions	Drawing No. 121A9035300-1		