

产品规格书

Product Specification

Model Name (产品名称)		TFT-LCD Module	
Part Number (产品型号)		HY0320GL43-S100	
Item (项目)	Prepared (拟制)	Checked (审核)	Approved (批准)
Signature (签名)			
Date (日期)			
Note (备注)			
Customer: (客户)			
		Signature (签名)	
		Date (日期)	

Revision Record

Version	Issued Date	Page	Old Description	New Description
01	2021-11-22	\	Initial release	\

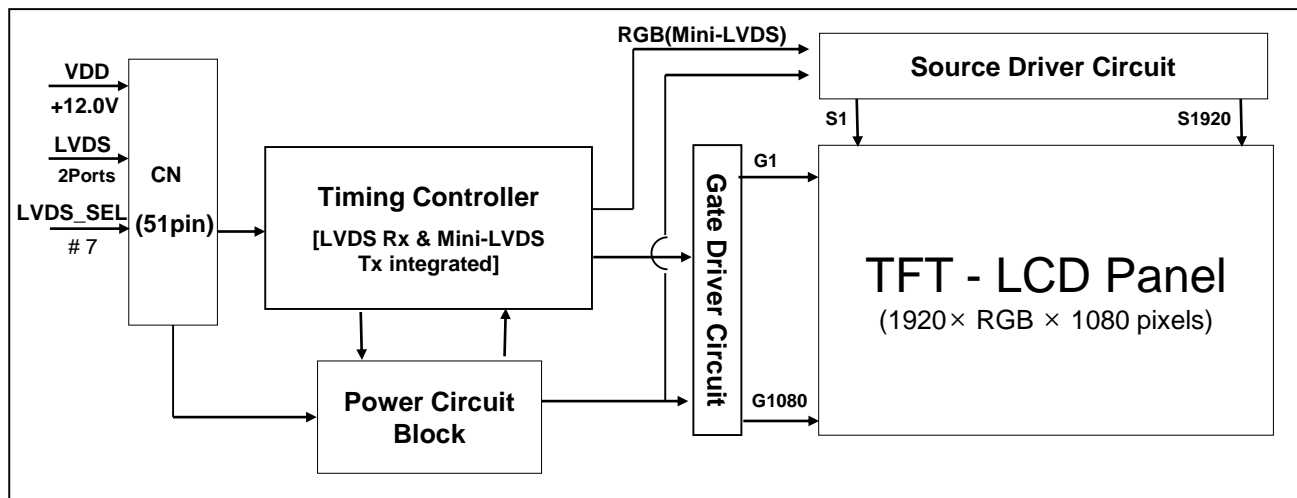
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1.0 GENERAL DESCRIPTION

1.1 Introduction

HY0320GL43 is a color active matrix TFT LCD open cell using amorphous silicon TFT's (Thin Film Transistors) as an active switching devices. This open cell has a 31.51 inch diagonally measured active area with FHD resolutions (1920 horizontal by 1080 vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical stripe and this open cell can display 16.7M colors. The TFT-LCD panel used for this open cell is adapted for a low reflection and higher color type.



1.2 Features

- LVDS interface with 2 pixel / clock
- High-speed response
- Low color shift image quality
- 8-bit color depth, display 16.7M colors
- High luminance and contrast ratio, low reflection and wide viewing angle
- DE (Data Enable) only mode
- ADSDS technology is applied for high display quality
- RoHS compliant

1.3 Application

- Commercial Digital Display
- Display Terminals for Control System
- Landscape and Portrait Display

1.4 General Specification

< Table 1. General Specifications >

Parameter		Specification	Unit	Remark
Active area		698.4(H) × 392.85 (V)	mm	
Number of pixels		1920(H) × 1080(V)	pixels	
Overall dimensions		725.2(H)*422.7(V)*18.4(D)	mm	
Pixel arrangement		Pixels RGB Vertical stripe		
Display colors		16.7M(8bits-true)	colors	
Display mode		Transmission mode, Normally Black		
Open Cell Transmittance			%	
Weight		TBD	gram	
Brightness		1000	cd/m ²	Typ.
Temperature	Operating	0~50	°C	
	Storage	0~50		
Surface Treatment		Haze 1% , 3H, Anti-Glare Layer(for Front) , Clear(for Rear)		

2.0 ABSOLUTE MAXIMUM RATINGS

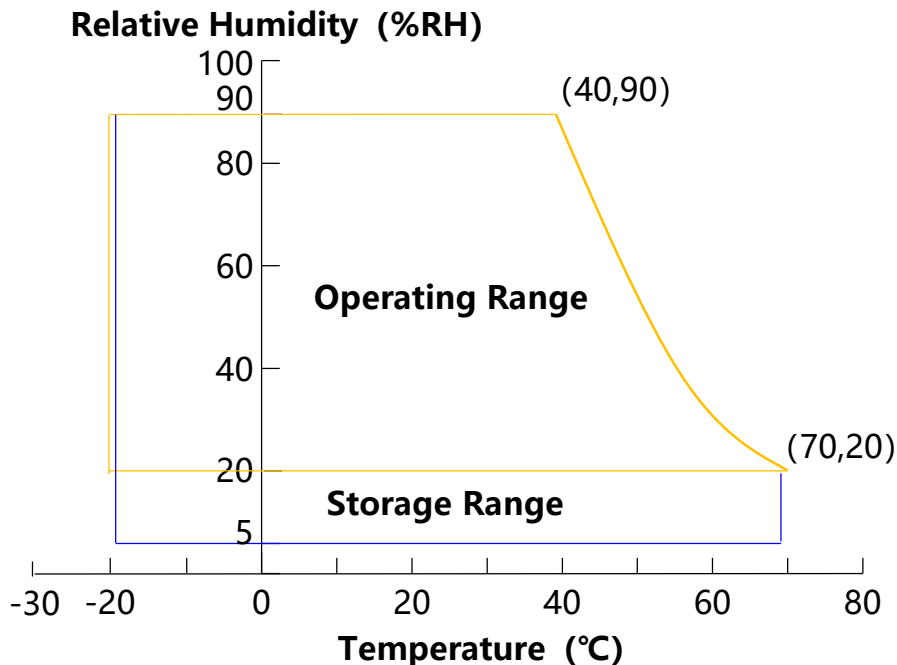
The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit. The operational and non-operational maximum voltage and current values are listed in Table 2.

< Table 2. Open Cell Electrical Specifications >

[VSS=GND=0V]

Parameter	Symbol	Min.	Max.	Unit	Remark
Power Supply Voltage	VDD	VSS-0.3	14	V	Ta = 25 °C
Operating Temperature	T _{OP}	-0	+50	°C	Note 1
	T _{SUR}	-0	+50	°C	
Storage Temperature	T _{ST}	-0	+60	°C	
Operating Ambient Humidity	Hop	10	80	%RH	
Storage Humidity	Hst	10	80	%RH	

Note 1 : Temperature and relative humidity range are shown in the figure below.
Wet bulb temperature should be 39 °C max. and no condensation of water.



3.0 ELECTRICAL SPECIFICATIONS

3.1 TFT LCD Open Cell

< Table 3. Open Cell Electrical Specifications >

[Ta =25±2 °C]

Parameter		Symbol	Values			Unit	Remark
			Min	Typ	Max		
Power Supply Input Voltage		VDD	10.8	12	14	Vdc	
Power Supply Ripple Voltage		VRP			300	mV	
Power Supply Current		IDD	-	333	630	mA	Note 1
Power Consumption		PDD		4.0	7.6	Watt	
Rush current		IRUSH	-	-	3.3	A	Note 2
LVDS Interface	LVDS Swing Voltage	VID	±100		±300	mV	Note 3
	Common Input Voltage	VLVC	1.0	1.2	1.4	V	
CMOS Interface	Input High Threshold Voltage	VIH	2.7	-	3.3	V	
	Input Low Threshold Voltage	VIL	0	-	0.6	V	

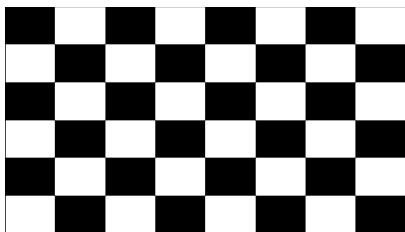
Note 1 : The supply voltage is measured and specified at the interface connector of LCM.

The current draw and power consumption specified is for VDD=12.0V,

Frame rate $f_v=60\text{Hz}$ and Clock frequency = 75.4MHz.

Test Pattern of power supply current

a) Typ : Mosaic 8 x 6 Pattern(L0/L255)
Pattern(L0/L255)



b) Max : H- Stripe

R	G	B	R	G	B
R	G	B	R	G	B
R	G	B	R	G	B
R	G	B	R	G	B

Note 2 : The duration of rush current is about 2ms and rising time of Power Input is 1ms(min)

Note 3 : The LVDS test point is at each terminal resistor

4.0 INTERFACE CONNECTION

4.1 Module Input Signal & Power

- Connector : IS050-C51B-C39-S (UJU) / FI-RE51S-HF-R1500 (JAE) or Equivalent.

< Table 4. Open Cell Input Connector Pin Configuration >

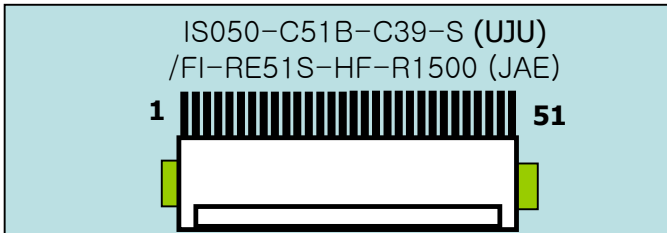
Pin No	Symbol	Description	Pin No	Symbol	Description
1	NC	No Connection	21	GND	Ground
2	SDA	I ² C Data	22	CH1[3]-	First pixel negative LVDS differential data input. Pair3
3	SCL	I ² C Clock	23	CH1[3]+	First pixel positive LVDS differential data input. Pair3
4	NC	Not Connected	24	NC	Not Connected
5	NC	Not Connected	25	NC	Not Connected
6	NC	Not Connected	26	NC or GND	Not Connected
7	SELLVDS	High: JEIDA Low or Open: VESA	27	NC	Not Connected
8	NC	Not Connected	28	CH2[0]-	Second pixel negative LVDS differential data input. Pair0
9	NC	Not Connected	29	CH2[0]+	Second pixel positive LVDS differential data input. Pair0
10	NC	Not Connected	30	CH2[1]-	Second pixel negative LVDS differential data input. Pair1
11	GND	Ground	31	CH2[1]+	Second pixel positive LVDS differential data input. Pair1
12	CH1[0]-	First pixel negative LVDS differential data input. Pair0	32	CH2[2]-	Second pixel negative LVDS differential data input. Pair2
13	CH1[0]+	First pixel positive LVDS differential data input. Pair0	33	CH2[2]+	Second pixel positive LVDS differential data input. Pair2
14	CH1[1]-	First pixel negative LVDS differential data input. Pair1	34	GND	Ground
15	CH1[1]+	First pixel positive LVDS differential data input. Pair1	35	CH2CLK-	Second pixel negative LVDS clock
16	CH1[2]-	First pixel negative LVDS differential data input. Pair2	36	CH2CLK+	Second pixel positive LVDS clock
17	CH1[2]+	First pixel positive LVDS differential data input. Pair2	37	GND	Ground
18	GND	Ground	38	CH2[3]-	Second pixel negative LVDS differential data input. Pair3
19	CH1CLK-	First pixel negative LVDS clock	39	CH2[3]+	Second pixel positive LVDS differential data input. Pair3
20	CH1CLK+	First pixel positive LVDS clock			

Product Specification

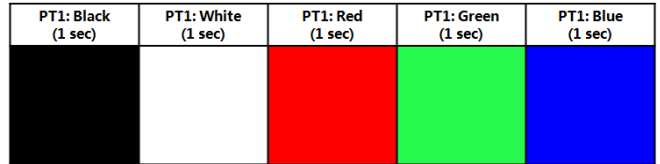
Pin No	Symbol	Description	Pin No	Symbol	Description
40	NC	Not Connected	46	GND	Ground
41	NC	Not Connected	47	NC	Not Connected
42	NC or GND	Not Connected	48	VCC	Input Voltage +12V
43	NC or GND	Not Connected	49	VCC	Input Voltage +12V
44	NC or GND	Ground	50	VCC	Input Voltage +12V
45	GND	Ground	51	VCC	Input Voltage +12V

- Notes :
1. NC(Not Connected) : This pins are only used for BOE internal operations.
 2. Input Level of LVDS signal is based on the IEA 664 Standard.
 3. LVDS_SEL : This pin is used for selecting LVDS signal data format.
 If this Pin : High (3.3V) → JEIDA LVDS format
 Otherwise : Low (GND) or Open (NC) → Normal NS LVDS format

Rear view of LCM



BIST Pattern



4.2 LVDS Interface

- LVDS Receiver : Timing Controller (LVDS Rx merged) / LVDS Data : Pixel Data

< Table 5. Open Cell Input Connector Pin Configuration >

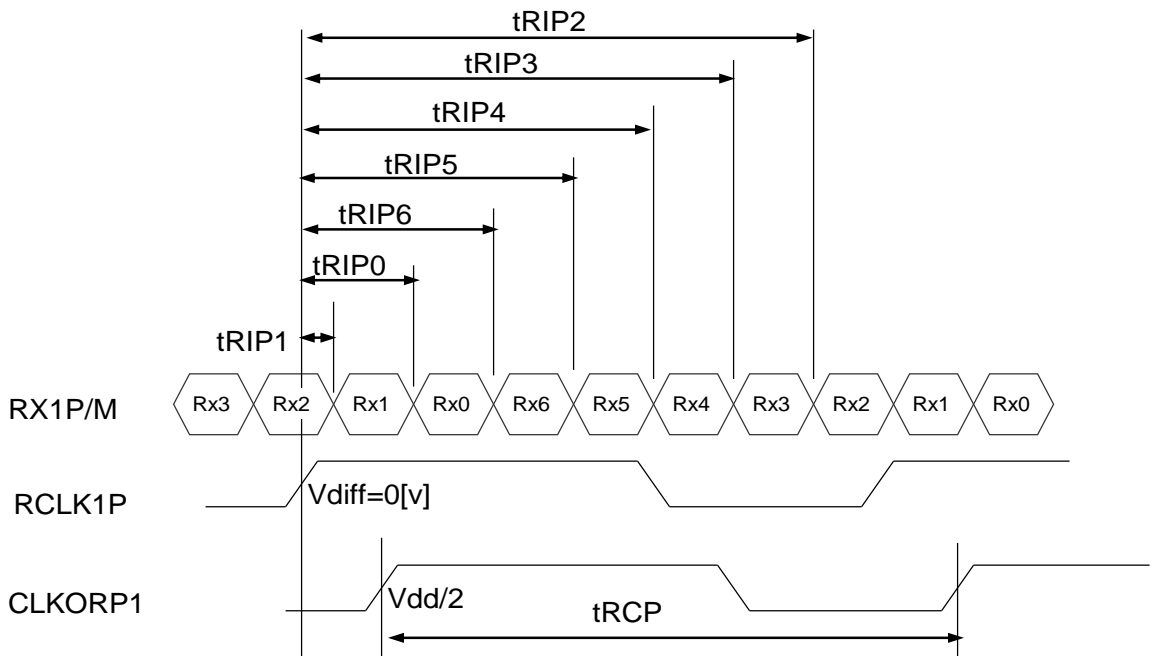
Channel No.	Data No.	8-bit LVDS Type	
		NS	JEIDA
0	Bit-0	R0	R2
	Bit-1	R1	R3
	Bit-2	R2	R4
	Bit-3	R3	R5
	Bit-4	R4	R6
	Bit-5	R5	R7
	Bit-6	G0	G2
1	Bit-0	G1	G3
	Bit-1	G2	G4
	Bit-2	G3	G5
	Bit-3	G4	G6
	Bit-4	G5	G7
	Bit-5	B0	B2
	Bit-6	B1	B3
2	Bit-0	B2	B4
	Bit-1	B3	B5
	Bit-2	B4	B6
	Bit-3	B5	B7
	Bit-4	HS	HS
	Bit-5	VS	VS
	Bit-6	DE	DE
3	Bit-0	R6	R0
	Bit-1	R7	R1
	Bit-2	G6	G0
	Bit-3	G7	G1
	Bit-4	B6	B0
	Bit-5	B7	B1
	Bit-6	-	

4.3 LVDS Rx Interface Timing Parameter

The specification of the LVDS Rx interface timing parameter is shown in Table 6.

<Table 6. LVDS Rx Interface Timing Specification>

Item	Symbol	Min	Typ	Max	Unit	Remark
CLKIN Period	tRCP	9.09	T	25	nsec	
Receiver Data Input Margin	tRMG	-0.40	-	0.40	nsec	fCLKIN=65MHz
Input Data 0	tRIP1	- tRMG	0.0	tRMG	Clock	
Input Data 1	tRIP0	T/7- tRMG	T/7	T/7+ tRMG	Clock	
Input Data 2	tRIP6	2 T/7- tRMG	2T/7	2T/7+ tRMG	Clock	
Input Data 3	tRIP5	3T/7- tRMG	3T/7	3T/7+ tRMG	Clock	
Input Data 4	tRIP4	4T/7- tRMG	4T/7	4T/7+ tRMG	Clock	
Input Data 5	tRIP3	5T/7- tRMG	5T/7	5T/7+ tRMG	Clock	
Input Data 6	tRIP2	6T/7- tRMG	6T/7	6T/7+ tRMG	Clock	

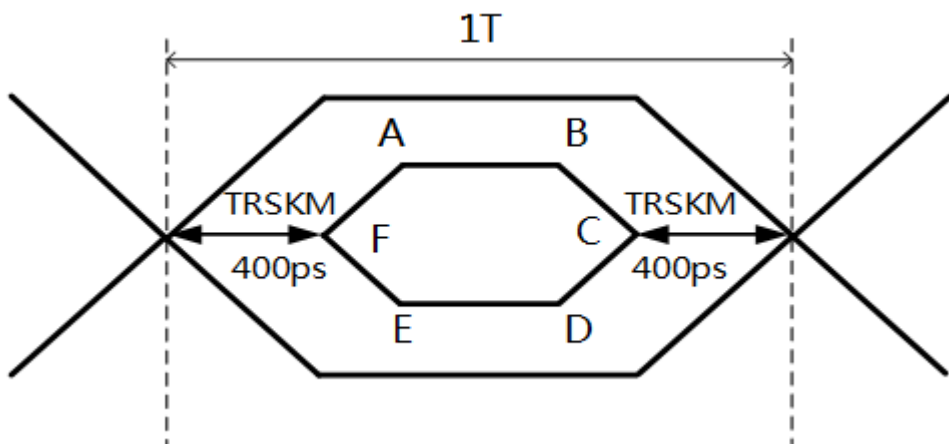


* Vdiff = (RXz+)-(RXz-),.... ,(RXCLK+)-(RXCLK-)

4.4 LVDS Rx Interface Eye Diagram

< Table 7. LVDS Rx Interface Eye Diagram >

Symbol	Min	Typ	Max	Unit	Note
A	—	100	—	mV	
B	—	100	—	mV	
C	—	0	—	mV	
D	—	-100	—	mV	
E	—	-100	—	mV	
F	—	0	—	mV	



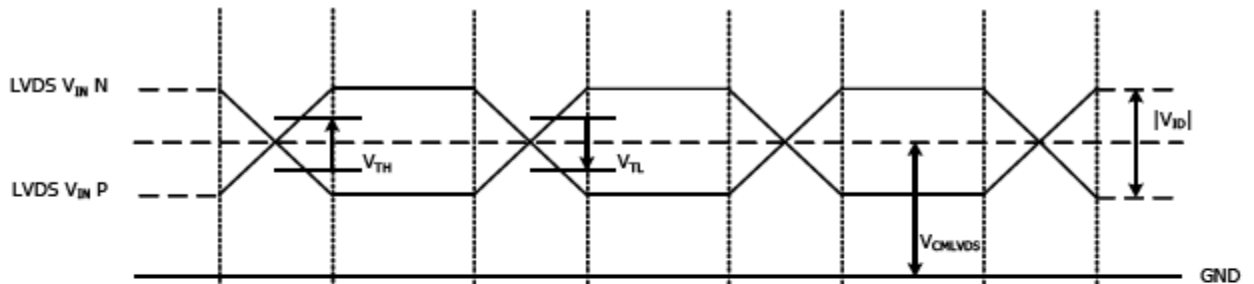
- Notes: 1. Time F to A, B to C, C to D, E to F is 150p second.
 2. LVDS clock=85Mhz.
 3. The time A to B= $1T-2*TRSKM-2*150ps$.

4.5 LVDS Receiver Differential Input

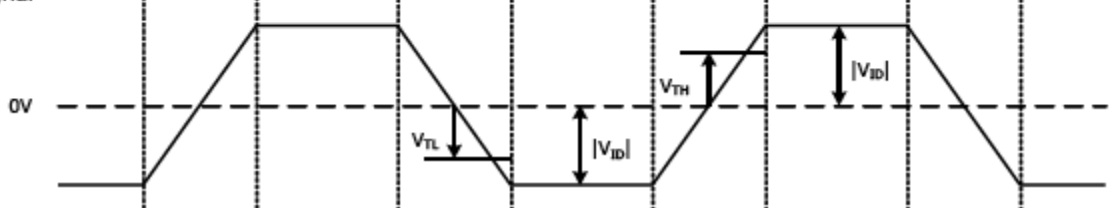
< Table 7-1. LVDS Receiver Differential Input >

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
LVDS Input High Threshold	V_{TH}	$V_{CMLVDS} = 1.2V$			+100	mV
LVDS Input Low Threshold	V_{TL}	$V_{CMLVDS} = 1.2V$	-100			mV
Single-End Input Voltage Range	V_{IN}		0		V_{CC_LVDS}	V
LVDS Input Common Mode Voltage	V_{CMLVDS}			1.2	$V_{CC_LVDS} - 0.4 \cdot V_{ID} / 2$	V
Differential Input Voltage	$ V_{ID} $		100		600	mV
Input Leakage Current	I_N		-10		+10	μA

Single-End



Differential Signal



5.0 SIGNAL TIMING SPECIFICATION

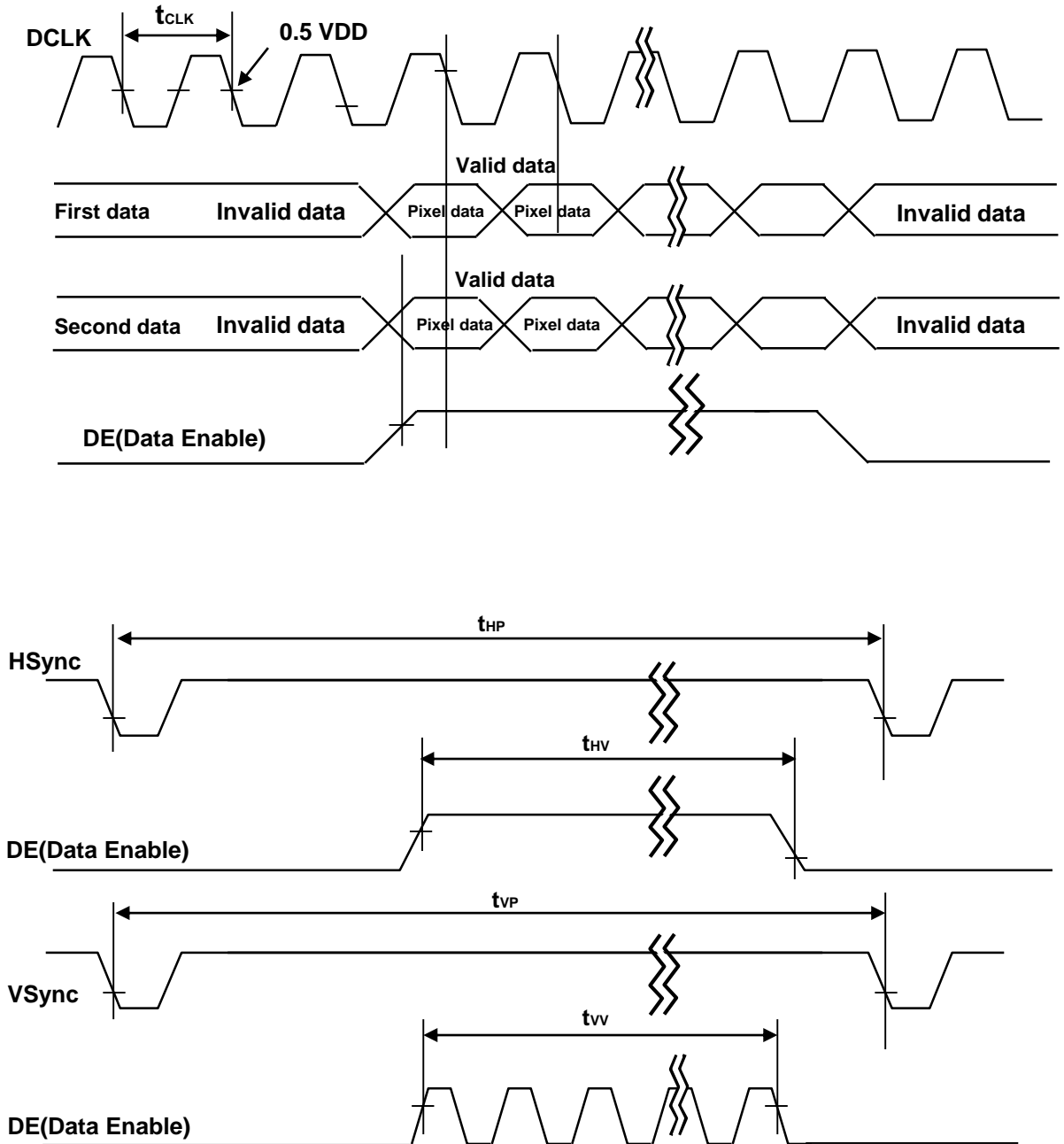
5.1 Timing Parameters (DE only mode)

< Table 8. Timing Table >

Item		Symbols	Min	Typ	Max	Unit	
Clock	Frequency	1/Tc	60	74.25 (92.8)	78	MHz	
	High Time	Tch	-	4/7Tc	-		
	Low Time	Tcl	-	3/7Tc	-		
Frame Period		Tv	1100	1125	1149	lines	
			48.5	60	63	Hz	
Horizontal Active Display Term		Valid	t _{HV}	-	960	-	t _{CLK}
		Total	t _{HP}	1060	1100	1200	t _{CLK}
Vertical Active Display Term		Valid	t _{VV}	-	1080	-	t _{HP}
		Total	t _{VP}	1100	1125	1149	t _{HP}

Notes: This product is DE only mode. The input of Hsync & Vsync signal does not have an effect on normal operation.

5.2 Signal Timing Waveform



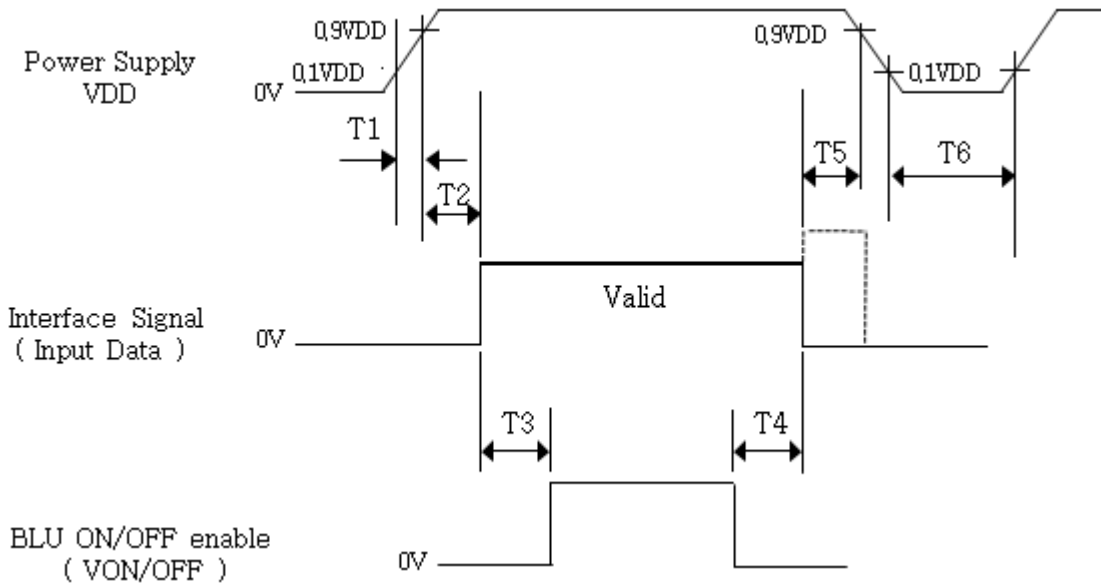
5.3 Input Signals, Basic Display Colors and Gray Scale of Colors

< Table 9. Input Signal and Display Color Table >

Color & Gray Scale		Input Data Signal																							
		Red Data								Green Data						Blue Data									
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale of Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	↑								↑						↑									
	▽	↓								↓						↓									
	Brighter	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	▽	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale of Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Darker	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	△	↑								↑						↑									
	▽	↓								↓						↓									
	Brighter	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	▽	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale of Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Darker	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	△	↑								↑						↑									
	▽	↓								↓						↓									
	Brighter	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	▽	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Gray Scale of White	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	△	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	
	Darker	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0
	△	↑								↑						↑									
	▽	↓								↓						↓									
	Brighter	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1
	▽	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

5.4 Power Sequence

To prevent a latch-up or DC operation of the Open Cell, the power on/off sequence shall be as shown in below



< Table 10. Sequence Table >

Parameter	Values			Units
	Min	Typ	Max	
T1	0.5	-	20	ms
T2	10	-	-	ms
T3	200	-	-	ms
T4	100	-	-	ms
T5	0	-	-	ms
T6	1	-	-	s

- Notes: 1. Back Light must be turn on after power for logic and interface signal are valid.
 2. Even though T1 is out of SPEC, it is still ok if the inrush current of VDD is below the limit.

5.5 Backlight Specification

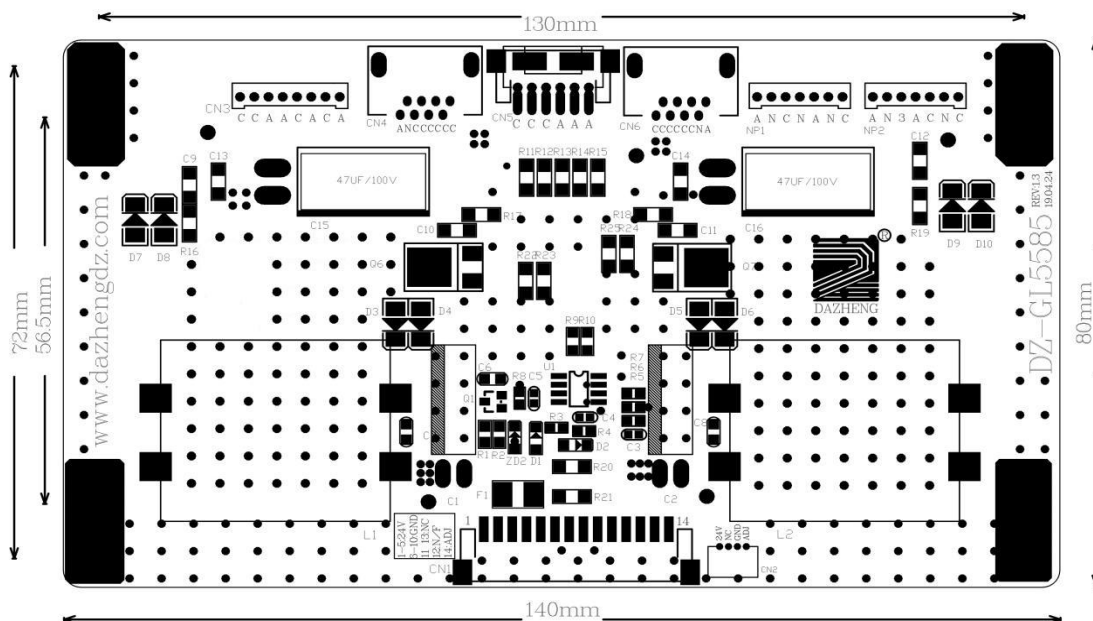
Parameter		Symbol	Values			Unit	notes		
			Min	Typ	Max				
LED Driver :									
Power Supply Input Voltage		VBL	23.8	24.0	24.8	Vdc	1		
Power Supply Input Current		IBL	-	2.1		A	1		
Power Supply Input Current (In-Rush)		In-rush	-	-	(TBD)	A	$V_{BL} = 12.0V$ $ExtV_{BR-B} = 100\%$ 3		
Power Consumption		PBL	-	51	50	W	1		
Input Voltage for Control System Signals	On/Off	On	V on	2.5	-	5.5	Vdc	On Duty 5	
		Off	V off	-0.3	0.0	0.5	Vdc		
	Brightness Adjust		$ExtV_{BR-B}$		30	-	100		%
					30	-	100		%
	$ExtV_{BR-B}$ Frequency		f_{PWM}		500	-	1500		Hz
	Pulse Duty Level (PWM)		High Level		2.5	-	5.5		Vdc
Low Level				0.0	-	0.5	Vdc		
LED :									
Life Time				30,000	50,000		Hrs	2	

notes :

1. Electrical characteristics are determined after the unit has been 'ON' and stable for approximately 60 minutes at $25 \pm 2^\circ C$. The specified current and power consumption are under the typical supply Input voltage 12V and V_{BR} ($ExtV_{BR-B} : 100\%$), it is total power consumption.
2. The life time (MTTF) is determined as the time which luminance of the LED is 50% compared to that of initial value at the typical LED current ($ExtV_{BR-B} : 100\%$) on condition of continuous operating in LCM state at $25 \pm 2^\circ C$.
3. The duration of rush current is about 200ms. This duration is applied to LED on time.
4. Even though inrush current is over the specified value, there is no problem if I²T spec of fuse is satisfied. $ExtV_{BR-B}$ signal have to input available duty range and sequence.
5. After Driver ON signal is applied, $ExtV_{BR-B}$ should be sustained from 30% to 100% more than 500ms. After that, $ExtV_{BR-B}$ 30% and 100% is possible

3.3 Specification of LED driver Board

(1) Dimension of P.C.B. / PCB 机械尺寸：长 140mm、宽 80mm、高 11mm
 Unit/单位：mm Tolerance/公差：±0.5mm



Input connector /输入插座: CN1			
Pin No. 引脚	Symbol 符号	Description/ 描述	Parameter /参数
1、2、3、4、5	+24V	Supply voltage/供电	23.5~25V
6、7、8、9、10	GND	Ground/接地	0V
14	DIM 0V	Dimming control/亮度控制 (有感光控制功能时此引脚不接输入线)	0V=Brightness Max 亮度最大 5V=Brightness Min 亮度最小
12	N/F	Standby/Operation/开关控制	On =2—5.0V Off =0-0.5V
11、13	NC	-	空

6.0 OPTICAL SPECIFICATIONS

The test of optical specifications shall be measured in a dark room (ambient luminance ≤ 1 lux and temperature $= 25 \pm 2^\circ\text{C}$) with the equipment of Luminance meter system (Goniometer system and PR730) and test unit shall be located at an approximate distance 50cm from the LCD surface at a viewing angle of θ and Φ equal to 0° . We refer to $\theta_{\varnothing=0}$ ($=\theta_3$) as the 3 o'clock direction (the "right"), $\theta_{\varnothing=90}$ ($=\theta_{12}$) as the 12 o'clock direction ("upward"), $\theta_{\varnothing=180}$ ($=\theta_9$) as the 9 o'clock direction ("left") and $\theta_{\varnothing=270}$ ($=\theta_6$) as the 6 o'clock direction ("bottom"). While scanning θ and/or \varnothing , the center of the measuring spot on the Display surface shall stay fixed. The measurement shall be executed after 30 minutes warm-up period. VDD shall be 1.2.0V +/-10% at 25°C . Optimum viewing angle direction is 6 'clock.

< Table 11. Optical Table >

[VDD = 12.0V, Frame rate = 60Hz, Ta = $25 \pm 2^\circ\text{C}$]

Parameter		Symbol	Condition	Min	Typ	Max	Unit	Remark
Viewing Angle	Horizontal	Θ_3	CR > 10		89		Deg.	Note 1
		Θ_9			89		Deg.	
	Vertical	Θ_{12}			89		Deg.	
		Θ_6			89		Deg.	
Contrast ratio		CR		900:1	1200:1	-		Note 2
Reproduction of color	White	W_x	$\Theta = 0^\circ$ (Center) Normal Viewing Angle	TYP. - 0.03	0.269	TYP. + 0.03		Note 3 (With BOE BLU)
		W_y			0.271			
	Red	R_x			0.620			
		R_y			0.346			
	Green	G_x			0.318			
		G_y			0.634			
	Blue	B_x			0.154			
		B_y			0.037			
Response Time	G to G	T_g		-	8	10	ms	Note 4
Gamma Scale				2.0	2.2	2.4		
Cell Transmittance					5.0		%	Note 5
Brightness				1000	800	-	cd/m ²	

Note :

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface.
2. Contrast measurements shall be made at viewing angle of $\theta=0^\circ$ and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state. (See Figure 1 shown in Appendix) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. The color chromaticity coordinates specified in Table 9 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel. The BLU is used by BOE.
4. Response time Tg is the average time required for display transition by switching the input signal as below table and is based on Frame rate fV =60Hz to optimize. Each time in below table is defined as Figure 2 and shall be measured by switching the

Measured Response Time	Target																	
	0	15	31	47	63	79	95	111	127	143	159	175	191	207	223	239	255	
Start	0																	
	15																	
	31																	
	47																	
	63																	
	79																	
	95																	
	111																	
	127																	
	143																	
	159																	
	175																	
	191																	
	207																	
	223																	
	239																	
255																		

5. Definition of Transmittance (T%) :

Module is with white(L255) signal input

$$\text{Transmittance} = \frac{\text{Luminance of LCD Module}}{\text{Luminance of BLU}} \times 100 \%$$

8.0 Reliability Test Condition

< Table 13. Reliability Test Condition >

Item	Test Condition
High-Temp/STG	Ta = 60 °C, 240 hrs
Low-Temp/STG	Ta = -20 °C, 240 hrs
High-Temp/HMD	Ta = 50 °C, 80%RH, 240hrs
High-Temp/OP	Ta = 50 °C, 240hrs
Low-Temp/OP	Ta = 0 °C, 240hrs
TST	Ta = -20 °C ↔ 60 °C (0.5 hr), 100 cycle

9.0 PRODCUT SERIAL NUMBER

TBD

10.0 PACKING INFORMATION

TBD

10.1 Packing Order

TBD

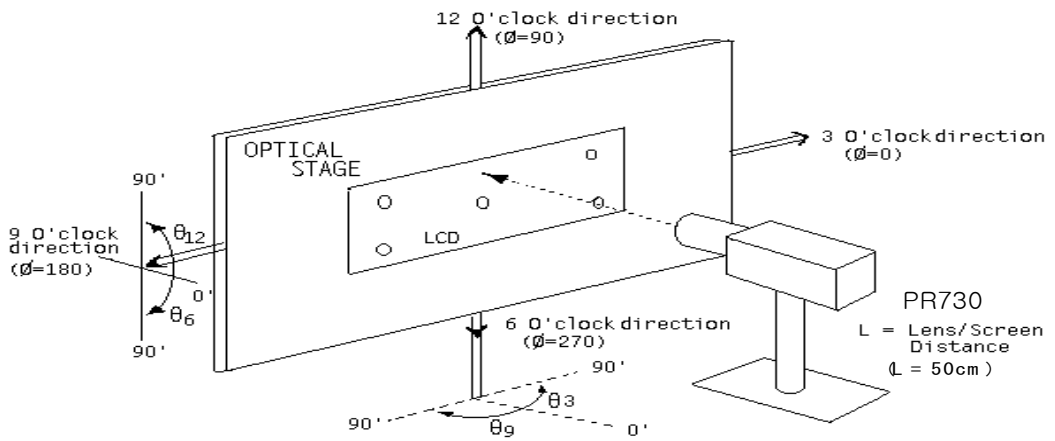
11.0 HANDLING & CAUTIONS

CAUTIONS

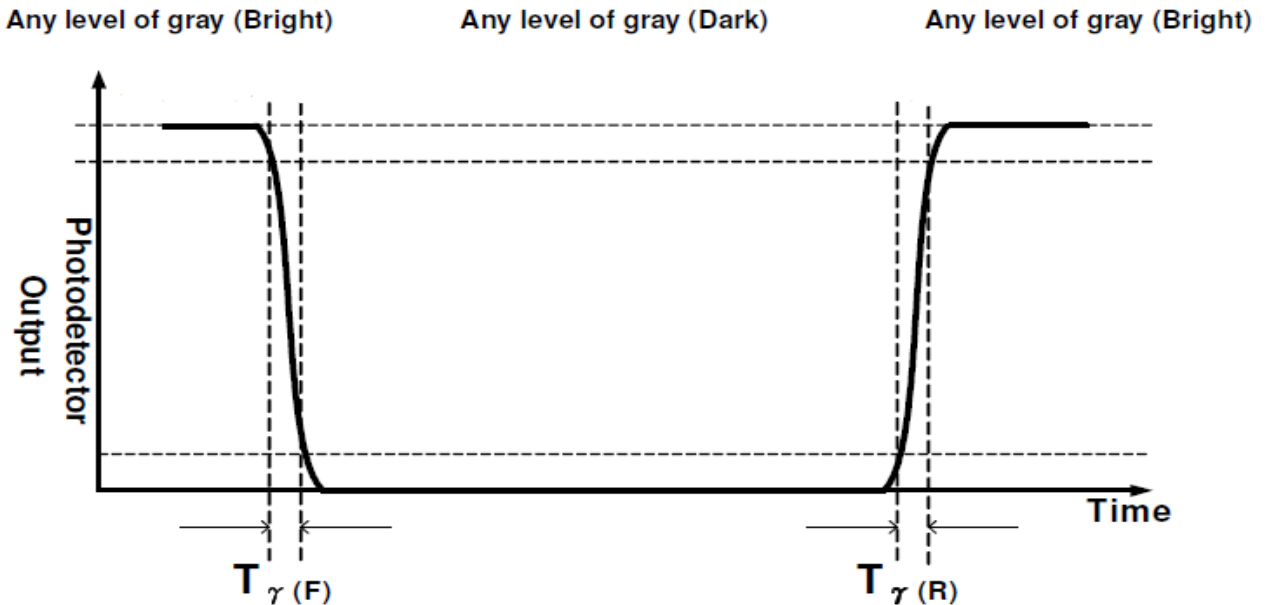
- (1) Cautions when taking out the Panel
Pick the pouch only, when taking out panel from a shipping package.
- (2) Cautions for handling the panel
As the electrostatic discharges may break the LCD Panel, handle the LCD panel with care. Peel a protection sheet off from the LCD panel surface as slowly as possible.
As the LCD panel and back -light element are made from fragile glass material, impulse and pressure to the LCD panel should be avoided.
As the surface of the polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.
Do not pull the interface connector in or out while the LCD panel is operating.
Put the panel display side down on a flat horizontal plane.
Handle connectors and cables with care.
- (3) Cautions for the operation
When the panel is operating, do not lose CLK, ENAB signals. If any one of these signals is lost, the LCD panel would be damaged.
Obey the supply voltage sequence. If wrong sequence is applied, the panel would be damaged.
- (4) Cautions for the atmosphere
Dew drop atmosphere should be avoided.
Do not store and/or operate the LCD panel in a high temperature and/or humidity atmosphere. Storage in an electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.
- (5) Cautions for the panel characteristics
Do not apply fixed pattern data signal to the LCD panel at product aging.
Applying fixed pattern for a long time may cause image sticking.
- (6) Other cautions
Do not disassemble and/or re-assemble LCD panel.
Do not re-adjust variable resistor or switch etc.
When returning the panel for repair or etc., Please pack the panel not to be broken. We recommend to use the original shipping packages.

12.0 APPENDIX

< Figure 1. Measurement Set Up >



< Figure 2. Response Time Testing >



13.0 Mechanical drawings of modules

