Approval Sheet

■ **Preliminary specification**

□ **Final specification**

Customer Name	
Product Description	**071inch FHD Micro-OLED Module**
Version	
Supplier	**BOE**
Module Code	

Customer Approval		**BOE Approval**	
SIGNATURE/TITLE	**DATE**	**SIGNATURE/TITLE**	**DATE**
PREPARED BY /		**PREPARED BY** /	
REVIEWED BY /		**REVIEWED BY** /	
APPROVED BY (R&D) /		**APPROVED BY (R&D)** /	
APPROVED BY (QA) /		**APPROVED BY (QA)** /	

Yunnan Invensight Optoelectronics Technology Co., Ltd.

Content

Revision

Version	Date	Description
V1.0	2021.09.09	Initial release
V1.1	2021.12.30	Revised according to the new modules
V1.2	2022.04.07	Correct the description error of EN_CMD2 in F0h; Correct the position of the protective film tearing hand in the drawing of section 12.

1.8 cm (Type 0.71) Active Matrix Color OLED Panel Module

1. Overview/Application

VX071FHP-NH7 is a 0.71 inch diagonal, FHD resolution (1920x1080), active matrix color OLED (Organic Light Emitting Display) panel module based on single crystal silicon backplane. The pixel circuits and driving IC are integrated on the silicon backplane to get the compact size and very low power consumption.

(Potential applications: Virtual Reality application (AR/VR), Head mounted displays, Near-Eye Displays etc.)

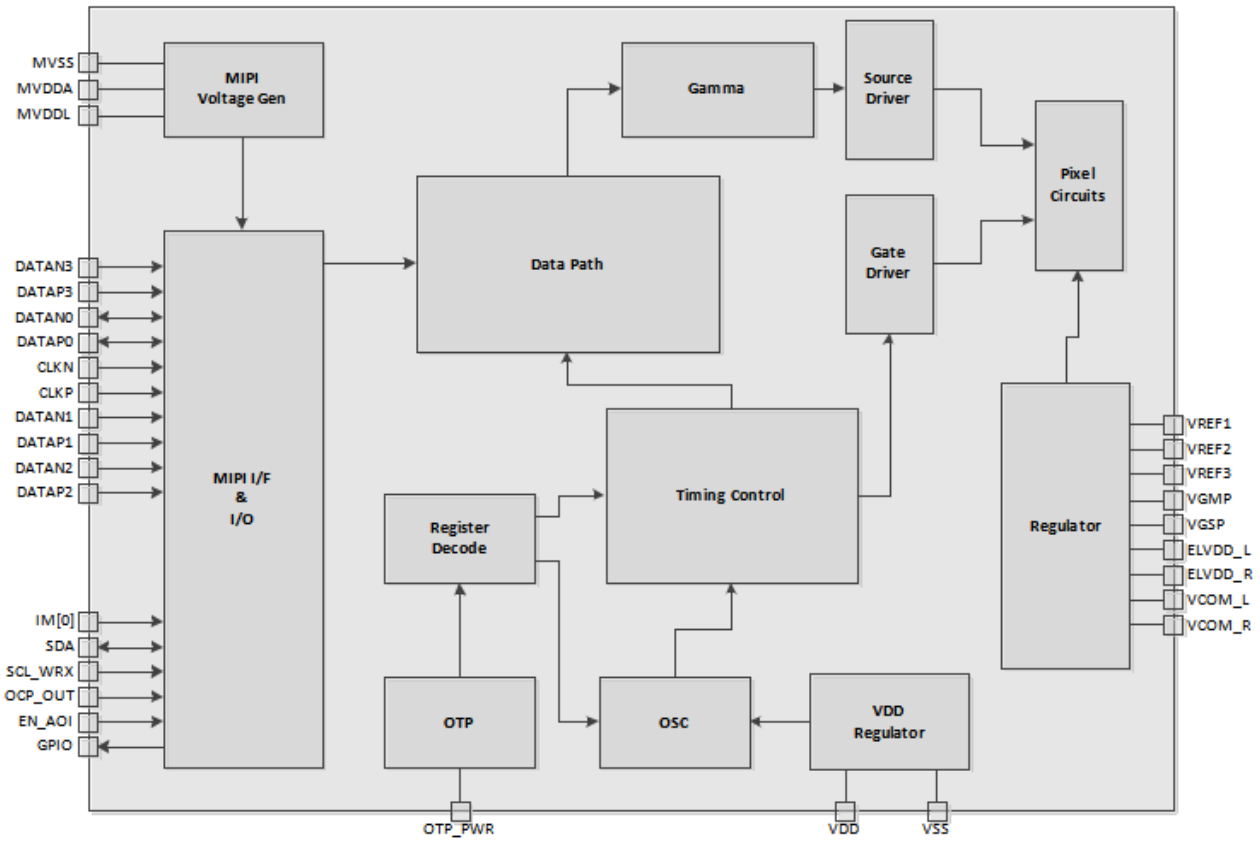
2. Features

- Small-size, high resolution 0.71" FHD Display PPI=3135
- AP Operated Resolution 1920x1080 up to 90Hz
- Full color mode, 16.7M colors
- Fast response
- Thin and light in weight
- High contrast (>10000:1)
- Idle mode for save power
- Scan direction selection, up or down
- Interface，Support MIPI only or MIPI+I2C
  Support VESA-DSC in-chip decoder (3X and 3.75X compression ratio)
  Support scaling up 1.33x (1440x810 to 1920x1080) and 1.5x (1280x720 to 1920x1080)

3. Module Structure

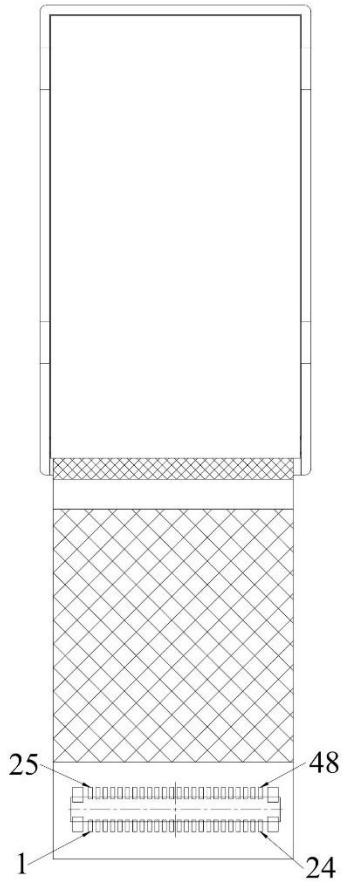
- Active matrix color OLED display with on-chip driver based on single crystal silicon transistors

4. System Block Diagram



5. Pin Description

5.1. Pin Assignment



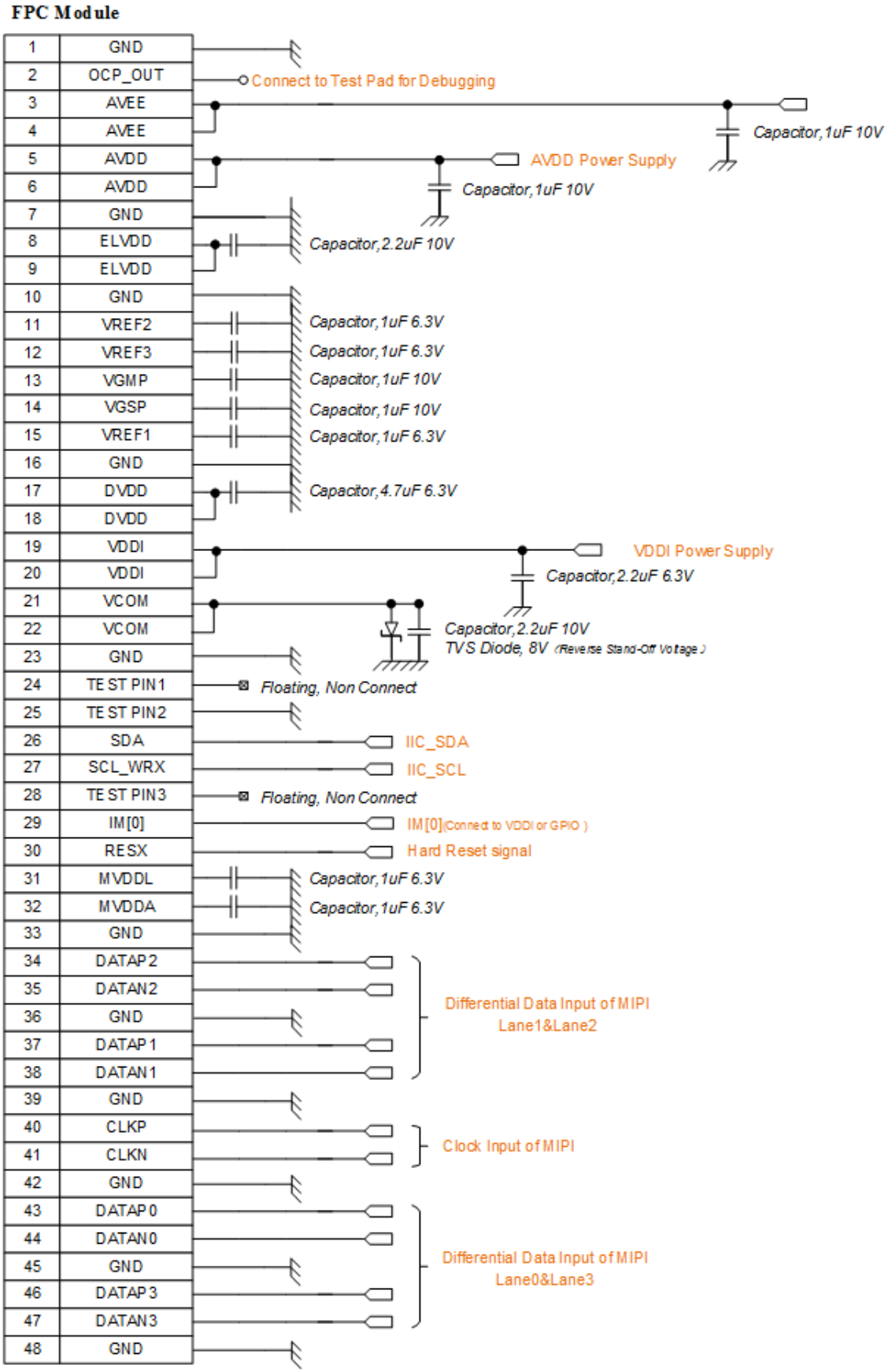
Bottom view

5.2. Pin Description of PCB Module

PIN No. (PCB Side)	Symbol	Type	Description
1	GND	Power Supply	Circuit ground
2	OCP_OUT	Output	Over current protect flag
3	AVEE	Power Supply	Power supply for OLED cell, connect a capacitor for stabilization
4	AVEE	Power Supply	Power supply for OLED cell, connect a capacitor for stabilization
5	AVDD	Power Supply	Power supply for OLED cell, connect a capacitor for stabilization
6	AVDD	Power Supply	Power supply for OLED cell, connect a capacitor for stabilization
7	GND	Power Supply	Circuit ground
8	ELVDD	Output	Power supply for OLED cell, connect a capacitor for stabilization
9	ELVDD	Output	Power supply for OLED cell, connect a capacitor for stabilization
10	GND	Power Supply	Circuit ground
11	VREF2	Output	VREF voltage, connect a capacitor for stabilization
12	VREF3	Output	VREF voltage, connect a capacitor for stabilization
13	VGMP	Output	Gamma top voltage, connect a capacitor for stabilization
14	VGSP	Output	Gamma bottom voltage, connect a capacitor for stabilization

<table>
<tr><td>15</td><td>VREF1</td><td>Output</td><td>VREF voltage, connect a capacitor for stabilization</td></tr>
<tr><td>16</td><td>GND</td><td>Power Supply</td><td>Circuit ground</td></tr>
<tr><td>17</td><td>DVDD</td><td>Output</td><td>Internal system Power, connect a capacitor for stabilization</td></tr>
<tr><td>18</td><td>DVDD</td><td>Output</td><td>Internal system Power, connect a capacitor for stabilization</td></tr>
<tr><td>19</td><td>VDDI</td><td>Power Supply</td><td>External power supply (1.8V for digital system power)</td></tr>
<tr><td>20</td><td>VDDI</td><td>Power Supply</td><td>External power supply (1.8V for digital system power)</td></tr>
<tr><td>21</td><td>VCOM</td><td>Output</td><td>Power supply for OLED cell, connect a capacitor for stabilization</td></tr>
<tr><td>22</td><td>VCOM</td><td>Output</td><td>Power supply for OLED cell, connect a capacitor for stabilization</td></tr>
<tr><td>23</td><td>GND</td><td>Power Supply</td><td>Circuit ground</td></tr>
<tr><td>24</td><td>TEST PIN1</td><td>Input</td><td>Test pin (no connect, floating)</td></tr>
<tr><td>25</td><td>TEST PIN2</td><td>Input</td><td>Test pin (connect to GND)</td></tr>
<tr><td>26</td><td>SDA</td><td>Input/Output</td><td>Bi-direction data pin in I2C I/F
If this pin is not used, please connect to VDDI</td></tr>
<tr><td>27</td><td>SCL_WRX</td><td>Input</td><td>Synchronous clock signal in I2C I/F
If this pin is not used, please connect to VDDI</td></tr>
<tr><td>28</td><td>TEST PIN3</td><td>Input</td><td>Test pin (no connect, floating)</td></tr>
<tr><td>29</td><td>IM[0]</td><td>Input</td><td>Use to select the Interface type
<table>
<tr><th>IM[0]</th><th>Command Execute</th><th>Image Write</th></tr>
<tr><td>0</td><td>MIPI</td><td>MIPI</td></tr>
<tr><td>1</td><td>I2C/MIPI</td><td>MIPI</td></tr>
</table></td></tr>
<tr><td>30</td><td>RESX</td><td>Input</td><td>This signal will reset the device and must be applied to properly initialize the chip, signal is active low</td></tr>
<tr><td>31</td><td>MVDDL</td><td>Output</td><td>Internal system Power, connect a capacitor for stabilization</td></tr>
<tr><td>32</td><td>MVDDA</td><td>Output</td><td>Internal system Power, connect a capacitor for stabilization</td></tr>
<tr><td>33</td><td>GND</td><td>Power Supply</td><td>Circuit ground</td></tr>
<tr><td>34</td><td>DATAP2</td><td>Input</td><td>Differential small amplitude signal of MIPI data input</td></tr>
<tr><td>35</td><td>DATAN2</td><td>Input</td><td>Differential small amplitude signal of MIPI data input</td></tr>
<tr><td>36</td><td>GND</td><td>Input</td><td>Circuit ground for MIPI</td></tr>
<tr><td>37</td><td>DATAP1</td><td>Input</td><td>Differential small amplitude signal of MIPI data input</td></tr>
<tr><td>38</td><td>DATAN1</td><td>Input</td><td>Differential small amplitude signal of MIPI data input</td></tr>
<tr><td>39</td><td>GND</td><td>Input</td><td>Circuit ground for MIPI</td></tr>
<tr><td>40</td><td>CLKP</td><td>Input</td><td>MIPI CLK</td></tr>
<tr><td>41</td><td>CLKN</td><td>Input</td><td>MIPI CLK</td></tr>
<tr><td>42</td><td>GND</td><td>Input</td><td>Circuit ground for MIPI</td></tr>
<tr><td>43</td><td>DATAP0</td><td>Input/Output</td><td>Differential small amplitude signal of MIPI data input</td></tr>
<tr><td>44</td><td>DATAN0</td><td>Input/Output</td><td>Differential small amplitude signal of MIPI data input</td></tr>
<tr><td>45</td><td>GND</td><td>Input</td><td>Circuit ground for MIPI</td></tr>
<tr><td>46</td><td>DATAP3</td><td>Input</td><td>Differential small amplitude signal of MIPI data input</td></tr>
<tr><td>47</td><td>DATAN3</td><td>Input</td><td>Differential small amplitude signal of MIPI data input</td></tr>
<tr><td>48</td><td>GND</td><td>Power Supply</td><td>Circuit ground</td></tr>
</table>

5.3. Peripheral Circuit



Mounting the capacitor for each power supply to ensure that the panel display normally.

Notes:

No.	Signal Name	Typical Value	Maximum Rated Voltage	Note
1	VDDI	Cap, 2.2uF	6.3V	
2	AVDD	Cap, 1.0uF	10V	
3	ELVDD	Cap, 2.2uF	10V	
4	AVEE	Cap, 1.0uF	10V	
5	DVDD	Cap, 4.7uF	6.3V	
6	MVDDA	Cap, 1uF	6.3V	
7	MVDDL	Cap, 1uF	6.3V	
8	VGMP	Cap, 1uF	10V	
9	VGSP	Cap, 1uF	10V	
10	VREF1	Cap, 1uF	6.3V	
11	VREF2	Cap, 1uF	6.3V	
12	VREF3	Cap, 1uF	6.3V	
13	VCOM	Cap, 2.2uF TVS	10V	

(1) There are totally 13 capacitors and 1 Schottky diode.

(2) The Schottky diode is placed between VCOM and ground, and the anode connect to Vcom, the cathode connect to GND.

6. Interface

VX071FHP-NH7 supports MIPI interface and inter-integrated circuit interface (I2C). MIPI or I2C is selected by IM0, the detail interface selection by IM0 pin and shows in below table.

IM0	Command Execute	Image Write
0	MIPI	MIPI
1	I2C/MIPI	MIPI

6.1. I2C Interface

The I2C-bus is for bi-directional, two-line communication between different ICs or modules. The two lines are the Serial Data Line (I2C_SDA) and Serial Clock Line (I2C_SCL). Both lines must be connected to a positive power supply via pull-up resistors. Data transfer can be initiated only when the bus is not busy. The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. The master generates all clock pulses, including the acknowledge ninth clock pulse.

6.1.1. I2C-Bus Protocol

Before any data is transmitted on the I2C-bus, the device which should response is addressed first. There are several slave addresses can be selected by MCU. The slave addressing is always carried out with the first byte transmitted after the START procedure.

Definition

-Transmitter: The device which sends the data to the bus.

-Receiver: The device which receives the data from the bus.

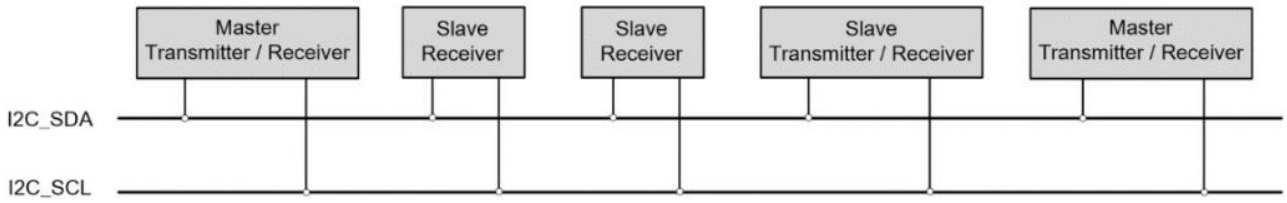
-Master: The device which initiates a transfer, generates clock signals and terminates a transfer.

-Slave: The device addressed by a master.

-Multi-master: More than one master can attempt to control the bus at the same time without corrupting the message.

-Arbitration: Procedure to ensure that. If more than one master simultaneously tries to control the bus, only one is allowed to do so and the message is not corrupted.

-Synchronization: Procedure to synchronize the clock signals of two or more devices.



6.1.2. Write Sequence

VX071FHP-NH7 supports register write sequence via I2C-bus transfer. The register writing supports single register write mode. The detailed transfer sequences are illustrated and described as below.

(1) Data transfer for register writing should follow the format shown as below.

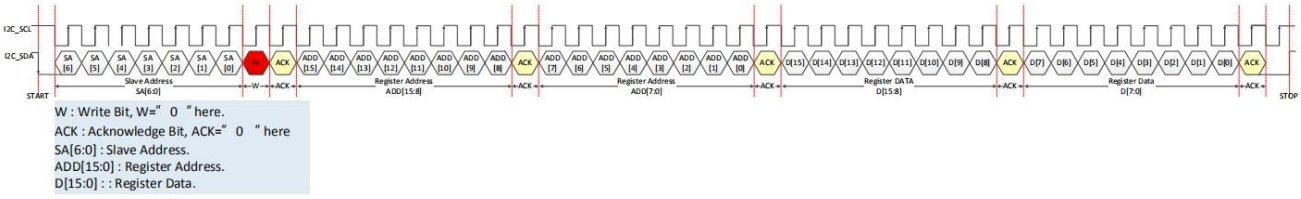
(2) After the START condition, a slave address is sent. R/$\overline{W}$ bit is setting to “0” for Write.

(3) The slave issues an ACK to the master.

(4) 8-bits register address transfer first then transfer the register data parameter.

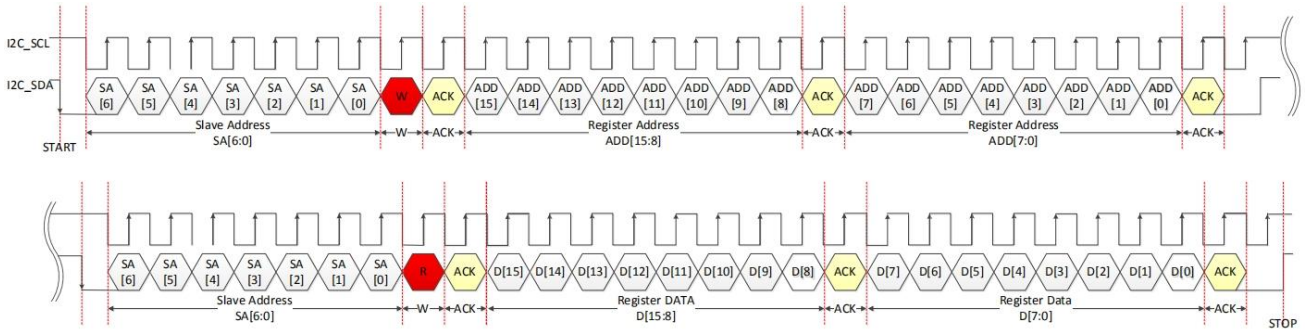
(5) A data transfer is always terminated by a STOP condition.

(6) The chip SA[6:0]=100_1100.



6.1.3. Read Sequence

VX071FHP-NH7 supports register read sequence via I2C-bus transfer. The register reading supports single register read mode. The register data reading transfer are shown as below.



W : Write Bit, W=" 0 " here.
R : Read Bit, R=" 1 " here.
ACK : Acknowledge Bit, ACK=" 0 " here
SA[6:0] : Slave Address.
ADD[15:0] : Read Register Address.
D[15:0] : : Read Register Return Data.

6.2. MIPI Interface

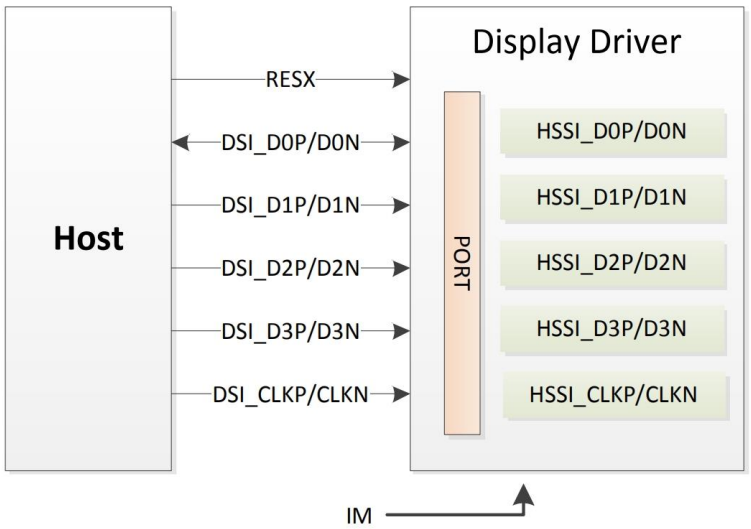
Display serial interface (DSI) specifies the interface between a host processor and a peripheral such as a display module. It builds on existing MIPI Alliance specification by adoption pixel formats and command set. The detail Lane configuration for DPHY is listed below.

There are one Clock Lane and 1~4 Data Lane. The configuration for DPHY between host and VX071FHP-NH7 shows as the table below.

Lane Pair	Available Operation Mode	
Clock Lane	Unidirectional Lane	Forward High-Speed Clock Escape Mode (ULPS only)
Data Lane 0	Bi-directional Lane	Forward High-Speed Data Bi-directional Escape Mode Bi-directional LPDT
Data Lane 1	Unidirectional Lane	Forward High-Speed Data No LPDT Escape Mode (ULPM only)
Data Lane 2	Unidirectional Lane	Forward High-Speed Data No LPDT Escape Mode (ULPM only)
Data Lane 3	Unidirectional Lane	Forward High-Speed Data No LPDT Escape Mode (ULPM only)

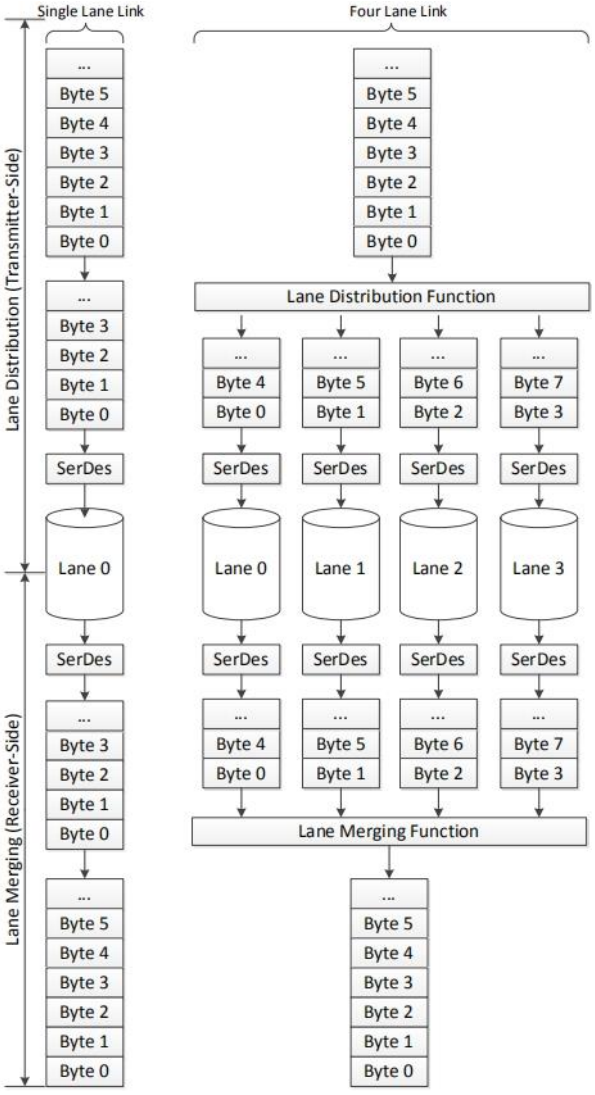
6.2.1. DSI System Configuration

VX071FHP-NH7 supports MIPI 1 port with 2, 3 or 4 lane configurations for DPHY. The system configuration is shown as the figure below. There are HW pin (IM) and registers (Lane_num_cfg, PSWAP, DSWAP) which can set the interface and lane related configuration.



6.2.2. Multi-Lane Distribution and Merging

DSI is a lane-scalable interface. Multi-lane implementations shall use a single common clock signal, shared by all data lane. In the transmitter, there will be a layer to distribute a sequence of packet bytes across N Lanes. And in the receiver, there will be a layer to merge this sequence of packet byte back to correct order. The data processing flow is shown as the figure below for DPHY one-lane/four-lane condition.



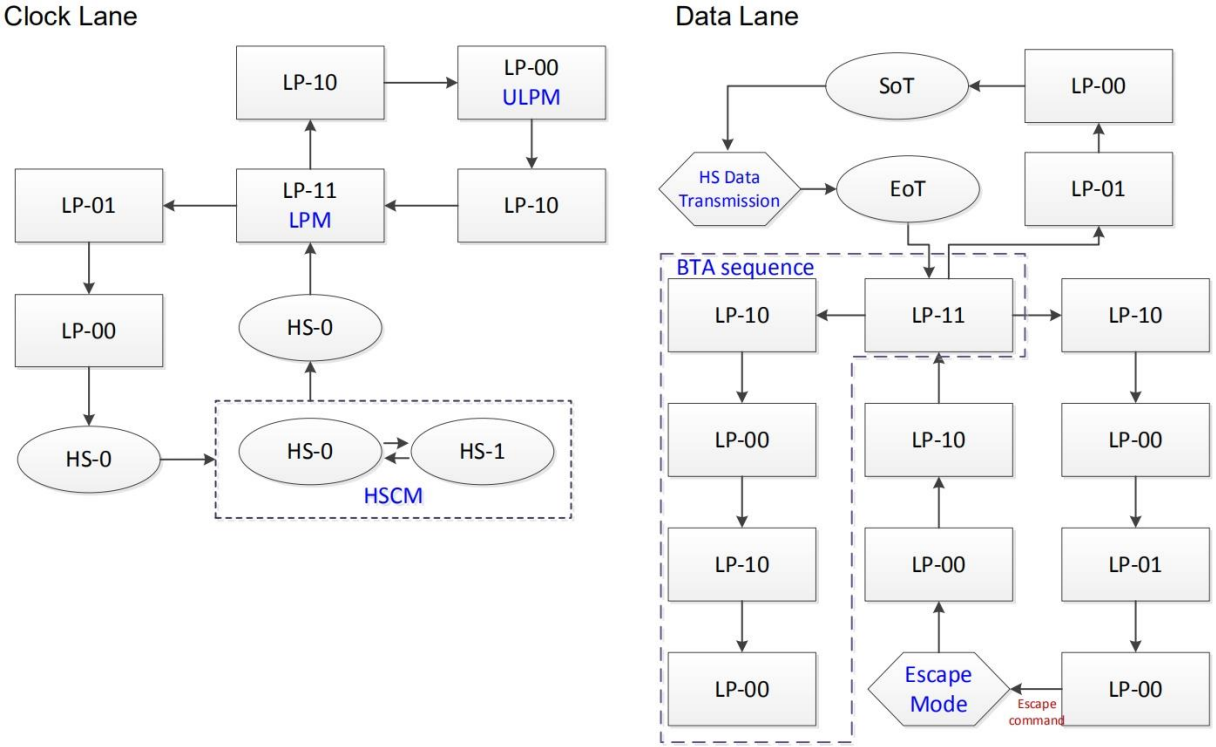
6.2.3. Interface Level Communication

DSI uses data and clock lane for DPHY communication. The Lane state is determined by driving certain Line levels. During normal operation, either a HS-TX or a LP-TX is driving a Lane. The HS-TX always drives the Lane differentially. The LP-TX drives two Lines for a Lane independently and single ended. These results of High-Speed Lane states and Low-Power Lane states for DPHY are as the table below.

State Code	Line Volatage Levels		High-Speed	Low-Power	
	Dp-Line	Dn-Line	Burst Mode	Control Mode	Escape Mode
HS-0	HS Low	HS High	Differential-0	N/A	N/A
HS-1	HS High	HS Low	Differential-1	N/A	N/A
LP-00	LP Low	LP Low	N/A	Bridge	Space
LP-01	LP Low	LP High	N/A	HS-Rqst	Mark-0
LP-10	LP High	LP Low	N/A	LP-Rqst	Mark-1
LP-11	LP High	LP High	N/A	Stop	N/A

6.2.4. Operation Modes

During normal operation a Lane will be either in Control or High-Speed mode. The clock lane can be driven into three different modes: Low-Power Mode (LPM), Ultra-Low-Power Mode (ULPM) or High-Speed Clock Mode (HSCM). The Data Lane can be driven into following different modes: Escape Mode, HS Data Transmission, Bi-directional Data Lane Turnaround (BTA). The entry and leaving protocol flow chart for DPHY are as below.



6.2.4.1. Escape Modes

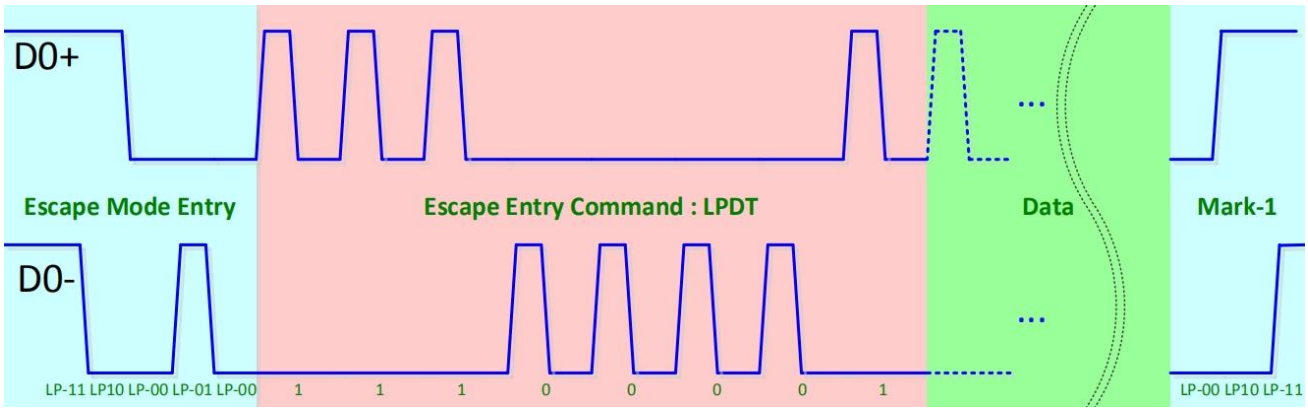
Escape mode is a special mode of operation for Data Lanes using Low-Power stated. With this mode some additional functionality becomes available. A data Lane shall enter Escape mode via Escape mode Entry procedure: LP-11 → LP-10 → LP-00 → LP-01 → LP-00. An 8-bit entry command shall be sent to indicate the requested action. The available Escape mode commands and actions are as the table below.

Escape Command	Command Type	Entry Command Pattern (First bit → Last bit)
Low-Power Data Transmission	Mode	1110 0001
Ultra-Low Power State	Mode	0001 1110
Undefined mode	Mode	1001 1111
Undefined mode	Mode	1101 1110
Remote Application Reset	Trigger	0110 0010
Tearing Effect	Trigger	0101 1101
Acknowledge	Trigger	0010 0001
Unknow	Trigger	1010 0000

6.2.4.2. Low Power Data Transmission

If the Escape mode Entry procedure is followed up by Entry Command for Low Power Data Transmission (LPDT). Data can be communicated by the protocol at low speed. The LPDT waveform is as follows and the figure below.

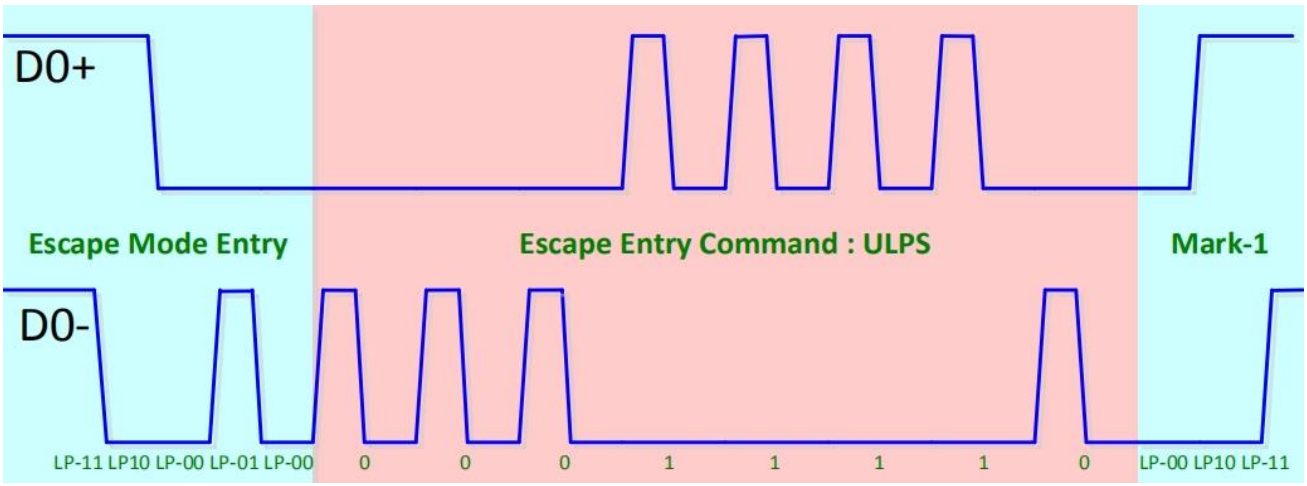
1. Escape mode Entry Sequence
2. Escape Entry Command (87h) for LPDT
3. LP data for LPDT
4. Mark-1 to leave Escape mode



6.2.4.3. Ultra-Low-Power State

The MCU can force data lane in Ultra-Low-Power State (ULPS) by Escape Mode with ULPS Entry Command. The sequence to force data lane in ULPS is as follows and the figure below.

1. Escape mode Entry Sequence
2. Escape Entry Command (78h) for ULPS
3. Mark-1 to leave Escape mode



6.2.5. High-Speed Data Transmission (HSDT)

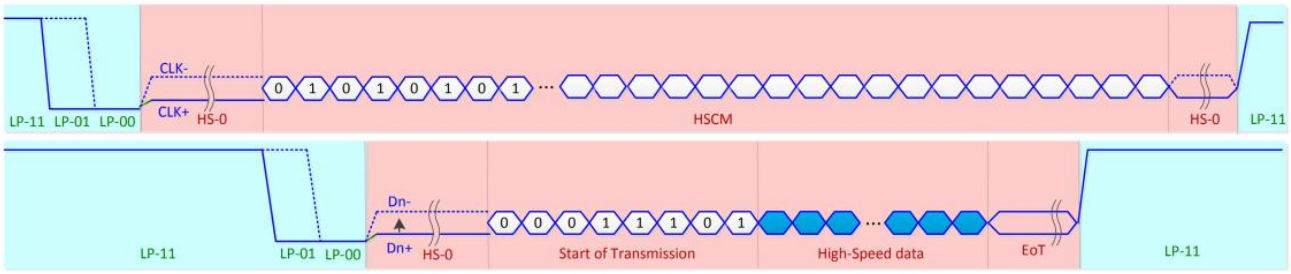
For High-Speed Data Transmission in DPHY, Clock lane have to enter High-Speed Clock Mode (HSCM) before Data lanes enter High-Speed Data Transmission. And the Data lanes have to leave High-Speed Data Transmission after Clock lanes already left HSCM. The High-Speed Data Transmission sequence for DPHY is as the figure below.

- **Data Lane**

1. HS request sequence: LP-11 → LP-01 → LP-00
2. Keep HS-0 for certain time
3. Start of Transmission sequence (B8h)
4. HS data for HSDT
5. End of Transmission sequence (HS-0 if last data bit is HS-1, HS-1 if last data bit is HS-0)
6. Back to LP-11 to leave HSDT

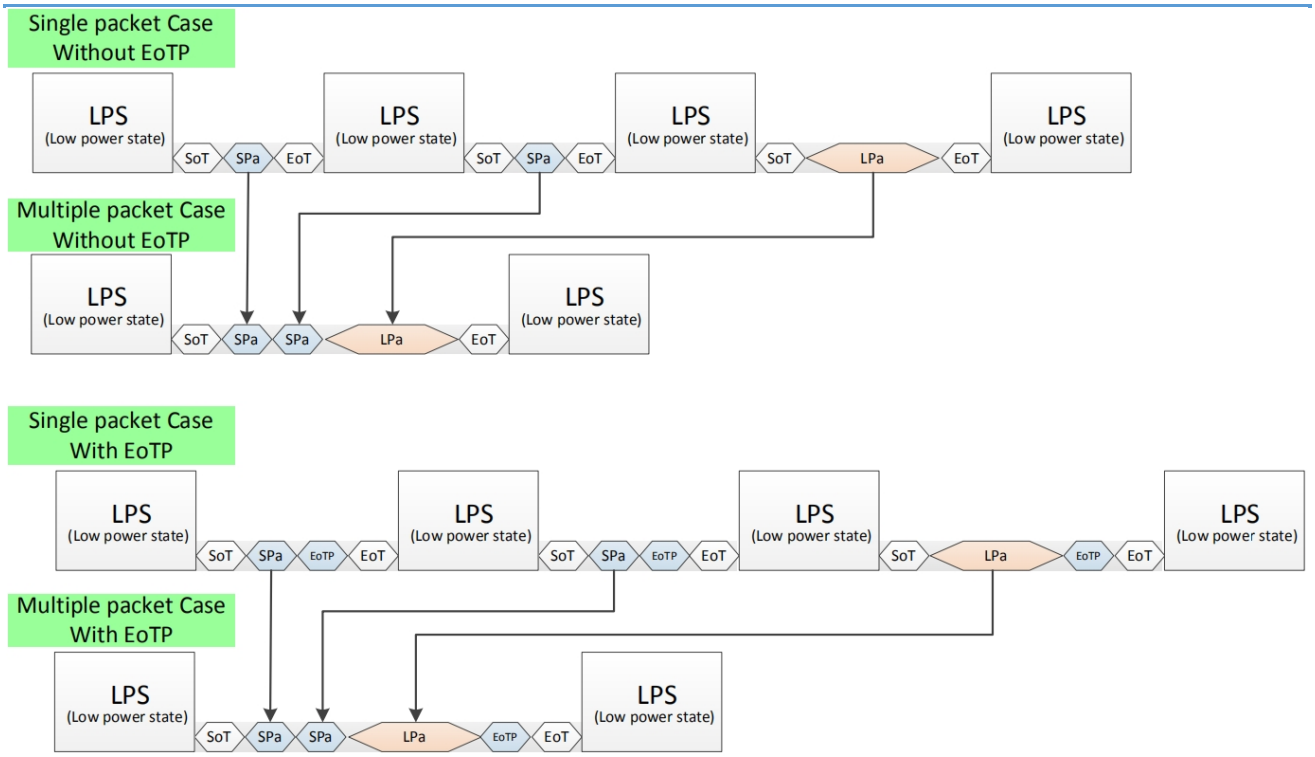
- **Clock Lane**

1. HS request sequence: LP-11 → LP-01 → LP-00
2. Keep HS-0 for certain time
3. High speed clock mode
4. Keep HS-0 for certain time
5. Back to LP-11 to leave HSCM



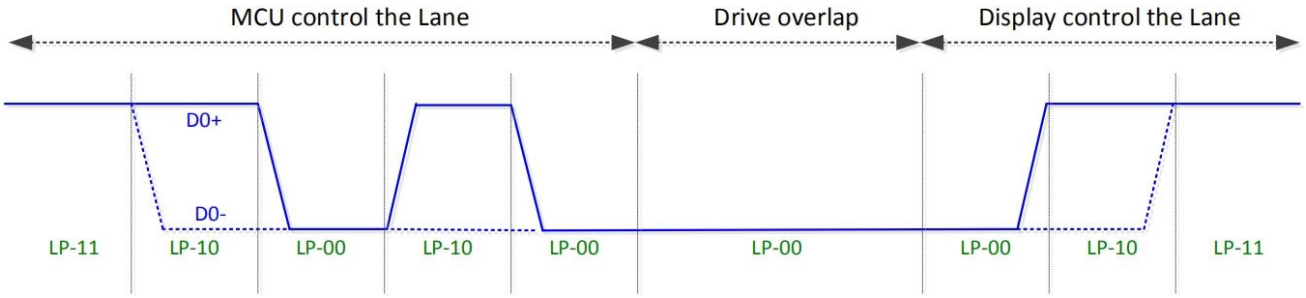
6.2.6. Burst of High-Speed Data Transmission

For HSDT, there can be one data packet or multiple packets in one HS burst. These data packets can be long packet (LPa) or Short packet (SPa). HSDT with End of Transmission Packet (EoTP) or without it is selectable. Examples are as below.



6.2.7. Bi-directional Lane Turnaround (BTA)

The transmission direction of a bi-directional lane can be swapped by means of a turnaround procedure. The procedure enable information transfer in the opposite direction and this procedure is the same for either a change from forward-to-reverse or reverse-to-forward direction. The BTA procedure is as follows and the figure below.

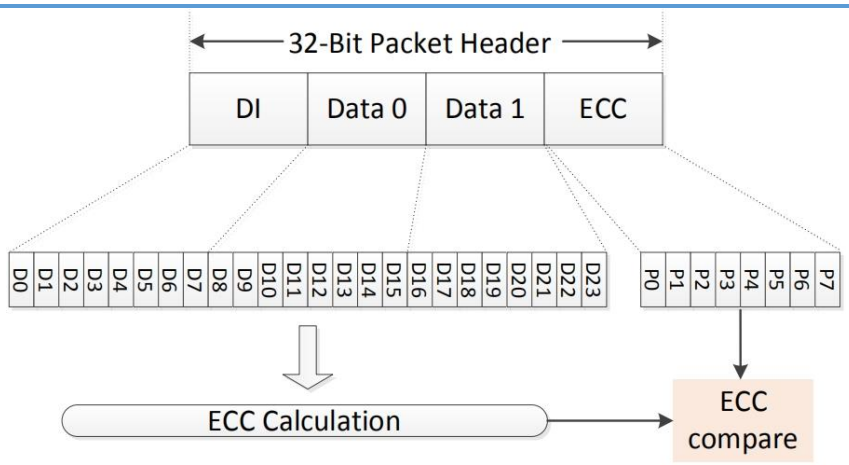


6.2.8. Interface Level Communication

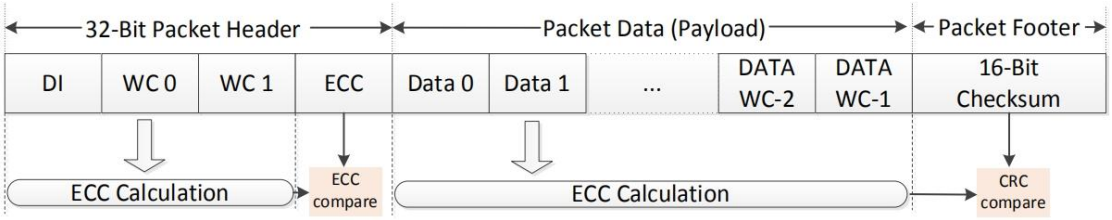
There are two packet structures are defined for communication: Short Packets (SPa) and Long Packets (LPa). For both packet structures, the Data Identifier (DI) is always the first bit of the packet.

6.2.8.1. General Packet Structure

For DPHY, Short Packets are four bytes in length including 1 byte DI, 2 bytes data or command and 1 byte Error Correction Code (ECC). The ECC byte is used to check if the first 3 bytes in Packet Header (DI and data) is correct or not. And the ECC byte allows single-bit error to be corrected and 2-bit errors to be detected. The packet format for Short Packets are illustrated as the following.

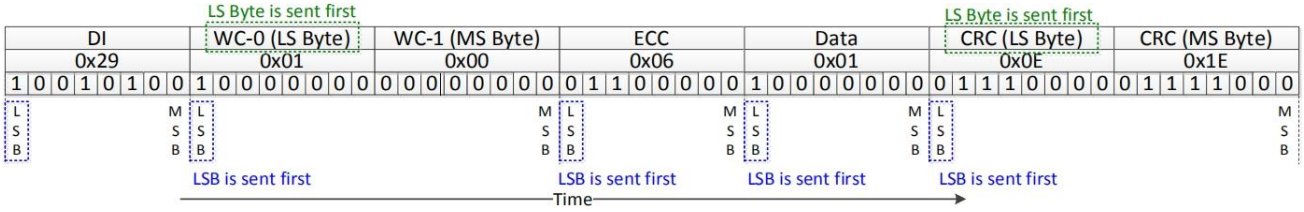


As to Long Packets, they shall consist of three elements: 4 bytes Packet Header, Data Payload with a variable number of bytes and 2 bytes Packet Footer. The Packet Header includes 1 byte DI, 2 bytes Word Count (WC) and 1 byte ECC. The Word Count in Packet Header will decide the number of total bytes of the Data Payload. The Packet Footer has 2 bytes Checksum used to check if the Payload Data is correct or not. The packet format for Long Packets are illustrated as the following.



6.2.8.2. Bit Order and Byte Order for Packets

The bit order for packets is the Least Signification Bit sent first and the Most Significant Bit sent last. And for the byte order for packets is the Least Signification Byte sent first and the Most Significant Byte sent last.



6.2.8.3. Common Packet Elements

There are several common elements for Long and Short Packets such as DI byte and ECC byte. The DI byte consists of 2-bit Virtual Channel identifier (VC = DI[7:6]) and 6-bit Data Type field (DT = DI[5:0]). The DI structure is as the following.

Data Identifier (DI)							
Virtual Channel (VC)		Data Type (DT)					
Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0

Virtual Channel is used to assign which peripherals for packets transmission. Data Type specifies if the packet is a Long or Short Packet and the packet format. The Data Type are defined as the table below.

Data Types for Peripheral-Sourced Packets

Data Type (hex)	Data Type (binary)	Description	Packet Size
0x02	00 0010	Acknowledge and Error Report	Short

0x11	01 0001	Generic Short READ Response, 1 byte returned	Short
0x12	01 0010	Generic Short READ Response, 2 bytes returned	Short
0x1A	01 1010	Generic Long READ Response	Long
0x1C	01 1100	DCS Long READ Response	Long
0x21	10 0001	DCS Short READ Response, 1 byte returned	Short
0x22	10 0010	DCS Short READ Response, 2 bytes returned	Short

Data Types for Processor-Sourced Packets

Data Type (hex)	Data Type (binary)	Description	Packet Size
0x01	00 0001	Sync Event, V Sync Start	Short
0x11	01 0001	Sync Event, V Sync End	Short
0x21	10 0001	Sync Event, H Sync Start	Short
0x31	11 0001	Sync Event, H Sync End	Short
0x07	00 0111	Compression Mode Command	Short
0x08	00 1000	End of Transmission packet (EoTp)	Short
0x03	00 0011	Generic Short WRITE, no parameters	Short
0x13	01 0011	Generic Short WRITE, 1 parameter	Short
0x23	10 0011	Generic Short WRITE, 2 parameters	Short
0x04	00 0100	Generic READ, no parameters	Short
0x14	01 0100	Generic READ, 1 parameter	Short
0x24	10 0100	Generic READ, 2 parameters	Short
0x05	00 0101	DCS Short WRITE, no parameters	Short
0x15	01 0101	DCS Short WRITE, 1 parameter	Short
0x06	00 0110	DCS READ, no parameters	Short
0x37	11 0111	Set Maximum Return Packet Size	Short
0x09	00 1001	Null Packet, no data	Long
0x19	01 1001	Blanking Packet, no data	Long
0x29	10 1001	Generic Long Write	Long
0x39	11 1001	DCS Long Write	Long
0x0A	00 1010	Picture Parameter Set	Long
0x0B	00 1011	Compressed Pixel Stream	Long
0x0E	00 1110	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	Long
0x1E	01 1110	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
0x2E	10 1110	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
0x3E	11 1110	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	Long

As to ECC, the host processor shall always calculate and transmit an ECC byte to identify the error for the Packet Header. The bits of ECC are defined as the rule below. The symbol '^' means XOR function. P7 and P6 are set to 0 because Error Correction Code is based on 64-bit value but this ECC implementation is only used for 24-bit value.

P7 = 0

P6 = 0

P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23

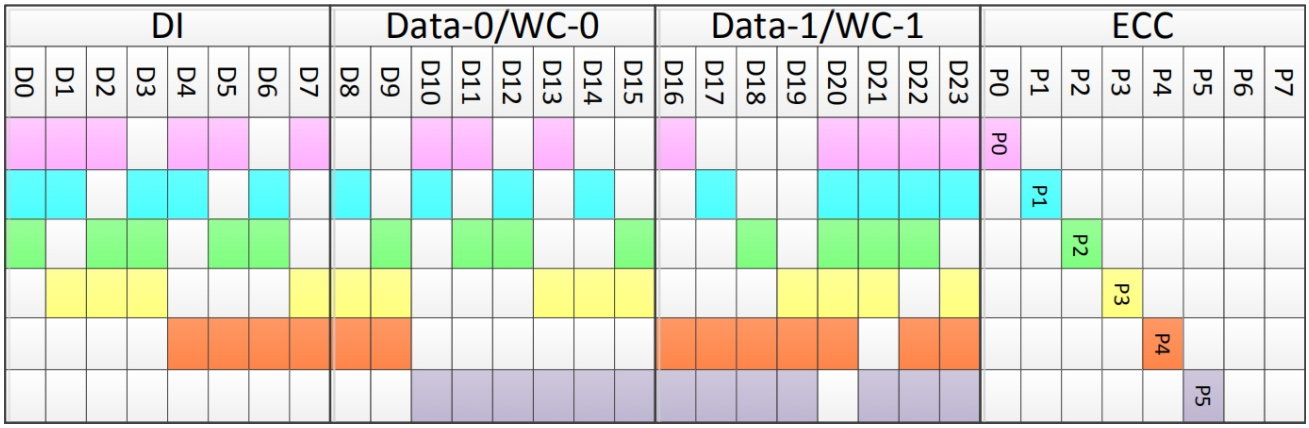
P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23

P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23

P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22

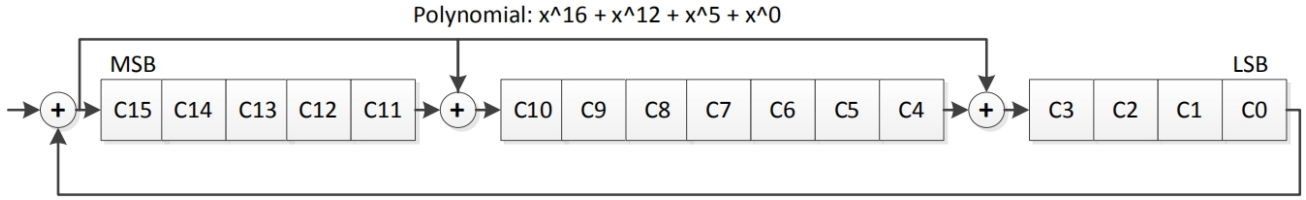
P1 = D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23

P0 = D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23



6.2.8.4. Packet Footer for Long Packets

The Packet Footer for Long Packets is a checksum value which is calculated from the Data Payload in the Long Packet. The checksum is using a 16-bit Cyclic Redundancy Check (CRC) with a generator polynomial of x^16 + x^12 + x^5 + x^0. The Receiver will calculate checksum value from received Data Payload and compare this CRC value with the Packet Footer sent by transmitter. If calculated CRC values equal to Packet Footer, the received Data Payload are correct. The CRC implementation is presented as the following.



6.2.8.5. Packet Pixel Stream Format

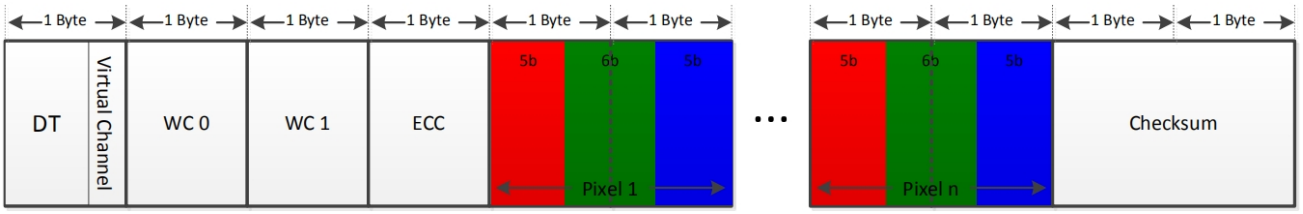
There are 4 packet pixel stream format: 16-bit RGB 5-6-5, 18-bit RGB 6-6-6, loosely packed 18-bit RGB 6-6-6 and 24-bit RGB 8-8-8. The Data Type for these pixel stream format are shown as the table below.

Data Type (hex)	Data Type (binary)	Description	Packet Size
0x0E	00 1110	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	Long
0x1E	01 1110	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
0x2E	10 1110	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
0x3E	11 1110	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	Long

Note: *VX071FHP-NH7 only support 24-bit RGB pixel stream format*

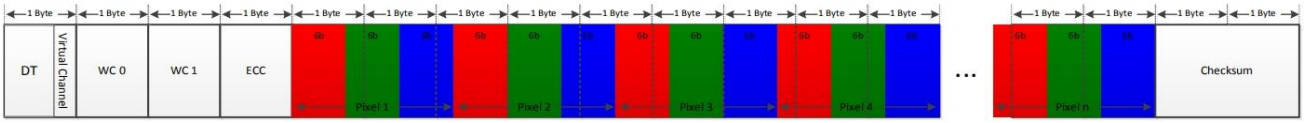
6.2.8.6. 16-bit RGB Format, Data Type = 0x0E

The data of 16-bit RGB pixel format comprise of five bits red, six bits green and five bits blue. Note that the "Green" component is split across two bytes. The pixel stream format is shown as the figure below.



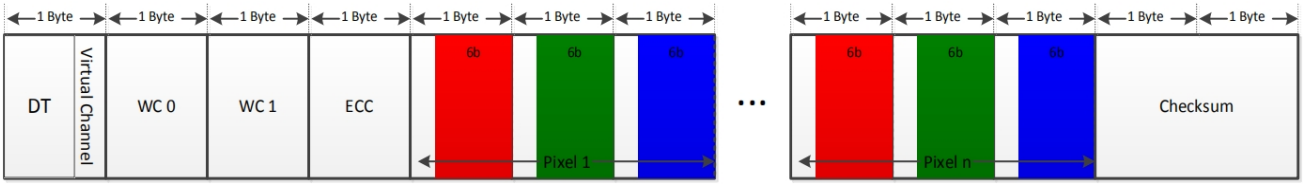
6.2.8.7. 18-bit RGB Format, Data Type = 0x1E

The data of 18-bit RGB pixel format comprise of six bits red, six bits green and six bits blue. The pixel stream format is shown as the figure below.



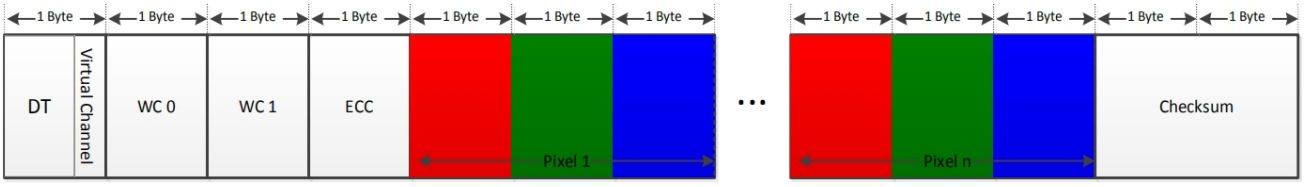
6.2.8.8. 18-bit Loosely RGB Format, Data Type = 0x2E

The data of 18-bit loosely RGB pixel format comprise of six bits red, six bits green and six bits blue. But the six bits of each color is shifted to the upper bits of the byte and the bit[1:0] of each payload byte are ignored. This requires more bandwidth than the “packed” format but requires less shifting and multiplexing logic in the packing and unpacking function. The pixel stream format is shown as the figure below.



6.2.8.9. 24-bit RGB Format, Data Type = 0x3E

The data of 24-bit RGB pixel format comprise of eight bits red, eight bits green and eight bits blue. The pixel stream format is shown as the figure below.



6.2.9. Peripheral-to-Processor LP Transmissions

All systems require bi-directional capability for returning READ data, acknowledge or error information to the Host Processor. It shall use Lane 0 for all peripheral-to-processor transmissions. Reverse-direction signaling shall only use Low Power mode of Transmission.

Packet structure for peripheral-to-processor transactions is the same as for the processor-to-peripheral direction. There are four basic types for peripheral-to-processor transactions: Acknowledge, Acknowledge and Error Report, Response to Read Request, Tearing Effect (TE).

Acknowledge and Error Report is a Short Packet sent if any errors were detected in preceding transmissions from the Host Processor. Once the Errors are reported, the accumulated errors in the error register are cleared.

An error report is a short packet comprised of two bytes following the DI byte and with an ECC byte following

the Error Report bytes. Detection and reporting of each error types is signified by setting the corresponding bit to “1”. The bit assignment for all error reporting is shown as the table below.

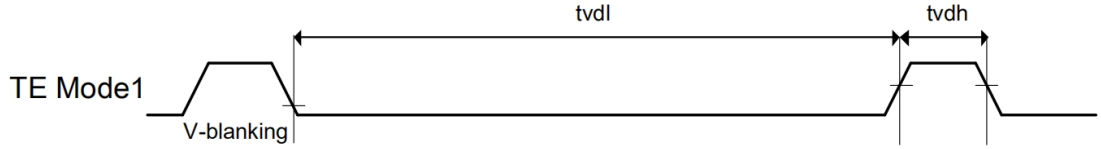
Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Peripheral Timeout Error
6	False Control Error
7	Contention Detected
8	ECC Error, singl-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Payload Checksum Error
11	DSI Data Type Not Recognized
12	DSI VC ID Invalid
13	Invalid Transmission Length
14	Reserved
15	DSI Protocol Violation

6.3. Tearing Effect Output

The tearing effect (TE) output signal used to be a synchronization signal for command mode display application. A command mode display has its own timing control and memory frame buffer. To avoid tearing effect, it is needed to synchronize timing between host and panel.

There are three kinds of TE mode supported from display module. These TE output signals can be enable, disable and select by DCS command 35h, 34h and 44h. In below shows the different TE output mode:

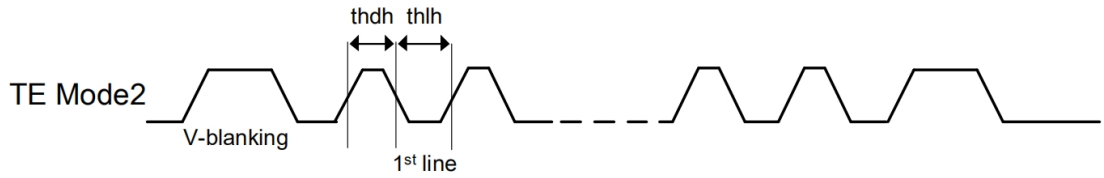
TE Mode1: The tearing effect output signal consists of V-Blanking only.



tvdh = display is not updated the data from memory frame buffer.

tvdl = display is updated the data from memory frame buffer.

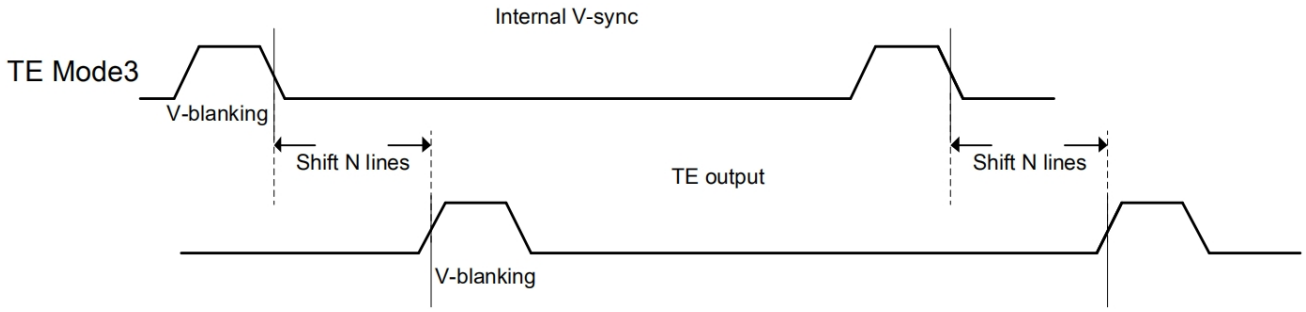
TE Mode2: The tearing effect output signal consists of V-Blanking and H-Blanking.



thdh = display is not updated the data from memory frame buffer.

thdl = display is updated the data from memory frame buffer.

TE Mode3: The tearing effect output signal consists of V-Blanking and H-Blanking.



N = the N-th line after V-blanking, which is set by 44h command.

Mode selection for TE output

TEON (35h), TEOFF (34h)	TEON (35h]), M(bit0)	STESL (44h), N[15:0]	TE Output
TEOFF	X	X	TE off (output low)
TEON	M = 0	N[15:0] = 0	TE mode1
TEON	M = 1	N[15:0] = 0	TE mode2
TEON	M = 0	N[15:0] ≠ 0	TE mode3

7. Electrical Characteristics

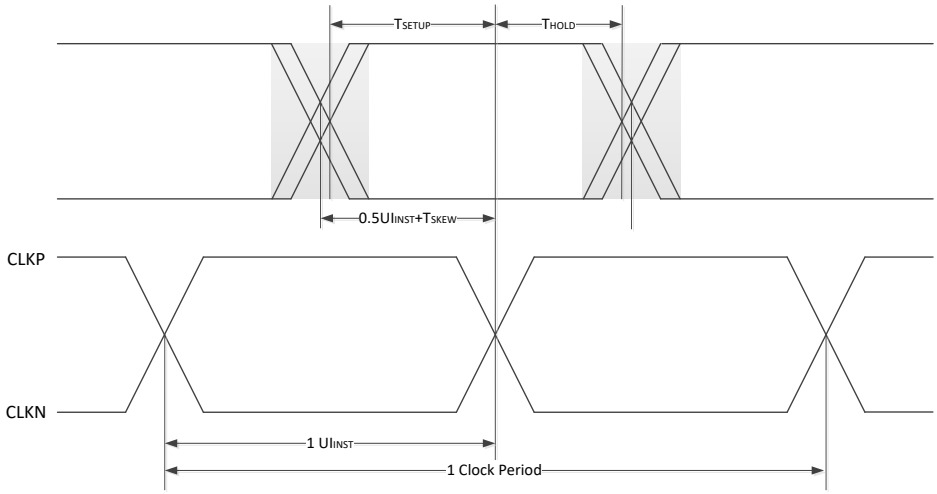
7.1. DC Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power & Operation Voltage/Current						
AVDD Input Level	AVDD Voltage	-	5.4	5.4	6	V
	AVDD Loading Current	Driving current≥ Loading current	-	-	200	mA
AVEE Input Level	AVEE Voltage	-	-5.4	-5.4	-6	V
	AVEE Loading Current	Driving current≥ Loading current	-	-	200	mA
VDDI Input Level	VDDI Voltage	-	-	1.8	-	V
	VDDI Loading Current	Driving current≥ Loading current	-	-	200	mA
Power Consumption	Total Consumption	@60Hz, 300nit, 1920x1080, 25℃	-	-	400	mW

7.2. AC Characteristics

7.2.1. MIPI High Speed Mode Characteristics

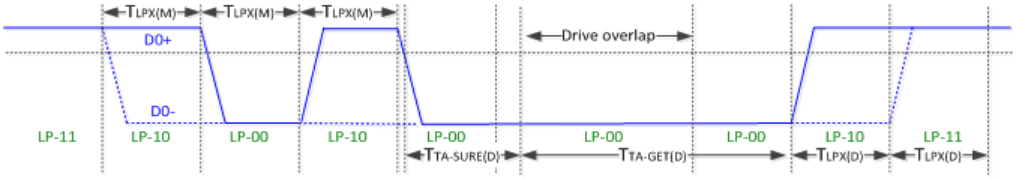
Parameter	Symbol	Min.	Typ.	Max.	Unit
UI instantaneous	UIINST	1	-	3	ns
T Data to Clock Skew	TSKEW	-0.15	-	0.15	UIHS
RX Data to Clock Setup Time Tolerance	TSETUP	0.15	-	-	UIHS
RX Data to Clock Hold Time Tolerance	THOLD	0.15	-	-	UIHS



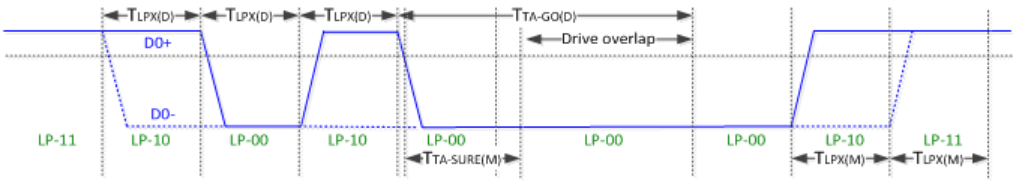
7.2.2. MIPI Low Power Mode Characteristics

Parameter	Description	Min.	Typ.	Max.	Unit
$T_{LPX(M)}$	Transmitted length of any Low-Power state period (MCU to display module)	50	-	-	ns
$T_{LPX(D)}$	Transmitted length of any Low-Power state period (display module to MCU)	50	-	-	ns
$T_{TA-SURE}$	Time that the new transmitter waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround	T_{LPX}	-	$2*T_{LPX}$	
T_{TA-GET}	Time that the new transmitter drives the Bridge state (LP-00) after accepting control during a Link Turnaround	$5*T_{LPX}$			
T_{TA-GO}	Time that the transmitter drives the Bridge state (LP-00) before releasing control during a Link Turnaround	$4*T_{LPX}$			

- Bus Turnaround from MPU to display module



- Bus Turnaround from display module to MPU



7.2.3. MIPI Video Timing Specification

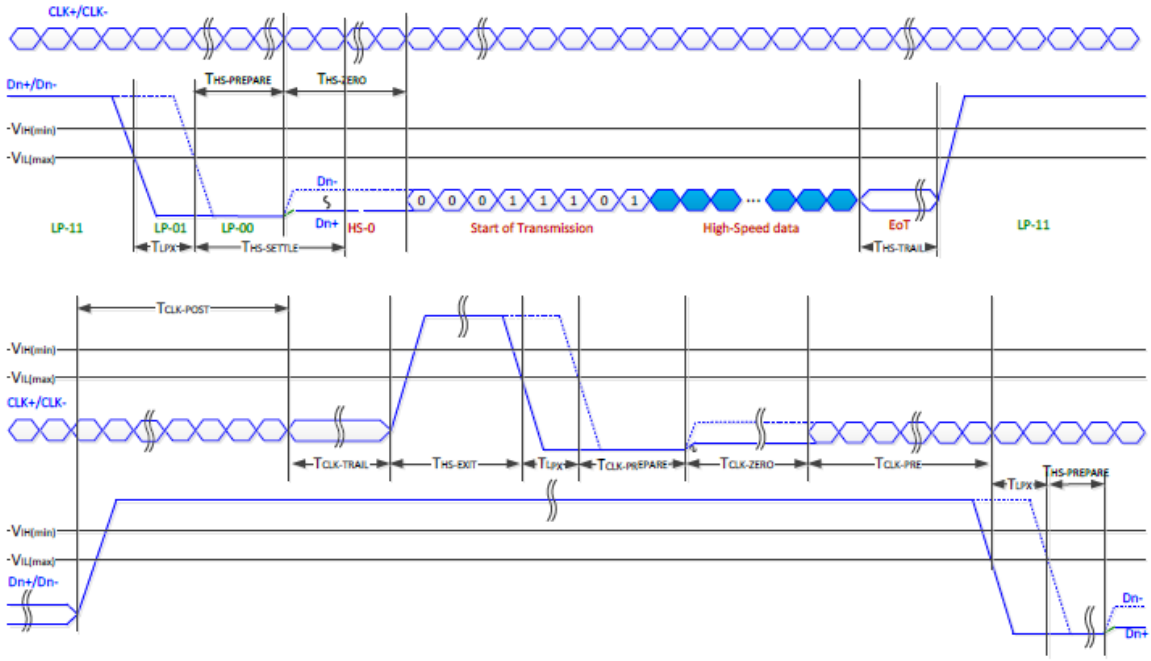
1920×1080					
H	Hsync	32	V	Vsync	4
	HBP	72		VBP	8
	Hactive	1920		Vactive	1080
	HFP	56		VFP	8

Recommended configuration of MIPI	
D-PHY V1.2 DSI 1.01 DCS V1.2	CLK Mode: Discontinue Mode
	MIPI Lane: 4 Lanes@60Hz
	Video Mode: Burst Mode
	HS Speed:300Mbps ~ 1.0Gbps per Lane
	LP Speed: 10Mbps (max)
	General Packet Structure：DCS Mode .Data Type of Packet：0x39 or 0x05 or 0x15

※This parameter is a typical example illustrating the display timing. BOE cannot assume responsibility for any problems arising out of the use of the circuit.

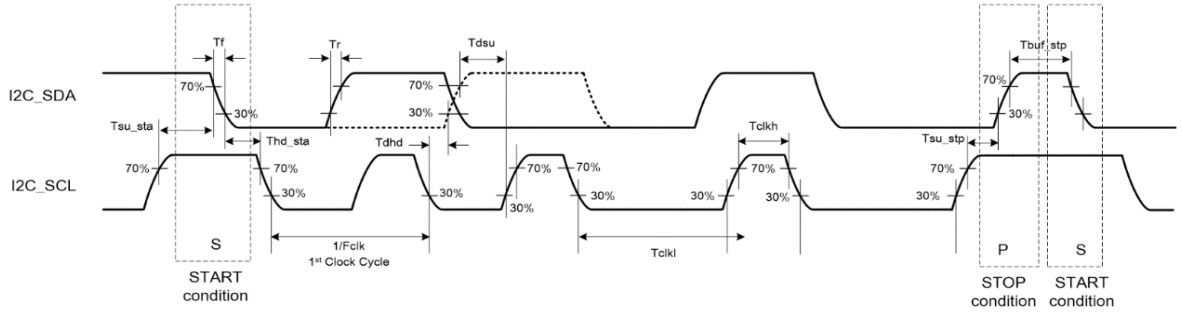
7.2.4. High Speed Mode Operation Timing Characteristics

Parameter	Description	Min.	Typ.	Max.	Unit
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of THS-TRAIL to the beginning of $T_{CLK-TRAIL}$	60ns + 52*UI	-	-	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode	8	-	-	UI
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	38	-	95	ns
$T_{CLK-SETTLE}$	Time interval during which the HS receiver should ignore any Clock Lane HS transitions, starting from the beginning of $T_{CLK-PREPARE}$	95	-	300	ns
$T_{CLK-TERM\_EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$	-	-	38	ns
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst	60	-	-	ns
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	$T_{CLK-PREPARE}$ + time that the transmitter drives the HS-0 state prior to starting the Clock	300	-	-	ns
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst	100	-	-	ns
T_{D-TERM_EN}	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$	-	-	35ns + 6*UI	ns
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40ns + 4*UI	-	85ns + 6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence	145ns + 10*UI	-	-	ns
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of $T_{HS-PREPARE}$. The HS receiver shall ignore any Data Lane transitions before the minimum value, and the HS receiver shall respond to any Data Lane transitions after the maximum value.	85ns + 6*UI	-	145ns + 10*UI	ns



7.2.5. I2C Interface Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
I2C Clock Frequency	Fclk	-	-	400	kHz
I2C Clock Low	Tclkl	1300	-	-	ns
I2C Clock High	Tclkh	600	-	-	ns
I2C Data Rising Time	Tdr	-	-	300	ns
I2C Data Falling Time	Tdf	-	-	300	ns
I2C Data Setup Time	Tdsu	100	-	-	ns
I2C Data Hold Time	Tdhd	-	-	TBD	ns
I2C Setup Time (Start Condition)	Tsu_sta	600	-	-	ns
I2C Hold Time (Start Condition)	Thd_sta	600	-	-	ns
I2C Setup Time (Stop Condition)	Tsu_stp	600	-	-	ns
I2C Bus Free Time (Stop Condition)	Tbuf_stp	1300	-	-	ns



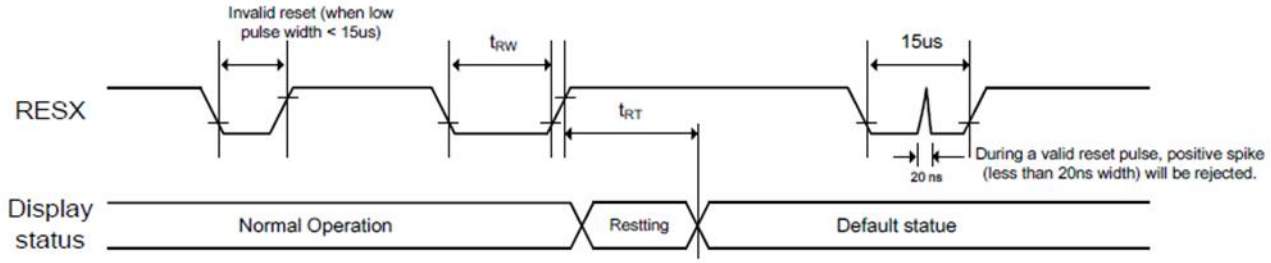
Notes:

No.	Item	Description
1	Slave address	0x4C
2	Pull-up resistor	4.7kΩ@100kbps
3	Read bit	Setting “1” for write
4	Write bit	Setting “0” for write
5	Start condition	SDA is setting from “1” to “0” when SCL is “1”

6	Stop condition	SDA is setting from “0” to “1” when SCL is “1”

7.2.6. Rest Timing Characteristics

When Reset happens in Sleep-out mode, the driver IC will enter blanking sequence with the maximum time 120 msec. Then driver IC will remain in blanking state and return IC’s default state. During reset complete time (tRT), data in OTP will be re-loaded and latched to internal registers. This data re-load is done every time when there is an H/W reset and completes within 20 msec after the rising edge of RESX. Therefore, it is necessary to wait at least 20 msec after releasing the RESX before sending commands. Moreover, the Sleep-out command cannot be sent in 120 msec. Spike (less than 20ns width) Rejection can also be applied during a valid reset pulse.

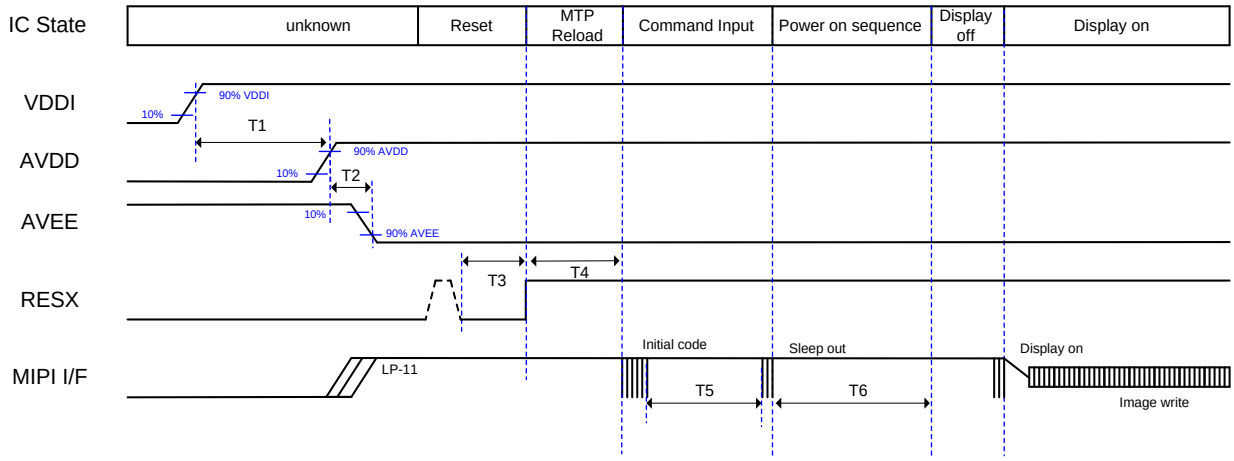


Reset time @ VDDI=1.65V to 1.95V, AVSS=VSS=MVSS=0V, Ta=-40 ℃ to 85 ℃

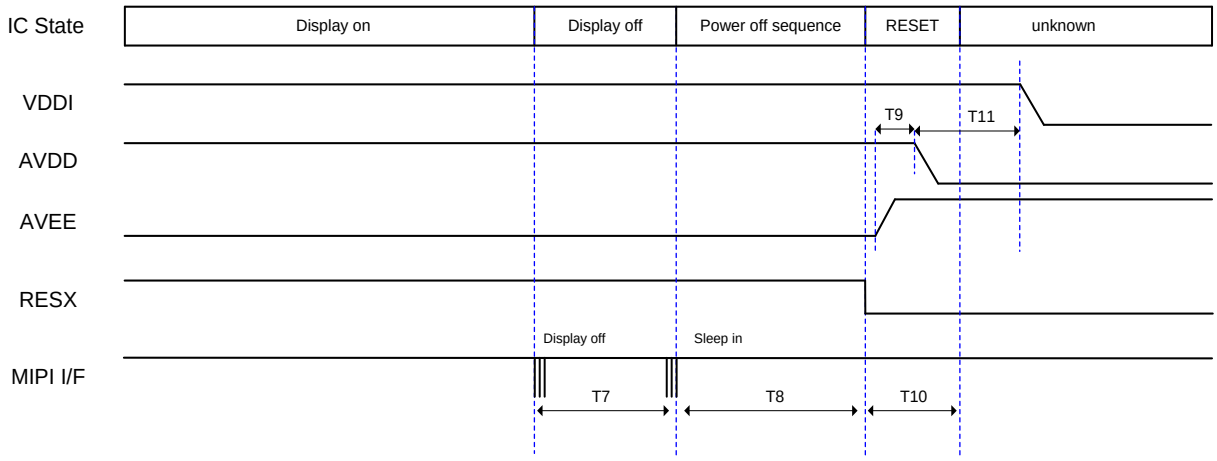
Signal	Symbol	Parameter	Min.	Typ.	Max.	Unit	Description
RESX	t_{RW}	Reset low pulse width	15	-	-	us	
	t_{RT}	Reset Complete time	-	-	20	ms	When reset applied at sleep-in mode
			-	-	120	ms	When reset applied at sleep-out mode

8. Power On/Off Sequence

Power on sequence



Power off sequence



Symbol	Min.	Typ.	Max.	Unit	Description
T1	1	-	-	ms	Power on time between AVDD and VDDI
T2	1	-	-	ms	Power on time between AVDD and AVEE
T3	1	-	-	ms	Effective hardware reset period
T4	20	-	-	ms	MTP reload time
T5	0	-	-	ms	The time is between initial code finished and sleep-out command
T6	2	-	-	VS	Power on sequence, the period can be modified
T7	1	-	-	VS	Blanking region
T8	-	1	-	VS	Power off sequence, the period can be modified
T9	1	-	-	ms	Power off time between AVEE and AVDD
T10	1	-	-	ms	Effective hardware reset period
T11	1	-	-	ms	Power off time between AVEE and VDDI

9. Description of Function

9.1. Display Mode

9.1.1. Power Mode

Item	Code value
Sleep in	0x10
Sleep out	0x11
Display on	0x29
Display off	0x28

9.1.2. Command Enable Mode

9.1.2.1. MAUCCTR (CMD1 F0h): Manufacture command Enable

Instruction	R/W	Address		Parameter								
		MIPI	Other	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
MAUCCTR	W	F0h	F000h	-	1	0	1	0	1	0	1	0
			F001h	-	-	-	-	EN_CMD2	PAGE[3:0]			

Description	This command is used to enable the access of CMD2 page. **EN_CMD2:** Enable access of CMD2 page. **EN_CMD2** / **Function**: 0h Disable; 1h Enable **PAGE[3:0]:** CMD2 Page selection. **PAGE[3:0]** / **Function**: 0h CMD2 Page0; 1h CMD2 Page1; 2h CMD2 Page2; 3h CMD2 Page3; Others Reserved
Restriction	-
Default	**Status**: Power On Sequence — **Default Value**: F000h AAh; F001h 00h

9.1.2.2. SCACTRL (CMD1 69h): Scaling up Control

Instruction	R/W	Address		Parameter								
		MIPI	Other	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
SCACTRL	R/W	69h	6900h	-	-	-	-	-	-	-	SC_MOD_SEL[1:0]	
Description	This command sets operation mode of MIPI clock lane during porch time. **SC_MOD_SEL[1:0]:** Scaling up ratio selection. **SC_MOD_SEL[1:0]** / **Function**: 0h Off; 1h 1.5x scaling up; 2h 1.33x scaling up; Others Reserved											
Restriction	-											
Default	**Status**: Power On Sequence — **Default Value**: 6900h 00h											

9.1.3. BIST Mode

9.1.3.1. BISTONOFF (CMD2 Page1 C4h): BIST On/Off Control

Instruction	R/W	Address		Parameter								
		MIPI	Other	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
BISTONOFF	R/W	C4h	C400h	-	1	0	1	0	0	1	0	1
			C401h	-	0	1	0	1	0	1	0	1
			C402h	-	-	-	-	-	-	-	-	BION1
			C403h	-	BION2	-	-	-	-	-	-	-
Description	This command is used to control BIST function (Free Run mode). BIST function enable step: 1. Enter Sleep-In (10h) mode and stop MIPI video data. 2. Setting PATENICYC[1:0] and BISTPATEN[11:0] to control the display cycle time and pattern.											

	3. Setting BION1 = "1" and BION2 = "1", the driver IC will start to run the BIST function. BIST function disable step: 1. Setting BION1 = "0" and BION2 = "0", the driver IC will return to normal function. 2. Sending MIPI video data and enter Sleep-Out (11h) mode for normal display.
Restriction	-
Default	**Status** / **Default Value** Power On Sequence: C400h AAh; C401h 55h; C402h 00h; C403h 00h

9.1.3.2. BISTSET (CMD2 Page1 C5h): BIST Control

Instruction	R/W	Address		Parameter								
		MIPI	Other	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
BISTSET	R/W	C5h	C500h	-	0	0	PATENICYC[1:0]		BISTPATEN[11:8]			
			C501h	-	BISTPATEN[7:0]							
			C502h	-	GRAY_LEVEL[7:0]							

Description

This command is used to set the display pattern in BIST function.

PATENICYC[1:0]: Cycle time between each display pattern.

PATENICYC[1:0]	Pattern cycle time
0h	256 Frame
1h	512 Frame
2h	1024 Frame
3h	2048 Frame

BISTPATEN[11:0]: Select the display pattern in BIST function.

BISTPATEN[11:0]	Description
BISTPATEN[0]	Red pattern
BISTPATEN[1]	Green pattern
BISTPATEN[2]	Blue pattern
BISTPATEN[3]	Black pattern
BISTPATEN[4]	Gray Level pattern (Set by BIST_GRAY_LEVEL[7:0])
BISTPATEN[5]	Vertical Gradation pattern
BISTPATEN[6]	Horizontal Gradation pattern
BISTPATEN[7]	Color Bar pattern
BISTPATEN[8]	Crosstalk with boundary pattern
BISTPATEN[11:9]	Reserved

Note1: *the patterns which the bit number of BISTPATEN[8:0] is set to "1" will display and change automatically.*

Note2: *When BISTPATEN[11:0]=12'h000, display pattern will be black pattern.*

GRAY_LEVEL[7:0]: Set the gray level when BISTPATEN[4] ="1" in BIST function.

GRAY_LEVEL[7:0]	Description
00h	Gray Level: 00h
01h	Gray Level: 01h

	02h	Gray Level: 02h
	:	:
	FDh	Gray Level: FDh
	FEh	Gray Level: FEh
	FFh	Gray Level: FFh
Restriction	-	
Default	Status	Default Value
	Power On Sequence	C500h 00h
		C501h 08h
		C502h FFh

9.2. Brightness Control (BC) Functions

9.2.1. BCCTR (CMD2 Page1 C2h): Brightness Control

Instruction	R/W	Address		Parameter								
		MIPI	Other	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
BCCTR	R/W	C2h	C200h	-							EM_WD_0[9:8]	
			C201h	-	EM_WD_0[7:0]							
			C202h	-							EM_WD_1[9:8]	
			C203h	-	EM_WD_1[7:0]							
			C204h	-							EM_WD_2[9:8]	
			C205h	-	EM_WD_2[7:0]							

Description

This command is used to adjust emission duty to adjust brightness.

EM_WD_x[9:0]: The percentage of emission duty.

EM_WD_x[9:0]	The percentage of emission duty
0h	1/1024
1h	2/1024
:	:
3FEh	1023/1024
3FFh	1024/1024

Restriction: EM_WD_1[9:0], EM_WD_2[9:0] and EM_WD_3[9:0] must be equal.

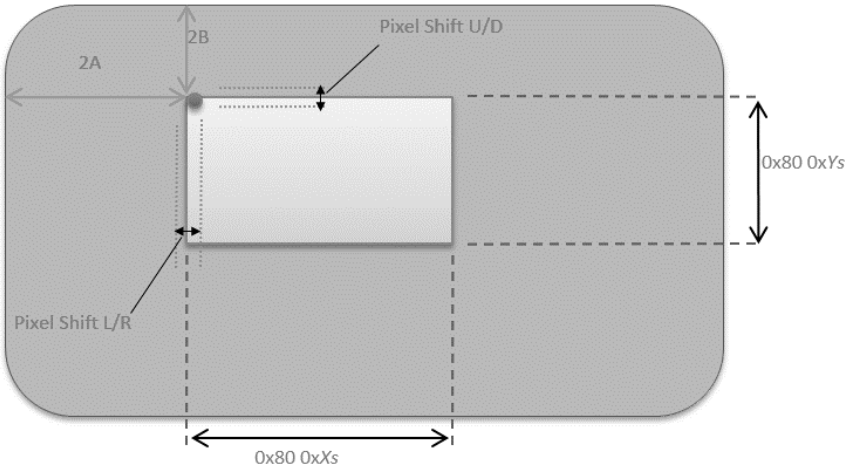
Default

Status	Default Value	
Power On Sequence	C200h	03h
	C201h	FFh
	C202h	03h
	C203h	FFh
	C204h	03h
	C205h	FFh

9.3. Display Active-Area (AA) Control

Item	Description	Address
Resolution	X- axis: support 4N, N = 160~480	CMD1 80h NC[8:0]
	Y- axis: support 4M, M = 120~270	CMD1 80h NL[8:0]
Display start point	X- axis start point	CMD1 2Ah

	Y- axis start point	CMD1 2Bh
Pixel shift	±16 pixels, step = 1 pixel	CMD2 Page0 B4h

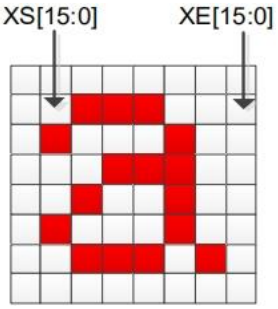


9.3.1. RESCTRL (CMD1 80h): Resolution Control

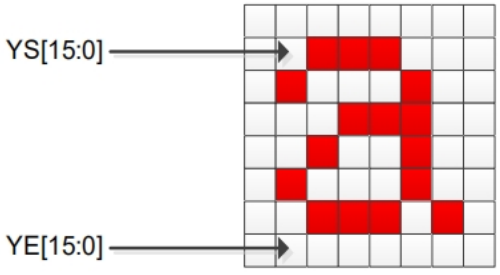
Instruction	R/W	Address		Parameter								
		MIPI	Other	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
RESCTRL	W	80h	8000h	-	-	-	-	-	-	-	-	1
			8001h	-	NC[7:0]							
			8002h	-	NL[7:0]							
			8003h	-	-	-	-	NC[8]	-	-	-	NL[8]
Description	This command is used to set panel type and display resolution. **NC[8:0]:** X-axis resolution = NC[8:0]*4. **NL[8:0]:** Y-axis resolution = NL[8:0]*4.											
Restriction	Resolution switch is only valid in Sleep in mode.											
Default	**Status**	**Default Value**										
	Power On Sequence	8000h	01h									
		8001h	E0h									
		8002h	0Eh									
		8003h	11h									

9.3.2. CASET (CMD1 2Ah): Column Address Set

Instruction	R/W	Address		Parameter								
		MIPI	Other	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
CASET	R/W	2Ah	2A00h	-	XS[15:8]							
			2A01h	-	XS[7:0]							
			2A02h	-	XE[15:8]							
			2A03h	-	XE[7:0]							
Description	This command indicates display start position of display module in columns. **XS[15:0]:** Display line start position. **XE[15:0]:** Display line end position.											

<table>
<tr><td></td><td> 
</td></tr>
<tr><td>Restriction</td><td>1. XS[15:0] must be equal to or less than XE[15:0]. When XS[15:0] or XE[15:0] is greater than maximum like below, data of out of range will be ignored. For example:
NC = “1E0h”; NL = “10Eh” (Resolution = 1920x1080)
Parameter range = 0 ≤ XS[15:0] ≤ XE[15:0] ≤ 1919 (77Fh)
2. When display module is on distribute driving mode, XS[15:0] and XE[15:0] should follow the rule as below:
XS[15:0]= 0 + 4N, N=integer
XE[15:0]= 3 + 4N, N=integer</td></tr>
<tr><td>Default</td><td><table>
<tr><th>Status</th><th colspan="2">Default Value</th></tr>
<tr><td rowspan="4">Power On Sequence</td><td>2A00h</td><td>00h</td></tr>
<tr><td>2A01h</td><td>00h</td></tr>
<tr><td>2A02h</td><td>07h</td></tr>
<tr><td>2A03h</td><td>7Fh</td></tr>
</table></td></tr>
</table>

9.3.3. RASET (CMD1 2Bh): Row Address Set

<table>
<tr><th rowspan="2">Instruction</th><th rowspan="2">R/W</th><th colspan="2">Address</th><th colspan="9">Parameter</th></tr>
<tr><th>MIPI</th><th>Other</th><th>D15-D8</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td rowspan="4">RASET</td><td rowspan="4">R/W</td><td rowspan="4">2Bh</td><td>2B00h</td><td>-</td><td colspan="9">YS[15:8]</td></tr>
<tr><td>2B01h</td><td>-</td><td colspan="9">YS[7:0]</td></tr>
<tr><td>2B02h</td><td>-</td><td colspan="9">YE[15:8]</td></tr>
<tr><td>2B03h</td><td>-</td><td colspan="9">YE[7:0]</td></tr>
<tr><td>Description</td><td colspan="12">This command indicates display start position of display module in rows.
YS[15:0]: Display line start position.
YE[15:0]: Display line end position.
 
</td></tr>
<tr><td>Restriction</td><td colspan="12">1. YS[15:0] must be equal to or less than YE[15:0]. When YS[15:0] or YE[15:0] is greater than maximum like below, data of out of range will be ignored. For example:
NC = “1E0h”; NL = “10Eh” (Resolution = 1920x1080)
Parameter range = 0 ≤ YS[15:0] ≤ YE[15:0] ≤ 1079 (437h)
2. When display module is on distribute driving mode, YS[15:0] and YE[15:0] should follow the rule</td></tr>
</table>

	as below: YS[15:0]= 0 + 4N, N=integer YE[15:0]= 3 + 4N, N=integer
Default	**Status** / **Default Value** Power On Sequence: 2B00h 00h; 2B01h 00h; 2B02h 04h; 2B03h 37h

9.3.4. PXLSHIFTCTR (CMD2 Page0 B4h): Pixel Shift Control

Instruction	R/W	Address		Parameter								
		MIPI	Other	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0
PXLSHIFTCTR	R/W	B4h	B400h	-	PIXEL_SHIFT_X_DIR	-	-	PIXEL_SHIFT_X_COUNT[4:0]				
			B401h	-	PIXEL_SHIFT_Y_DIR	-	-	PIXEL_SHIFT_Y_COUNT[4:0]				

Description

This command is used to control pixel shift.

PIXEL_SHIFT_X_DIR: Pixel shift direction of X-axis

PIXEL_SHIFT_X_DIR	Pixel Shift Direction of X-axis
0h	Left
1h	Right

PIXEL_SHIFT_X_COUNT[4:0]: Pixel shift of X-axis

PIXEL_SHIFT_X_COUNT[4:0]	Pixel Shift of X-axis
0h	0 pixels
1h	1 pixel
2h	2 pixels
:	
Eh	14 pixels
Fh	15 pixels
10h	16 pixels
Others	Reserved

PIXEL_SHIFT_Y_DIR: Pixel shift direction of Y-axis

PIXEL_SHIFT_Y_DIR	Pixel Shift Direction of Y-axis
0h	Up
1h	Down

PIXEL_SHIFT_Y_COUNT[4:0]: Pixel shift of Y-axis

PIXEL_SHIFT_Y_COUNT[4:0]	Pixel Shift of Y-axis
0h	0 lines
1h	1 line
2h	2 lines
:	
Eh	14 lines
Fh	15 lines

	10h	16 lines	
	Others	Reserved	
Restriction	-		
Default	**Status**	**Default Value**	
	Power On Sequence	B400h	00h
		B401h	00h

9.4. MADCTL (CMD1 36h): Set Scan Direction

Instruction	**R/W**	**Address**		**Parameter**								
		MIPI	**Other**	**D15-D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
MADCTL	R/W	36h	3600h	-	-	-	-	-	0	-	RSMX	RSMY

Description

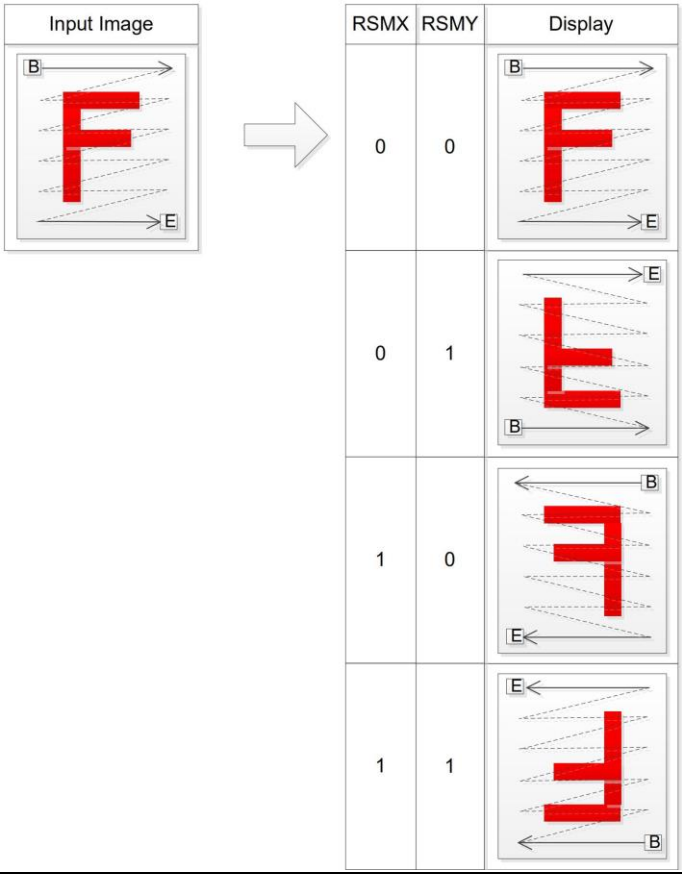
This command set scan direction of source and gate

RSMX: Horizontal Flip.

RSMX	**Scan direction**
0h	Normal Display
1h	Horizontal Flip

RSMY: Vertical Flip.

RSMY	**Scan direction**
0h	Normal Display
1h	Vertical Flip



Restriction	-		
Default	**Status**	**Default Value**	
	Power On Sequence	3600h	00h

9.5. Read module display status

9.5.1. RDDPM (CMD1 0Ah): Read Display Power Mode

<table>
<tr><th rowspan="2">Instruction</th><th rowspan="2">R/W</th><th colspan="2">Address</th><th colspan="10">Parameter</th></tr>
<tr><th>MIPI</th><th>Other</th><th>D15-D8</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td>RDDPM</td><td>R</td><td>0Ah</td><td>0A00h</td><td>-</td><td>BSTON</td><td>-</td><td>-</td><td>SLPON</td><td>NOR</td><td>DISPON</td><td>-</td><td>-</td></tr>
<tr><td>Description</td><td colspan="13">This command indicates the status of display driver’s power and operation mode:
BSTON: Boost Status.
<table><tr><th>BSTON</th><th>Comment</th></tr><tr><td>0h</td><td>Boost off</td></tr><tr><td>1h</td><td>Boost on</td></tr></table>
SLPON: Sleep in/out.
<table><tr><th>SLPON</th><th>Comment</th></tr><tr><td>0h</td><td>Sleep in</td></tr><tr><td>1h</td><td>Sleep out</td></tr></table>
NOR: Display Normal Mode on/off.
<table><tr><th>NOR</th><th>Comment</th></tr><tr><td>0h</td><td>Display Normal Off</td></tr><tr><td>1h</td><td>Display Normal On</td></tr></table>
DISPON: Display On/Off.
<table><tr><th>DISPON</th><th>Comment</th></tr><tr><td>0h</td><td>Display Off</td></tr><tr><td>1h</td><td>Display On</td></tr></table></td></tr>
<tr><td>Restriction</td><td colspan="13">-</td></tr>
<tr><td>Default</td><td colspan="13"><table><tr><th colspan="2">Status</th><th colspan="2">Default Value</th></tr><tr><td colspan="2">Power On Sequence</td><td>0A00h</td><td>08h</td></tr></table></td></tr>
</table>

9.5.2. MERR (CMD1 68h): MIPI Error Report

<table>
<tr><th rowspan="2">Instruction</th><th rowspan="2">R/W</th><th colspan="2">Address</th><th colspan="9">Parameter</th></tr>
<tr><th>MIPI</th><th>Other</th><th>D15-D8</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th></tr>
<tr><td rowspan="2">MERR</td><td rowspan="2">R</td><td rowspan="2">68h</td><td>6800h</td><td>-</td><td colspan="7">ERPA[15:8]</td></tr>
<tr><td>6801h</td><td>-</td><td colspan="7">ERPA[7:0]</td></tr>
<tr><td>Description</td><td colspan="11">This command is used to read DSI errors of MIPI port A.
<table><tr><th>Symbol</th><th>Description</th></tr><tr><td>ERPA[15]</td><td>DSI Protocol Violation</td></tr><tr><td>ERPA[14]</td><td>Reserved</td></tr><tr><td>ERPA[13]</td><td>Invalid Transmission Length</td></tr><tr><td>ERPA[12]</td><td>DSI VC ID Invalid</td></tr><tr><td>ERPA[11]</td><td>DSI Data Type Not Recognized</td></tr><tr><td>ERPA[10]</td><td>Payload Checksum Error (Long packet only)</td></tr><tr><td>ERPA[9]</td><td>ECC Error, multi-bit (detected, not corrected)</td></tr></table></td></tr>
</table>

	ERPA[8]	ECC Error, single-bit (detected, not corrected)	
	ERPA[7]	Contention Detected	
	ERPA[6]	False Control Error	
	ERPA[5]	Peripheral Timeout Error	
	ERPA[4]	Low-Power Transmit Sync Error	
	ERPA[3]	Escape Mode Entry Command Error	
	ERPA[2]	EoT Sync Error	
	ERPA[1]	SoT Sync Error	
	ERPA[0]	SoT Error	
Restriction	-		
Default	**Status**	**Default Value**	
	Power On Sequence	6800h	00h
		6801h	00h

10. Optical Characteristics

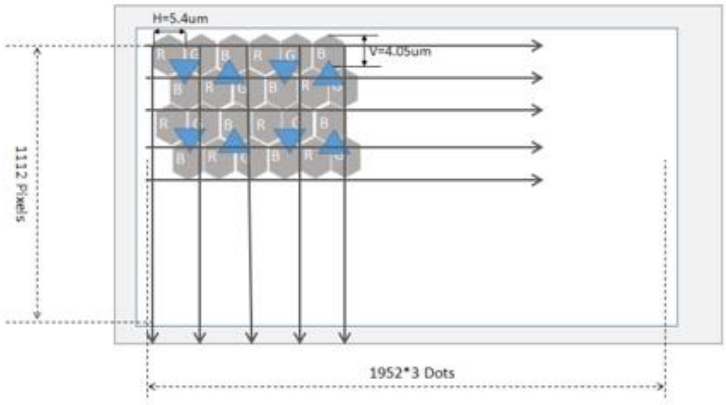
Item			**Specification**
Brightness (W255)	L		300±20% cd/m2
Uniformity	W255, 9 points		>85%
View Angle	W255 Lum Decay (< 50%)		-45°~45°
	W255 Color Shift(Δu'v' < 0.025)		-20°~20°
Contrast	CR		>10000:1
Color Coordinate	Red	CIE-x	0.63±0.05
		CIE-y	0.34±0.05
	Green	CIE-x	0.20±0.05
		CIE-y	0.65±0.05
	Blue	CIE-x	0.15±0.05
		CIE-y	0.09±0.05
	White	CIE-x	0.31±0.05
		CIE-y	0.33±0.05
Color Gamut (NTSC)			>80%
Color Temperature			>5000K

Notes:

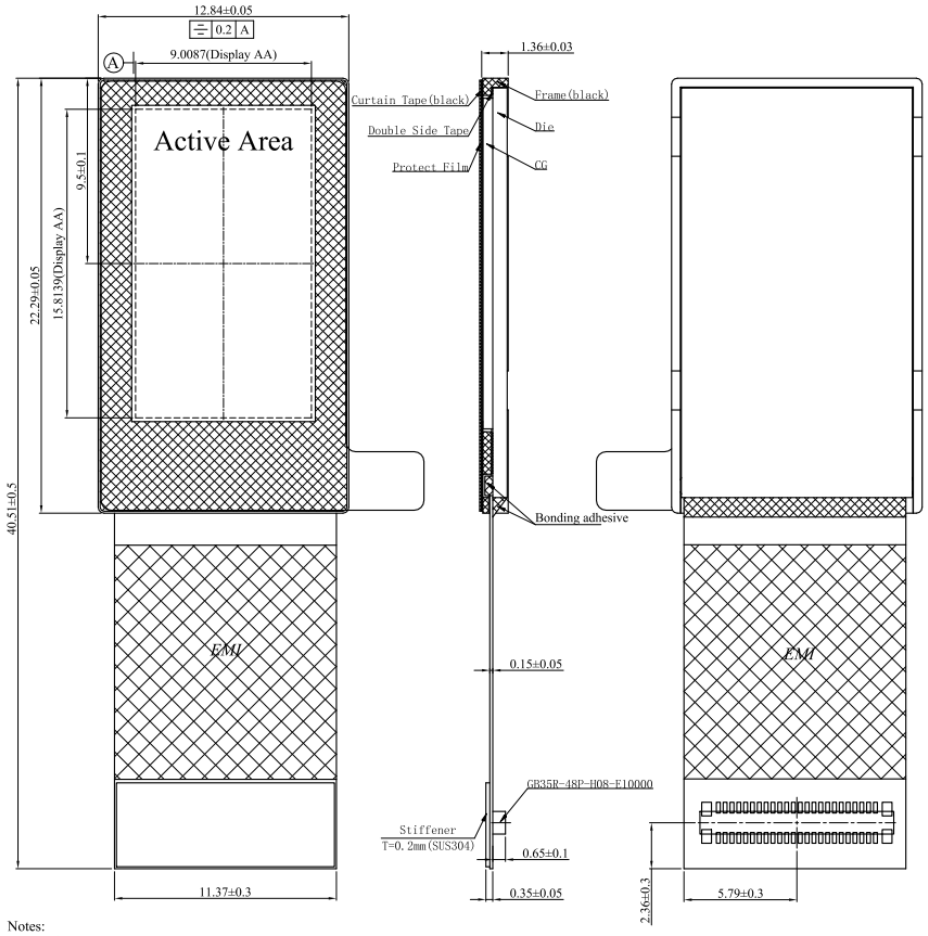
1. *The brightness of the product will be measured after 5 minutes of stabilization for the white screen at room temperature.*
2. *The formula of the brightness uniformity at 9 points of the white screen is Uniformity = 1 - (Max. - Min.)/(Ave.), and the Max., Min. and Ave. represent the maximum, minimum and average of the brightness of 9 points, respectively.*
3. *Measurement temperature: 25℃.*
4. *Measurement point (Except for uniformity): Screen center point.*
5. *All white display: All RGB signal data is set to High.*
6. *All black display: All RGB signal data is set to Low.*

7. *Luminance and chromaticity: Measure the luminance and chromaticity in all white display.*
8. *Contrast: Measure the luminance in all white display (@150 cd/m^2) and all black display, and substitute them into the formula below.*
9. *Contrast = Luminance in all white display/Luminance in all black display.*

11. Pixel Alignment



12. Module Drawing (Unit: mm)



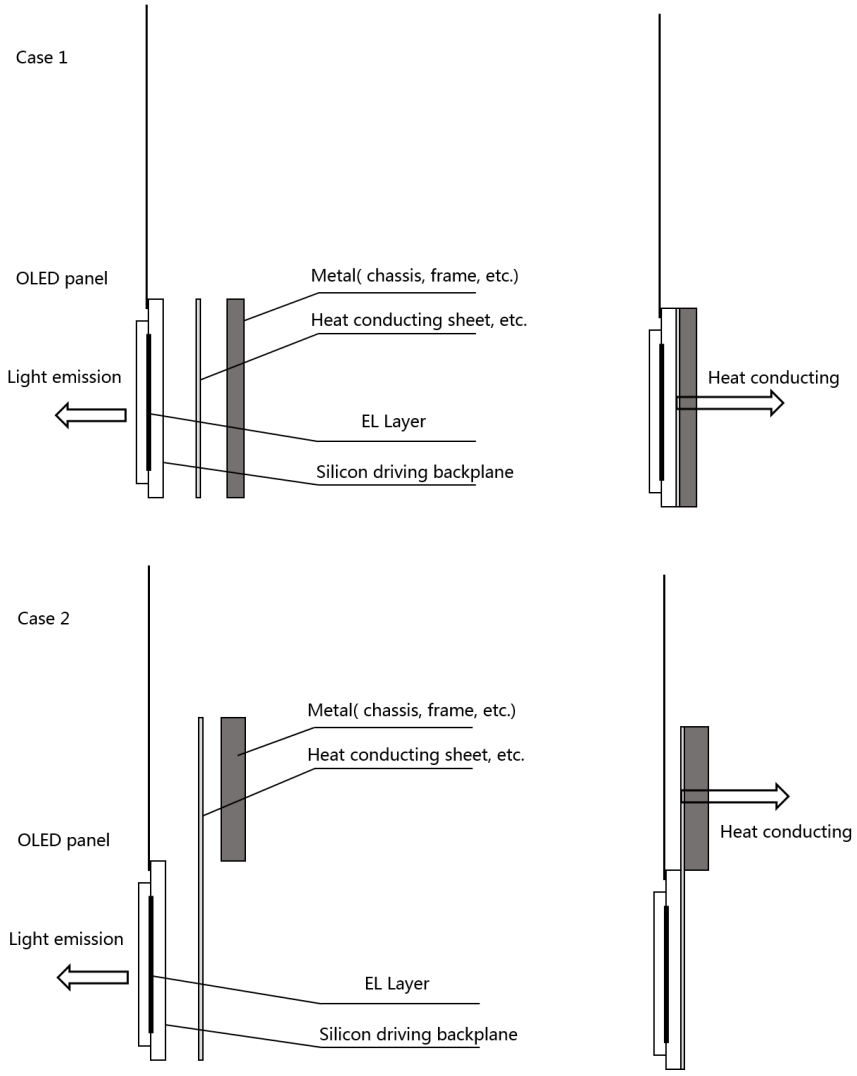
Notes:
1、Display：0.71 1920*1080 Micro OLED;
2、Connector：GB35R-48P-H08-E10000;
3、General Tolerance：±0.1;
4、Conformity with RoHS and Halogen Free.

13. Recommended Items

13.1. Suppression of the Panel Temperature

Temperature of organic EL panel tends to rise due to power consumption (heat generation) by the EL emission layer and the integrated silicon drive circuit. The temperature rise may cause luminance rise at initial state, or luminance drop by over time.

The temperature change in panel can be suppressed by establishing a thermal connection between panel rear surface (silicon substrate surface) and metal (chassis, frame, metal structure, etc.) at panel mount area, and the heat conducting sheet size can be changed. So highly recommend the heat conductive sheet between them as show in below. In order to ensure the normal operation of the screen, the heat dissipation must be done to ensure that the screen temperature < 60℃.



14. Notes on Handling

14.1.Static charge prevention

Be sure to take the following protective measures. Organic EL panels are easily damaged by static charges.

(1) Use non-chargeable gloves.

(2) Use a wrist strap connecting ground when handling.

(3) Do not touch any electrodes on the panel.

(4) Wear non-chargeable clothes and conductive shoes.

(5) Install grounded conductive mats on the working floor and working table.

(6) Keep the panel away from any charged materials.

14.2.Protection from dust and dirt

(1) Operate in a clean environment.

(2) Do not touch the panel surface. The surface is easily scratched.When cleaning on panel surface, use a clean-room wiper with isopropyl alcohol. Be careful not to leave stains on the surface.

(3) Use ionized air to blow dust off the panel surface.

14.3.Others

(1) Do not drop the module.

(2) Do not twist or bend the module.

(3) Keep the module away from heat sources.

(4) Not be close the module to water or other solvents.

(5) Do not store or use the module at high temperatures or high humidity circumstance, as the circumstance may affect module specifications.

(6) When disposing of this, regard it as industrial waste and please comply with related regulations.

(7) Do not store or use the panel in reactive chemical substance (including alcohol) environments, as these may affect the specifications.