SPECIFICATION

[◉] Preliminary Specification
[ ] Final Specification

Description **21.3” 2048x2560(RGB) TFT-LCD Module**

Part Number **P2130QSF2MA01**

Customer		Industrial Product Dept, PDBU Tianma Microelectronics Co., Ltd.	
Signatures	Date	Approved By	Date
		Guanchen Zhu	2023-9-7
		Reviewed By	
		Guanchen Zhu	2023-9-7
		Prepared By	
		Jie Zhou	2023-9-6
Comments:			

* This cover page is for your Comments and Signatures back to TIANMA.

REVISION HISTORY

Rev	Date	Page	Revision Items	Editor
1.0	2023/4/26	-	Preliminary spec	Lixian.Xu
1.1	2023/9/6	-	P2 2. General Specifications Weight T.B.D.=>(2260)±10% Luminance T.B.D.=> 1250 Power Consumption(LCD): Typ. 7.56, Max. 10.8 Power Consumption(Backlight): Typ. (40.8), Max. (43.0) P18 7.5 Display Positions Add content about display positions. P21 8. Optical Characteristics Contrast Ratio Min. 1400=> Min. 1600 P24 9. Reliability Test Low Temperature Operation Ta=-10℃ => Ta=0℃ P26 10.2 Markings Update marking information. P27 11. Packing Instruction Update packing information.	Zhou Jie

CONTENTS

1. Summary

1.1 General Description

This is a 21.3 inch a-Si TFT-LCD module with Normal- Black technology. It is composed of a TFT-LCD panel, a driver circuit, POL, PCB and a LED backlight unit.

1.2 Application

- Color monitor system

1.3 Features

- Ultra-wide viewing angle : Super Fine TFT(SFT)
- High resolution
- High luminance
- Interface：LVDS(4 ports)
- This product will comply with the European RoHS Directive (2011/65/EU) and Delegated Directive (2015/863/EU, Amending Annex II of 2011/65/EU)

2. General Specifications

1.1

Feature		Spec	Unit
Display Spec	Size	21.3 inch	
	Resolution	2048x2560(RGB)	
	Pixel Pitch	0.165x0.165	mm
	TFT Active Area	337.92x422.40	mm
	Technology Type	a-Si	
	Pixel Configuration	R.G.B horizontal Stripe	
	Display Mode	SFT, Normally Black	
	Surface Treatment	AG	
	Viewing Direction	ALL	
Mechanical Characteristics	LCM (W x H x D)	354.9x442.3x20.9	mm
	Weight	(2260)	g
Optical Characteristics	Luminance	Typ. 1250	cd/m^2
	Contrast Ratio	Typ:2200	
	NTSC	Typ:72	%
	Viewing Angle	Typ:88/88/88/88	degree
Electrical Characteristics	Interface	LVDS(4 port)	
	Color Depth	1073.74M(Real 10bit)	color
	Power Consumption	LCD: Typ. 7.56, Max. 10.8 Backlight: Typ. 40.8, Max. 43.0	W

Table 2.1 General TFT Specifications

Note 1: Requirements on Environmental Protection: Q/S0002.

Note 2: LCM weight tolerance: ± 10%

3. LCD Module Block Diagram

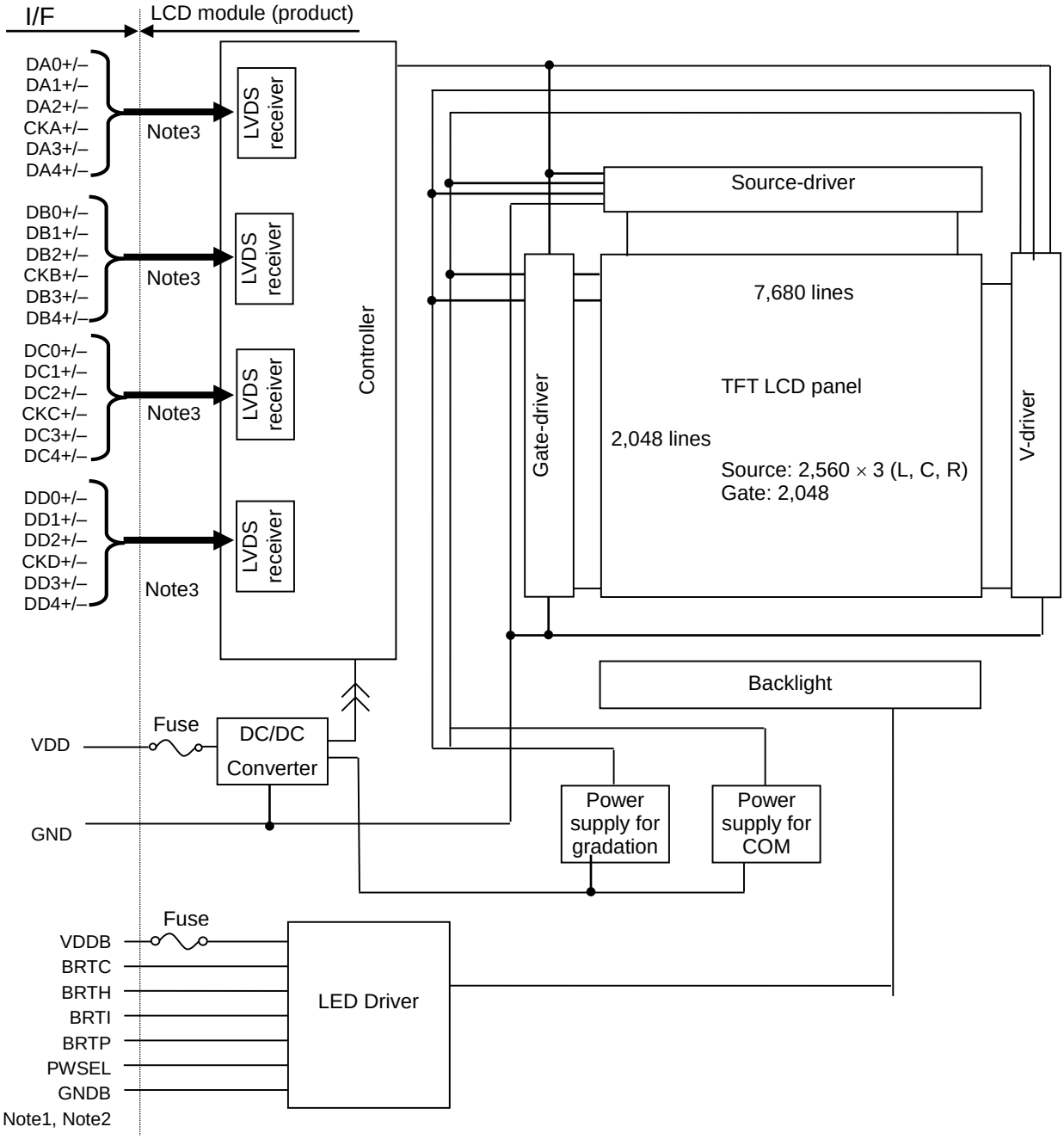


Figure 3.1 LCD Module Block Diagram

Note1: Relations between GND (Signal ground), FG (Frame ground) and GNDB (LED driver ground) in the LCD module are as follows.

GND - FG	Connected
GND - GNDB	Not connected
FG - GNDB	Not connected

Note2: GND, FG and GNDB must be connected to customer equipment's ground, and it is recommended that these grounds to be connected together in customer equipment.

Note3: Each pair of the LVDS signal lines has 100Ω terminating resistance.

4. Input / Output Terminals

4.1 CN1/CN2/CN3 Pin assignment (LCD Interface)

4.1.1 CN1 Pin assignment

CN1 Connector Information	
LCD Module connector	MSAKS24020P41
Matching connector	FI-RE41HL

Table 4.1.1.1 CN1 Connector information

PIN #	Symbol	P/I	Description	Remark
1	GND	P	GND	Note4
2	GND	P	GND	--
3	GND	P	GND	--
4	DC0-	I	LVDS differential data input -	Note3
5	DC0+	I	LVDS differential data input +	Note3
6	GND	P	GND	--
7	DC1-	I	LVDS differential data input -	Note3
8	DC1+	I	LVDS differential data input +	Note3
9	GND	P	GND	--
10	DC2-	I	LVDS differential data input -	Note3
11	DC2+	I	LVDS differential data input +	Note3
12	GND	P	GND	--
13	CKC-	I	LVDS differential CLK input -	Note3
14	CKC+	I	LVDS differential CLK input +	Note3
15	GND	P	GND	--
16	DC3-	I	LVDS differential data input -	Note3
17	DC3+	I	LVDS differential data input +	Note3
18	GND	P	GND	--
19	DC4-	I	LVDS differential data input -	Note3
20	DC4+	I	LVDS differential data input +	Note3
21	GND	P	GND	--
22	DD0-	I	LVDS differential data input -	Note3
23	DD0+	I	LVDS differential data input +	Note3
24	GND	P	GND	--
25	DD1-	I	LVDS differential data input -	Note3
26	DD1+	I	LVDS differential data input +	Note3
27	GND	P	GND	--
28	DD2-	I	LVDS differential data input -	Note3
29	DD2+	I	LVDS differential data input +	Note3
30	GND	P	GND	--
31	CKD-	I	LVDS differential CLK input -	Note3
32	CKD+	I	LVDS differential CLK input +	Note3
33	GND	P	GND	--
34	DD3-	I	LVDS differential data input -	Note3

PIN #	Symbol	P/I	Description	Remark
35	DD3+	I	LVDS differential data input +	Note3
36	GND	P	GND	--
37	DD4-	I	LVDS differential data input -	Note3
38	DD4+	I	LVDS differential data input +	Note3
39	GND	P	GND	--
40	GND	P	GND	Note3
41	GND	P	GND	Note3

Table 4.1.1.2 CN1 Pin Assignment for LCD Interface

Note1: P/I definition: I---Input, P---Power/Ground
Note2: All of the GND pins should be connected to the system ground.
Note3: Twist pair wires with 100Ω (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.
Note4: All GND and VCC terminals should be used without any non-connected lines.

4.1.2 CN2 Pin assignment

CN2 Connector Information	
LCD Module connector	MSAKS24020P51
Matching connector	FI-RE51HL

Table 4.1.2.1 CN2 Connector information

PIN #	Symbol	P/I	Description	Remark
1	GND	P	GND	Note4
2	GND	P	GND	--
3	GND	P	GND	--
4	DA0-	I	LVDS differential data input -	Note3
5	DA0+	I	LVDS differential data input +	Note3
6	GND	P	GND	--
7	DA1-	I	LVDS differential data input -	Note3
8	DA1+	I	LVDS differential data input +	Note3
9	GND	P	GND	--
10	DA2-	I	LVDS differential data input -	Note3
11	DA2+	I	LVDS differential data input +	Note3
12	GND	P	GND	--
13	CKA-	I	LVDS differential CLK input -	Note3
14	CKA+	I	LVDS differential CLK input +	Note3
15	GND	P	GND	--
16	DA3-	I	LVDS differential data input -	Note3
17	DA3+	I	LVDS differential data input +	Note3
18	GND	P	GND	-
19	DA4-	I	LVDS differential data input -	Note3
20	DA4+	I	LVDS differential data input +	Note3
21	GND	P	GND	--
22	DB0-	I	LVDS differential data input -	Note3

PIN #	Symbol	P/I	Description	Remark
23	DB0+	I	LVDS differential data input +	Note3
24	GND	P	GND	--
25	DB1-	I	LVDS differential data input -	Note3
26	DB1+	I	LVDS differential data input +	Note3
27	GND	P	GND	--
28	DB2-	I	LVDS differential data input -	Note3
29	DB2+	I	LVDS differential data input +	Note3
30	GND	P	GND	--
31	CKB-	I	LVDS differential CLK input -	Note3
32	CKB+	I	LVDS differential CLK input +	Note3
33	GND	P	GND	-
34	DB3-	I	LVDS differential data input -	Note3
35	DB3+	I	LVDS differential data input +	Note3
36	GND	P	GND	--
37	DB4-	I	LVDS differential data input -	Note3
38	DB4+	I	LVDS differential data input +	Note3
39	GND	I	GND	--
40	GND	P	GND	--
41	RSVD	/	For internal use, Keep this pin Open.	
42	RSVD	/	For internal use, Keep this pin Open.	
43	RSVD	/	For internal use, Keep this pin Open.	
44	RSVD	/	For internal use, Keep this pin Open.	
45	GND	P	GND	
46	GND	P	GND	
47	GND	P	GND	
48	RSVD	/	For internal use, Keep this pin Open.	
59	RSVD	/	For internal use, Keep this pin Open.	
50	RSVD	/	For internal use, Keep this pin Open.	
51	GND	P	GND	

Table 4.1.2.2 CN2 Pin Assignment for LCD Interface

Note1: P/I definition: I---Input, P---Power/Ground.
Note2: All of the GND pins should be connected to the system ground.
Note3: Twist pair wires with 100Ω (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.
Note4: All GND and VCC terminals should be used without any non-connected lines.

4.1.3 CN3 Pin assignment

CN3 Connector Information	
LCD Module connector	53261-1271
Matching connector	51021-1200

Table 4.1.3.1 CN3 Connector information

PIN #	Symbol	P/I	Description	Remark
1	GND	P	Signal ground	--
2	GND	P		--
3	GND	P		--
4	GND	P		--
5	GND	P		--
6	GND	P		--
7	VDD	P	Power supply	--
8	VDD	P		--
9	VDD	P		--
10	VDD	P		--
11	VDD	P		--
12	VDD	P		--

Table 4.1.3.2 CN3 Pin Assignment for LCD Interface

Note1: P/I definition: I---Input, P---Power/Ground
Note2: All VDD and GND terminals should be used without any non-connected lines.

4.2 CN201/CN202 Pin assignment (LED Driver Interface)

4.2.1 CN201 Pin assignment

CN201 Connector Information	
LCD Module connector	DF3EA-10P-2H
Matching connector	DF3-10S-2C

Table 4.2.1.1 CN201 Connector information

PIN #	Symbol	P/I	Description	Remark
1	GNDB	P	LED driver ground	--
2	GNDB	P		--
3	GNDB	P		--
4	GNDB	P		--
5	GNDB	P		--
6	VDDB	P	Power supply	--
7	VDDB	P		--
8	VDDB	P		--
9	VDDB	P		--
10	VDDB	P		--

Table 4.2.1.2 CN201 Pin Assignment for LCD Interface

Note1: P/I definition: I---Input, P---Power/Ground
Note2: All VDDB and GNDB terminals should be used without any non-connected lines.

4.2.2 CN202 Pin assignment

CN202 Connector Information	
LCD Module connector	53261-0971
Matching connector	51021-0900

Table 4.2.2.1 CN202 Connector information

PIN #	Symbol	P/I/O	Description	Remark
1	PWSEL	I	Selection of luminance control signal method	--
2	GNDB	P	LED driver ground	--
3	BRTP	I	BRTP signal	--
4	BRTI	I	Luminance control terminal	--
5	BRTH	I		--
6	BRTC	I	Backlight ON/OFF control signal	--
7	N. C.	/	-	--
8	GNDB	P	LED driver ground	--
9	GNDB	P		--

Table 4.2.2.2 CN202 Pin Assignment for LCD Interface

Note1: P/I definition: I---Input, P---Power/Ground.
Note2: All of the GND pins should be connected to the system ground.
Note3: When VDDB is 0V or BRTC is Low, PWSEL must be set to Low or Open.
Note4: All GNDB terminals should be used without any non-connected lines.

4.3 Positions of socket

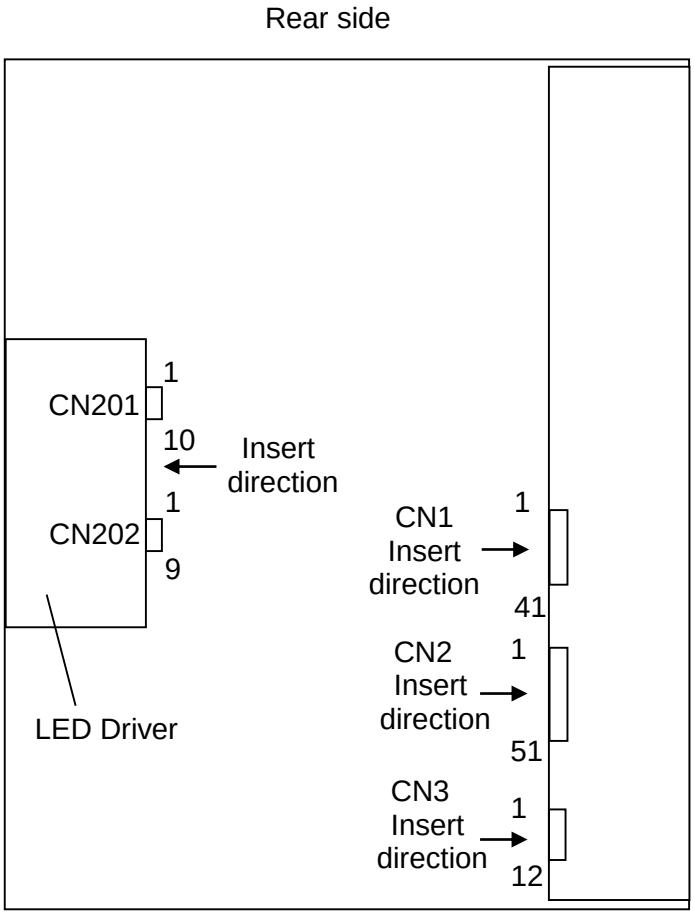


Figure 4.3.1 Position of aocket

Note1: The definition of 1st pin for CN201 and CN202 are different from datasheet of connector.

5. Absolute Maximum Ratings

GND=0V

Parameter			Symbol	Rating	Unit	Remarks
Power supply voltage	LCD panel signal processing board		VDD	-0.3 to +15.0	V	Ta= 25°C
	LED driver		VDDB	-0.3 to +28.0	V	
Input voltage for signals	LCD panel signal processing board Note1		Vi	-0.3 to +2.8	V	VDD= 12.0V Ta= 25°C
	LED driver	BRTI signal	VBI	-0.3 to +1.5	V	VDDB= 24.0V Ta= 25°C
		BRTP signal	VBP	-0.3 to +5.5	V	
		BRTC signal	VBC	-0.3 to +5.5	V	
		PWSEL signal	VBS	-0.3 to +5.5	V	
Storage temperature			Tst	-20 to +60	°C	-
Operating temperature		Center of front surface	TopF	0 to +60	°C	Note2
		Edge of front surface	TopF	0 to +65	°C	Note2
		Edge of rear surface	TopR	0 to +70	°C	Note3
Relative humidity Note4, Note6			RH	≤ 95	%	Ta ≤ 40°C
				≤ 85	%	40°C < Ta ≤ 50°C
				≤ 55	%	50°C < Ta ≤ 60°C
Absolute humidity Note4, Note6			AH	≤ 70 Note5	g/m^3	Ta > 60°C

Table 5.1 Absolute Maximum Ratings

Note1: DA0+/-, DA1+/-, DA2+/-, DA3+/-, DA4+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, DB4+/-, CKB+/-, DC0+/-, DC1+/-, DC2+/-, DC3+/-, DC4+/-, CKC+/-, DD0+/-, DD1+/-, DD2+/-, DD3+/-, DD4+/-, CKD+/-.
Note2: Measured at LCD panel surface (including self-heat).
Note3: Measured at LCD module's rear shield surface (including self-heat).
Note4: No condensation.
Note5: Water amount at Ta= 60°C and RH= 55%.
Note6: Rapid change of humidity and temperature may cause degradation of the image quality.

6. Electrical Characteristics

6.1 DC Characteristics for Panel Driving

(Ta=25℃)

Parameter		Symbol	min.	typ.	max.	Unit	Remarks
Power supply voltage		VDD	10.8	12.0	13.2	V	-
Power supply current		IDD	-	630 Note1	900 Note2	mA	at VDD= 12.0V
Permissible ripple voltage		VRP	-	-	200	mVp-p	for VDD Note3,4,5
Differential input threshold voltage	High	VTH	-	-	+100	mV	at VCM= 1.2V Note6,7
	Low	VTL	-100	-	-	mV	
Input voltage swing		VI	0	-	2.4	V	Note7
Terminating resistance		RT	-	100	-	Ω	-

Table 6.1.1 Operating Voltages

Note1: Checkered flag pattern [by IEC 61747-6].
Note2: Pattern for maximum current.
Note3: This product works even if the ripple voltage levels are over the permissible values, but there might be noise on the display image.
Note4: The permissible ripple voltage includes spike noise.
Note5: The load variation influence does not include.
Note6: Common mode voltage for LVDS driver.
Note7: DA0+/-, DA1+/-, DA2+/-, DA3+/-, DA4+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, DB4+/-, CKB+/-, DC0+/-, DC1+/-, DC2+/-, DC3+/-, DC4+/-, CKC+/-, DD0+/-, DD1+/-, DD2+/-, DD3+/-, DD4+/-, CKD+/-.

6.2 DC Characteristics for Backlight Driving

(Ta=25℃)

Parameter			Symbol	min.	typ.	max.	Unit	Remarks
Power supply voltage			VDDB	22.8	24.0	25.2	V	Note1
Power supply current			IDDB	-	1700	1790 Note2	mA	VDDB= 24.0V, At the maximum luminance control
Permissible ripple voltage			VRPB	-	-	200	mVp-p	for VDDB Note3, 4, 5
Input voltage for signals	BRTI signal		VBI	0	-	1.0	V	-
	BRTP signal	High	VBPH	2.0	-	5.25	V	
		Low	VBPL	0	-	0.8	V	
	BRTC signal	High	VBCH	2.0	-	5.25	V	
		Low	VBCL	0	-	0.8	V	
	PWSEL signal	High	VBSH	2.0	-	5.25	V	
		Low	VBSL	0	-	0.8	V	
Input current for signals	BRTI signal		IBI	-200	-	-50	μA	
	BRTP signal	High	IBPH	-	-	1,000	μA	
		Low	IBPL	-600	-	-	μA	
	BRTC signal	High	IBCH	-	-	300	μA	
		Low	IBCL	-300	-	-	μA	
	PWSEL signal	High	IPSH	-	-	1,000	μA	
		Low	IPSL	-600	-	-	μA	
LED life time			-	-	50000	-	Hrs	Note6

Table 6.2.1 LED Backlight Characteristics

Note1: When designing of the power supply, take the measures for prevention of surge voltage.
Note2: This value excludes peak current such as overshoot current.
Note3: This product works even if the ripple voltage levels are over the permissible values, but there might be noise on the display image.
Note4: The permissible ripple voltage includes spike noise.
Note5: The power supply lines (VDDB and GNDB) may have ripple voltage during luminance control of LED. There is the possibility that the ripple voltage produces acoustic noise and signal wave noise in audio circuit and so on.
Note6: Optical performance should be evaluated at Ta=25℃.Only If LED is driven by high current, high ambient temperature & humidity condition. The life time of LED will be reduced. Operating life means brightness goes down to 50% of initial brightness. Typical operating life time is an estimated data.

6.3 Luminance Control

6.3.1 Luminance control methods

(Ta= 25°C)

<table>
<tr><th>Method</th><th>Adjustment and luminance ratio</th><th>PWSEL terminal</th><th>BRTP terminal</th></tr>
<tr><td>Variable resistor control

Note1</td><td>• Adjustment
The variable resistor (R) for luminance control should be 10kΩ ±5%, 1/10W. Minimum point of the resistance is the minimum luminance and maximum point of the resistance is the maximum luminance.
The resistor (R) must be connected between BRTH-BRTI terminals.
 
• Luminance ratio Note3
<table><tr><th>Resistance</th><th>Luminance ratio</th></tr><tr><td>720Ω</td><td>10% (typ.)</td></tr><tr><td>10kΩ</td><td>100%</td></tr></table></td><td rowspan="2">High or Open</td><td rowspan="2">Open</td></tr>
<tr><td>Voltage control

Note1</td><td>• Adjustment
Voltage control method works, when BRTH terminal is 0V and VBI voltage is input between BRTI-BRTH terminals. This control method can carry out continuation adjustment of luminance. Luminance is the maximum when BRTI terminal is Open.
• Luminance ratio Note3
<table><tr><th>BRTI Voltage (VBI)</th><th>Luminance ratio</th></tr><tr><td>0.085V</td><td>10% (typ.)</td></tr><tr><td>1.0V</td><td>100%</td></tr></table></td></tr>
<tr><td>Pulse width modulation (PWM)

Note1
Note2
Note4</td><td>• Adjustment
Pulse width modulation (PWM) method works, when PWSEL terminal is Low and PWM signal (BRTP signal) is input into BRTP terminal. The luminance is controlled by duty ratio of BRTP signal. Keep BRTI and BRTH terminals Open when using PWM method.
• Luminance ratio Note3
<table><tr><th>Duty ratio</th><th>Luminance ratio</th></tr><tr><td>5%</td><td>5% (typ.)</td></tr><tr><td>100%</td><td>100%</td></tr></table></td><td>Low</td><td>BRTP signal</td></tr>
</table>

Table 6.3.1.1 Luminance control methods

Note1: In case of the variable resistor control method and the voltage control method, noises may appear on the display image depending on the input signals timing for LCD panel signal processing board. **Use Pulse width modulation (PWM) method, if interference noises appear on the display image!**

Note2: The LED driver will stop working, if the Low period of BRTP signal is more than 50ms while BRTC signal is High or Open. Then the backlight will not turn on anymore, even if BRTP signal is input again. This is not out of order. The LED driver will start to work when power is supplied again.

Note3: These data are the target values.

Note4: See "**6.3.2 Detail of BRTP timing**".

6.3.2 Detail of BRTP timing

(1) Timing diagrams

- Outline chart

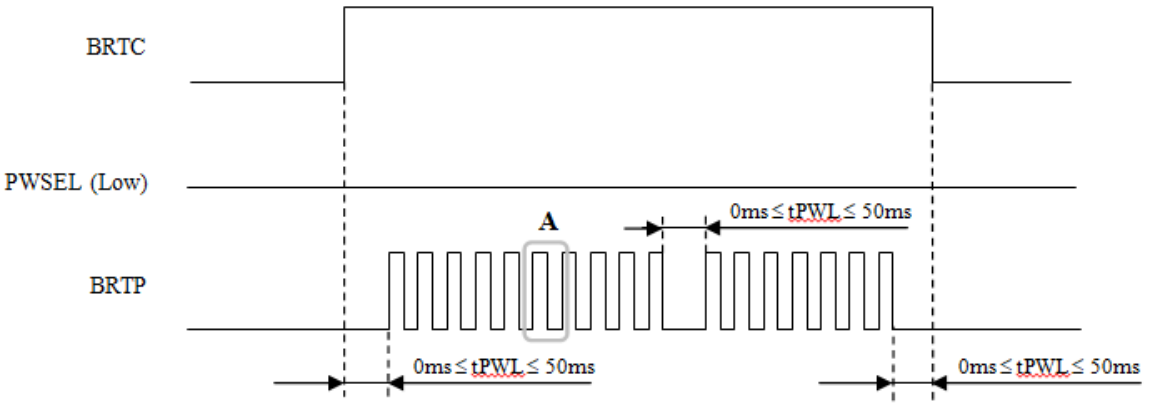


Figure 6.3.2.1 Outline chart

- Detail of **A** part

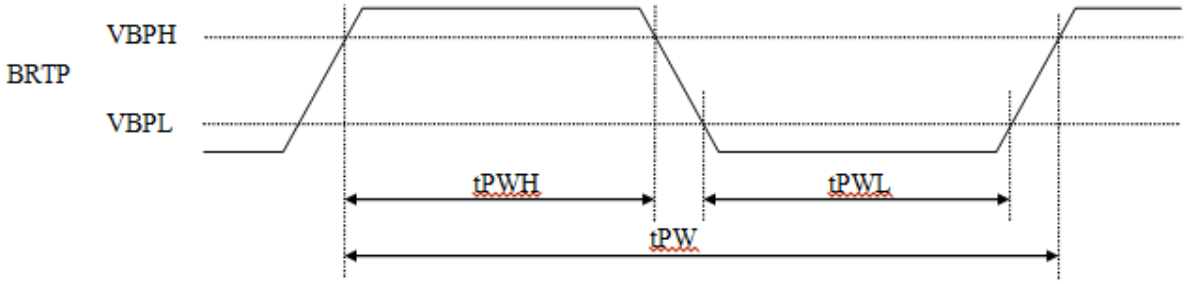


Figure 6.3.2.2 Detail of A part

(2) Each parameter

Parameter	Symbol	min.	typ.	max.	Unit	Remarks
PWM frequency	f_{PWM}	185	-	20k	Hz	Note1,2,3
PWM duty ratio	DR_{PWM}	5	-	100	%	Note4,5
PWM pulse width	tPWH	(2.5)	-	-	μs	Note1,4,5

Table 6.3.2.1 Each parameter

Note1: Definition of parameters is as follows.

$$f_{PWM} = \frac{1}{tPW} \quad , DR_{PWM} = \frac{tPWH}{tPW}$$

Note2: A recommended f_{PWM} value is as follows.

$$f_{PWM} = \frac{2n-1}{4} \times fv$$

(n= integer, fv= frame frequency of LCD module)

Note3: Depending on the frequency used, a noise may appear on the screen, please conduct a thorough evaluation.

Note4: While the BRTC signal is high, do not set the tPWH (PWM pulse width) is less than the minimum values. It may cause abnormal working of the backlight. In this case, turn the backlight off and then on again by BRTC signal.

Note5: Regardless of the PWM frequency, both PWM duty ratio and PWM pulse width must be always more than the minimum values.

7. Interface Timing Characteristics

7.1 Method of Connection for LVDS Transmitter

	Bit mapping	Transmitter Pin Assignment THine THC63LVD1023B	Output Connector		CN1 Pin No.	CN1 Signal name
Pixel data A	RA4	R14				
	RA5	R15		Note1		
	RA6	R16	ATA-	→	4	DA0-
	RA7	R17	ATA+	→	5	DA0+
	RA8	R18				
	RA9	R19				
	GA4	G14				
	GA5	G15				
	GA6	G16				
	GA7	G17	ATB-	→	7	DA1-
	GA8	G18	ATB+	→	8	DA1+
	GA9	G19				
	BA4	B14				
	BA5	B15				
	BA6	B16				
	BA7	B17				
	BA8	B18	ATC-	→	10	DA2-
	BA9	B19	ATC+	→	11	DA2+
	Hsync	HSYNC				
	Vsync	VSYNC				
	DE	DE				
	RA2	R12				
	RA3	R13				
	GA2	G12	ATD-	→	16	DA3-
	GA3	G13	ATD+	→	17	DA3+
	BA2	B12				
	NA3	B13				
	N.C.	-				
	RA0	R10				
	RA1	R11				
	GA0	G10	ATE-	→	19	DA4-
	GA1	G11	ATE+	→	20	DA4+
	BA0	B10				
	BA1	B11				
	N.C.	-				
	CLK	CLK	ATCLK-	→	13	CKA-
			ATCLK+	→	14	CKA+
Pixel data B	RB4	R24				
	RB5	R25				
	RB6	R26	BTA-	→	22	DB0-
	RB7	R27	BTA+	→	23	DB0+
	RB8	R28				
	RB9	R29				
	GB4	G24				
	GB5	G25				
	GB6	G26				
	GB7	G27	BTB-	→	25	DB1-
	GB8	G28	BTB+	→	26	DB1+
	GB9	G29				
	BB4	B24				
	BB5	B25				
	BB6	B26				
	BB7	B27				
	BB8	B28	BTC-	→	28	DB2-
	BB9	B29	BTC+	→	29	DB2+
	Hsync	HSYNC				
	Vsync	VSYNC				
	DE	DE				
	RB2	R22				
	RB3	R23				
	GB2	G22	BTD-	→	34	DB3-
	GB3	G23	BTD+	→	35	DB3+
	BB2	B22				
	BB3	B23				
	N.C.	-				
	RB0	R20				
	RB1	R21				
	GB0	G20	BTE-	→	37	DB4-
	GB1	G21	BTE+	→	38	DB4+
	BB0	B20				
	BB1	B21				
	N.C.	-				
	CLK	CLK	BTCLK-	→	31	CKB-
			BTCLK+	→	32	CKB+

Note1: Twist pair wires with 100Ω (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.

	Bit mapping	Transmitter Pin Assignment THine THC63LVD1023B	Output Connector		CN2 Pin No.	CN2 Signal name
Pixel data C	RC4	R14	CTA- CTA+	Note1 → →		
	RC5	R15				
	RC6	R16			4	DC0-
	RC7	R17			5	DC0+
	RC8	R18				
	RC9	R19				
	GC4	G14				
	GC5	G15	CTB- CTB+			
	GC6	G16				
	GC7	G17		→	7	DC1-
	GC8	G18		→	8	DC1+
	GC9	G19				
	BC4	B14				
	BC5	B15				
	BC6	B16	CTC- CTC+			
	BC7	B17				
	BC8	B18		→	10	DC2-
	BC9	B19		→	11	DC2+
	Hsync	HSYNC				
	Vsync	VSYNC				
	DE	DE				
	RC2	R12	CTD- CTD+			
	RC3	R13				
	GC2	G12		→	16	DC3-
	GC3	G13		→	17	DC3+
	BC2	B12				
	BC3	B13				
	N.C.	-				
	RC0	R10	CTE- CTE+			
	RC1	R11				
	GC0	G10		→	19	DC4-
	GC1	G11		→	20	DC4+
	BC0	B10				
	BC1	B11				
	N.C.	-				
	CLK	CLK	CTCLK- CTCLK+	→ →	13 14	CKC- CKC+
Pixel data D	RD4	R24	DTA- DTA+			
	RD5	R25				
	RD6	R26		→	22	DD0-
	RD7	R27		→	23	DD0+
	RD8	R28				
	RD9	R29				
	GD4	G24				
	GD5	G25	DTB- DTB+			
	GD6	G26				
	GD7	G27		→	25	DD1-
	GD8	G28		→	26	DD1+
	GD9	G29				
	BD2	B24				
	BD3	B25				
	BD6	B26	DTC- DTC+			
	BD7	B27				
	BD8	B28		→	28	DD2-
	BD9	B29		→	29	DD2+
	Hsync	HSYNC				
	Vsync	VSYNC				
	DE	DE				
	RD2	R22	DTD- DTD+			
	RD3	R23				
	GD2	G22		→	34	DD3-
	GD3	G23		→	35	DD3+
	BD2	B22				
	BD3	B23				
	N.C.	-				
	RD0	R20	DTE- DTE+			
	RD1	R21				
	GD0	G20		→	37	DD4-
	GD1	G21		→	38	DD4+
	BD0	B20				
	BD1	B21				
	N.C.	-				
	CLK	CLK	DTCLK- DTCLK+	→ →	31 32	CKD- CKD+

Note1: Twist pair wires with 100Ω (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.

7.2 Timing Characteristics

Parameter			Symbol	min.	typ.	max.	Unit	Remarks
CLK	Frequency		1/ tc	68.27	72.94	74.69	MHz	13.71ns (typ.)
	Duty ratio		-	See the data sheet of LVDS transmitter.			-	-
	Rise time, Fall time		-				ns	-
DATA	CLK-DATA	Setup time	-				ns	-
		Hold time	-				ns	-
	Rise time, Fall time		-				ns	-
DE	Horizontal	Cycle	th	-	9.570	-	μs	104.5kHz (typ.)
				684	698	1009	CLK	
		Display period	thd	640			CLK	-
	Vertical (One frame)	Cycle	tv	-	20	-	ms	50.0Hz (typ.)
				2086	2,090	2317	H	
		Display period	tvd	2,064			H	-
	CLK-DE	Setup time	-	See the data sheet of LVDS transmitter.			ns	-
		Hold time	-				ns	-
	Rise time, Fall time		-				ns	-

Table 7.2.1 Timing characteristics

Note1: Definition of parameters is as follows:
tc= 1CLK, th= 1H
Note2: See the data sheet of LVDS transmitter.
Note3: Vertical cycle (tv) should be specified in integral multiple of Horizontal cycle (th).
Note4: Definition for landscape.

7.3 Input Signal Timing Chart

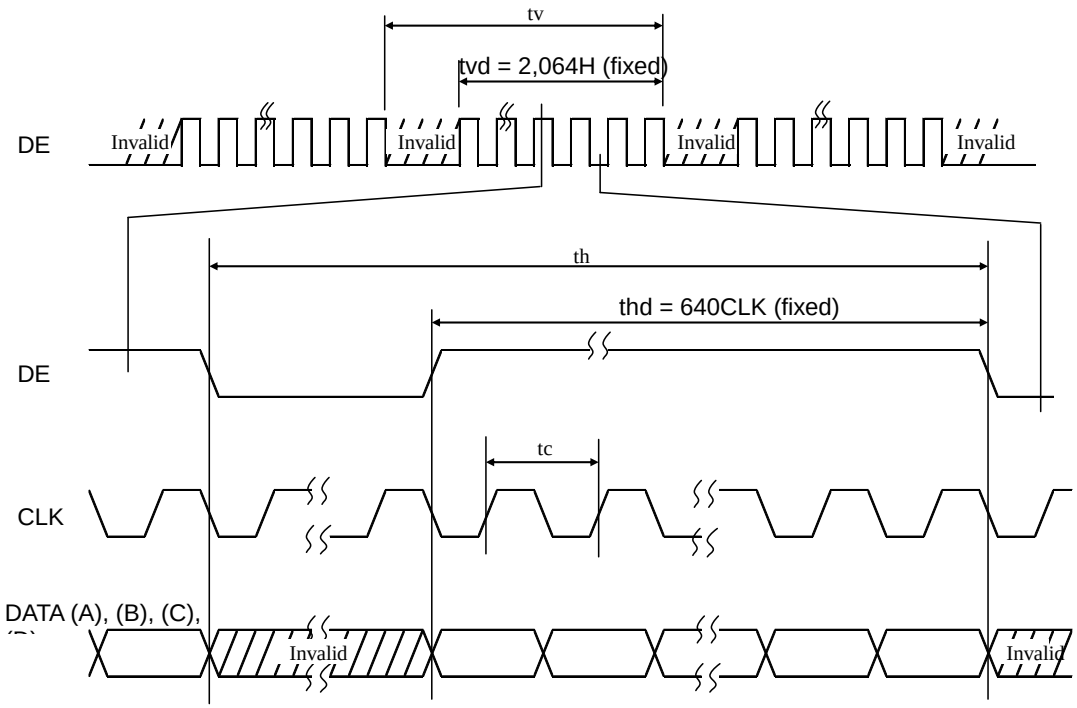


Figure 7.3.1 Input signal timing chart

7.4 Input Data Mapping

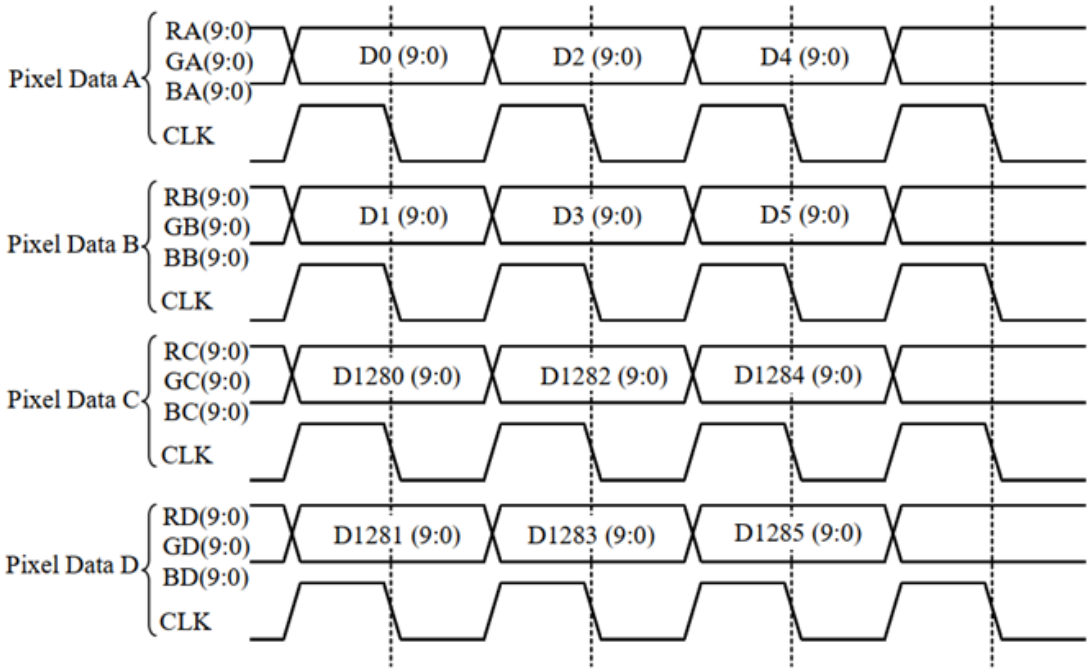
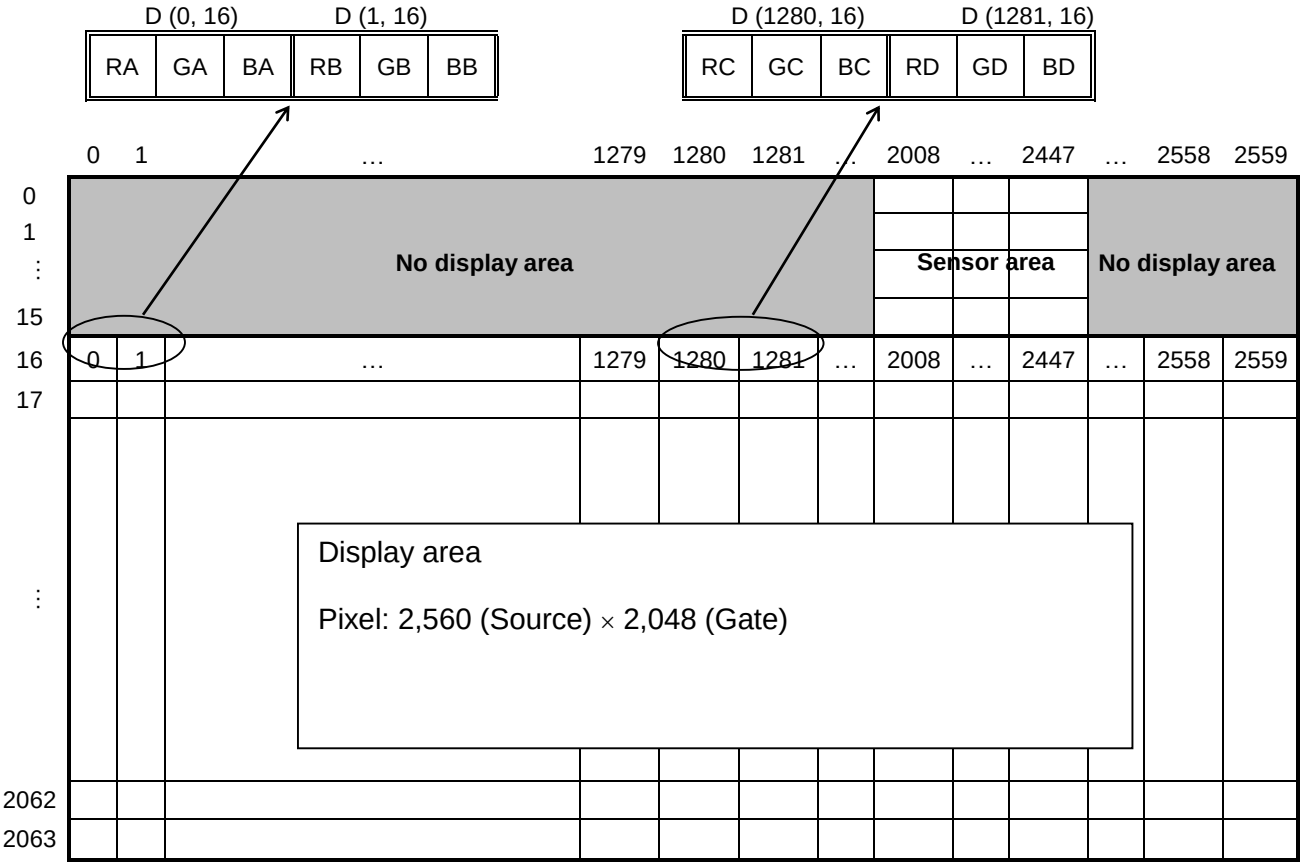


Figure 7.4.1 LVDS data transmission method

Note1: Definition for landscape.

7.5 Input Data Mapping

1.1



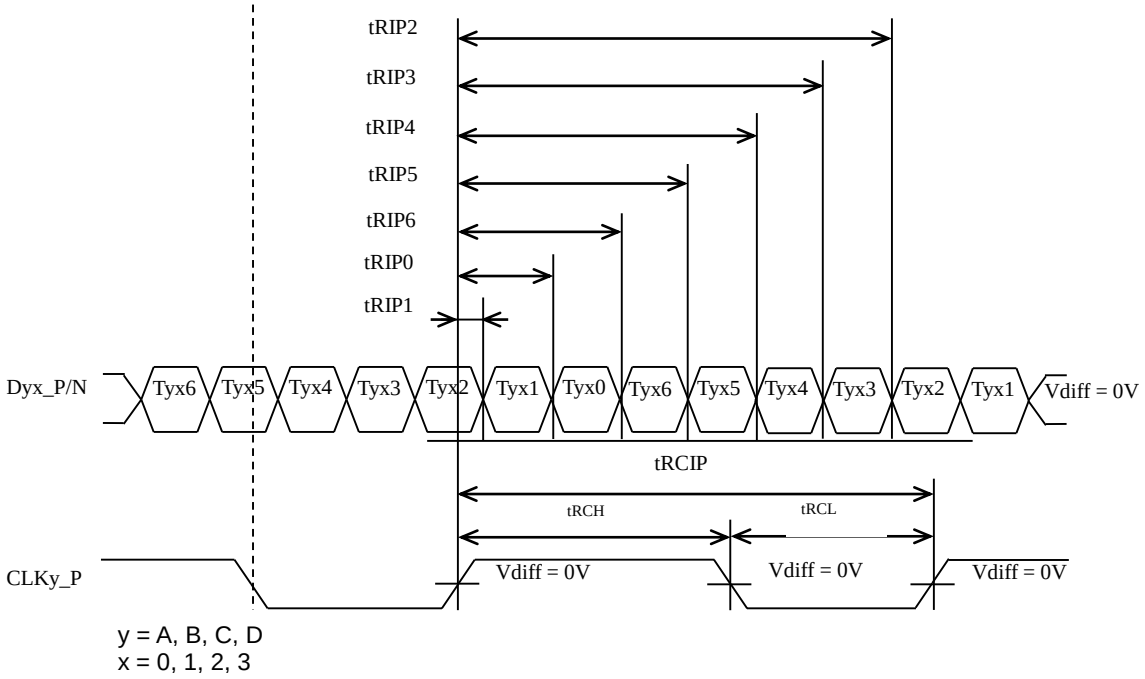
Note1： Definition for landscape.

Note2: Please notice the different definition for up and down on above sketch and "**10.1 Mechanical Drawing Of LCM**".

7.6 LVDS Rx AC SPEC

Symbol	Parameter	min.	typ.	max.	Unit
t_{RCIP}	CKy_+ Period	13.39	-	14.64	ns
t_{RCIH}	CKy_+ High pulse width	-	$\frac{4}{7}t_{RCIP}$	-	ns
t_{RCIL}	CKy_+ Low pulse width	-	$\frac{3}{7}t_{RCIP}$	-	ns
t_{RMG}	Receiver Data Input Margin CLK=72.94MHz Note1	-0.5	-	0.5	ns
t_{RIP1}	Input Data Position 0	$-\lvert t_{RMG}\rvert$	0.0	$+\lvert t_{RMG}\rvert$	ns
t_{RIP0}	Input Data Position 1	$\frac{t_{RCIP}}{7}-\lvert t_{RMG}\rvert$	$\frac{t_{RCIP}}{7}$	$\frac{t_{RCIP}}{7}+\lvert t_{RMG}\rvert$	ns
t_{RIP6}	Input Data Position 2	$2\frac{t_{RCIP}}{7}-\lvert t_{RMG}\rvert$	$2\frac{t_{RCIP}}{7}$	$2\frac{t_{RCIP}}{7}+\lvert t_{RMG}\rvert$	ns
t_{RIP5}	Input Data Position 3	$3\frac{t_{RCIP}}{7}-\lvert t_{RMG}\rvert$	$3\frac{t_{RCIP}}{7}$	$3\frac{t_{RCIP}}{7}+\lvert t_{RMG}\rvert$	ns
t_{RIP4}	Input Data Position 4	$4\frac{t_{RCIP}}{7}-\lvert t_{RMG}\rvert$	$4\frac{t_{RCIP}}{7}$	$4\frac{t_{RCIP}}{7}+\lvert t_{RMG}\rvert$	ns
t_{RIP3}	Input Data Position 5	$5\frac{t_{RCIP}}{7}-\lvert t_{RMG}\rvert$	$5\frac{t_{RCIP}}{7}$	$5\frac{t_{RCIP}}{7}+\lvert t_{RMG}\rvert$	ns
t_{RIP2}	Input Data Position 6	$6\frac{t_{RCIP}}{7}-\lvert t_{RMG}\rvert$	$6\frac{t_{RCIP}}{7}$	$6\frac{t_{RCIP}}{7}+\lvert t_{RMG}\rvert$	ns

Note1: Measured at FPGA input Pin.



7.7 Power On/Off Sequence

7.7.1 LCD panel signal processing board

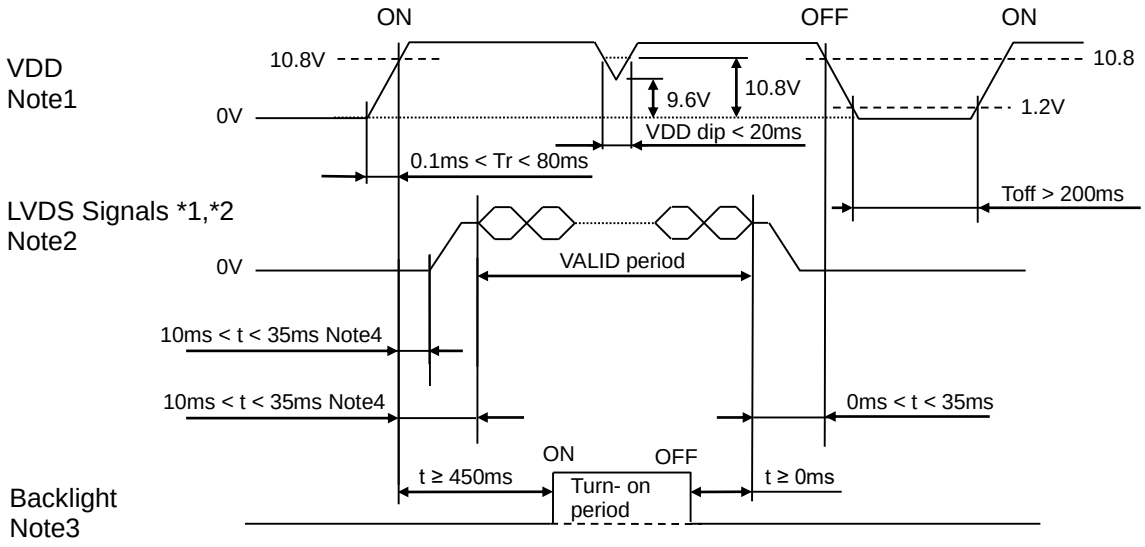


Figure 7.6.1.1 LCD panel signal processing board

Note1: If there is a voltage variation (voltage drop) at the rising edge of VDD below 10.8V, there is a possibility that a product does not work due to a protection circuit.

Note2: LVDS signals must be set to Low or High-impedance, except the VALID period (See above sequence diagram), in order to avoid the circuitry damage.
If some of signals are cut while this product is working, even if the signal input to it once again, it might not work normally. If a customer stops the display and function signals, VDD also must be shut down.

Note3: The backlight should be turned on within the turn-on period, in order to avoid unstable data display.

Note4: After turning VDD on, terminal voltages on LVDS input terminals (*1) will rise. This is caused by initial operation of the product.

7.7.2 LED Driver

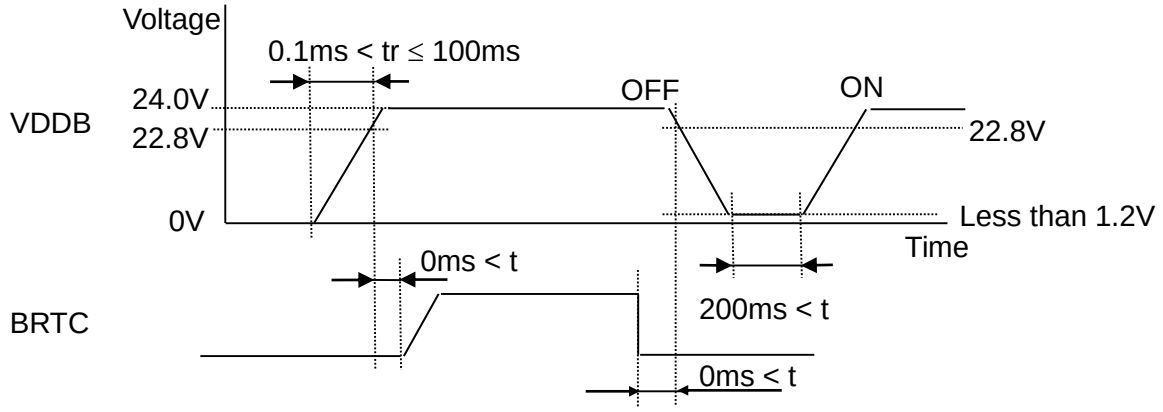


Figure 6.4.2.1 LED driver

Note1: If tr is more than 100ms, the backlight will be turned off by a protection circuit for LED driver.

Note2: When VDDB is 0V or BRTC is Low, PWSEL must be set to Low or Open.

8. Optical Characteristics

1.1

Item		Symbol	Condition	Min	Typ	Max	Unit	Remark
View Angles		θT	CR≧10	70	88	--	degree	Note2,3
		θB		70	88	--		
		θL		70	88	--		
		θR		70	88	--		
Contrast Ratio		CR	θ=0°	1600	2200	--		Note 3
Response Time		T_{ON}	25℃	--	25	40	ms	Note 4
		T_{OFF}						
Chromaticity	**White**	x	CIE1931-XYZ	0.264	0.294	0.324		Note 1,5
		y		0.279	0.309	0.339		
	Red	x		0.620	0.650	0.680		Note 1,5
		y		0.304	0.334	0.364		
	Green	x		0.281	0.311	0.341		Note 1,5
		y		0.588	0.618	0.648		
	Blue	x		0.122	0.152	0.183		Note 1,5
		y		0.035	0.065	0.095		
Uniformity		U		80	--	--	%	Note 6
NTSC		-		65	72	--	%	Note 5
Luminance		L		(1000)	1250	--	cd/m^2	Note 7

Table 8.1 Optical Parameters

Test Conditions:

1. These are initial characteristics.
2. Measurement conditions are as follows.
   Ta= 25°C, VDD= 12.0V, VDDB= 24.0V, PWM duty ratio: 100%,
   Display mode: QSXGA, Horizontal cycle= 1/104.5kHz, Vertical cycle= 1/50.0Hz

Note1: Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 5 Minutes operation, the optical characteristics are measured at the center point of the LCD screen.

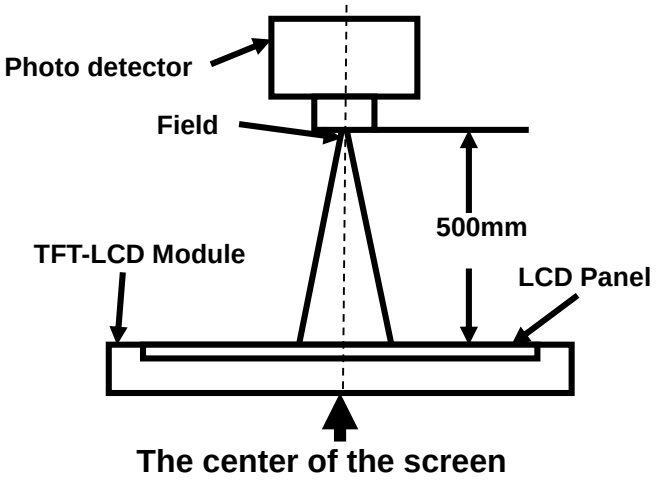


Fig1.Measurement Set Up

Note2: Definition of viewing angle range and measurement system. Viewing angle is measured at the center point of the LCD 。

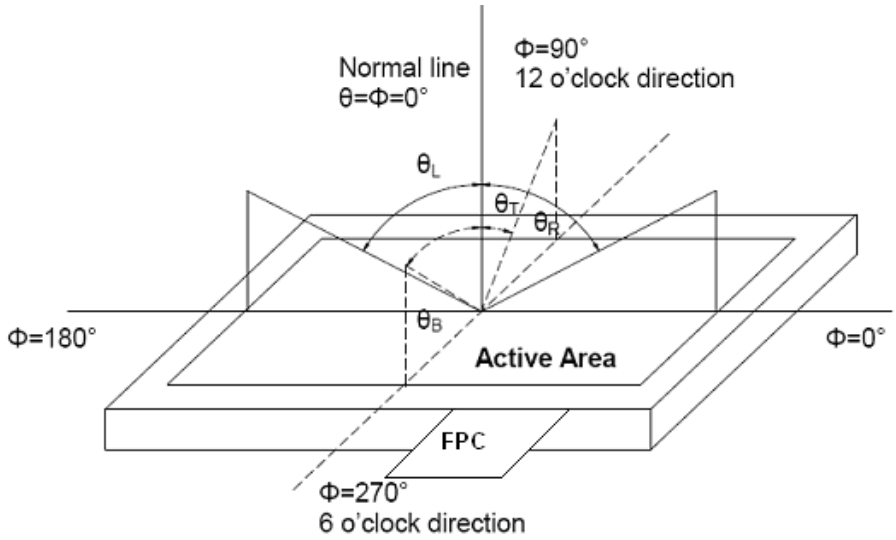


Fig2. Measurement viewing angle

Note3: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD is on the "White" state}}{\text{Luminance measured when LCD is on the "Black" state}}$$

Note4: Definition of Response time

For SFT LCM, the response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time (T_r) is the time between photo detector output intensity changed from 10% to 90%. And fall time (T_f) is the time between photo detector output intensity changed from 90% to 10%.

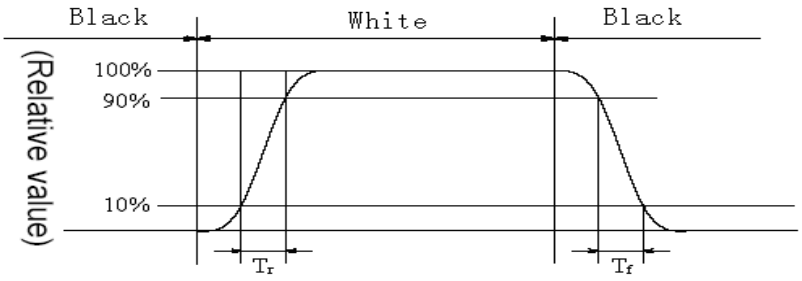


Fig3.Response Time Testing(SFT)

Note5: Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of LCD.

Note6: Definition of Luminance Uniformity

Active area is divided into 9 measuring areas (Refer Fig.5). Every measuring point is placed at the center of each measuring area.

Luminance Uniformity (U) = Lmin/ Lmax

Lmax: The measured Maximum luminance of all measurement position.

Lmin: The measured Minimum luminance of all measurement position.

L-------Active area length; W----- Active area width

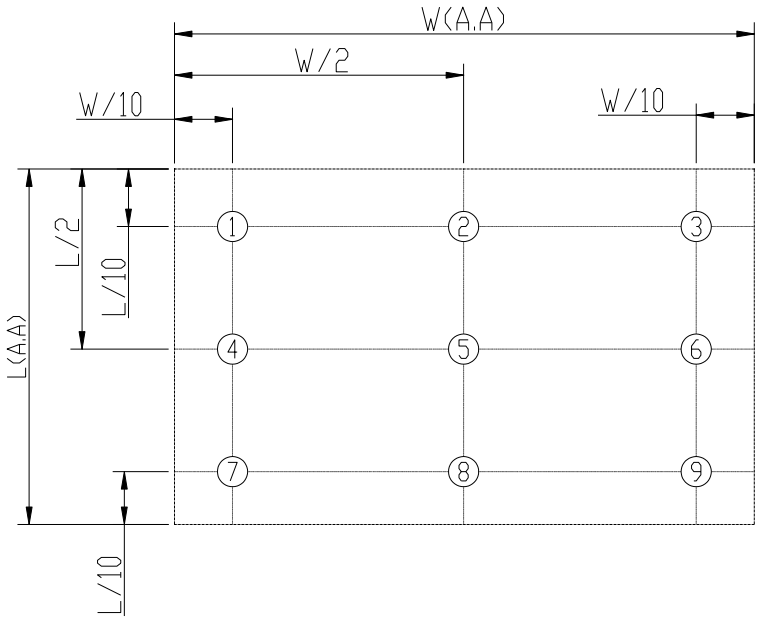


Fig4. Luminance Uniformity Measurement Locations(9 points)

Note7: Definition of Luminance:

Measure the luminance of white state at center point.

1.1

9. Reliability Test

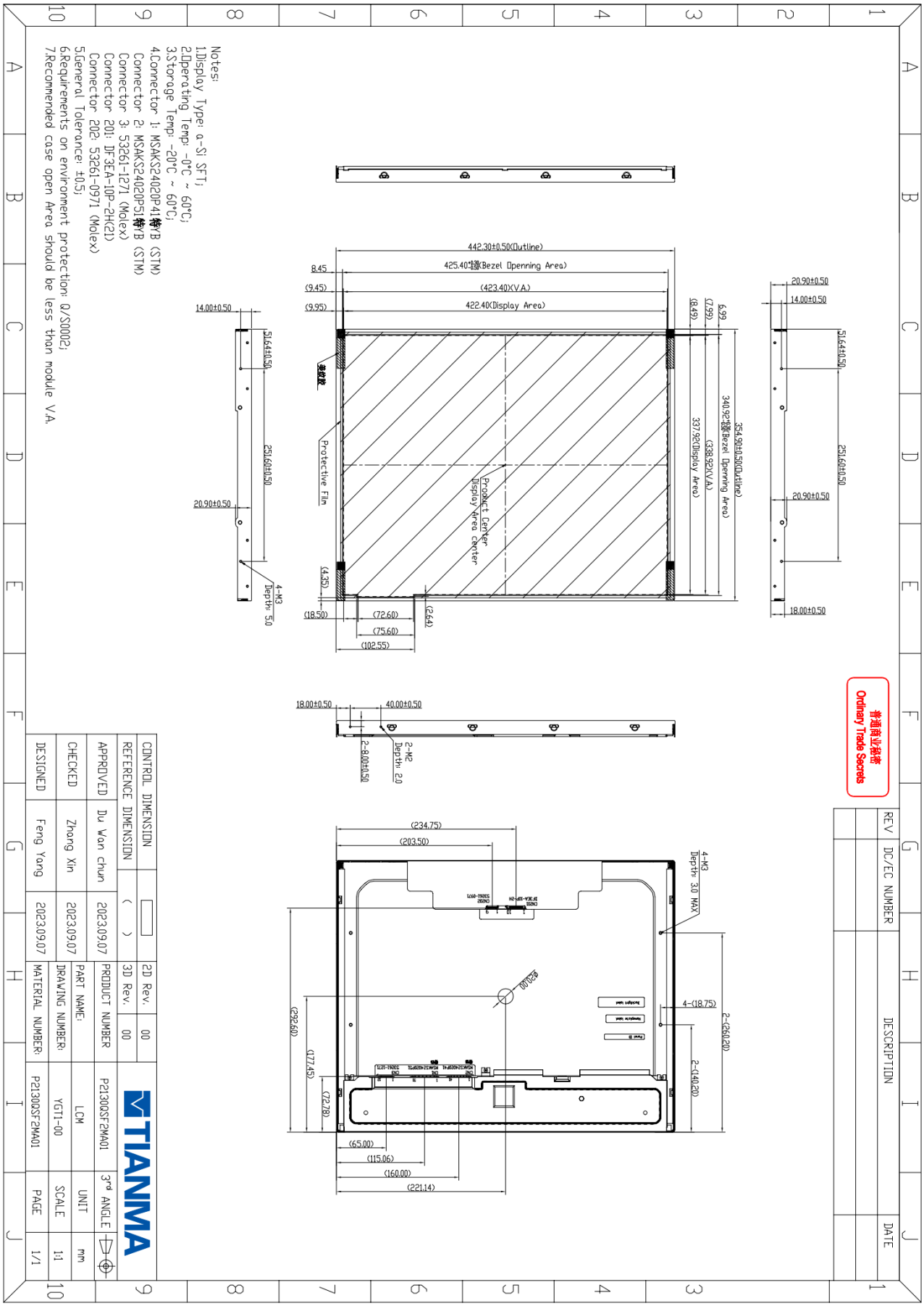
No	Test Item	Test condition	Criterion
1	High Temperature Operation	Ta = +60℃, 240 hours	IEC60068-2-2,GB2423.2
2	Low Temperature Operation	Ta = 0℃, 240 hours	IEC60068-2-1,GB2423.1
3	High Temperature and Humidity(operational)	Ta = +60℃, 60% RH max,240hours	IEC60068-2-2,GB2423.2
4	Thermal Shock (non-operational)	-20℃ 30 min~ +60℃ 30 min, Change time:5min, 100 Cycle	IEC60068-2-1,GB2423.1
5	Heat cycle (Operation)	-0℃1hour~60℃1hour 50cycles, 4 hours/cycle	IEC60068-2-78,GB/T2423.3
6	ESD (operational)	C=150pF, R=330Ω，9points/panel Air:±15KV, 25times; Contact:±8KV, 25 times; （Environment: 15℃～35℃, 30%～60%, 86Kpa～106Kpa）	IEC61000-4-2
7	Vibration(non-operational)	5~100HZ，11.76m/s2 1min/cycle 10times Per X\Y\Z	-
8	Mechanical Shock (non-operational)	294m/s2, 11ms 3times ±X、±Y、±Z	-
9	Package Vibration	Frequency range：5~20-200Hz, PSD:0.01-0.01-0.001 Total:0.781g2/Hz， Time：X/Y/Z 30min for each direction	GB/T 4857.23-2012
10	Package Drop Test	Height:60cm; 1corner,3edges,6surfaces	GB/T 4857.5-1992

Table 9.1 RA test condition

Note1: Temperature is the ambient temperature of sample
Note2: Before cosmetic and function test, the product must have enough recovery time, at least 24 hours at room temperature.
Note3: In the standard condition, there shall be no practical problem that may affect the display function. After the reliability test, the product's function only be guaranted, but not for all of the cosmetic specification.

10. Mechanical Drawing

10.1 Mechanical Drawing Of LCM



10.2 Markings

1.1

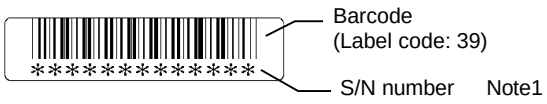
The marking is attached to this product.

10.2.1 Nameplate label

Nameplate label

10.2.2 Barcode label

Barcode label



Note1: **Do not attach anything like another label on the nameplate label!**

11. Packing Instruction

1.1

Tianma will pack products to deliver to customer in accordance with Tianma 's packing specifications, and will deliver products to customer in such a condition that products will not suffer from a damage during transportation. The delivery conditions are as follows.

Parameter	Packing box type	Unit
Size	612(W) x 425 (H) x 520 (D) (typ.)	mm
Weight	2.38(typ.)	kg
Total weight	13.68(typ.) (with 5 products)	kg

11.1 Inner Packing Box

5 products are packed as the maximum in an packing box (See "11.1 Outline Figure for Packing").The type name and quantity are shown on outside of the packing box, either labeling or printing. In case the packing box with products is dropped from a height of 40cm or more, there is a risk of damage to products.

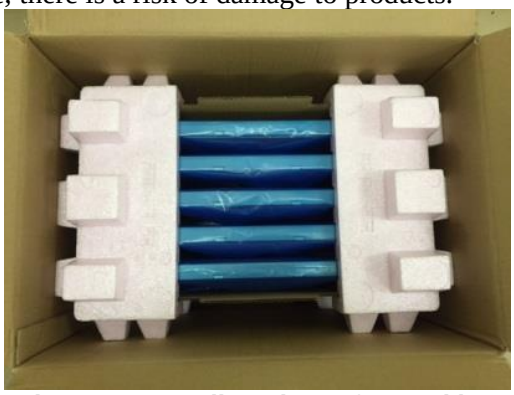


Figure 11.1 Outline Figure for Packing

12. Precautions for Use of LCD Modules

12.1 Handling Precautions

(1) The display panel is made of glass. Do not subject it to mechanical shock by dropping it, etc.
(2) If the display panel is damaged and the liquid crystal fluid inside it leaks out be sure not to get any in your mouth. If the fluid comes into contact with your skin or clothes promptly wash it off using soap and water.
(3) Do not apply excessive force to the display surface or the bezel since this may cause the color tone to vary.
(4) The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle the polarizer carefully.
(5) If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If it is still not completely clear use a moist cloth with one of the following solvents:
  - Isopropyl alcohol
  - Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Specifically, do not use the following:
  - Water
  - Ketone
  - Aromatic solvents

(6) Do not disassemble the LCD Module.
(7) If powered off, do not apply the input signals.
(8) To prevent destruction of the module by static electricity, be careful to maintain an optimum work environment.
(9) Be sure to ground your body when handling the LCD Modules.
(10) Tools used for assembly, must be properly grounded.
(11) To reduce the amount of static electricity generated, do not conduct assembly or other work under very low humidity conditions.
(12) The LCD Module is covered with a film to protect the display surface, remove film slowly under the ionizer.

12.2 Storage precautions

(1) When storing the LCD modules avoid exposure to direct sunlight or to the light of fluorescent lamps.
(2) The LCD modules should be stored within the rated storage temperature range. The recommend condition is: Temperature: 0 ~ 35 ℃ at normal humidity.
(3) The LCD modules should be stored in a room without acid, alkali or other harmful gas.

12.3 Transportation Precautions

The LCD modules should not be dropped or subject to violent mechanical shock during transportation. Also they should avoid excessive pressure, water, high humidity and direct sunlight.

12.4 Screen saver Precautions

Not display the fixed pattern for a long time. Use a screen saver, if the fixed pattern is displayed on the screen

12.5 Safety Precautions

(1) When you waste damaged or unnecessary LCDs, it is recommended to crush LCDs into pieces and wash them off with solvents such as acetone and ethanol, which should later be burned
(2) Be sure to turn off the power supply when inserting or disconnecting the LED backlight cable.
(3) LED driver should be designed carefully to limit or stop its function when over current is detected on the LED.