BOE LCD Module Specification

Module P/N: JH134N00900

Version: 1.0

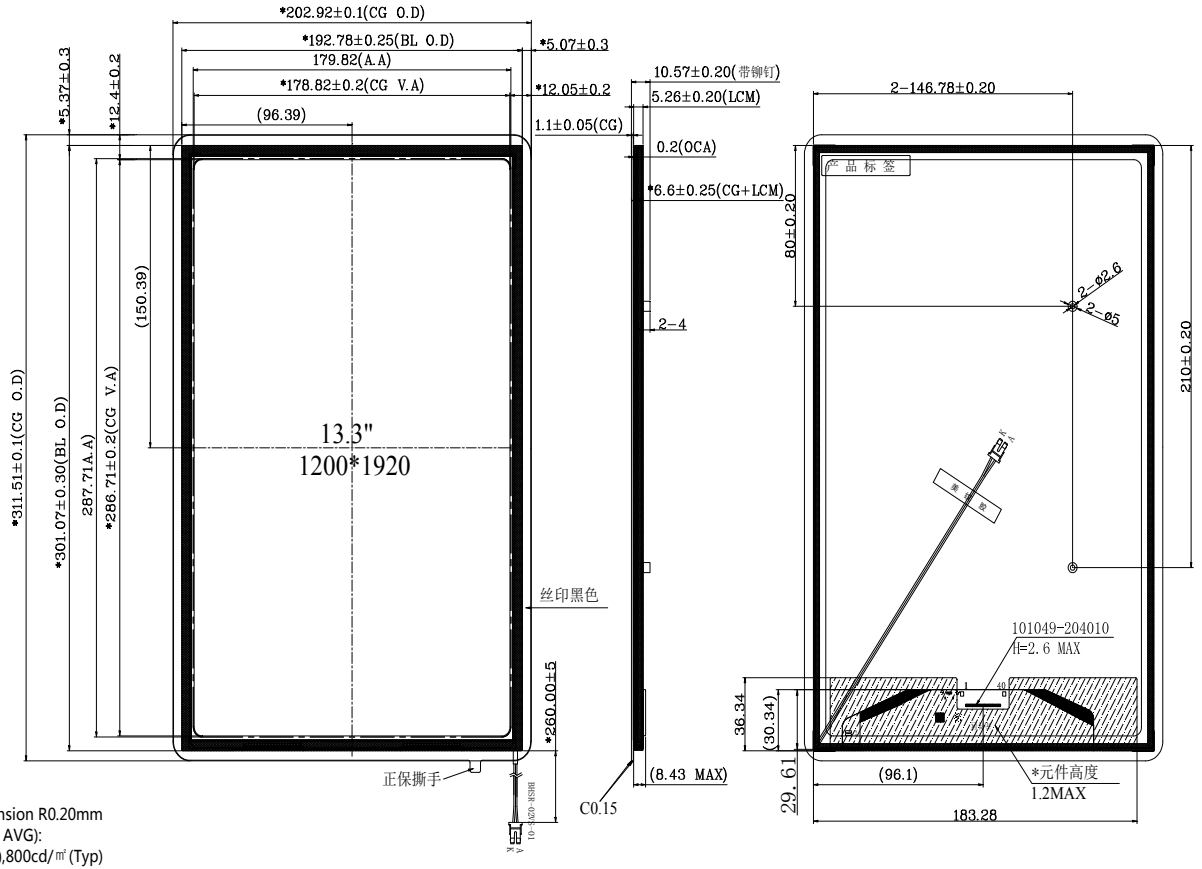
Description : 13.4 inch TFT 1200*1920 Pixels with
LED backlight, wide viewing angle

1. General Features

Item	Spec	Remark
Display Mode	Normally Black transmissive	
Gray Scale Inversion Direction	ALL o'clock	
Input Signals	MIPI + IIC	
Outside Dimensions	202.92(W)×311.51(H)×6.6(D)	mm; With CG
Active Area	179.82(W)×287.71(H)	mm
Number of Pixels	1200×RGB×1920 Pixels	
Dot Pitch	149.85(H)×149.85(V)	um
Pixel Arrangement	RGB Vertical Stripes	
Drive IC	FT8201S	

2.Outline Dimension

REV.	DRG DATE	DESCRIPTION	DRAWN BY
1.0			
2.0			
3.0			



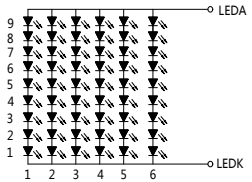
40 PIN	
Pin	DESCRIPTION
1-2	LEDA
3	NC
4-5	LEDK
6	NC
7	GND
8	GND
9	D0P_M
10	D0N_M
11	GND
12	D1P_M
13	D1N_M
14	GND
15	CLKP_M
16	CLKN_M
17	GND
18	D2P_M
19	D2N_M
20	GND
21	D3P_M
22	D3N_M
23	GND
24	GND
25	NC
26-27	VSP
28	NC
29-30	VSN
31	NC
32	VDD 3.3V
33-34	IOVCC
35	LCD_RST
36	GND
37	TP_RESX1
38	TP_INT
39	TP_SDA
40	TP_SCL

Notes:
1.Unit:mm
2.Do not scale drawing
3.All radii without dimension R0.20mm
4.Luminous instensity(9 AVG):
Module:700cd/㎡(Min),800cd/㎡(Typ)
5.Uniformity:80%(Min)
54LED=VF:24.3V(Min);27.0V(Typ);29.7V(Max); IF:300mA(Typ)
6.The color coordinates:

	MIN	TYP	MAX
x	0.235	0.265	0.295
y	0.255	0.285	0.315

7.⚠Modification rev.number
8.draft angle 1.0°
9.Genral Tolerance:±0.20mm
10.Mark mold cavity indentification in recess approximately where indicated
11. "*" For important dimension "( )" for reference dimention
12. Operating temp.:-30°C~+80°C 240Hour
Storage temp.: -30°C~+80°C 240Hour
13.RoHs must be complied.(Use Lead-free process)

盖板注意:
1.盖板材质:旭硝子AS2，原材厚度T=1.1mm；表面硬度≥6H(750g);2D
2.盖板折射率：1.52，光弹系数：27.5;
3.强化参数:CS:≥450Mpa；DOL≥9um;
上跨距20mm下跨距40mm,压杆φ6mm，测试速度10mm/min，4PB（B10）≥ 450Mpa;
4.钢球跌落要求：64g钢球，45cm高度，中心点3次，不破损;
5.盖底油墨为哑黑，油墨阻抗≥1000兆欧;
6.LENS油墨区域达因值≥32 Dyne,Arcotest,5s不收缩;
7.油墨附着力≥4B，油墨厚度≤15um；丝印黑色，要求100%遮光
8.耐石油醚擦拭：百格3M600胶带90° 拉起无掉墨;
9.油墨通过100°C水煮2H，使用3M610胶纸测试百格，附着力必须达4B，被粘区域与其它区域不得出现明显色差
10.油墨丝印不能有透空，杂点，划伤，绝不能有掉墨现象;
11.CG油墨的不透明性（OD值）：黑 OD≥5.0
12.CG翘曲度≤0.5mm;（油墨面朝下，CG中间凸起）
13、无卤，符合欧盟RoHS标准



Backlight LED Circuit
LED 电路图 9串6并

DRG DATE	20250701	TITLE.	总成 OUTLINE			
CHECK		MODEL.	JH134T00900			
CHECK		DWG No.		REV.	UNIT	SIZE
APPROVE		PAGE	1 OF 1		mm	A4

(3)

3. Reliability and Inspection Standard

1	High Temperature	Storage	80℃, 96Hrs	Inspection after 2-4hours storage at room temperature,the samples should be free from defects: 1,Air bubble in the LCD. 2,Seal leak. 3,Non-display. 4,Missing segments. 5,Glass crack. 6,Current IDD is twice higher than initial value. 7,The surface shall be free from damage.
		Operation	70℃, 96Hrs	
2	Low Temperature	Storage	-30℃, 96Hrs	
		Operation	-20℃, 96Hrs	
3	High Temperature and High Humidity		40℃, 90%RH, 48Hrs	
4	Temperature Cycle(storage)		-20 ~ 60℃, 1H/cycle , Total 10 Cycles,	

REMARK:
1,The Test samples should be applied to only one test item.
2,Sample for each test item is 5pcs.
3,For Damp Proof Test, Pure water(Resistance＞10MΩ)should be used.
4,Failure Judgment Criterion: Basic Specification Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.

4.LCM Description

4.1 Absolute Maximum Ratings

The following are maximum values which, if exceeded may cause operation or damage to the unit.

(AVDD = 4.5V ~ 6.5V, AVEE = -4.5V ~ -6.5V, VDDI = 1.65V ~ 1.95V, Ta = -30°C ~ 85°C)

Parameter	Symbol	Rating	Unit	Note
Power Supply Voltage 1	VDDI-VSS	-0.3 ~ +1.95	V	
Power Supply Voltage 2	VDD-VSS	-0.3 ~ +1.35	V	
Power Supply Voltage 3	AVDD-VSS	-0.3 ~ +6.5	V	
Power Supply Voltage 4	VSS-AVEE	-0.3 ~ +6.5	V	
Power Supply Voltage 5	VGH-VGL	-0.3 ~ +32	V	
Input Voltage	Vt	-0.3 ~ VDDI+0.3	V	

Note1. The maximum applicable voltage on any pin with respect to 0V.

Note2. Device is subject to be damaged permanently if stresses beyond those absolute maximum ratings listed above.

4.2 Electrical Specification

4.2.1 Driving TFT LCD Panel

Item		Sym.	Min	Typ.	Max	Unit	Note
I/O and Logical power		IOVCC	1.65	1.8	1.95	V	
Analog supply power		VSP	5.6	5.8	6.0	V	
		VSN	-6.0	-5.8	-5.6		
Logic Input Voltage	Low Voltage	V_{IL}	0	-	$0.3I_{OVCC}$	V	
	High Voltage	V_{IH}	$0.7I_{OVCC}$	-	I_{OVCC}	V	
Logic Output Voltage	Low Voltage	V_{OL}	0	-	$0.2I_{OVCC}$	V	
	High Voltage	V_{OH}	$0.8I_{OVCC}$	-	I_{OVCC}	V	

4.2.2 Driving Backlight

Item	Sym.	Min	Typ.	Max	Unit	Note
Backlight driving voltage	V_F	24.3	-	29.7	V	
Backlight driving current	I_F	-	300	-	mA	
Backlight Power Consumption	W_{BL}	-	-	-	mW	
Life Time	-	10,000	20,000	-		Note 3

Note 1: (Unless specified, the ambient temperature Ta=25℃)

Note 2: The recommended operating conditions refer to a range in which operation of this product is guaranteed. Should this range is exceeded, the operation cannot be guaranteed even if the values may be without the absolute maximum ratings.

Note 3: If LED is driven by high current, high ambient temperature & humidity condition. The life time of LED will be reduced. Operating life means brightness goes down to 50% initial brightness. Typical operating life time is estimated data.

4.3 Optical Specifications

Optical characteristics are determined after the unit has been 'ON' and stable for approximately 30 minutes in a dark environment at 25 ℃. The values specified are at an approximate distance 500mm from the LCD surface at a viewing angle of Φ and θ equal to 0°.

Item	Sym.	Values			Unit	Note
		Min.	Typ.	Max.		
1)Contrast Ratio	C/R	1000	1500	-		FIG.1
2)Luminance Uniformity	δ WHITE	75	80	-	%	Note5
3)TCM Luminance	L	700	800	-	cd/m^2	FIG.1
4)Response time	Tr+Tf	-	-	35	ms	FIG.2
5)Viewing Angle	Θ_L	-	80	-	Degree	FIG.3
	Θ_R	-	80	-		
	Θ_U	-	80	-		
	Θ_D	-	80	-		
6)Chromaticity	Wx	Typ-0.03	0.26	Typ+0.03		FIG.1
	Wy		0.28			
	Rx		TBD			
	Ry		TBD			
	Gx		TBD			
	Gy		TBD			
	Bx		TBD			
	By		TBD			
7)NTSC	CIE1931	55	60	--	%	FIG.1

◆ Measurement System

Notes:

1. Contrast Ratio(CR) is defined mathematically as :

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

2. Surface luminance is the center point across the LCD surface 500mm from the surface with all pixels displaying white. For more information see FIG 1.

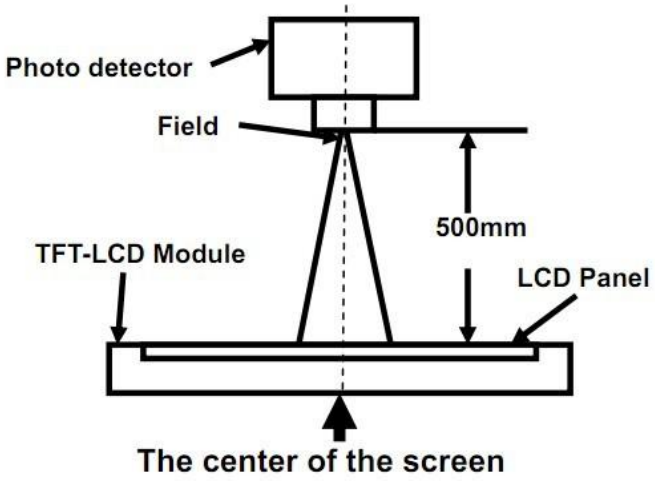
3. Response time is the time required for the display to transition from white to black (Rising Time, Tr) and from black to white (Falling Time, Tf). For additional information see FIG 2.

4. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see FIG 3.

5. The uniformity in surface luminance（δ WHITE）is determined by measuring luminance at each test position 1 through 9, and then dividing the maximum luminance of 9 points luminance by minimum luminance of 9 points luminance.

$$\delta \text{ WHITE} = \frac{\text{Minimum Surface Luminance with all white pixels}}{\text{Maxi mum Surface Luminance with all white pixels}}$$

FIG. 1 Optical Characteristic Measurement Equipment and Method



Item	Photo detector	Field
Contrast Ratio	SR-3A	1°
Luminance		
Chromaticity		
Lum Uniformity		
Response Time	BM-7A	2°

FIG. 2 The definition of Response Time

The response time is defined as the following figure and shall be measured by switching the input signal for “black” and “white”.

Response Time = Rising Time(Tr) + Falling Time(Tf)

- Rising Time(Tr) : Full White 90% → Full White 10% Transmittance.
- Falling Time(Tf) : Full White 10% → Full White 90% Transmittance.

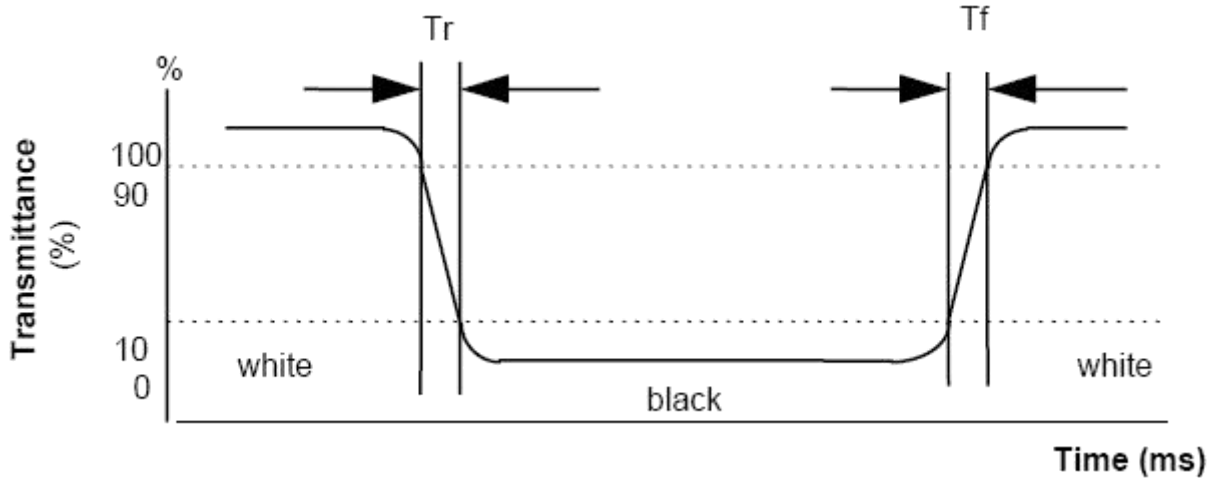
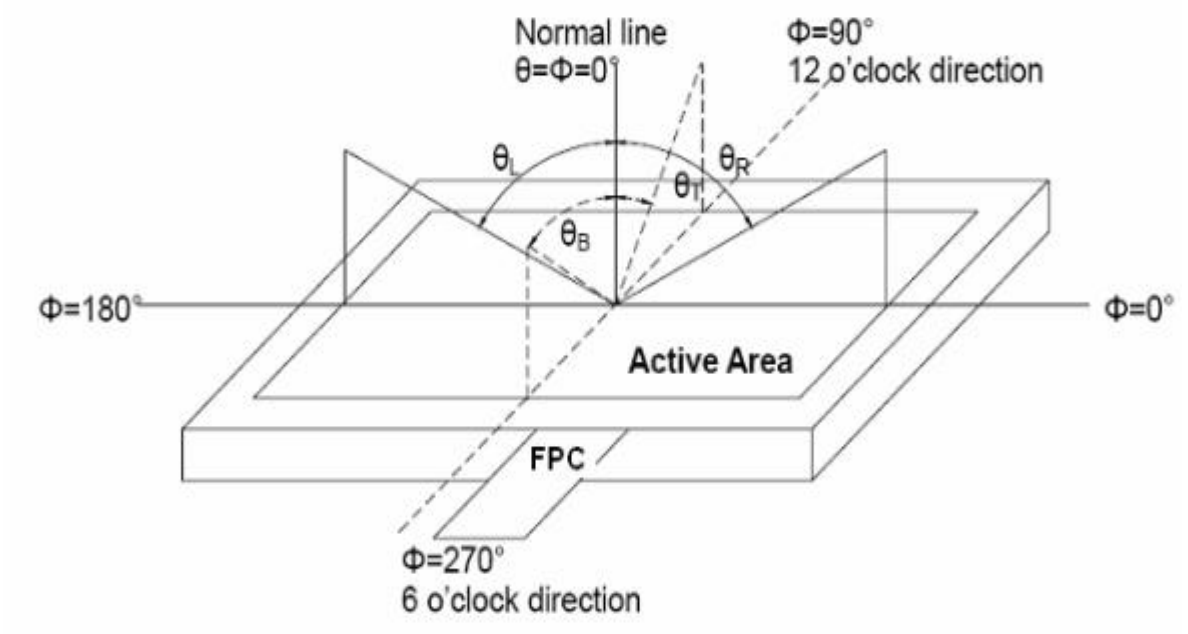
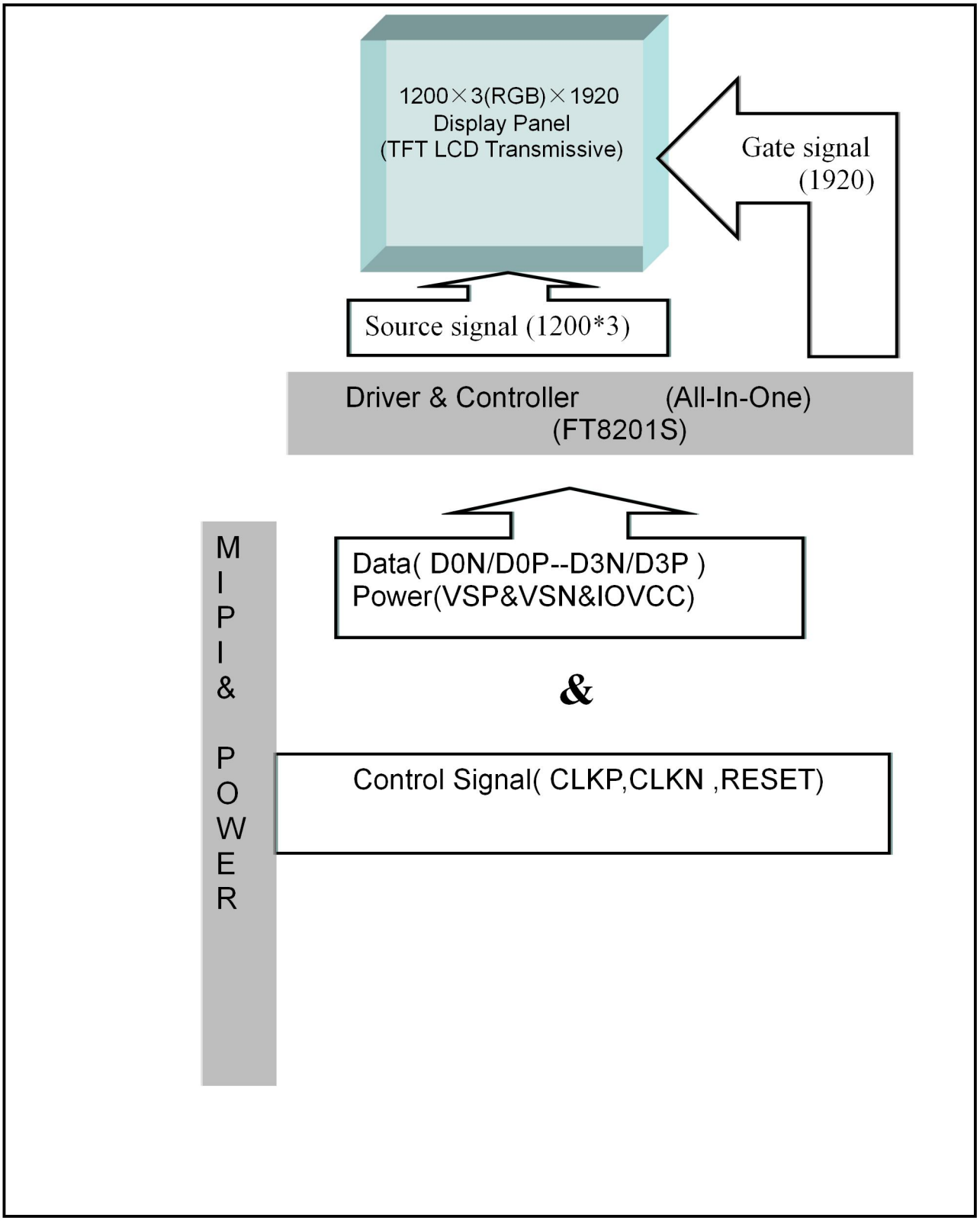


FIG. 3 The definition of Viewing Angle

Use Fig. 1(Test Procedure) under Measurement System to measure the contrast from the measuring direction specified by the conditions as the following figure.



4.4 Block Diagram



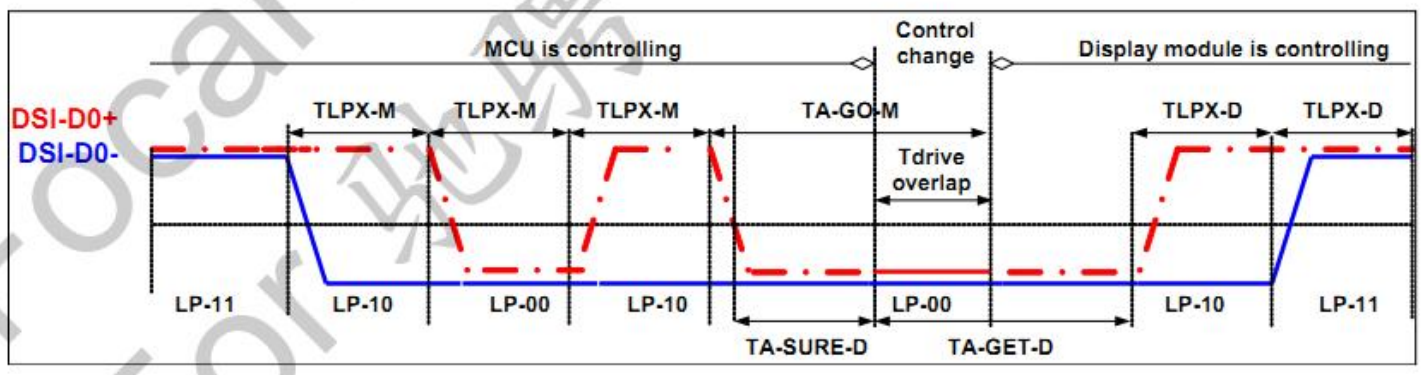
4.5 Pin Description

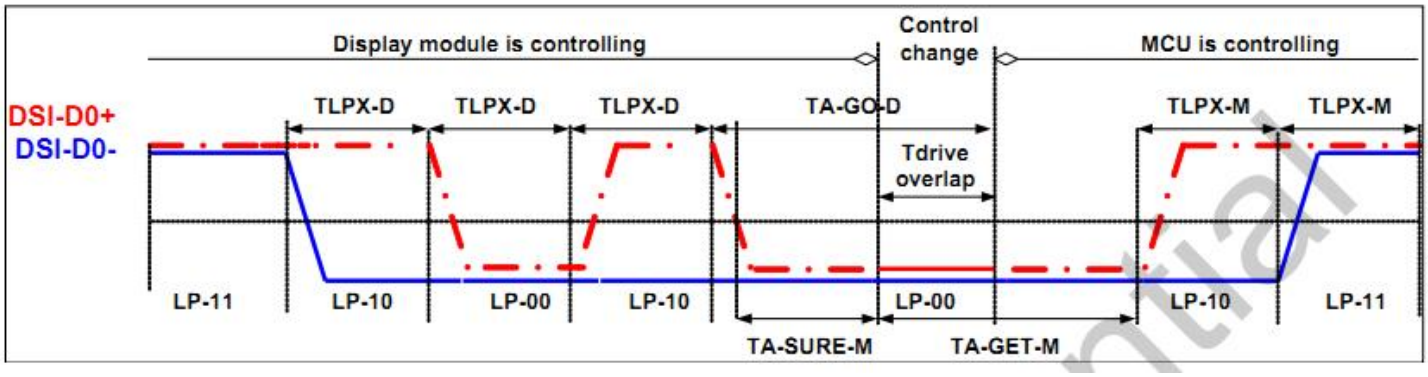
Item	Terminal	Functions
1-2	LEDA	B/L Power input PIN anode
3	NC	NC
4-5	LED-	B/L Power input PIN negative
6	NC	NC
7	GND	Ground
8	GND	Ground
9	D0P_M	Positive polarity of low voltage differential data0 signal
10	D0N_M	Negative polarity of low voltage differential data0 signal
11	GND	Ground
12	D1P_M	Positive polarity of low voltage differential data1 signal
13	D1N_M	Negative polarity of low voltage differential data1 signal
14	GND	Ground
15	CLKP_M	positive polarity of low voltage differential clock signal
16	CLKN_M	Negative polarity of low voltage differential clock signal
17	GND	Ground
18	D2P_M	Positive polarity of low voltage differential data2 signal
19	D2N_M	Negative polarity of low voltage differential data2 signal
20	GND	Ground
21	D3P_M	Positive polarity of low voltage differential data3 signal
22	D3N_M	Negative polarity of low voltage differential data3 signal
23	GND	Ground
24	GND	Ground
25	NC	NC
26	VSP	Positive power supply 5.8V
27	VSP	Positive power supply 5.8V
28	NC	NC
29	VSN	Negative power supply -5.8V
30	VSN	Negative power supply -5.8V
31	NC	NC
32	VDD	NC
33	IOVCC	I/O Power supply 1.8V
34	IOVCC	I/O Power supply 1.8V
35	RESET	LCD Reset, High=1.8V
36	GND	Ground
37	TP-RESET	IIC Reset, High=1.8V
38	TP-INT	IIC Interrupt
39	TP-SDA	IIC Interface data
40	TP-SCL	IIC Interface clock

4.6 Timing Characteristics

4.6.1 LP Power Mode Transmission

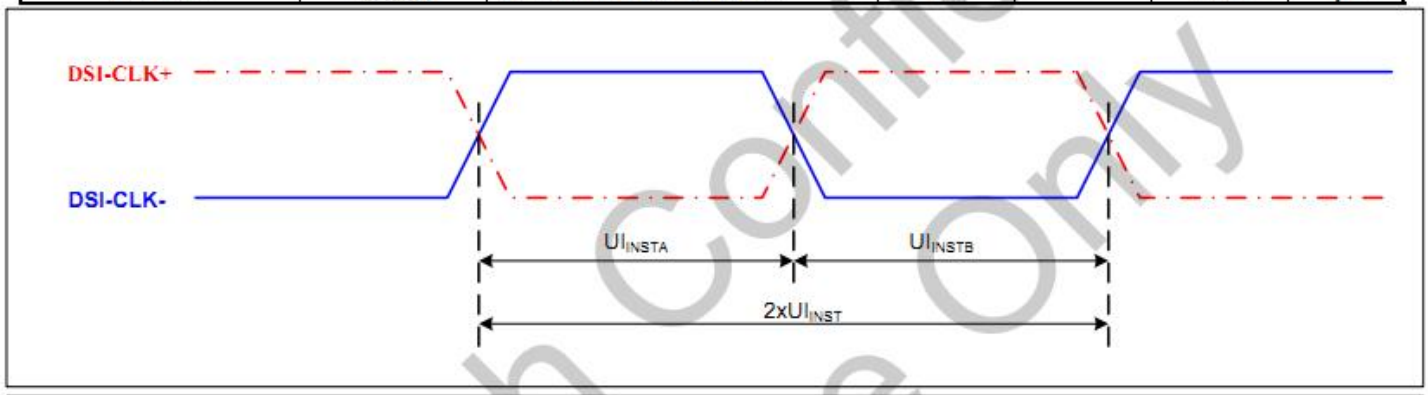
Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
Low Power mode						
DSI-D0+/-	T_{LPX-M}	Transmitted length of any Low-Power state period (MCU)	50	-	-	ns
DSI-D0+/-	$T_{TA-SURE-M}$	The display module waits after the LP-10 before transmitting the LP-00 (MCU)	T_{LPX-M}	-	$2XT_{LPX-M}$	ns
DSI-D0+/-	$T_{TA-GET-M}$	The display module drives the LP-00 before releasing MCU control	$5XT_{LPX-M}$	-	-	ns
DSI-D0+/-	$T_{TA-GO-M}$	The display drives the LP-00 after accepting control	$4XT_{LPX-M}$	-	-	ns
DSI-D0+/-	Ratio T_{LPX}	Ratio of (TLPX-M/TLPX-D) for driving overlap	2/3	-	3/2	-
DSI-D0+/-	T_{LPX-D}	Transmitted length of any Low-Power state period (Display)	50	58	-	ns
DSI-D0+/-	$T_{TA-SURE-D}$	The MCU waits after the LP-10 before transmitting the LP-00 (Display)	T_{LPX-D}	-	$2XT_{LPX-D}$	ns
DSI-D0+/-	$T_{TA-GET-D}$	The MCU drives the LP-00 before releasing Display control	$5XT_{LPX-D}$	-	-	ns
DSI-D0+/-	$T_{TA-GO-D}$	The MCU drives the LP-00 after accepting control	$4XT_{LPX-D}$	-	-	ns

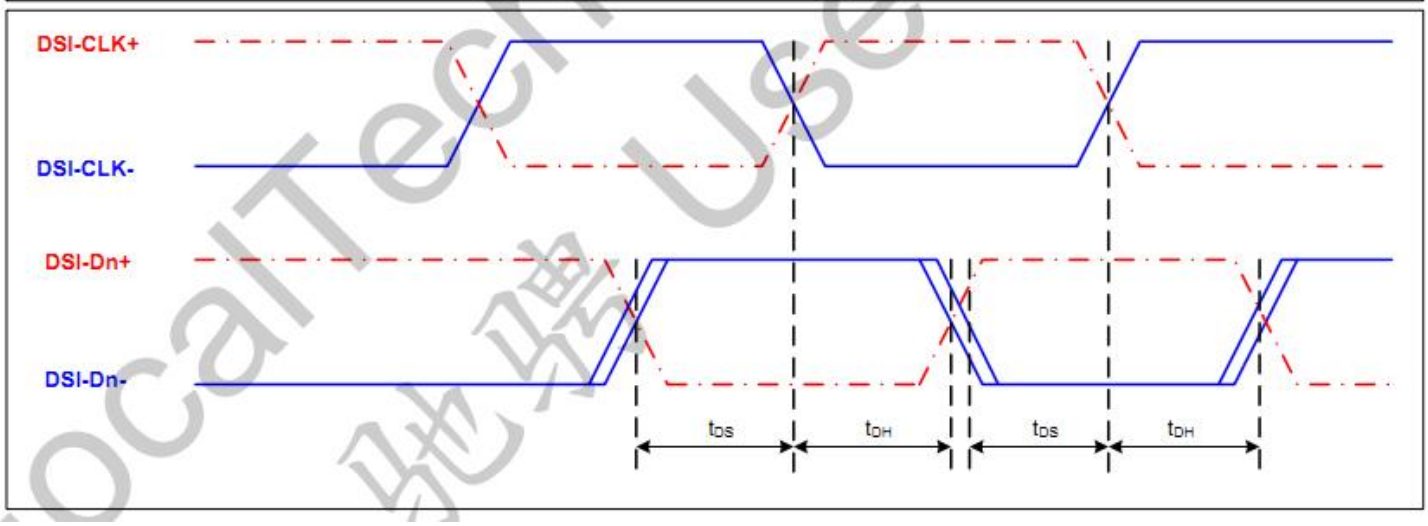


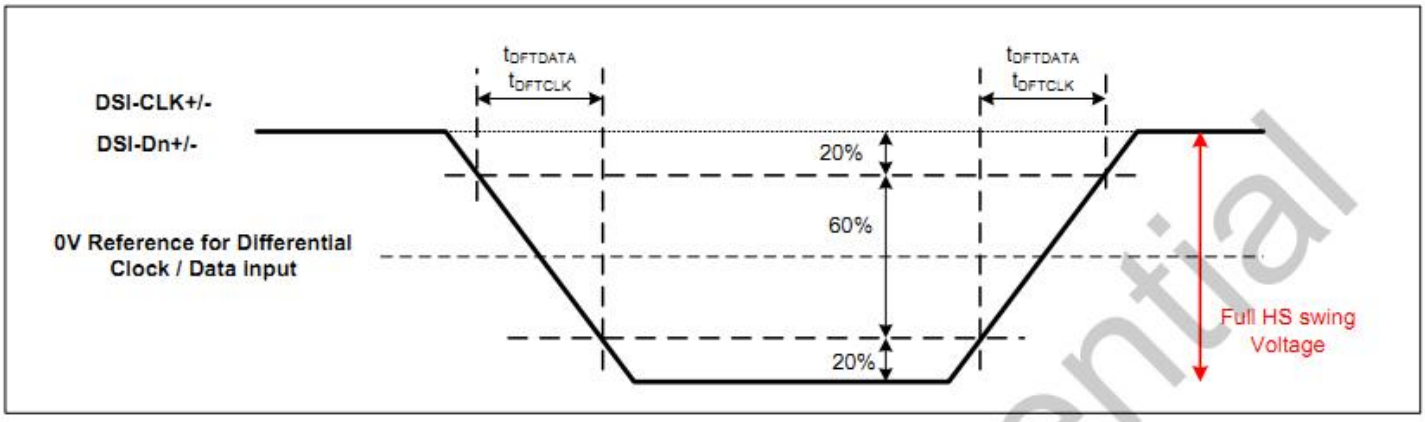


4.6.2 High Speed Mode Transmission

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
High Speed Mode						
DSI-CLK+/-	$2xUI_{INST}$	Double UI instantaneous	1.54	-	25	ns
DSI-CLK+/-	UI_{INSTA} , UI_{INSTB}	UI instantaneous Halfs	0.77	-	12.5	ns
DSI-Dn+/-	t_{DS}	Data to clock setup time	0.15	-	-	UI
DSI-Dn+/-	t_{DH}	Data to clock hold time	0.15	-	-	UI
DSI-CLK+/-	t_{DRTCLK}	Differential rise time for clock	150	-	0.3UI	ps
DSI-Dn+/-	$t_{DRTDATA}$	Differential rise time for data	150	-	0.3UI	ps
DSI-CLK+/-	t_{DFTCLK}	Differential fall time for clock	150	-	0.3UI	ps
DSI-Dn+/-	$t_{DFTDATA}$	Differential fall time for data	150	-	0.3UI	ps







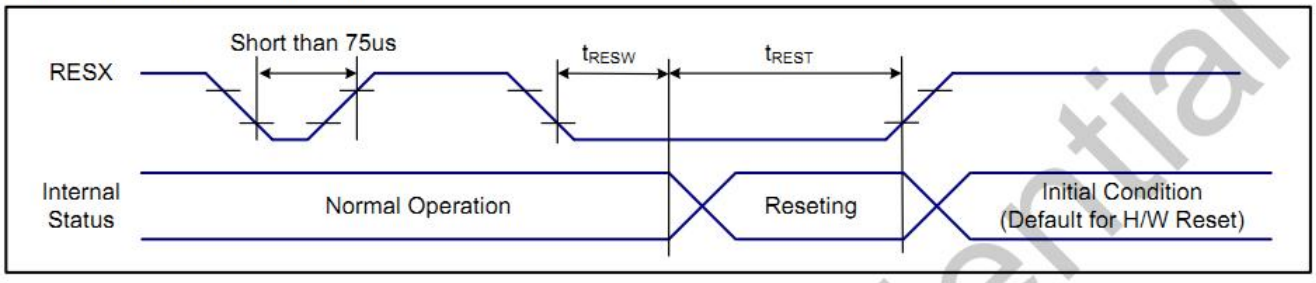
4.6.3 MIPI DC Character

(Ta = -30°C ~ 85°C)

Parameter	Symbol	Conditions	Specification			Unit
			MIN	TYP	MAX	
Power supply voltage for MIPI Interface						
Power supply voltage for MIPI interface	LVDSVDD	-	1.2	1.25	1.3	V
LPDT Input Characteristics						
Pad signal voltage range	V_I	-	-50	-	1350	mV
Ground Shift	V_{GNDSH}	-	-50	-	50	mV
Logic 0 input threshold	V_{IL}	-	-	-	550	mV
Logic 1 input threshold	V_{IH}	-	880	-		mV
Input hysteresis	V_{HYST}	-	25	-	-	mV
LPDT Output Characteristics						
Output low level	V_{OL}	-	-50	-	50	mV
Output high level	V_{OH}	Note 1	1.2	1.25	1.3	V
Logic 0 contention threshold	V_{ILCD}	-	-	-	200	mV
Logic 1 contention threshold	V_{IHCD}	-	450	-	-	mV
Output impedance of LPDT	Z_{OLP}	-	110	-	-	Ω
Hi-speed Input Characteristics						
Single-end input low voltage	V_{ILHS}	-	-40	-	-	mV
Single-end input high voltage	V_{IHHS}	-	-	-	460	mV
Single-end threshold for HS termination enable	$V_{TERM-EN}$	-	-	-	450	mV
Differential input low threshold	V_{IDTL}	-	-70	-	-	mV
Differential input high threshold	V_{IDTH}	-	-	-	70	mV
Common mode voltage	V_{CMRXDC}	-	70	-	330	mV
Differential input impedance	Z_{ID}	-	80	100	125	Ω

4.6.4 Reset Operation

t_{RESW} shorter than 75us, Reset will be rejected.



VSS=0V, VDDI = 1.65V ~ 1.95V, Ta = -30°C to 85°C

Symbol	Parameter	MIN	TYP	MAX	Note	Unit
t_{RESW}	*1) Reset low pulse minimum width	150	-	-	Reset signal recognized	us
t_{REST}	*2) Reset complete time	5	-	120	Reset action complete	ms

Table: Reset input timing

Note 1. RESX low pulse that is too short does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 75us	Reset Rejected
Longer than 150us	Reset Recognized
Between 75us and 150us	Reset sequence starts (It depends on voltage and temperature condition.)

Note 2. Once Reset low pulse is recognized, system requires RESX remaining low for another 5ms to complete H/W reset.

Note 3. During H/W Reset flow, ID0 ~ ID4 and VCOM value in OTP will be latched to internal register during this period. This loading is done every time when H/W reset is complete ; The H/W reset sequence is complete when RESX is remaining low longer than tRESW + tREST.

5 Touch Description

5.1 Features and General Specification

Item	Contents	Unit
Cover Glass	1.1mm	
Size	13.4''	Inch
Outline of Cover Lens	202.92*311.51±0.1	mm
Cover Lens VA	178.82*286.71±0.15	mm
Transmittance	≥85%	
Surface treatment	/	
Surface Hardness	≥6H	

5.2 IIC interface Characteristics

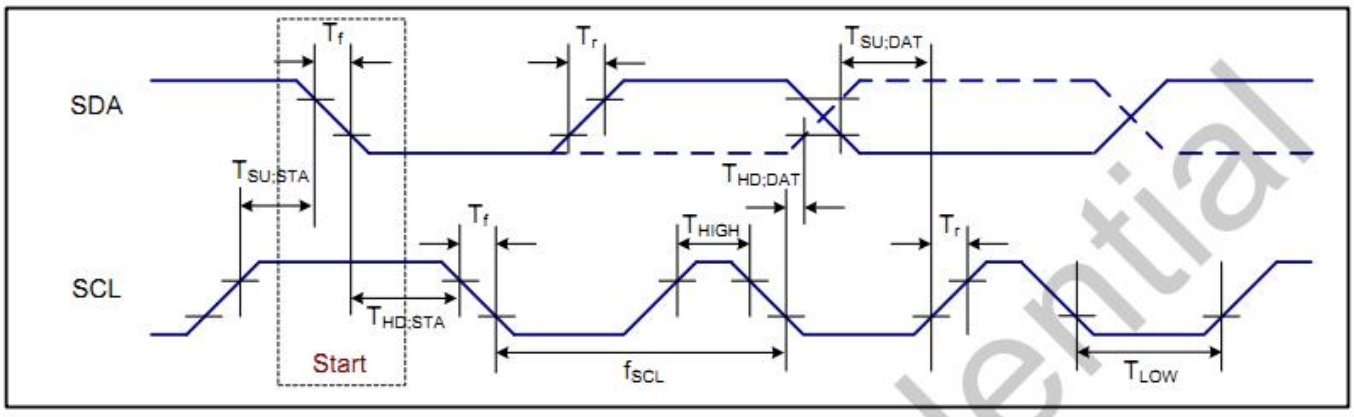


Table: I2C Interface Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{SCLK}	SCL clock frequency	-	10	-	400	kHz
T_{LOW}	SCL clock LOW period	-	1.2	-	-	us
T_{HIGH}	SCL clock HIGH period	-	0.6	-	-	us
$T_{SU;DATA}$	data set-up time	-	250	-	-	ns
$T_{HD;DATA}$	data hold time	-	0	-	0.9	us
T_r	SCL and SDA rise time	Note 2	$20+0.1C_b$	-	300	ns
T_f	SCL and SDA fall time	Note 2	$20+0.1C_b$	-	300	ns
T_f	SDA fall time for read out	-	$20+0.1C_b$	-	1000	ns
C_b	Capacitive load represented by each bus line	-	-	-	400	pF
$T_{SU;STA}$	Setup time for a repeated START condition	-	0.6	-	-	us
$T_{HD;STA}$	START condition hold time	-	0.6	-	-	us
$T_{SU;STO}$	Setup time for STOP condition	-	0.6	-	-	us
T_{SW}	Tolerable spike width on bus	Note 1	-	-	50	ns
T_{BUF}	BUS free time between a STOP and START condition	-	4.7	-	-	us

Note1: The device inputs SDA and SCL are filtered and will reject spikes on the bus lines of width $<t_{SW(max)}$.

Note2: The rise and fall times specified here refer to the driver device and are part of the general fast I^2C-bus specification. C_b = capacitive load per bus line.

Note3: All timing values are valid within the operating supply voltage and ambient temperature ranges and are referenced to V_{IL} and V_{IH} with an input voltage swing of VSS to VDDI