Data Sheet No. PD60240

International
IOR Rectifier

IRS20124(S)PbF

Digital Audio Driver with Discrete Deadtime and Protection

Features

- 200 V high voltage ratings deliver up to 1000 W output power in Class D audio amplifier applications
- Integrated deadtime generation and bi-directional over-current sensing simplify design
- Programmable compensated preset deadtime for improved THD performances over temperature
- High noise immunity
- Shutdown function protects devices from overload conditions
- Operates up to 1 MHz
- 3.3 V/5 V logic compatible input
- RoHS compliant

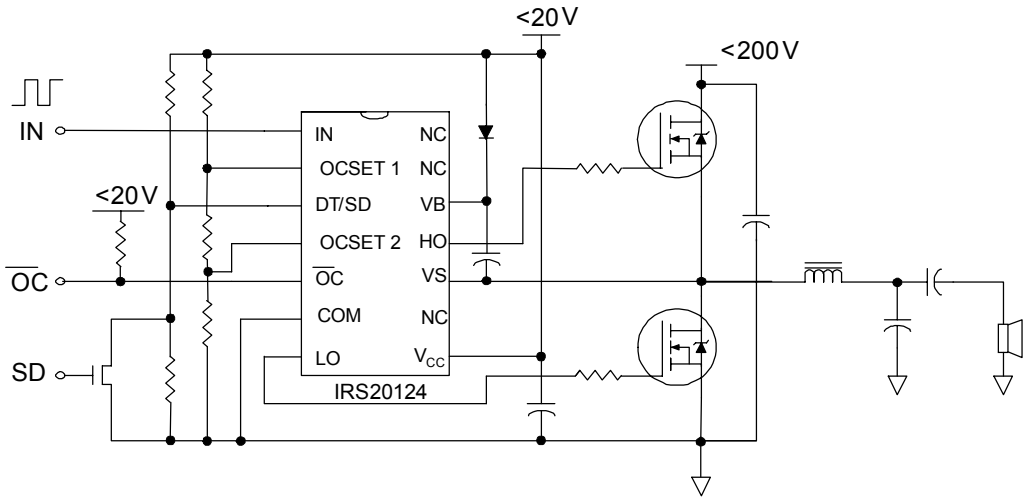
Product Summary

V_{SUPPLY}	200 V max.
I_O+/-	1 A / 1.2 A typ.
Selectable Deadtime	15 ns, 25 ns, 35 ns, 45 ns typ.
Prop Delay Time	60 ns typ.
Bi-Directional Over-Current Sensing	

Package

14-Lead SOIC

Typical Application Diagram



Description

The IRS20124 is a high voltage, high speed power MOSFET driver with internal deadtime and shutdown functions specially designed for Class D audio amplifier applications.

The internal dead time generation block provides accurate gate switch timing and enables tight deadtime settings for better THD performances.

In order to maximize other audio performance characteristics, all switching times are designed for immunity from external disturbances such as V_{CC} perturbation and incoming switching noise on the DT pin. Logic inputs are compatible with LSTTL output or standard CMOS down to 3.0 V without speed degradation. The output drivers feature high current buffers capable of sourcing 1.0 A and sinking 1.2 A. Internal delays are optimized to achieve minimal deadtime variations. Proprietary HVIC and latch immune CMOS technologies guarantee operation down to V_S= –4 V, providing outstanding capabilities of latch and surge immunities with rugged monolithic construction.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. All currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
V_B	High-side floating supply voltage	-0.3	220	V
V_S	High-side floating supply voltage	V_B-20	V_B+0.3	
V_{HO}	High-side floating output voltage	Vs-0.3	V_B+0.3	
V_{CC}	Low-side fixed supply voltage	-0.3	20	
V_{LO}	Low-side output voltage	-0.3	Vcc+0.3	
V_{IN}	Input voltage	-0.3	Vcc+0.3	
V_{OC}	OC pin input voltage	-0.3	Vcc+0.3	
V_{OCSET1}	OCSET1 pin input voltage	-0.3	Vcc+0.3	
V_{OCSET2}	OCSET2 pin input voltage	-0.3	Vcc+0.3	
dVs/dt	Allowable Vs voltage slew rate	-	50	V/ns
P_D	Maximum power dissipation	-	1.25	W
Rth_{JA}	Thermal resistance, junction to ambient	-	100	°C/W
T_J	Junction temperature	-	150	°C
T_S	Storage temperature	-55	150	
T_L	Lead temperature (soldering, 10 seconds)	-	300	

Recommended Operating Conditions

For proper operation, the device should be used within the recommended conditions. The Vs and COM offset ratings are tested with all supplies biased at a 15 V differential.

Symbol	Definition	Min.	Max.	Units
V_B	High-side floating supply absolute voltage	Vs+10	Vs+18	V
V_S	High-side floating supply offset voltage	Note 1	200	
V_{HO}	High-side floating output voltage	V_S	V_B	
V_{CC}	Low-side fixed supply voltage	10	18	
V_{LO}	Low-side output voltage	0	V_{CC}	
V_{IN}	Logic input voltage	0	V_{CC}	
V_{OC}	OC pin input voltage	0	V_{CC}	
V_{OCSET1}	OCSET1 pin input voltage	0	V_{CC}	
V_{OCSET2}	OCSET2 pin input voltage	0	V_{CC}	
T_A	Ambient Temperature	-40	125	°C

Note 1: Logic operational for V_S equal to -8 V to 200 V. Logic state held for V_S equal to -8 V to $-V_{BS}$.

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15 V, C_L = 1n F and T_A = 25 °C unless otherwise specified. Fig. 2 shows the timing definitions.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{on}	High & low-side turn-on propagation delay	—	60	80	ns	V_S=0 V
t_{off}	High & low-side turn-off propagation delay	—	60	80		V_S=200 V
t_r	Turn-on rise time	—	25	40		
t_f	Turn-off fall time	—	15	35		
t_{sd}	Shutdown propagation delay	—	140	200		
t_{oc}	Propagation delay time from V_S>V_{soc}+ to OC	—	280	—		OC_{SET1}=3.22 V OC_{SET2}=1.20 V
$t_{woc\ min}$	OC pulse width	—	100	—		
$t_{oc\ filt}$	OC input filter time	—	200	—		
DT1	Deadtime: LO turn-off to HO turn-on (DT_{LO-HO}) & HO turn-off to LO turn-on (DT_{HO-LO})	0	15	40		V_{DT}>V_{DT1}
DT2	Deadtime: LO turn-off to HO turn-on (DT_{LO-HO}) & HO turn-off to LO turn-on (DT_{HO-LO})	5	25	50		V_{DT1}>V_{DT}> V_{DT2}
DT3	Deadtime: LO turn-off to HO turn-on (DT_{LO-HO}) & HO turn-off to LO turn-on (DT_{HO-LO})	10	35	60		V_{DT2}>V_{DT}>V_{DT3}
DT4	Deadtime: LO turn-off to HO turn-on (DT_{LO-HO}) & HO turn-off to LO turn-on (DT_{HO-LO})V_DT= V_{DT4}	15	45	70		V_{DT3}>V_{DT}>V_{DT4}

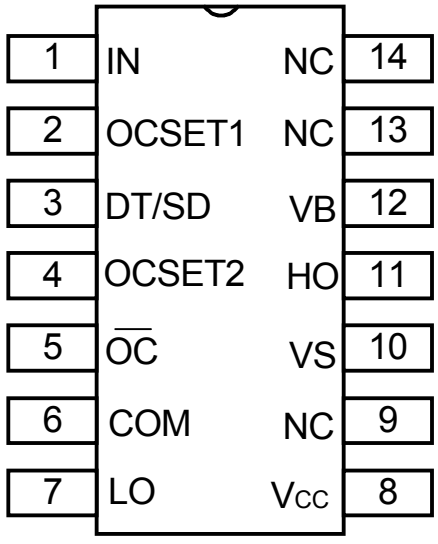
Static Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15 V and T_A = 25 °C unless otherwise specified.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
V_{IH}	Logic high input voltage	2.5	—	—	V	Vcc=10 V -20 V
V_{IL}	Logic low input voltage	—	—	1.2		
V_{OH}	High level output voltage, $V_{BIAS} - V_O$	—	—	1.2		Io=0 A
V_{OL}	Low level output voltage, V_O	—	—	0.1		
UV_{CC+}	V_{CC} supply UVLO positive threshold	8.3	9.0	9.7		
UV_{CC-}	V_{CC} supply UVLO negative threshold	7.5	8.2	8.9		
UV_{BS+}	High-side well UVLO positive threshold	8.3	9.0	9.7		
UV_{BS-}	High-side well UVLO negative threshold	7.5	8.2	8.9		
I_{QBS}	High-side quiescent current	—	—	1	mA	
I_{QCC}	Low-side quiescent current	—	—	4		V_{DT}=Vcc
I_{LK}	High-to-low-side leakage current	—	—	50	µA	V_B=V_S =200 V
I_{IN+}	Logic “1” input bias current	—	3	10		V_{IN}=3.3 V
I_{IN-}	Logic “0” input bias current	—	0	1.0		V_{IN} = 0 V
I_{o+}	Output high short circuit current (source)	—	1.0	—	A	Vo=0 V, PW<10 µs
I_{o-}	Output low short circuit current (sink)	—	1.2	—		Vo=15 V, PW<10 µs
V_{DT1}	DT mode select threshold 1	0.8(Vcc)	0.89(Vcc)	0.97(Vcc)	V	
V_{DT2}	DT mode select threshold 2	0.51(Vcc)	0.57(Vcc)	0.63(Vcc)		
V_{DT3}	DT mode select threshold 3	0.32(Vcc)	0.36(Vcc)	0.40(Vcc)		
V_{DT4}	DT mode select threshold 4	0.21(Vcc)	0.23(Vcc)	0.25(Vcc)		
V_{SOC+}	OC threshold in V_S	0.75	1.0	1.25		OC_{SET1}=3.22 V OC_{SET2}=1.20 V
V_{SOC-}	OC threshold in V_S	-1.25	-1.0	-0.75		OC_{SET1}=3.22 V OC_{SET2}=1.20 V

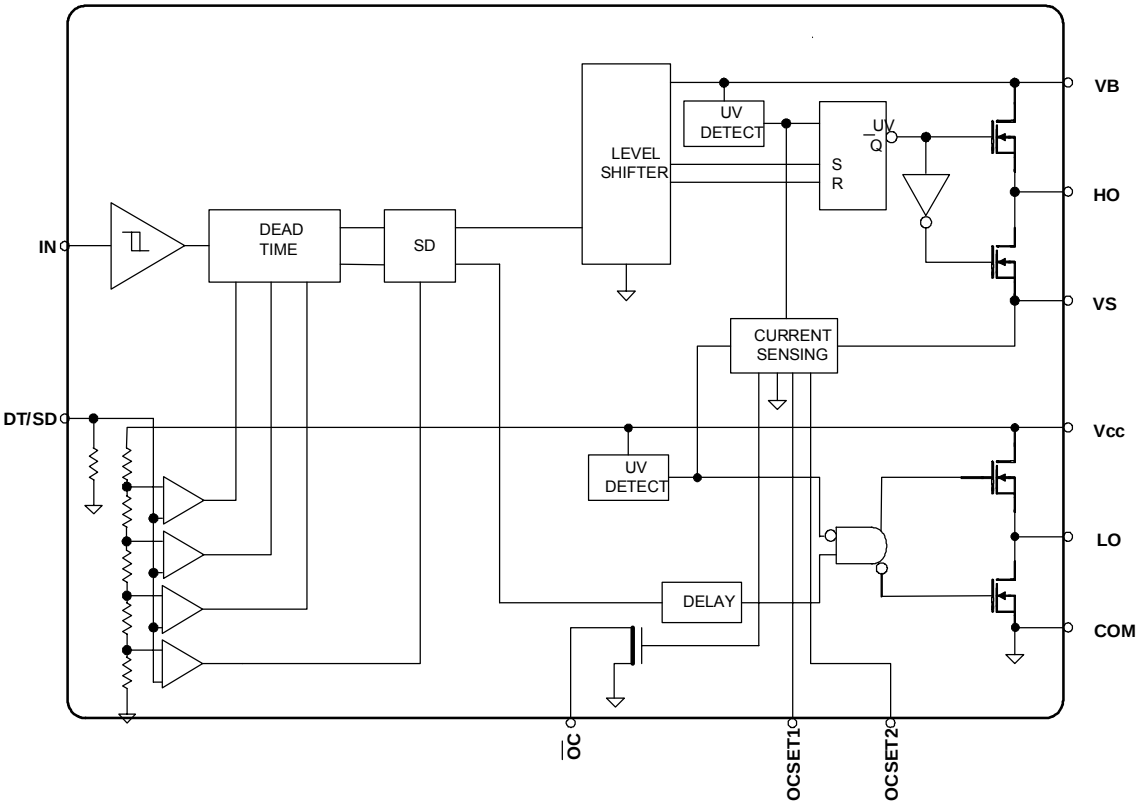
Lead Definitions

Symbol	Description
VCC	Low-side logic supply voltage
VB	High-side floating supply
HO	High-side output
VS	High-side floating supply return
IN	Logic input for high-side and low-side gate driver outputs (HO and LO), in phase with HO
DT/SD	Input for programmable deadtime, referenced to COM. shutdown LO and HO when tied to COM
COM	Low-side supply return
LO	Low-side output
OC	Over-current output (negative logic)
OC_{SET1}	Input for setting negative over current threshold
OC_{SET2}	Input for setting positive over current threshold



IR20124S 14 Lead SOIC (narrow body)

Block Diagram



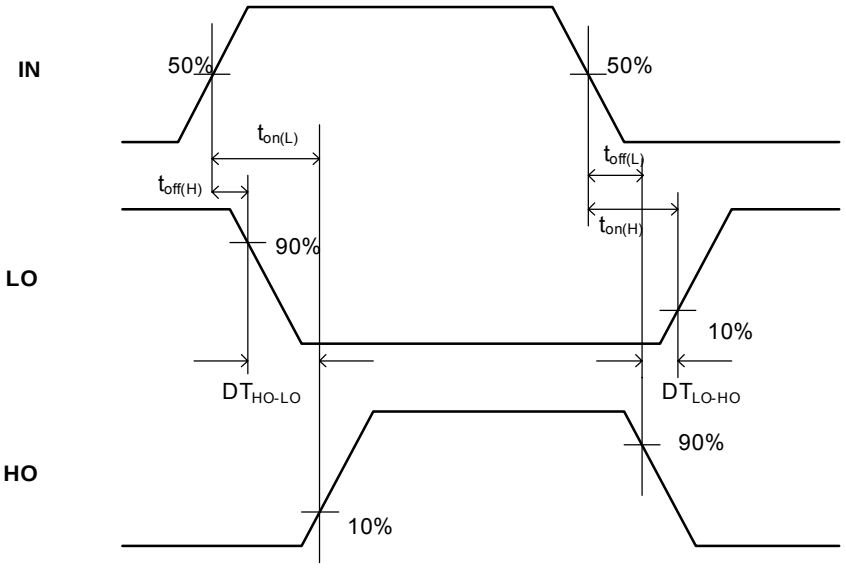


Figure 1. Switching Time Waveform Definitions

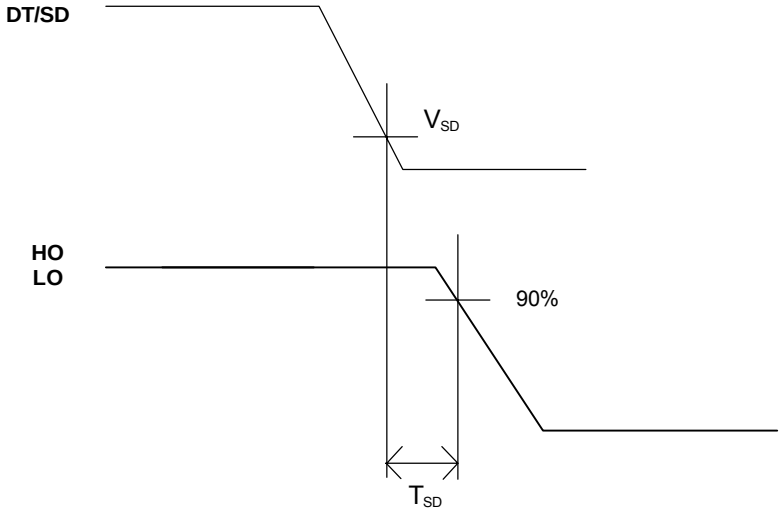


Figure 2. Shutdown Waveform Definitions

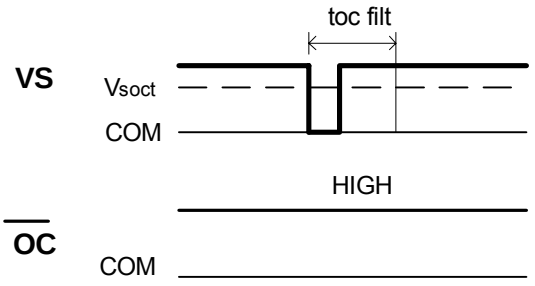


Figure 3. OC Input FilterTime Definitions

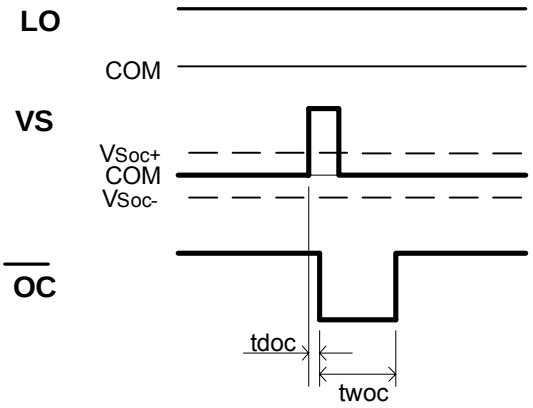


Figure 4. OC Waveform Definitions

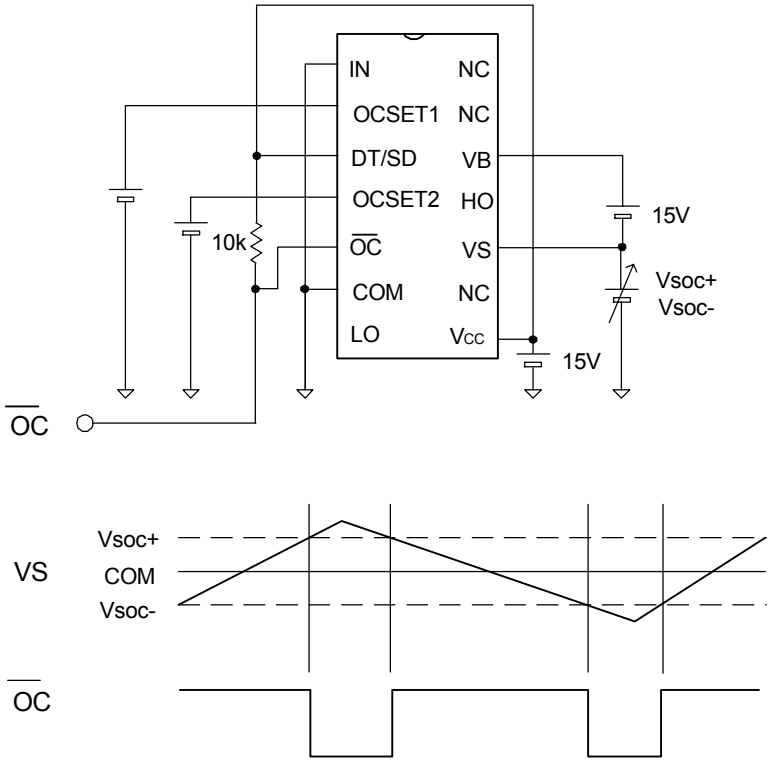


Figure 5. OC Waveform Definitions

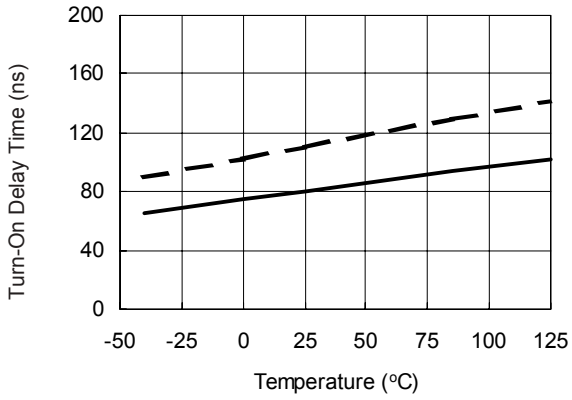


Figure 6A. Turn-On Time vs. Temperature

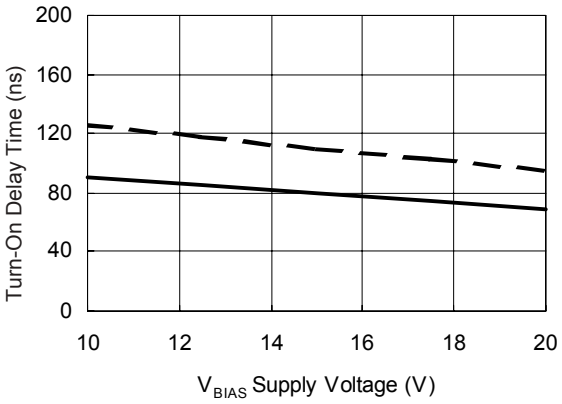


Figure 6B. Turn-On Time vs. Supply Voltage

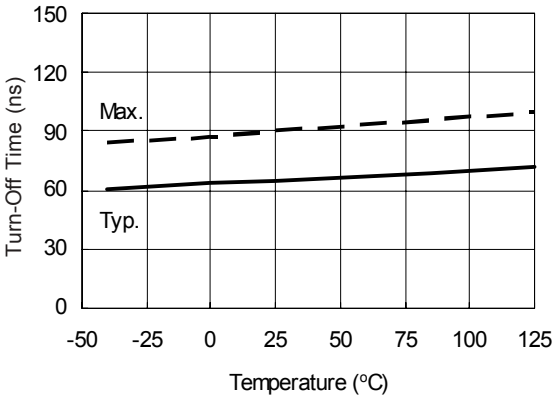


Figure 7A. Turn-Off Time vs. Temperature

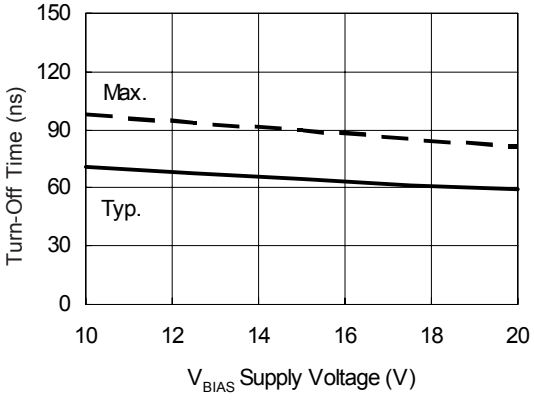
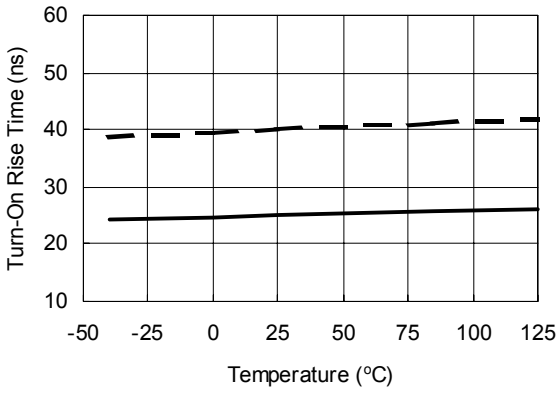


Figure 7B. Turn-Off Time vs. Supply Voltage



Fiure 8A. Turn-On Rise Time vs.Temperature

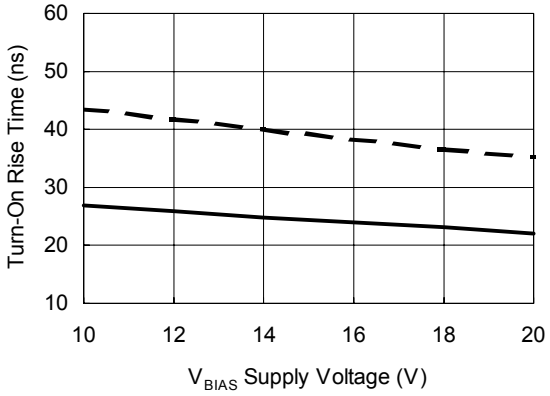


Figure 8B. Turn-On Rise Time vs. Supply Voltage

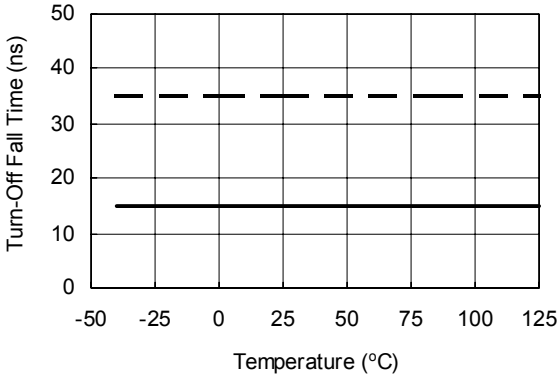


Figure 9A. Turn-Off Fall Time vs. Temperature

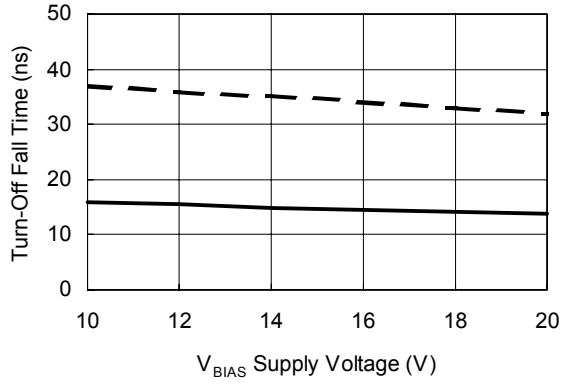


Figure 9B. Turn-Off Fall Time vs. Supply Voltage

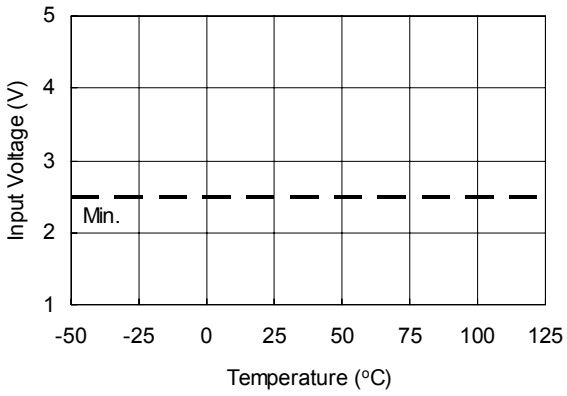


Figure 10A. Logic "1" Input Voltage vs. Temperature

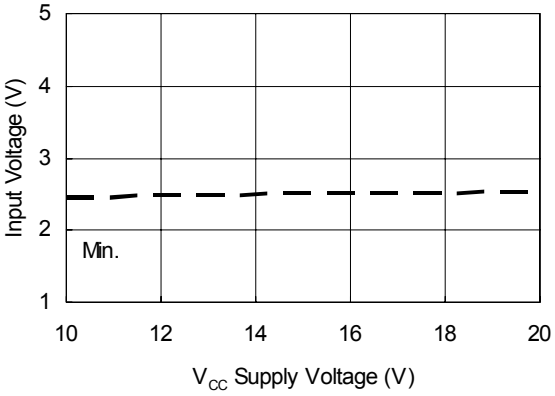


Figure 10B. Logic "1" Input Voltage vs. Supply Voltage

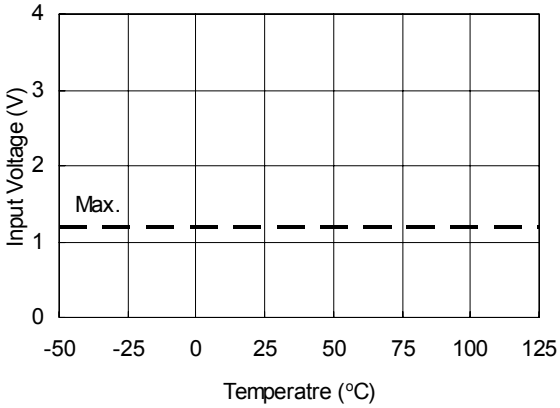


Figure 11A. Logic "0" Input Voltage vs. Temperature

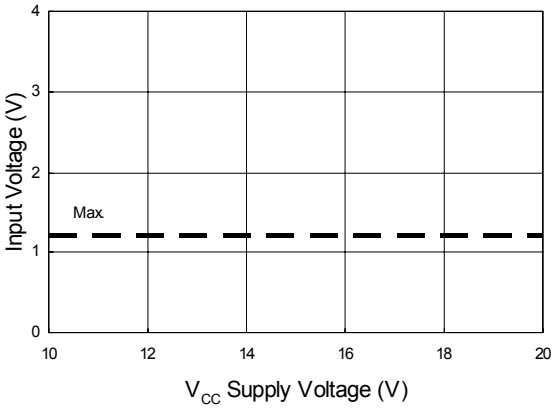


Figure 11B. Logic "0" Input Voltage vs. Supply Voltage

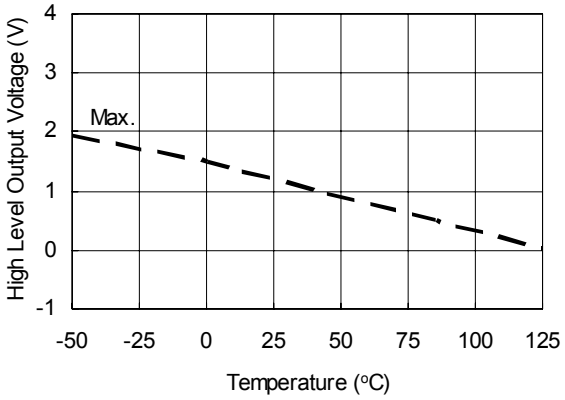


Figure 12A. High Level Output vs. Temperature

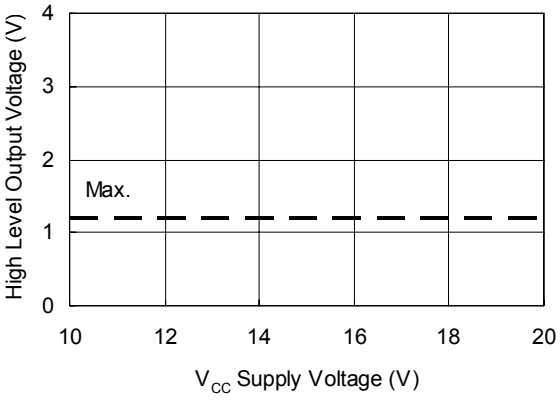


Figure 12B. High Level Output vs. Supply Voltage

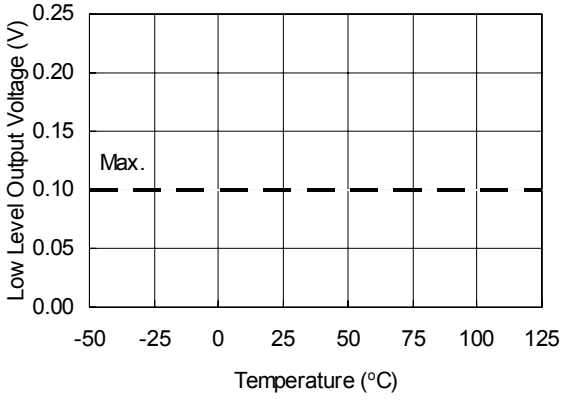


Figure 13A. Low Level Output vs.Temperature

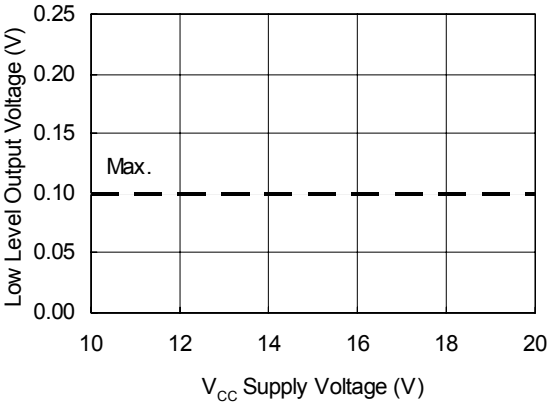


Figure 13B. Low Level Output vs. Supply Voltage

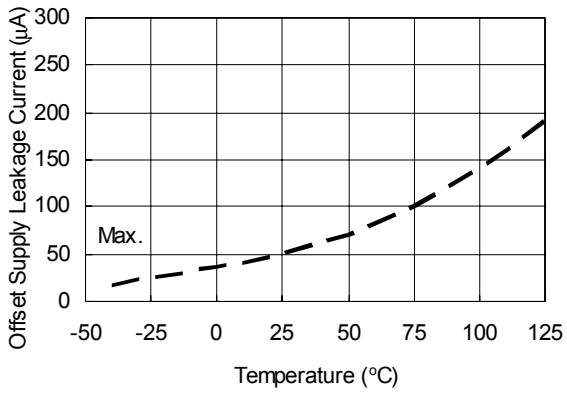


Figure 14A. Offset Supply Leakage Current vs. Temperature V_B= 200 V

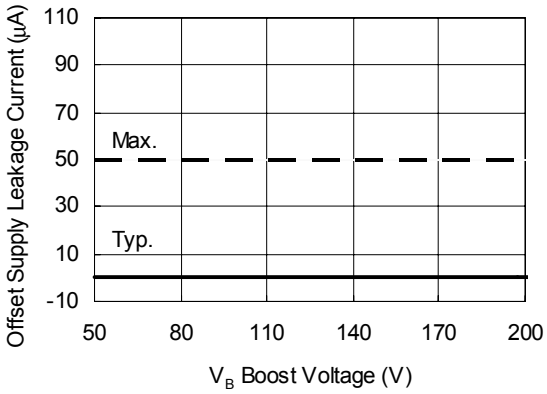


Figure 14B. Offset Supply Leakage Current vs. Supply Voltage

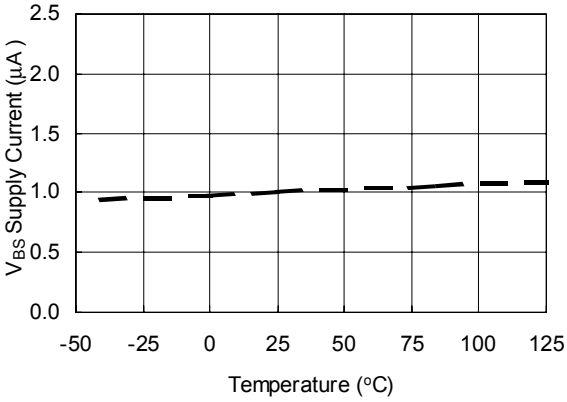


Figure 15A. V_{BS} Supply Current vs. Temperature

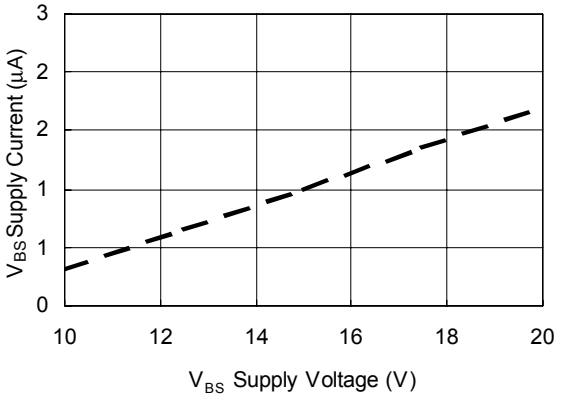


Figure 15B. V_{BS} Supply Current vs. Supply Voltage

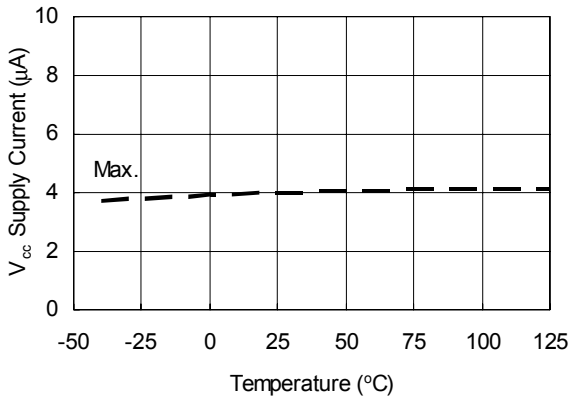


Figure 16A. V_{CC} Supply Current vs. Temperature

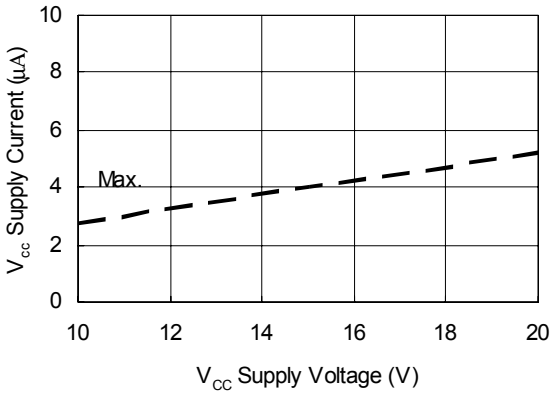


Figure 16B. V_{CC} Supply Current vs. Supply Voltage

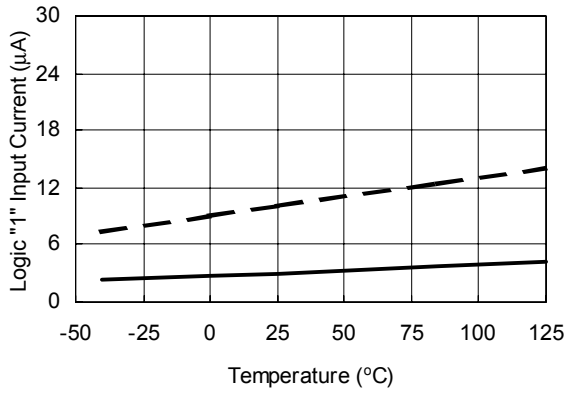


Figure 17A. Logic "1" Input Current vs. Temperature

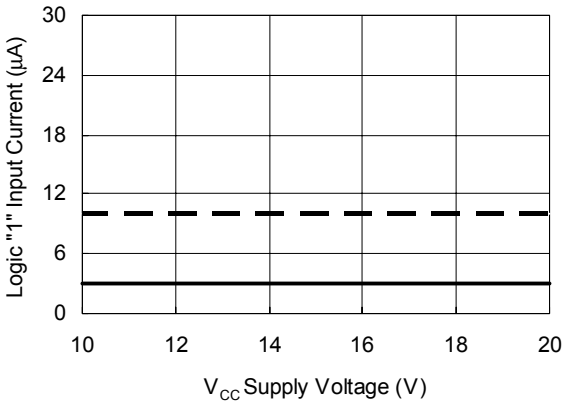


Figure 17B. Logic "1" Input Current vs. Supply Voltage

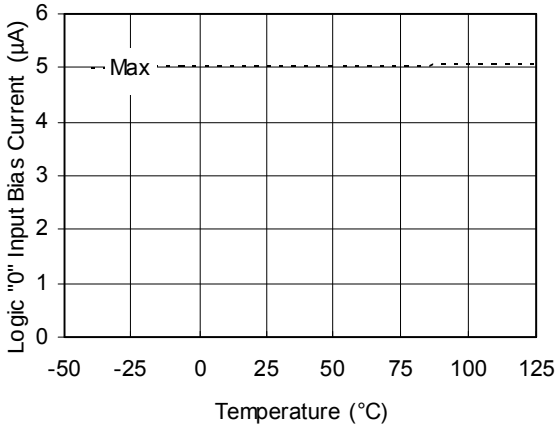


Figure 18A. Logic "0" Input Bias Current vs. Temperature

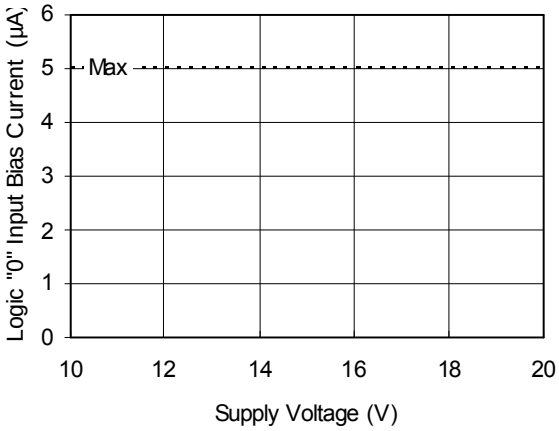


Figure 18B. Logic "0" Input Bias Current vs. Voltage

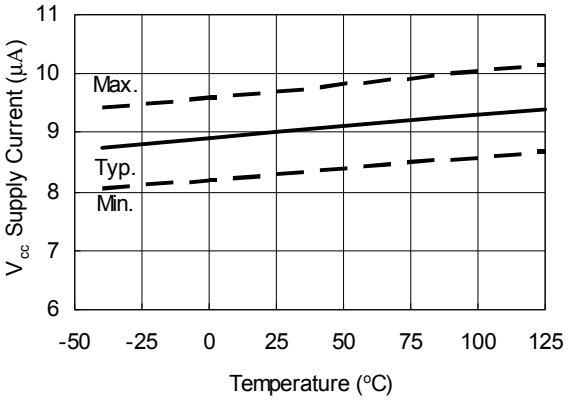


Figure 19. V_{cc} Undervoltage Threshold (+) vs. Temperature

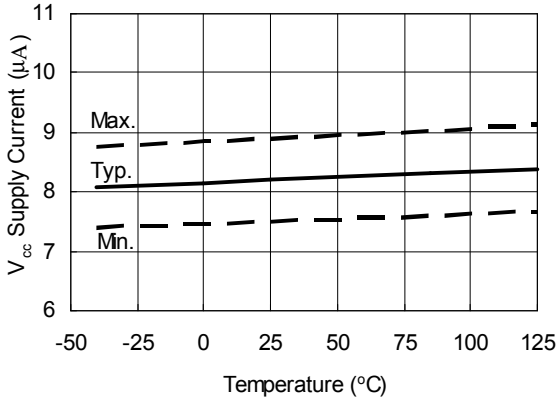


Figure 20. V_{cc} Undervoltage Threshold (-) vs. Temperature

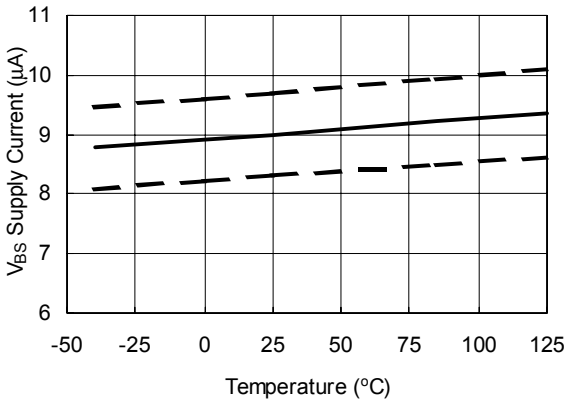


Figure 21. V_{BS} Undervoltage Threshold (+) vs. Temperature

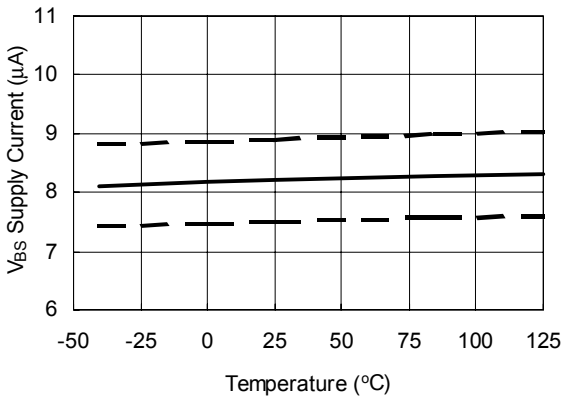


Figure 22. V_{BS} Undervoltage Threshold (-) vs. Temperature

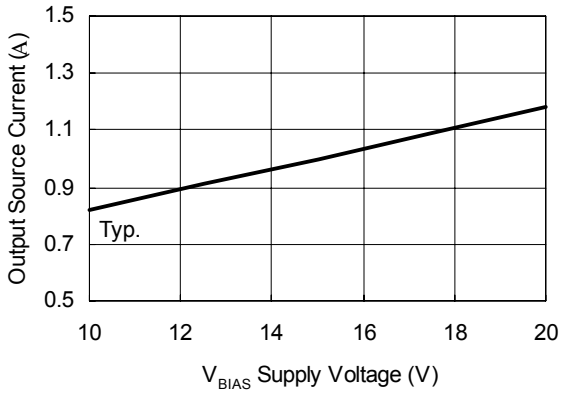


Figure 23. Output Source Current vs. Supply Voltage

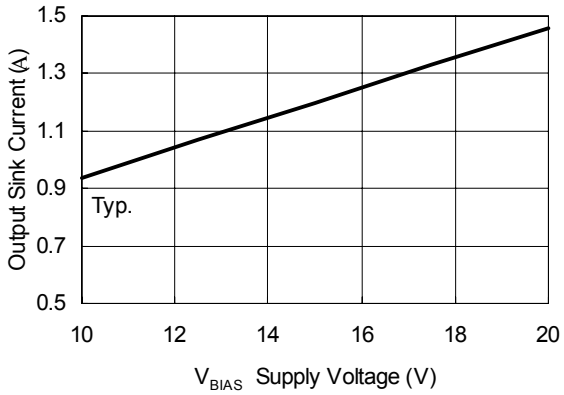


Figure 24. Output Sink Current vs. Supply Voltage

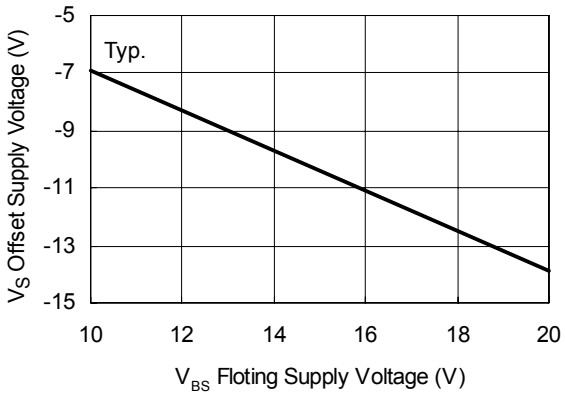


Figure 25. Maximum V_S Negative Offset vs. Supply Voltage

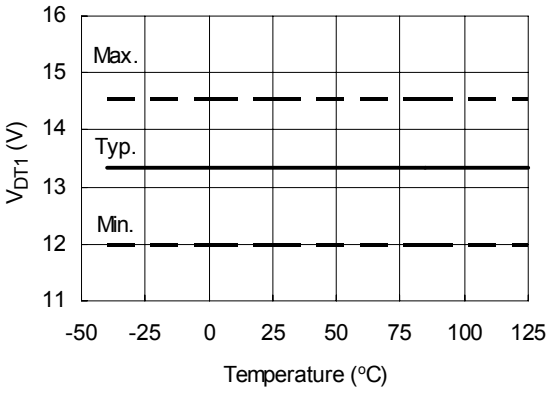


Figure 26. DT Mode Select Threshold (1) vs. Temperature

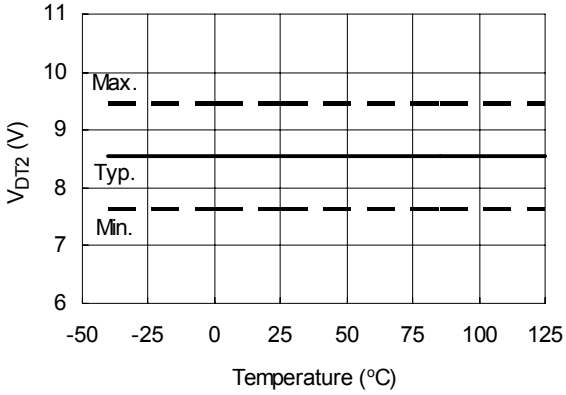


Figure 27. DT Mode Select Threshold (2) vs. Temperature

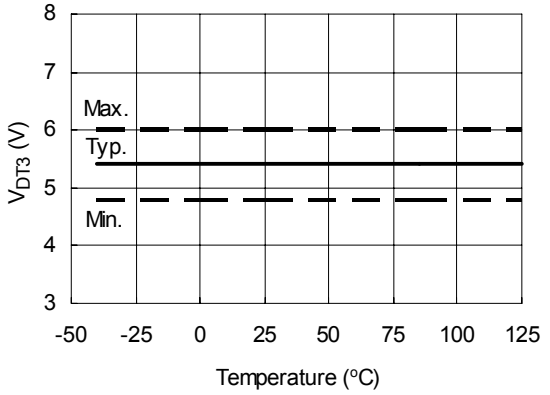


Figure 28. DT Mode Select Threshold (3) vs. Temperature

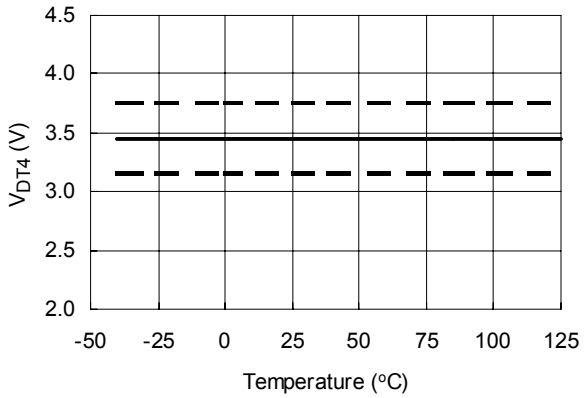


Figure 29. DT Mode Select Threshold (4) vs. Temperature

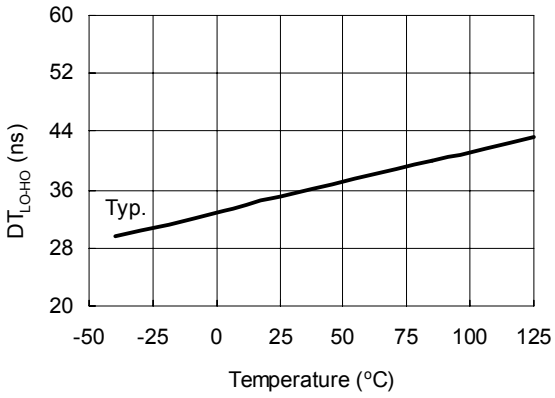


Figure 30. DT LO Turn-Off to HO TurnOon (3) vs. Temperature

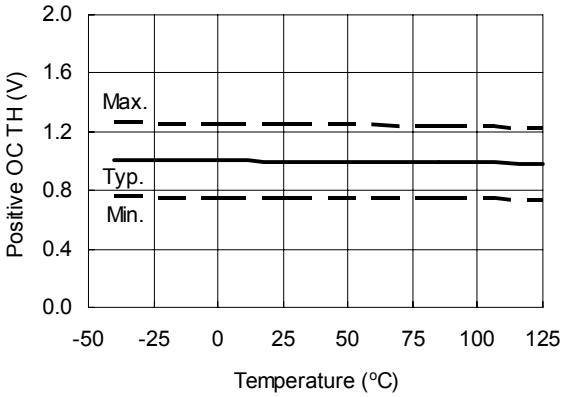


Figure 31. Positive OC Threshold(+) in V_S vs. Temperature

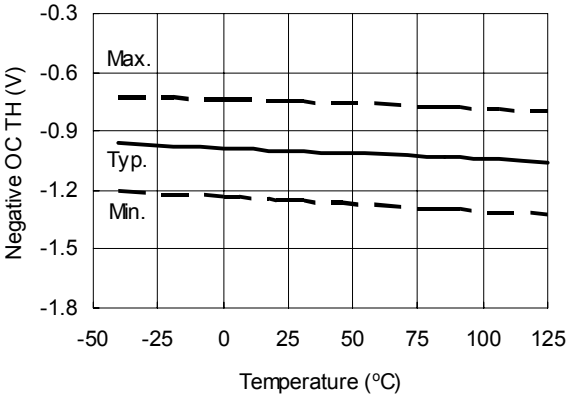


Figure 32. Negative OC Threshold(-) in V_S vs. Temperature

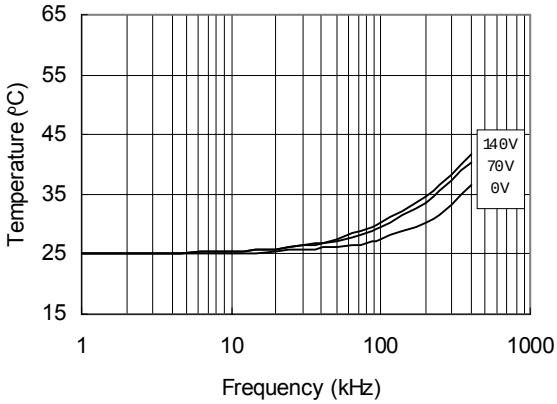


Figure 33. IRS20124S vs. Frequency (IRFBC20)
R_{gate}=33 Ω, V_{CC}=12 V

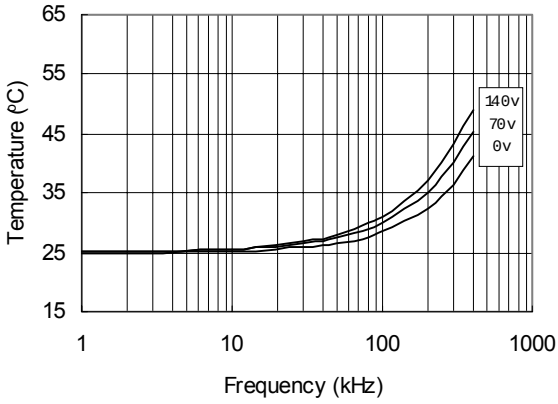


Figure 34. IRS20124S vs. Frequency (IRFBC30)
R_{gate}=22 Ω, V_{CC}=12 V

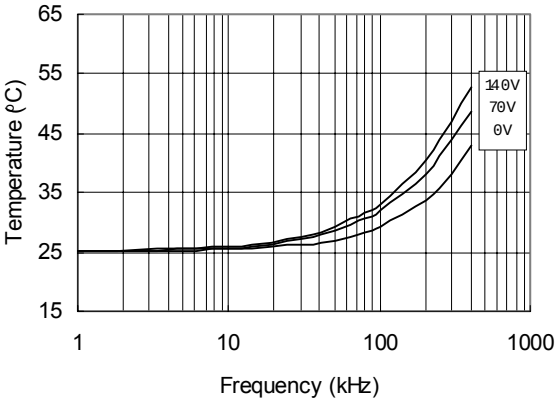


Figure 35. IRS20124S vs. Frequency (IRFBC40)
R_{gate}=15 Ω, V_{CC}=12 V

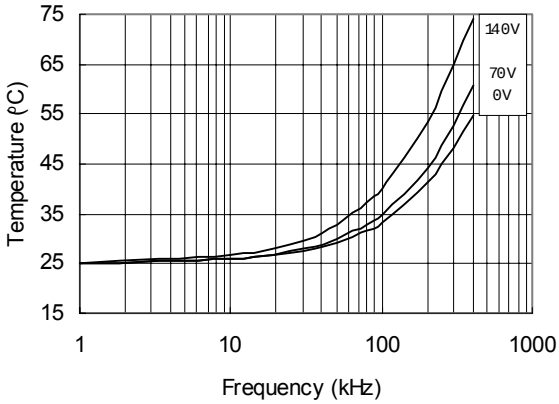


Figure 36. IRS20124S vs. Frequency (IRFPE50)
R_{gate}=10 Ω, V_{CC}=12 V

Functional description

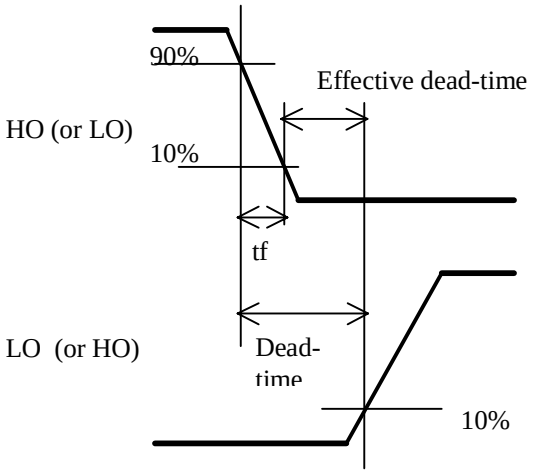
Programmable Dead-time

The IRS20124 has an internal deadtime generation block to reduce the number of external components in the output stage of a Class D audio amplifier. Selectable deadtime through the DT/SD pin voltage is an easy and reliable function, which requires only two external resistors. The deadtime generation block is also designed to provide a constant deadtime interval, independent of V_{cc} fluctuations. Since the timings are critical to the audio performance of a Class D audio amplifier, the unique internal deadtime generation block is designed to be immune to noise on the DT/SD pin and the Vcc pin. Noise-free programmable deadtime function is available by selecting deadtime from four preset values, which are optimized and compensated.

How to Determine Optimal Deadtime

Please note that the effective deadtime in an actual application differs from the deadtime specified in this datasheet due to finite fall time, t_f. The deadtime value in this datasheet is defined as the time period from the starting point of turn-off on one side of the switching stage to the starting point of turn-on on the other side as shown in Fig. 5. The fall time of MOSFET gate voltage must be subtracted from the deadtime value in the datasheet to determine the effective dead time of a Class D audio amplifier.

(Effective deadtime)
= (Deadtime in datasheet) – (fall time, t_f)

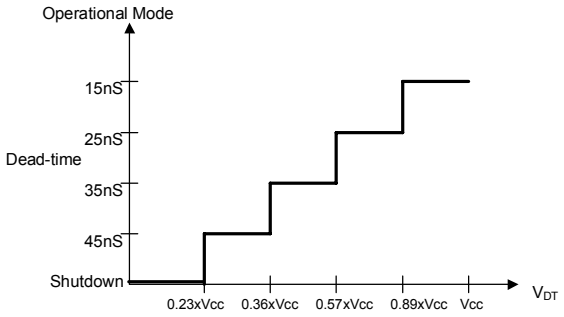


Effective Deadtime

A longer deadtime period is required for a MOSFET with a larger gate charge value because of the longer t_f. A shorter effective deadtime setting is always beneficial to achieve better linearity in the Class D switching stage. However, the likelihood of shoot-through current increases with narrower deadtime settings in mass production. Negative values of effective deadtime may cause excessive heat dissipation in the MOSFETs, potentially leading to their serious damage. To calculate the optimal deadtime in a given application, the fall time (t_f)for both output voltages, HO and LO, in the actual circuit needs to be measured. In addition, the effective deadtime can also vary with temperature and device parameter variations. Therefore, a minimum effective deadtime of 10 ns is recommended to avoid shoot-through current over the range of operating temperatures and supply voltages.

DT/SD pin

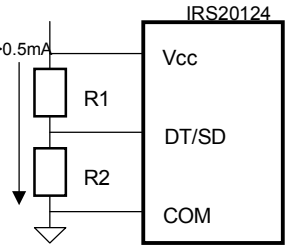
DT/SD pin provides two functions: 1) setting deadtime and 2) shutdown. The IRS20124 determines its operation mode based on the voltage applied to the DT/SD pin. An internal comparator translates which mode is being used by comparing internal reference voltages. Threshold voltages for each mode are set internally by a resistive voltage divider off V_{CC}, negating the need of using a precise absolute voltage to set the mode.



Deadtime Settings vs V_{DT} Voltage

Design Example

Table 1 shows suggested values of resistance for setting the deadtime. Resistors with up to 5% tolerance can be used if these listed values are followed.



External Resistor

Deadtime mode	R1 (Ω)	R2 (Ω)	DT/SD (V)
DT1	<10k	Open	1.00 (Vcc)
DT2	3.3k	8.2k	0.71 (Vcc)
DT3	5.6k	4.7k	0.46 (Vcc)
DT4	8.2k	3.3k	0.29 (Vcc)

Table 1. Suggested Resistor Values for Deadtime Settings

Shutdown

Since IRS20124 has internal deadtime generation, independent inputs for HO and LO are no longer provided. Shutdown mode is the only way to turn off both MOSFETs simultaneously to protect them from over current conditions. If the DT/SD pin detects an input voltage below the threshold, $V_{DT4,}$ the IRS20124 will output 0 V at both HO and LO outputs, forcing the switching output node to go into a high impedance state.

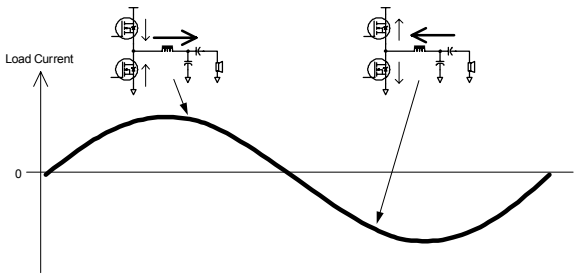
Over Current Sensing

In order to protect the power MOSFET, IRS20124 has a feature to detect over-current conditions, which can occur when speaker wires are shorted together. The over-current shutdown feature can be configured by combining the current sensing function with the shutdown mode via the DT/SD pin.

Load Current Direction in Class D Audio Application

In a Class D audio amplifier, the direction of the load current alternates according to the audio input signal. An over current condition can therefore happen during either a positive current cycle or a negative current cycle. It should be noted that

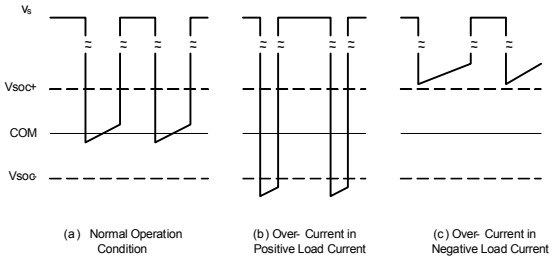
each MOSFET carries a part of the load current in an audio cycle. Bi-directional current sensing offers over current detection capabilities in both cases by monitoring only the low side MOSFET.



Direction in MOSFET Current and Load Current

Bi-Directional Current Sensing

IRS20124 has an over-current detection function utilizing $R_{DS(ON)}$ of the low side switch as a current sensing shunt resistor. Due to the proprietary HVIC process, the IRS20124 is able to sense negative as well as positive current flow, enabling bi-directional load current sensing without the need for any additional external passive components.

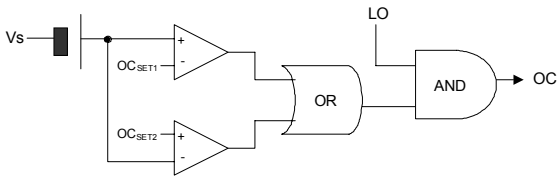


Vs Waveform in Over-Current Condition

IRS20124 measures the current during the period when the low side MOSFET is turned on. Under normal operating conditions, V_S voltage for the low side switch is well within the trip threshold boundaries, V_{SOC-} and V_{SOC+}. In the case of Fig. 9(b) which demonstrates the amplifier sourcing too much current to the load, the Vs node is found below the trip level, V_{SOC-}. In Fig. 9(c) with opposite current direction, the amplifier sinks too much current from the load, positioning V_S well above trip level, V_{SOC+}.

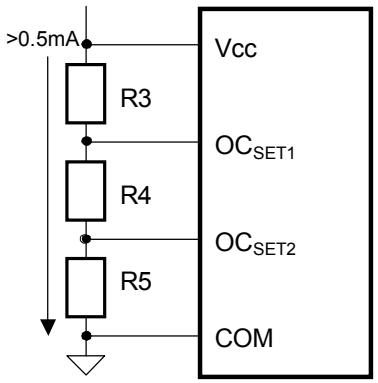
Once the voltage in V_S exceeds the preset threshold, the OC pin pulls down to COM to detect an over-current condition.

Since the switching waveform usually contains over/under shoot and associated oscillatory artifacts on their transient edges, a 200 ns blanking interval is inserted in the V_S voltage sensing block at the instant the low side switch is engaged. Because of this blanking interval, the OC function will be unable to detect over current conditions if the low side ON duration less than 200 ns.



Simplified Functional Block Diagram of Bi-Directional Current Sensing

The bi-directional current sensing block has an internal V level shifter feeding the signal to the comparator. OC_{SET1} sets the threshold, and is given a trip level at V_{SOC+}, which is OC_{SET1} -V. In the same way, for a given OC_{SET2}, V_{SOC-} is set at OC_{SET2} -V.



External Resistor Network to Set OC Threshold

How to set OC Threshold

The positive and negative trip thresholds for bi-directional current sensing are set by the voltages at OC_{SET1} and OC_{SET2}.

The trip threshold voltages, V_{SOC+} and $V_{SOC+,}$ are determined by the required trip current levels, I_{TRIP+} I_{TRIP-}, and $R_{DS(ON)}$ in the low side MOSFET.
Since the sensed voltage of V_S is shifted up by 2.21 V internally and compared with the voltages fed to the OC_{SET1} and OC_{SET2} pins, the required value of OC_{SET1} with respect to COM is

$$V_{OCSET1} = V_{SOC+} + 2.21\ V = I \times R_{DS(ON)} + 2.21\ V$$

The same relation holds between OC_{SET2} and $V_{SOC-,}$

$$V_{OCSET2} = V_{SOC-} + 2.21\ V = I \times R_{DS(ON)} + 2.21\ V$$

In general, $R_{DS(ON)}$ has a positive temperature coefficient that needs to be considered when the threshold level is being set. Please also note that, in the negative load current direction, the sensing voltage at the V_S node is limited by the body diode of the low side MOSFET as explained later.

Design Example

This example demonstrates how to use the external resistor network to set I_{TRIP+} and I_{TRIP-} to be ±11 A, using a MOSFET that has $R_{DS(ON)}$=60 μΩ.

$$V_{ISET1} = V_{TH+} + 2.21\ V = I_{TRIP+} \times R_{DS(ON)} + 2.21 V = 11 \times 60\ \mu\Omega + 2.21\ V = 2.87\ V$$
$$V_{ISET2} = V_{TH-} + 2.21\ V = I_{TRIP-} \times R_{DS(ON)} + 2.21 V = (-11)\ V \ 60\ \mu\Omega + 2.21\ V = 1.55\ V$$

The total resistance of resistor network is based on the voltage at the V_{CC} and required bias current in this resistor network.

$$R_{total} = R3 + R4 + R5 = Vcc / I_{bias} = 12\ V\ /\ 1\ \mu A = 12\ k\Omega$$

The expected voltage across R3 is Vcc- V_{ISET1} = 12 V - 2.87 V=9.13 V. Similarly, the voltages across R4 is V_{SOC+} - V_{SOC-} = 2.87 V - 1.55 V =1.32 V, and the voltage across R5 is V_{ISET2}= 1.55 V respectively.

R3 =9.13 V/ I_{bias} = 9.13kΩ
R4 =1.32 V/ I_{bias} = 1.32kΩ
R5 =1.55 V/ I_{bias} = 1.55kΩ

Choose R3= 9.09 kΩ R4=1.33 kΩ, R5=1.54 kΩ from E-96 series.
Consequently, actual threshold levels are
V_{SOC+} =2.88 V gives I_{TRIP+} = 11.2 A
V_{SOC-} =1.55 V gives I_{TRIP-} = -11.0 A

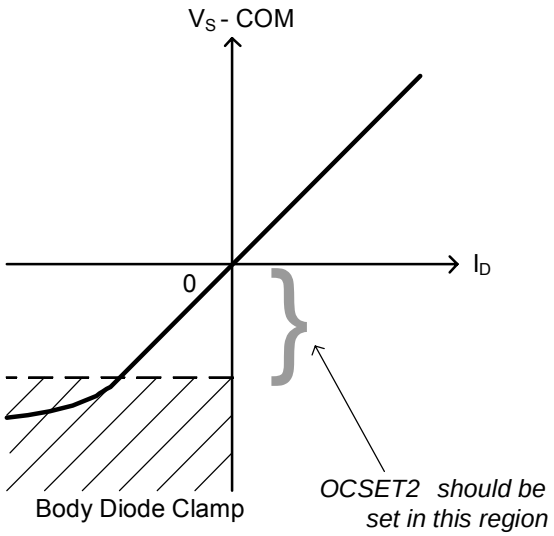
Resisters with 1% tolerances are recommended.

OC Output Signal

The OC pin is a 20 V open drain output. The OC pin is pulled down to ground when an over current condition is detected. A single external pull-up resistor can be shared by multiple IRS20124 OC pins to form the ORing logic. In order for a micro-processor to read the OC signal, this information is buffered with a mono stable multi vibrator to ensure 100 ns minimum pulse width.
Because of unpredictable logic status of the OC pin, the OC signal should be ignored during power up/down.

Limitation from Body Diode in MOSFET

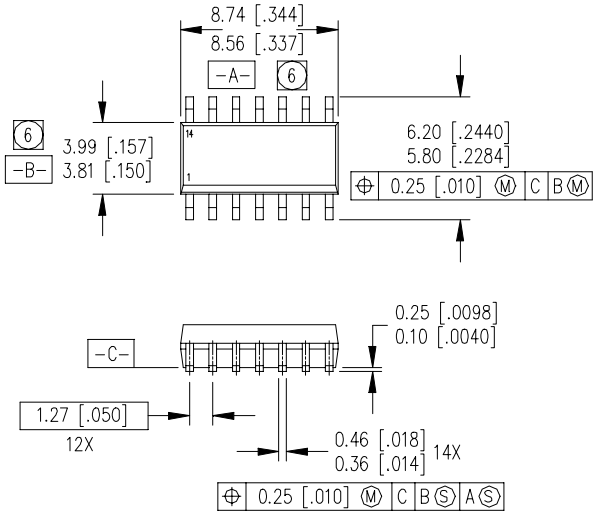
When a Class D stage outputs a positive current, flowing from the Class D amp to the load, the body diode of the MOSFET will turn on when the drain to source voltage of the MOSFET become larger than the diode forward drop voltage. In such a case, the sensing voltage at the V_S pin of the IRS20124 is clamped by the body diode. This means that the effective $R_{DS(ON)}$ is now much lower than expected from $R_{DS(ON)}$ of the MOSFET, and the V_S node my not able to reach the threshold to turn the OC output on before the MOSFET fails. Therefore, the region where body diode clamping takes a place should be avoided when setting V_{SOC-}.



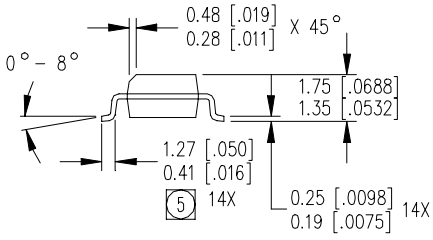
Body Diode in MOSFET Clamps vs Voltage

For further application information for gate driver IC please refer to AN-978 and DT98-2a. For further application information for class D application, please refer to AN-1070 and AN-1071.

Case Outline



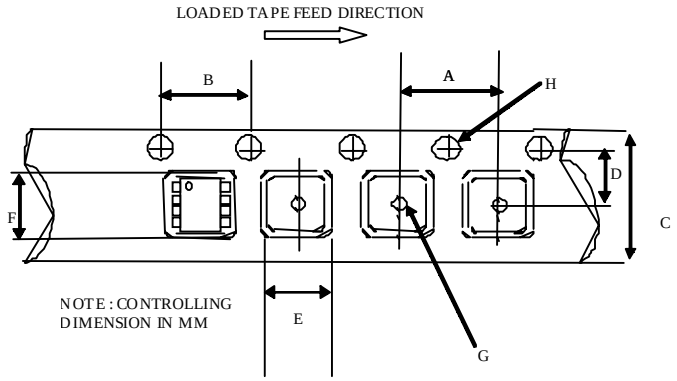
NOTES:
1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982.
2 CONTROLLING DIMENSION: MILLIMETER
3 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4 OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AB.
5 DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.
6 DIMENSION DOES NOT INCLUDE MOLD PROTUSIONS. MOLD PROTUSIONS SHALL NOT EXCEED 0.15 [.006].



14 Lead SOIC (narrow body)

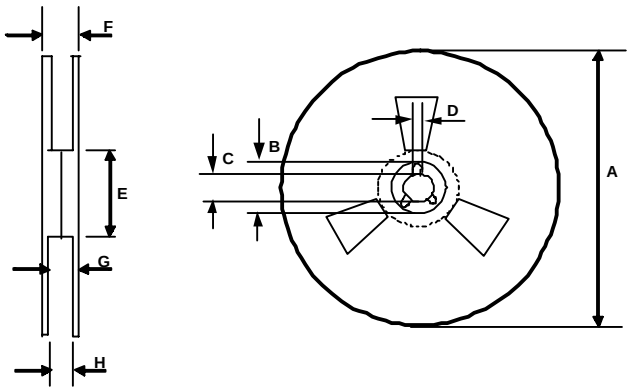
01-6019
01-3063 00 (MS-012AB)

Tape & Reel
14-Lead SOIC



CARRIER TAPE DIMENSION FOR 14SOICN

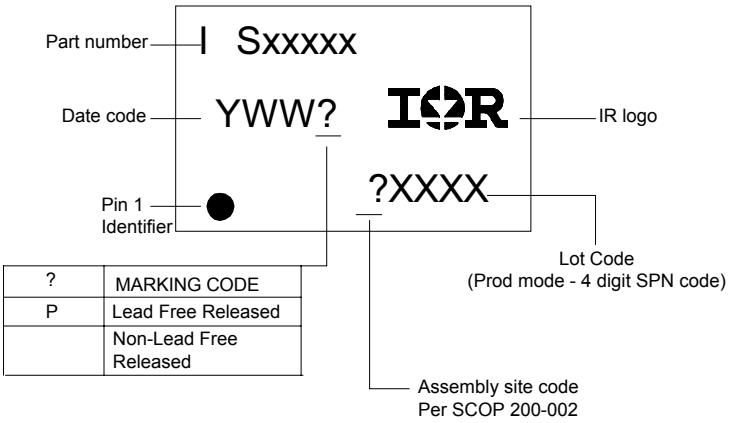
	Metric		Imperial	
Code	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	15.70	16.30	0.618	0.641
D	7.40	7.60	0.291	0.299
E	6.40	6.60	0.252	0.260
F	9.40	9.60	0.370	0.378
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 14SOICN

	Metric		Imperial	
Code	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	22.40	n/a	0.881
G	18.50	21.10	0.728	0.830
H	16.40	18.40	0.645	0.724

LEADFREE PART MARKING INFORMATION



?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Released

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14-Lead SOIC IRS20124SPbF
14-Lead SOIC Tape & Reel IRS20124STRPbF

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This product has been designed and qualified for the industrial level.
Qualification standards can be found at IR's Web Site http://www.irf.com

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