

Complementary Darlington Power Transistor

DPAK For Surface Mount Applications

MJD122, NJVMJD122 (NPN), MJD127, NJVMJD127 (PNP)

Designed for general purpose amplifier and low speed switching applications.

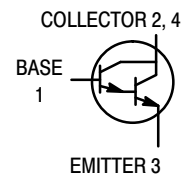
Features

- Lead Formed for Surface Mount Applications in Plastic Sleeves
- Surface Mount Replacements for 2N6040–2N6045 Series, TIP120–TIP122 Series, and TIP125–TIP127 Series
- Monolithic Construction With Built-in Base-Emitter Shunt Resistors
- High DC Current Gain: $h_{FE} = 2500$ (Typ) @ $I_C = 4.0$ Adc
- Epoxy Meets UL 94 V-0 @ 0.125 in
- ESD Ratings:
 - ◆ Human Body Model, $3B > 8000$ V
 - ◆ Machine Model, $C > 400$ V
- NJV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

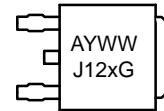
**SILICON
POWER TRANSISTOR
8 AMPERES
100 VOLTS, 20 WATTS**



**DPAK
CASE 369C
STYLE 1**



MARKING DIAGRAM



- A = Assembly Location
- Y = Year
- WW = Work Week
- x = 2 or 7
- G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	100	Vdc
Collector-Base Voltage	V_{CB}	100	Vdc
Emitter-Base Voltage	V_{EB}	5	Vdc
Collector Current Continuous Peak	I_C	8 16	Adc
Base Current	I_B	120	mAdc
Total Power Dissipation @ $T_C = 25\text{ }^\circ\text{C}$ Derate above $25\text{ }^\circ\text{C}$	P_D	20 0.16	W W/ $^\circ\text{C}$
Total Power Dissipation (Note 1) @ $T_A = 25\text{ }^\circ\text{C}$ Derate above $25\text{ }^\circ\text{C}$	P_D	1.75 0.014	W W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	6.25	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient (Note 1)	$R_{\theta JA}$	71.4	$^\circ\text{C/W}$

1. These ratings are applicable when surface mounted on the minimum pad sizes recommended.

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ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage ($I_C = 30\text{ mA}$, $I_B = 0$)	$V_{CE(sus)}$	100	–	Vdc
Collector Cutoff Current ($V_{CE} = 50\text{ Vdc}$, $I_B = 0$)	I_{CEO}	–	10	μAdc
Collector Cutoff Current ($V_{CB} = 100\text{ Vdc}$, $I_E = 0$)	I_{CBO}	–	10	μAdc
Emitter Cutoff Current ($V_{BE} = 5\text{ Vdc}$, $I_C = 0$)	I_{EBO}	–	2	mA

ON CHARACTERISTICS

DC Current Gain ($I_C = 4\text{ Adc}$, $V_{CE} = 4\text{ Vdc}$) ($I_C = 8\text{ Adc}$, $V_{CE} = 4\text{ Vdc}$)	h_{FE}	1000 100	12,000 –	–
Collector-Emitter Saturation Voltage ($I_C = 4\text{ Adc}$, $I_B = 16\text{ mA}$) ($I_C = 8\text{ Adc}$, $I_B = 80\text{ mA}$)	$V_{CE(sat)}$	– –	2 4	Vdc
Base-Emitter Saturation Voltage (Note 2) ($I_C = 8\text{ Adc}$, $I_B = 80\text{ mA}$)	$V_{BE(sat)}$	–	4.5	Vdc
Base-Emitter On Voltage ($I_C = 4\text{ Adc}$, $V_{CE} = 4\text{ Vdc}$)	$V_{BE(on)}$	–	2.8	Vdc

DYNAMIC CHARACTERISTICS

Current-Gain-Bandwidth Product ($I_C = 3\text{ Adc}$, $V_{CE} = 4\text{ Vdc}$, $f = 1\text{ MHz}$)	$ h_{fe} $	4	–	MHz
Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f = 0.1\text{ MHz}$) MJD127, NJVMJD127 MJD122, NJVMJD122	C_{ob}	– –	300 200	pF
Small-Signal Current Gain ($I_C = 3\text{ Adc}$, $V_{CE} = 4\text{ Vdc}$, $f = 1\text{ kHz}$)	h_{fe}	300	–	–

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

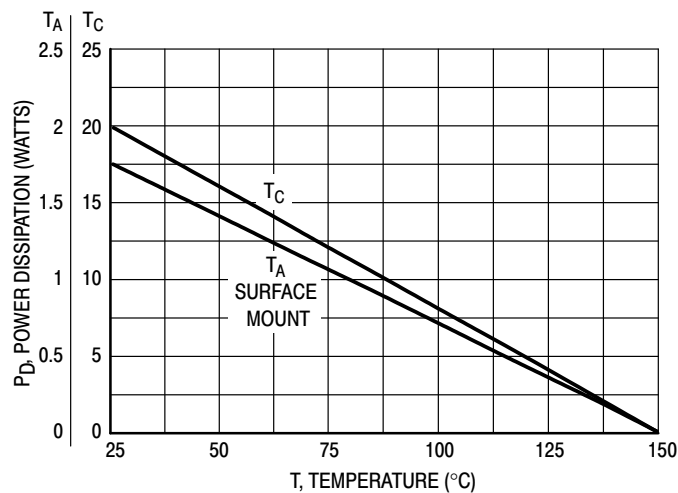


Figure 1. Power Derating

TYPICAL ELECTRICAL CHARACTERISTICS

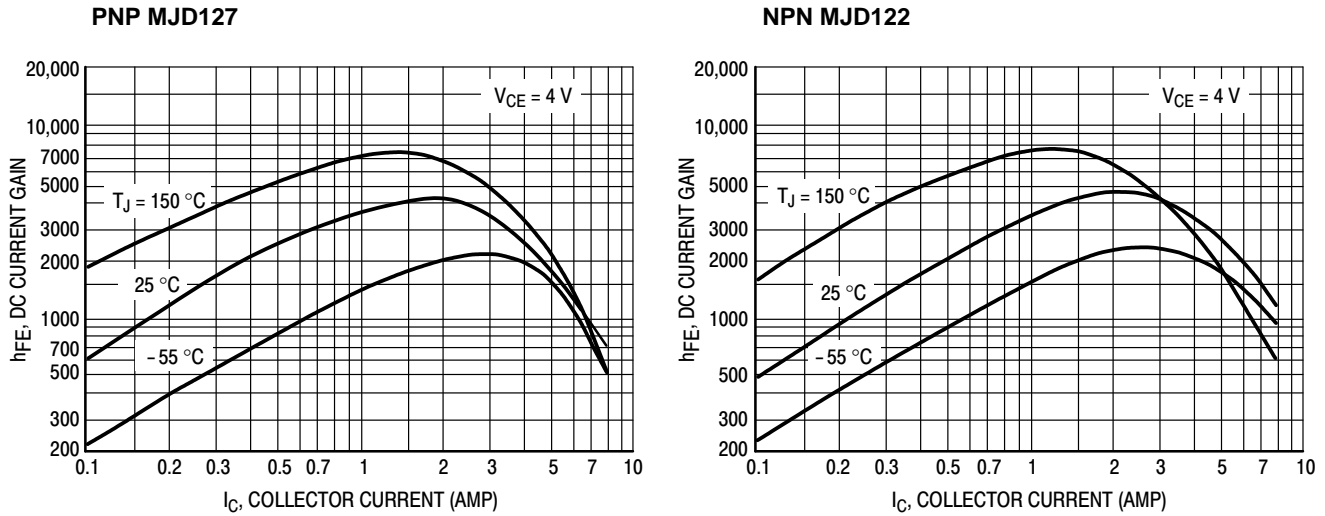


Figure 2. DC Current Gain

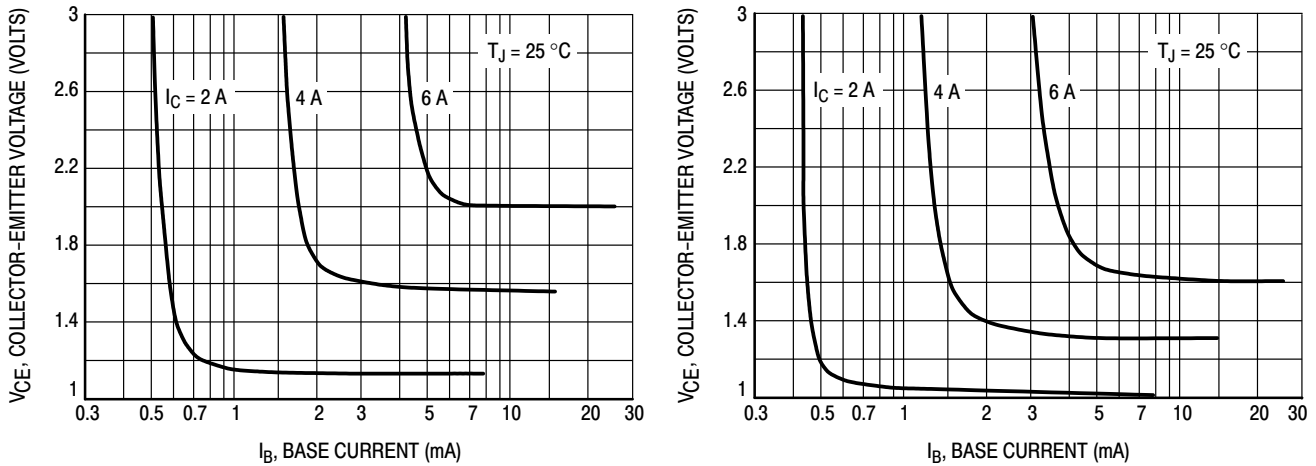


Figure 3. Collector Saturation Region

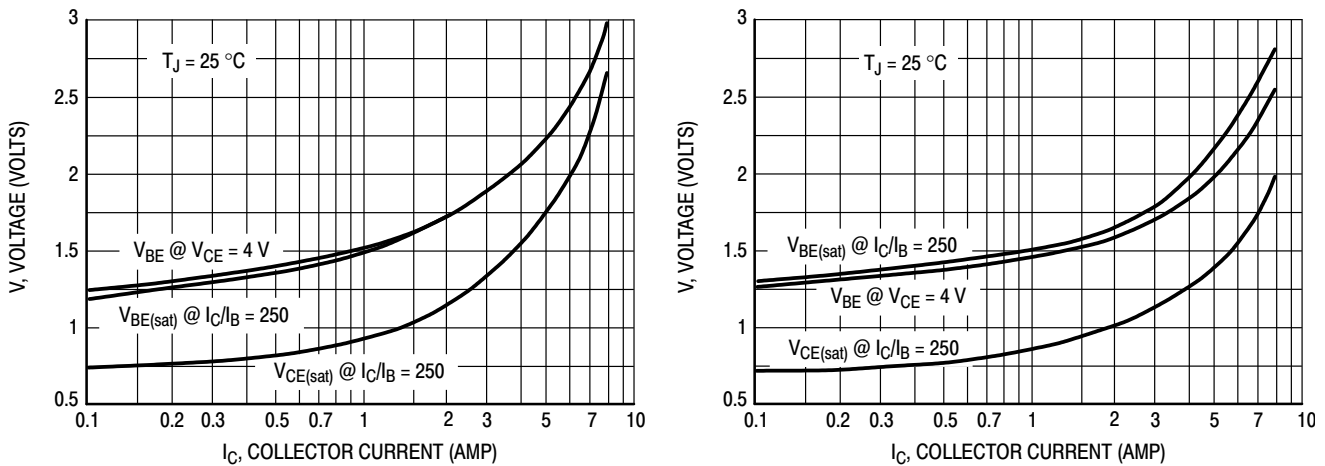


Figure 4. "On" Voltages

TYPICAL ELECTRICAL CHARACTERISTICS

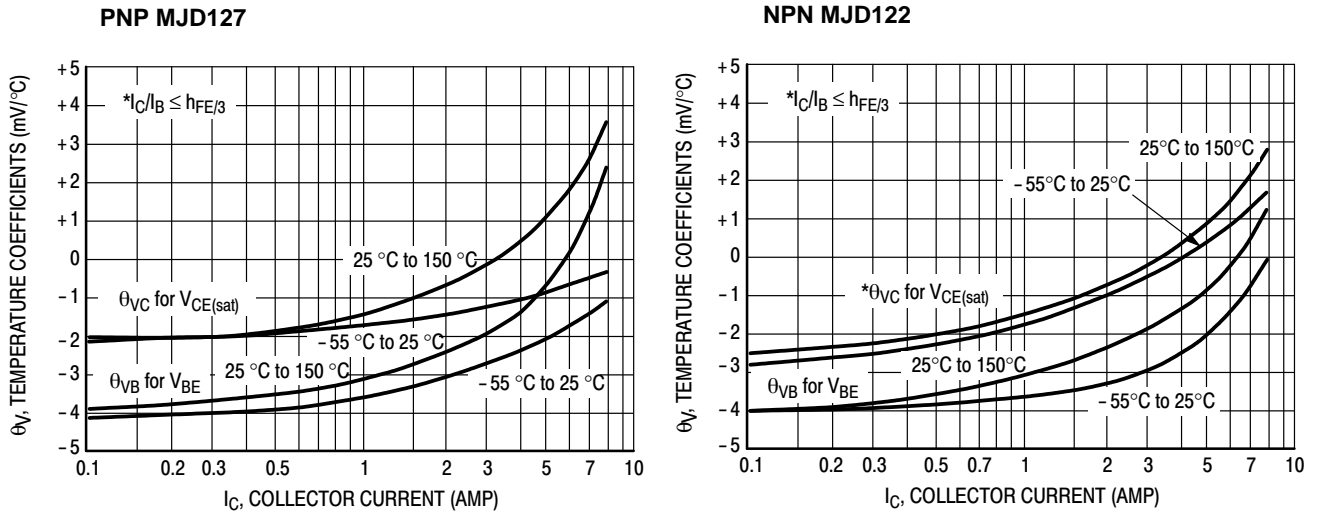


Figure 5. Temperature Coefficients

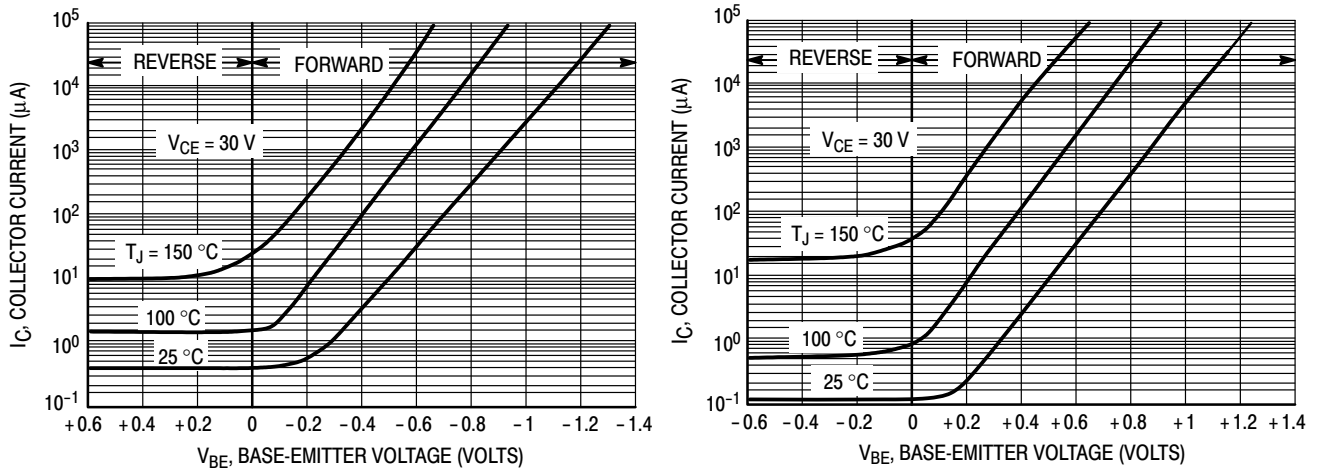


Figure 6. Collector Cut-Off Region

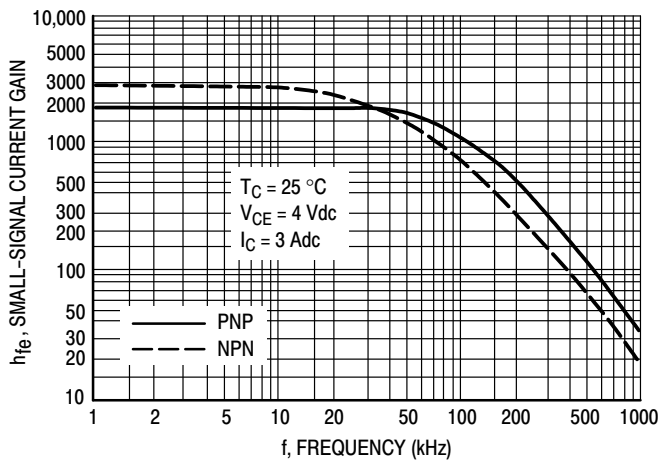


Figure 7. Small-Signal Current Gain

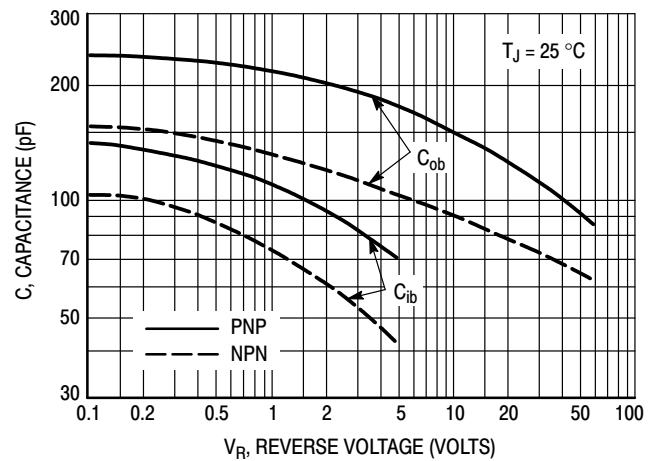


Figure 8. Capacitance

MJD122, NJVMJD122 (NPN), MJD127, NJVMJD127 (PNP)

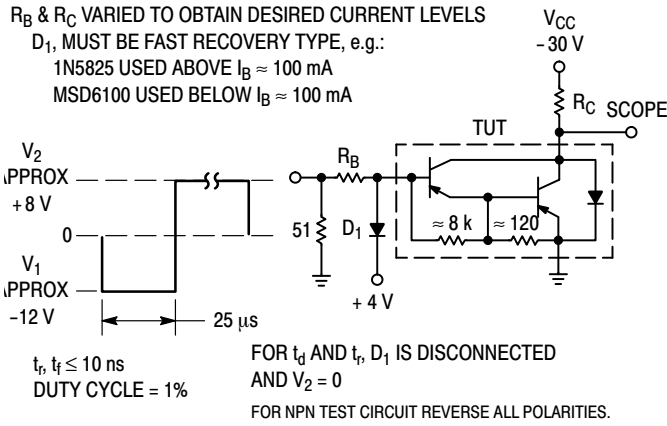


Figure 9. Switching Times Test Circuit

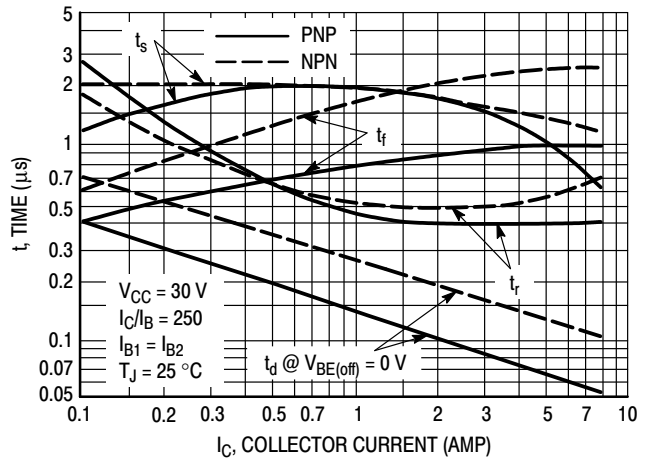


Figure 10. Switching Times

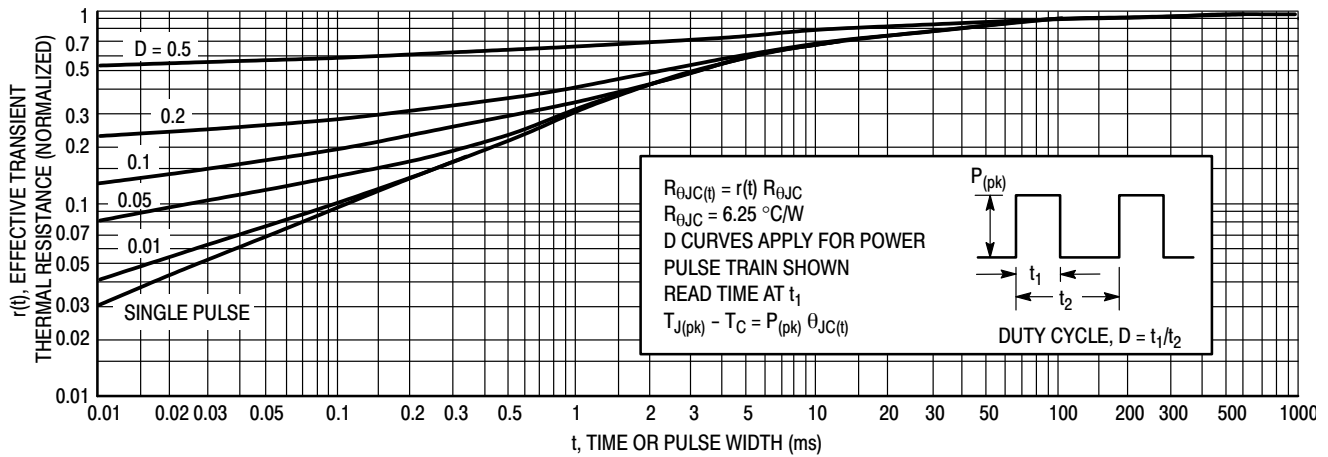


Figure 11. Thermal Response

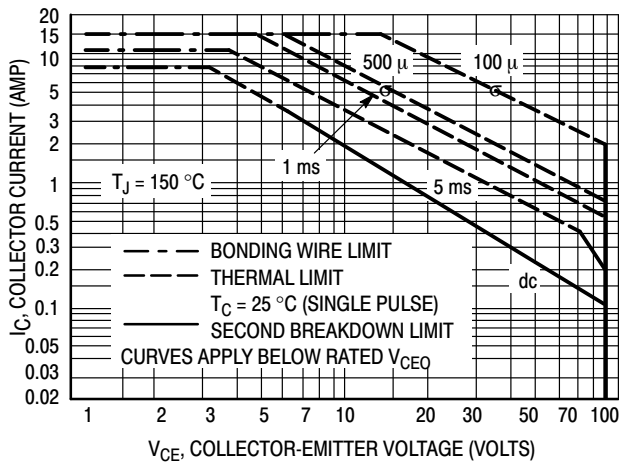


Figure 12. Maximum Forward Bias Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on $T_{J(pk)} = 150$ °C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 150$ °C. $T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

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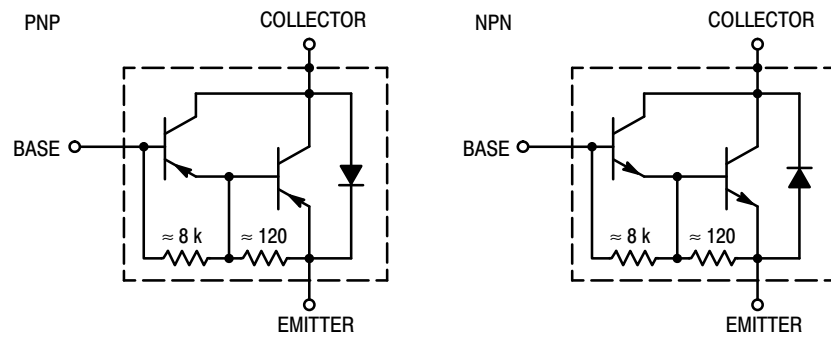


Figure 13. Darlington Schematic

ORDERING INFORMATION

Device	Package Type	Shipping†
MJD122G	DPAK (Pb-Free)	75 Units / Rail
MJD122T4G	DPAK (Pb-Free)	2,500 / Tape & Reel
NJVMJD122T4G*	DPAK (Pb-Free)	2,500 / Tape & Reel
MJD127G	DPAK (Pb-Free)	75 Units / Rail
MJD127T4G	DPAK (Pb-Free)	2,500 / Tape & Reel
NJVMJD127T4G*	DPAK (Pb-Free)	2,500 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

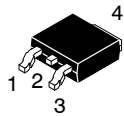
* NJV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable

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REVISION HISTORY

Revision	Description of Changes	Date
16	Rebranded the document to onsemi format.	4/1/2026

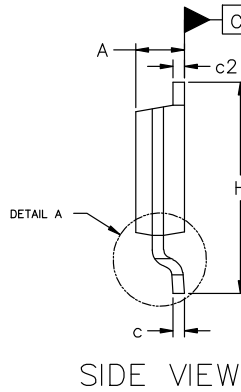
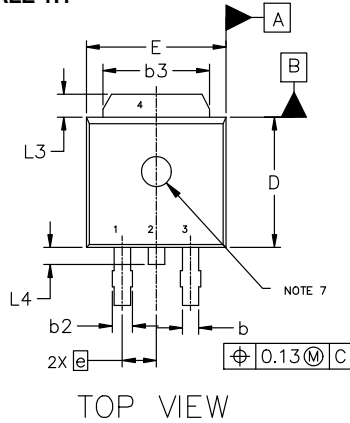
This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.



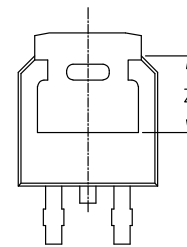
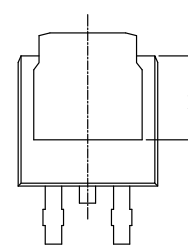
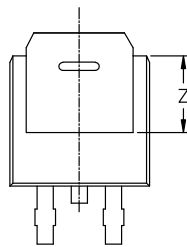
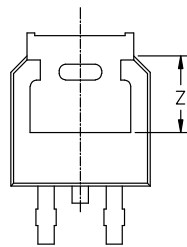
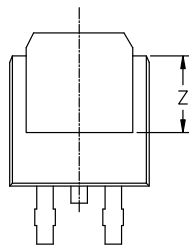
DPAK3 6.10x6.54x2.28, 2.29P
CASE 369C
ISSUE J

DATE 12 AUG 2025

SCALE 1:1



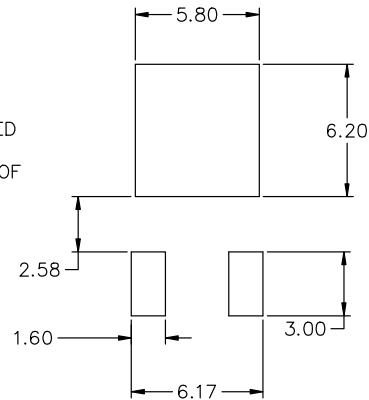
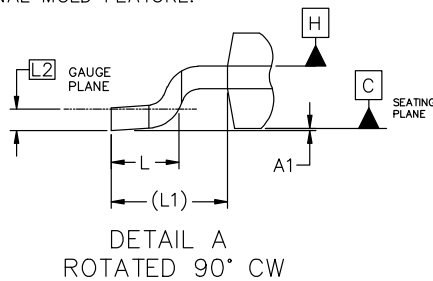
MILLIMETERS			
DIM	MIN	NOM	MAX
A	2.18	2.28	2.38
A1	0.00	---	0.13
b	0.63	0.76	0.89
b2	0.72	0.93	1.14
b3	4.57	5.02	5.46
c	0.46	0.54	0.61
c2	0.46	0.54	0.61
D	5.97	6.10	6.22
E	6.35	6.54	6.73
e	2.29 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90 REF		
L2	0.51 BSC		
L3	0.89	---	1.27
L4	---	---	1.01
Z	3.93	---	---



ALTERNATE CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15mm PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.



RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

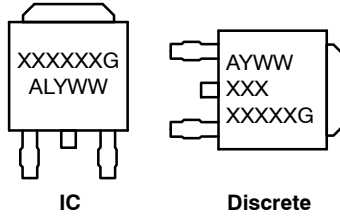
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DESCRIPTION:	DPAK3 6.10x6.54x2.28, 2.29P	PAGE 1 OF 2

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DPAK3 6.10x6.54x2.28, 2.29P
CASE 369C
ISSUE J

DATE 12 AUG 2025

**GENERIC
MARKING DIAGRAM***



- XXXXXX = Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

- | | | | | |
|--|--|---|---|--|
| <p>STYLE 1:
 PIN 1. BASE
 2. COLLECTOR
 3. EMITTER
 4. COLLECTOR</p> | <p>STYLE 2:
 PIN 1. GATE
 2. DRAIN
 3. SOURCE
 4. DRAIN</p> | <p>STYLE 3:
 PIN 1. ANODE
 2. CATHODE
 3. ANODE
 4. CATHODE</p> | <p>STYLE 4:
 PIN 1. CATHODE
 2. ANODE
 3. GATE
 4. ANODE</p> | <p>STYLE 5:
 PIN 1. GATE
 2. ANODE
 3. CATHODE
 4. ANODE</p> |
| <p>STYLE 6:
 PIN 1. MT1
 2. MT2
 3. GATE
 4. MT2</p> | <p>STYLE 7:
 PIN 1. GATE
 2. COLLECTOR
 3. EMITTER
 4. COLLECTOR</p> | <p>STYLE 8:
 PIN 1. N/C
 2. CATHODE
 3. ANODE
 4. CATHODE</p> | <p>STYLE 9:
 PIN 1. ANODE
 2. CATHODE
 3. RESISTOR ADJUST
 4. CATHODE</p> | <p>STYLE 10:
 PIN 1. CATHODE
 2. ANODE
 3. CATHODE
 4. ANODE</p> |

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