



# Product Specification

G101EAN01.0

AU OPTRONICS CORPORATION

( V ) Preliminary Specifications

( ) Final Specifications

|                   |  |
|-------------------|--|
| <b>Module</b>     | <b>10.1"(10.01") WXGA 16:10 Color TFT-LCD</b>              |
| <b>Model Name</b> | <b>G101EAN01.0</b>   |
| <b>Note</b>       | <b><i>LED Backlight without driving circuit design</i></b> |

| Customer   | Date  |
|--|-------|
| _____  | _____ |
| <b>Checked &amp; Approved by</b>                                     |       |
| _____  | _____ |
| <p>Note: This Specification is subject to change without notice.</p> |       |

| Approved by   | Date       |
|---|------------|
| Grace Hung  | 2019/01/04 |
| <b>Prepared by</b>  |            |
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## Record of Revision

| Version and Date  | Page | Old description           | New Description                             |
|-------------------|------|---------------------------|---|
| 0.0 Oct. 09, 2018 | All  | First draft specification | -   |
| 0.1 Jan. 04, 2019 | 25   |                           | Modify Shipping Label location in rear view |
|                   |      |                           |   |
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## 1. Operating Precautions

- 1) Since front polarizer is easily damaged, please be cautious and not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or soft cloth.
- 5) Since the panel is made of glass, it may be broken or cracked if dropped or bumped on hard surface.
- 6) To avoid ESD (Electro Static Discharge) damage, be sure to ground yourself before handling TFT-LCD Module.
- 7) Do not open nor modify the module assembly.
- 8) Do not press the reflector sheet at the back of the module to any direction.
- 9) In case if a module has to be put back into the packing container slot after it was taken out from the container, do not press the center of the LED light bar edge. Instead, press at the far ends of the LED light bar edge softly. Otherwise the TFT Module may be damaged.
- 10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 11) TFT-LCD Module is not allowed to be twisted & bent even force is added on module in a very short time. Please design your display product well to avoid external force applying to module by end-user directly.
- 12) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (IEC60950 or UL1950), or be applied exemption.
- 13) Severe temperature condition may result in different luminance, response time and lamp ignition voltage.
- 14) Continuous operating TFT-LCD display under low temperature environment may accelerate lamp exhaustion and reduce luminance dramatically.
- 15) Continuous displaying fixed pattern may induce image sticking. It's recommended to use screen saver or shuffle content periodically if fixed pattern is displayed on the screen.
- 16) Disconnecting power supply before handling LCD modules, it can prevent electric shock, DO NOT TOUCH the electrode parts, cables, connectors and LED circuit part of TFT module that a LED light bar build in as a light source of back light unit. It can prevent electrostatic breakdown.

## 2. General Description

G101EAN01.0 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and LED backlight system. The screen format is intended to support the 16:10 WXGA, 800(H) x1280(V) screen and 16.7M colors (Real 8 bits) without LED backlight driving circuit. All input signals are MIPI interface compatible.

G101EAN01.0 is designed for a display unit of notebook style personal computer and industrial machine.

G101EAN01.0 is a RoHS product.

## 2.1 Display Characteristics

The following items are characteristics summary on the table under 25 °C condition:

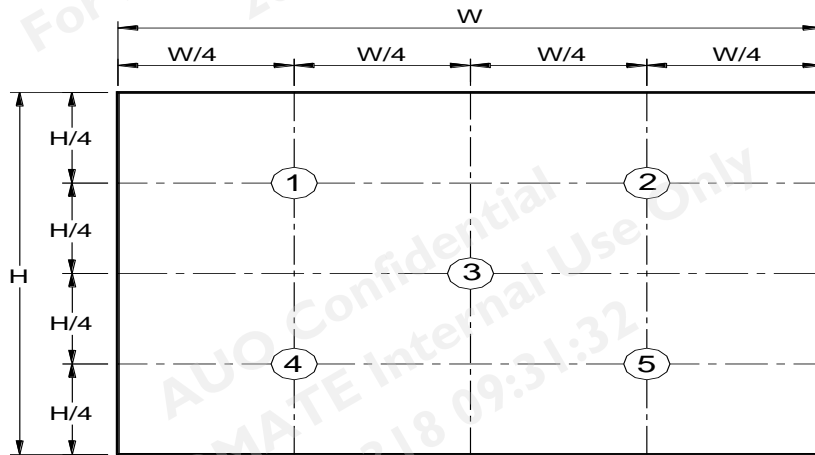
| Items   | Unit                            | Specifications   |     |        |                                      |
|---|---------------------------------|--|-----|--------|--------------------------------------|
| Screen Diagonal   | [mm]                            | 255.397  |     |        |                                      |
| Active Area   | [mm]                            | 135.36(H) x 216.576(V)   |     |        |                                      |
| Pixels H x V  |                                 | 800 x 3(RBG) x 1280  |     |        |                                      |
| Pixel Pitch   | [mm]                            | 0.1692 X 0.1692  |     |        |                                      |
| Pixel Format  |                                 | R.G.B. Vertical Stripe   |     |        |                                      |
| Display Mode  |                                 | AHVA, Normally Black   |     |        |                                      |
| White Luminance   | [cd/m <sup>2</sup> ]            | 350 typ. (center point)  |     |        |                                      |
| Luminance Uniformity                                      | $\delta_{5P}$<br>$\delta_{13P}$ | 5P Max. 1.25<br>13P Max. 1.33  |     |        |                                      |
| Contrast Ratio  |                                 | Typ. 1000:1, min 800:1   |     |        |                                      |
| Response Time   | [ms]                            | Typ.30   |     |        |                                      |
| Nominal Input Voltage VDD                                 | [Volt]                          | VDD=3.3V typ. / IOVCC=1.8V typ.  |     |        |                                      |
| Power Consumption   | [Watt]                          | Logic: 0.4 W @ full white pattern<br>BLU: 1.82 W max (1.76 W typ). , w/o effi. |     |        |                                      |
| Weight  | [Grams]                         | 161 g Max  |     |        |                                      |
| Physical Size   | [mm]                            |  | Min | Typ    | Max                                  |
|   |                                 | Length   |     | 232.43 |                                      |
|   |                                 | Width  |     | 150.3  |                                      |
|   |                                 | Thickness  | --- | ---    | 2.65 (Panel side)<br>4.8 (PCBA side) |
| Electrical Interface                                      |                                 | MIPI   |     |        |                                      |
| Surface Treatment   |                                 | Anti Glare   |     |        |                                      |
| Support Color   |                                 | 16.7M colors ( Real 8 bits )   |     |        |                                      |
| Temperature Range<br>Operating<br>Storage (Non-Operating) | [°C]<br>[°C]                    | 0 to +50<br>-20 to +60   |     |        |                                      |
| RoHS Compliance   |                                 | RoHS Compliance  |     |        |                                      |

## 2.2 Optical Characteristics

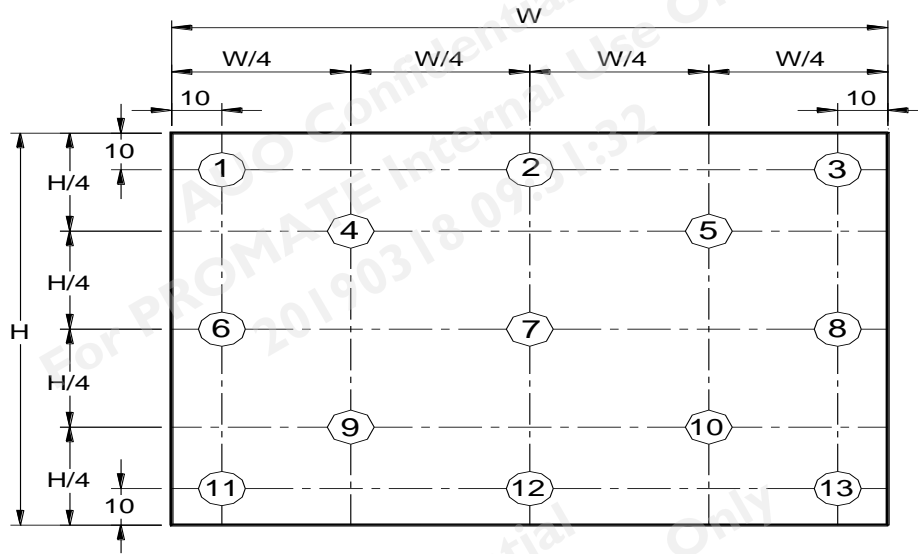
The optical characteristics are measured under stable conditions at 25 °C (Room Temperature):

| Item                             | Symbol               | Conditions                                | Min.     | Typ.     | Max.  | Unit              | Note     |
|----------------------------------|----------------------|---|----------|----------|-------|-------------------|----------|
| White Luminance                  |                      | 5 points average                          | 300      | 350      | ---   | cd/m <sup>2</sup> | 1, 4, 5. |
| Viewing Angle                    | $\theta_R$           | Horizontal (Right)<br>CR $\geq$ 10 (Left) | 80       | 85       | ---   | degree            | 4, 9     |
|                                  | $\theta_L$           |   | 80       | 85       | ---   |                   |          |
|                                  | $\psi_H$<br>$\psi_L$ | Vertical (Upper)<br>CR $\geq$ 10 (Lower)  | 80<br>80 | 85<br>85 | ---   |                   |          |
| Luminance Uniformity             | $\delta_{5P}$        | 5 Points                                  | ---      | ---      | 1.25  |                   | 1, 3, 4  |
| Luminance Uniformity             | $\delta_{13P}$       | 13 Points                                 | ---      | ---      | 1.33  |                   | 2, 3, 4  |
| Contrast Ratio                   | CR                   |   | 800      | 1000     | ---   |                   | 4, 6     |
| Cross talk                       | %                    |   | ---      | ---      | TBD   |                   | 4, 7     |
| Response Time                    | $T_{RT}$             | Rising + Falling                          | ---      | 30       | 35    | msec              | 4, 8     |
| Color / Chromaticity Coordinates | Red                  | Rx  | 0.578    | 0.608    | 0.638 | CIE 1931          | 4        |
|                                  |                      | Ry  | 0.325    | 0.355    | 0.385 |                   |          |
|                                  | Green                | Gx  | 0.309    | 0.339    | 0.369 |                   |          |
|                                  |                      | Gy  | 0.568    | 0.598    | 0.628 |                   |          |
|                                  | Blue                 | Bx  | 0.125    | 0.155    | 0.185 |                   |          |
|                                  |                      | By  | 0.057    | 0.087    | 0.117 |                   |          |
|                                  | White                | Wx  | 0.270    | 0.300    | 0.330 |                   |          |
|                                  |                      | Wy  | 0.290    | 0.320    | 0.350 |                   |          |
|                                  | NTSC                 | %   |          | 55       | 60    |                   |          |

**Note 1:** 5 points position (Ref: Active area)



**Note 2:** 13 points position (Ref: Active area)



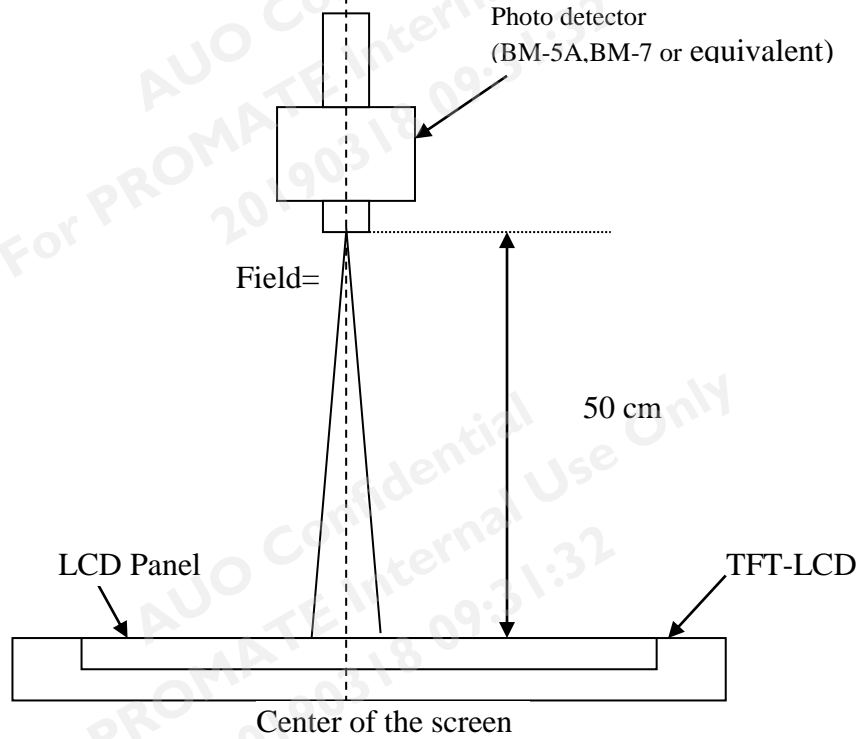
**Note 3:** The luminance uniformity of 5 or 13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{w5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{w13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

**Note 4:** Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room, and it should be measured in the center of screen.



**Note 5 :** Definition of Average Luminance of White ( $Y_L$ ):

Measure the luminance of gray level 63 at 5 points ·  $Y_L = [L (1)+ L (2)+ L (3)+ L (4)+ L (5)] / 5$   
 $L (x)$  is corresponding to the luminance of the point X at Figure in Note (1).

**Note 6 :** Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "White" state}}{\text{Brightness on the "Black" state}}$$

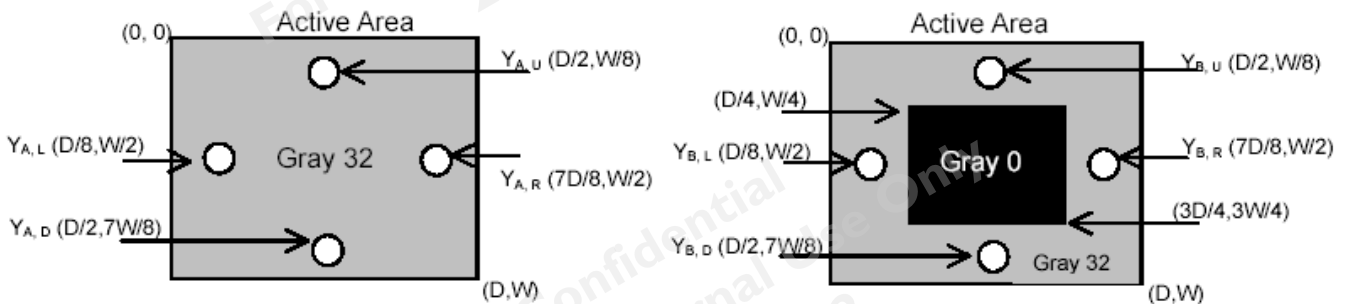
**Note 7 :** Definition of Cross Talk (CT)

$$CT = | Y_B - Y_A | / Y_A \times 100 (\%)$$

Where

$Y_A$  = Luminance of measured location without gray level 0 pattern (cd/m<sup>2</sup>)

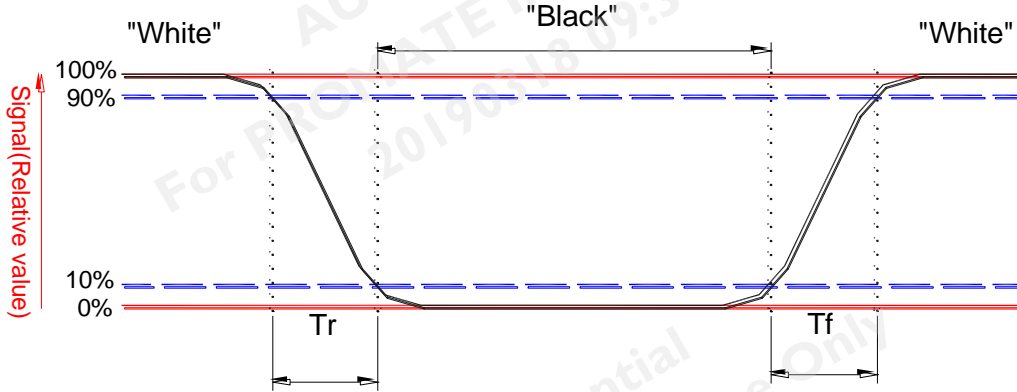
$Y_B$  = Luminance of measured location with gray level 0 pattern (cd/m<sup>2</sup>)





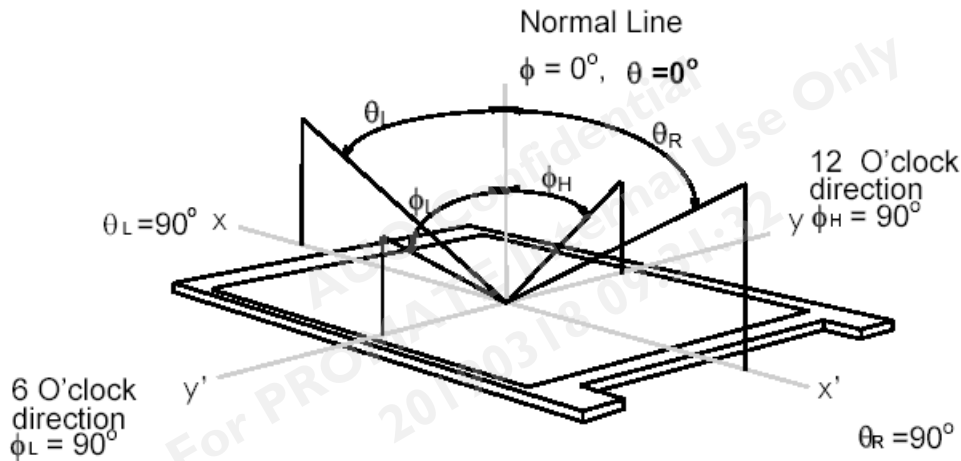
**Note 8:** Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from "Black" to "White" (falling time) and from "White" to "Black" (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.



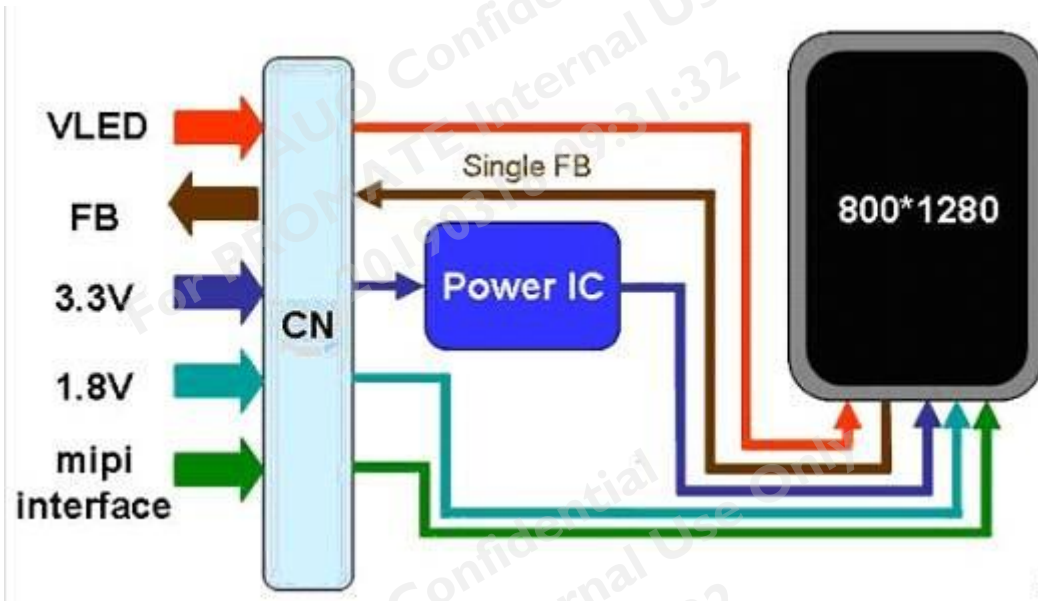
**Note 9.** Definition of viewing angle

Viewing angle is the measurement of contrast ratio  $\geq 10$ , at the screen center, over a  $180^\circ$  horizontal and  $180^\circ$  vertical range (off-normal viewing angles). The  $180^\circ$  viewing angle range is broken down as follows;  $90^\circ$  ( $\theta$ ) horizontal left and right and  $90^\circ$  ( $\Phi$ ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



## 3. Functional Block Diagram

The following diagram shows the functional block of the 10.1 inches wide Color TFT/LCD 39 Pin one channel Module



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## 4. Absolute Maximum Ratings

An absolute maximum rating of the module is as following:

### 4.1 Absolute Ratings of TFT LCD Module

| Item                    | Symbol | Min  | Max  | Unit   | Conditions |
|-------------------------|--------|------|------|--------|------------|
| Logic/LCD Drive Voltage | Vin    | -0.3 | +4.0 | [Volt] | Note 1,2   |

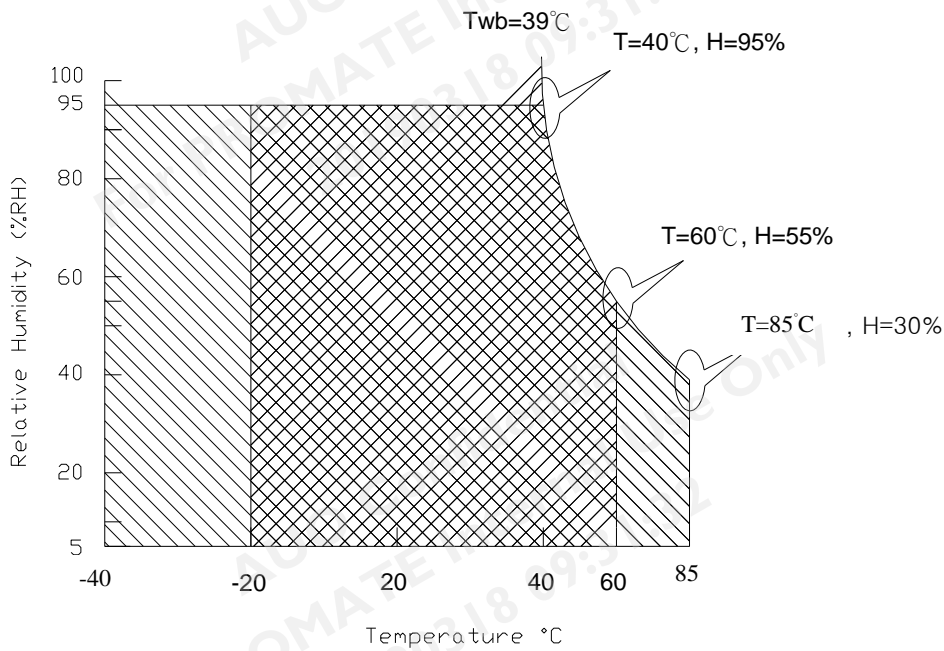
### 4.2 Absolute Ratings of Environment

| Item                  | Symbol | Min | Max | Unit  | Conditions |
|-----------------------|--------|-----|-----|-------|------------|
| Operating Temperature | TOP    | 0   | +50 | [°C]  | Note 3     |
| Operation Humidity    | HOP    | 5   | 95  | [%RH] | Note 3     |
| Storage Temperature   | TST    | -20 | +60 | [°C]  | Note 3     |
| Storage Humidity      | HST    | 5   | 95  | [%RH] | Note 3     |

Note 1: At Ta (25°C )

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range Storage Range +

## 5. Electrical Characteristics

### 5.1 TFT LCD Module

#### 5.1.1 Power Specification

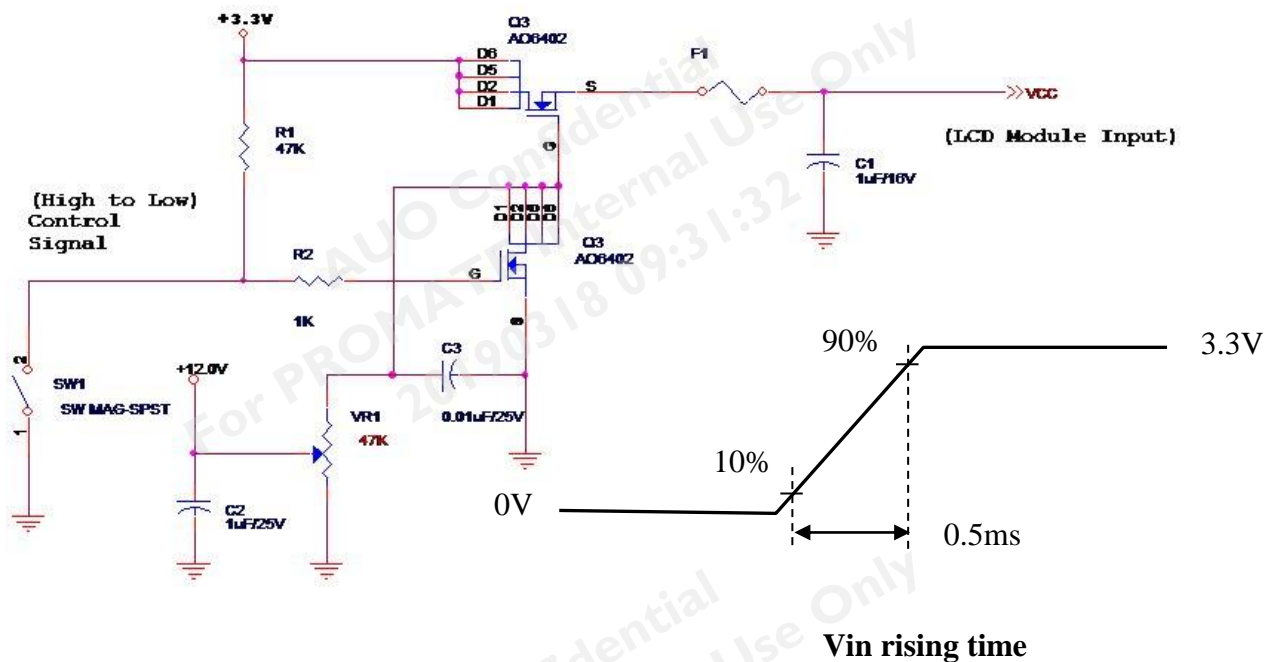
Input power specifications are as follows. The power specification are measured under 25°C and frame frequency under 60Hz

| Symble             | Parameter               | Min | Typ | Max   | Units  | Note |
|--------------------|-------------------------|-----|-----|-------|--------|------|
| IOVCC              | Logic/LCD Drive Voltage | 1.7 | 1.8 | 1.9   | [Volt] |      |
| P <sub>IOVCC</sub> | IOVCC Power             | -   | -   | 0.054 | [Watt] |      |
| I <sub>IOVCC</sub> | IOVCC Current(RMS)      | -   | 30  | -     | [mA]   |      |

| Symble            | Parameter                                | Min | Typ | Max  | Units       | Note   |
|-------------------|--|-----|-----|------|-------------|--------|
| VDD               | Logic/LCD Drive Voltage                  | 3.0 | 3.3 | 3.6  | [Volt]      |        |
| P <sub>VDD</sub>  | VDD Power                                | -   | -   | 0.4  | [Watt]      | Note 1 |
| I <sub>VDD</sub>  | VDD Current(RMS)                         | -   | 121 | -    | [mA]        |        |
| IRush             | Inrush Current                           | -   | -   | 1500 | [mA]        | Note 2 |
| VDD <sub>rp</sub> | Allowable Logic/LCD Drive Ripple Voltage | -   | -   | 100  | [mV]<br>p-p |        |

Note 1 : Maximum Measurement Condition : White Pattern at 3.3V driving voltage.

Note 2 : Measure Condition

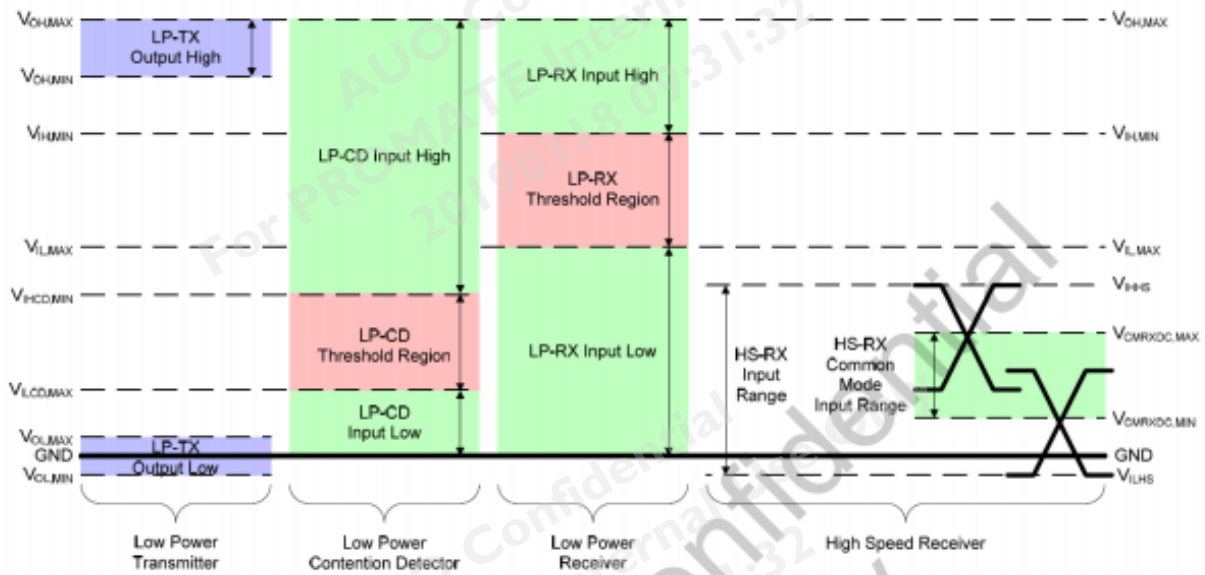


## 5.1.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

MIPI DC characteristics are as follows:

| Parameter                                      | Symbol    | Conditions | Specification |     |         | Unit |
|--|-----------|------------|---------------|-----|---------|------|
|  |           |            | MIN           | TYP | MAX     |      |
| <b>Power supply voltage for MIPI Interface</b> |           |            |               |     |         |      |
| Power supply voltage for MIPI interface        | VDDAM     | -          | 1.75          | 2.8 | 6.0     | V    |
|  | LVDSVDD   | -          | 1.15          | 1.2 | 1.375   | V    |
| <b>LPDT Input Characteristics</b>              |           |            |               |     |         |      |
| Pad signal voltage range                       | VI        | -          | -50           | -   | 1350    | mV   |
| Ground Shift                                   | VGND SH   | -          | -50           | -   | 50      | mV   |
| Logic 0 input threshold                        | VIL       | -          | 0             | -   | 550     | mV   |
| Logic 1 input threshold                        | VIH       | -          | 880           | -   | LVDSVDD | mV   |
| Input hysteresis                               | VHYST     | -          | 25            | -   | -       | mV   |
| <b>LPDT Output Characteristics</b>             |           |            |               |     |         |      |
| Output low level                               | VOL       | -          | -50           | -   | 50      | mV   |
| Output high level                              | VOH       | -          | 1.1           | 1.2 | 1.3     | V    |
| Logic 1 contention threshold                   | VIHCD,MIN | -          | 450           | -   | LVDSVDD | mV   |
| Logic 0 contention threshold                   | VILCD,MAX | -          | 0             | -   | 200     | mV   |
| Output impedance of LPDT                       | ZOLP      | -          | 80            | 100 | 125     | ohm  |
| <b>Hi-speed Input/Output Characteristics</b>   |           |            |               |     |         |      |
| Single-end input low voltage                   | VILHS     | -          | -40           | -   | -       | mV   |
| Single-end input high voltage                  | VIHHS     | -          | -             | -   | 460     | mV   |
| Common mode voltage                            | VCMRXDC   | -          | 70            | -   | 330     | mV   |
| Hi-speed transmit voltage                      | VOD       | -          | 140           | 200 | 250     | mV   |
| Differential input impedance                   | ZID       | -          | 80            | 100 | 125     | ohm  |



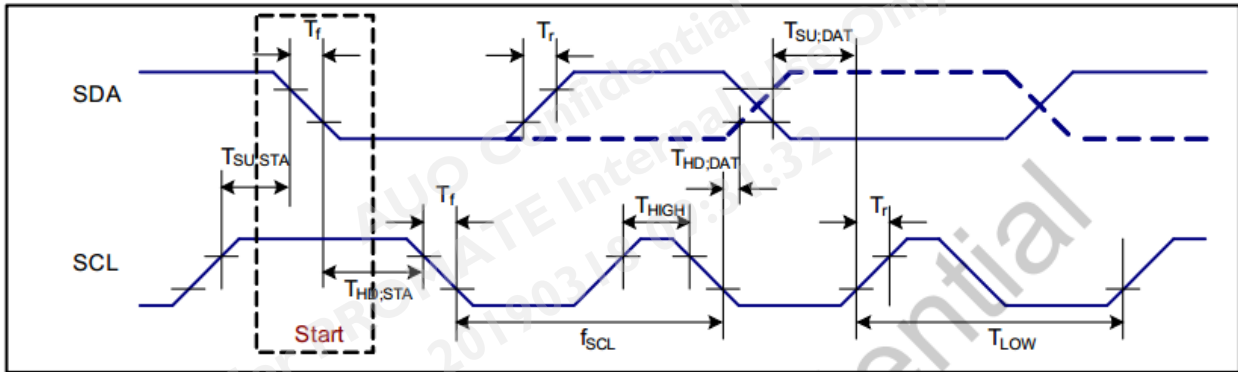


Table: I2C Interface Characteristics

| Symbol        | Parameter  | Conditions | Min.        | Typ. | Max. | Unit |
|---------------|--|------------|-------------|------|------|------|
| $f_{SCLK}$    | SCL clock frequency                              | -          | DC          | -    | 400  | KHz  |
| $T_{LOW}$     | SCL clock LOW period                             | -          | 1.3         | -    | -    | #s   |
| $T_{HIGH}$    | SCL clock HIGH period                            | -          | 0.6         | -    | -    | #s   |
| $T_{SU,DATA}$ | data set-up time                                 | -          | 100         | -    | -    | ns   |
| $T_{HD,DATA}$ | data hold time                                   | -          | 0           | -    | 0.9  | #s   |
| $T_r$         | SCL and SDA rise time                            | Note 2     | $20+0.1C_b$ | -    | 300  | ns   |
| $T_f$         | SCL and SDA fall time                            | Note 2     | $20+0.1C_b$ | -    | 300  | ns   |
| $T_f$         | SDA fall time for read out                       | -          | $20+0.1C_b$ | -    | 1000 | ns   |
| $C_b$         | Capacitive load represented by each bus line     | -          | -           | -    | 400  | pF   |
| $T_{SU,STA}$  | Setup time for a repeated START condition        | -          | 0.6         | -    | -    | #s   |
| $T_{HD,STA}$  | START condition hold time                        | -          | 0.6         | -    | -    | #s   |
| $T_{SU,STO}$  | Setup time for STOP condition                    | -          | 0.6         | -    | -    | #s   |
| $T_{SW}$      | Tolerable spike width on bus                     | Note 1     | -           | -    | 50   | ns   |
| $T_{BUF}$     | BUS free time between a STOP and START condition | -          | 1.3         | -    | -    | #s   |

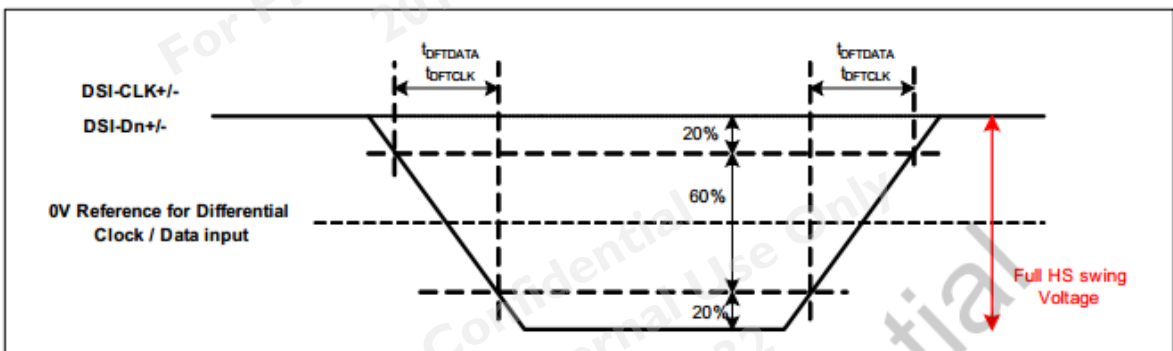
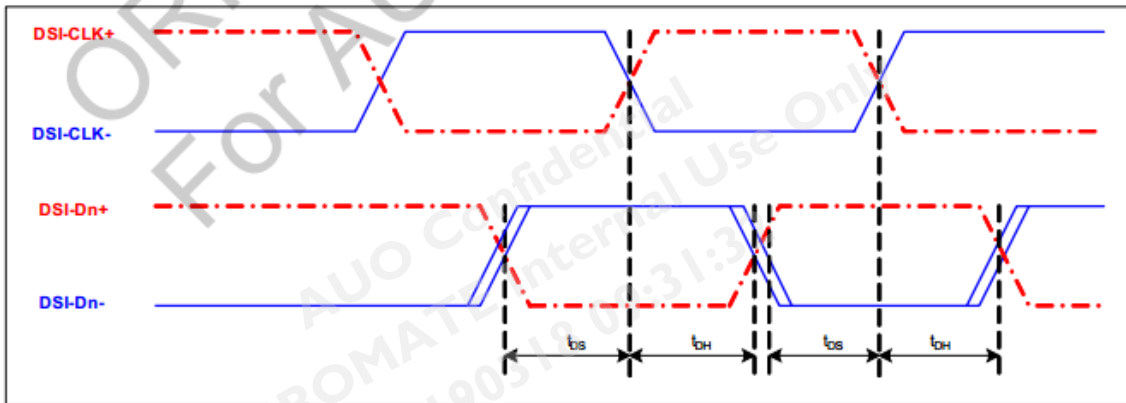
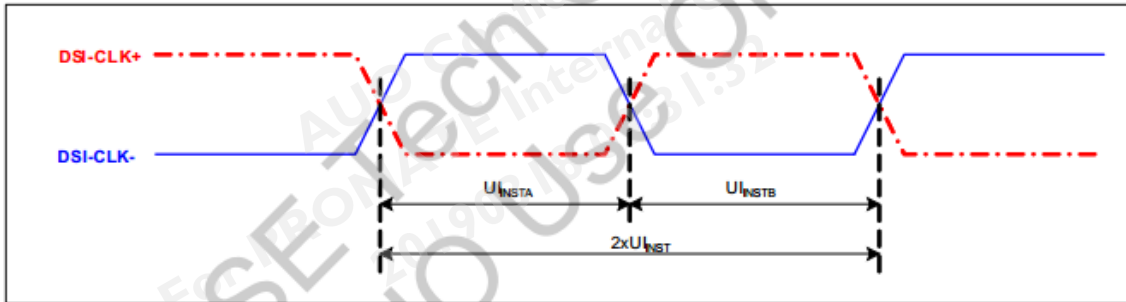
**Note1:** The device inputs SDA and SCL are filtered and will reject spikes on the bus lines of width  $<t_{SW(max)}$ .

**Note2:** The rise and fall times specified here refer to the driver device and are part of the general fast I<sup>2</sup>C-bus specification.  $C_b$  = capacitive load per bus line.

**Note3:** All timing values are valid within the operating supply voltage and ambient temperature ranges and are referenced to  $V_{L}$  and  $V_{IH}$  with an input voltage swing of  $V_{SS}$  to  $V_{DD1}$

## MIPI High-Speed Data-clock Timing

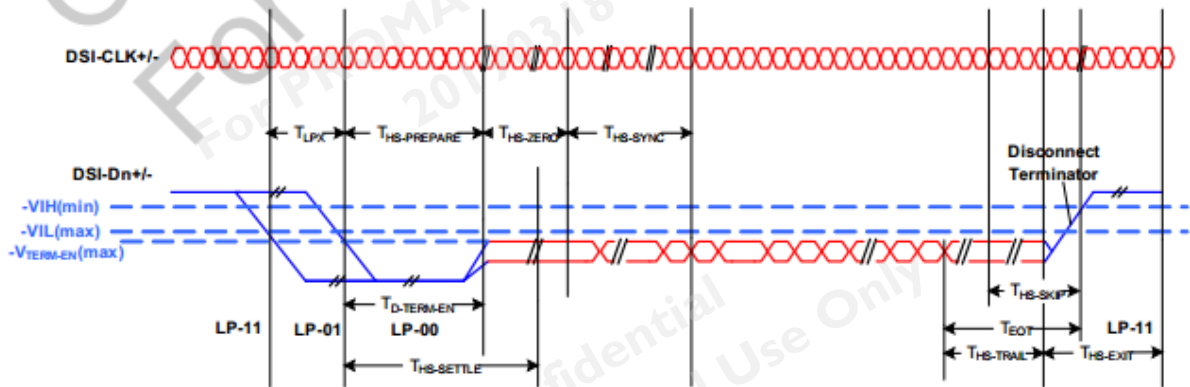
| Parameter              | Symbol                 | Parameter                        | Specification |     |       | Unit |
|------------------------|------------------------|----------------------------------|---------------|-----|-------|------|
|                        |                        |                                  | MIN           | TYP | MAX   |      |
| <b>High Speed Mode</b> |                        |                                  |               |     |       |      |
| DSI-CLK+/-             | $2xU_{INST}$           | Double UI instantaneous          | 2.22          | -   | 25    | ns   |
| DSI-CLK+/-             | $U_{INSTA}, U_{INSTB}$ | UI instantaneous Halfs           | 1.11          | -   | 12.5  | ns   |
| DSI-Dn+/-              | $t_{DS}$               | Data to clock setup time         | 0.15          | -   | -     | UI   |
| DSI-Dn+/-              | $t_{DH}$               | Data to clock hold time          | 0.15          | -   | -     | UI   |
| DSI-CLK+/-             | $t_{DRTCLK}$           | Differential rise time for clock | 150           | -   | 0.3UI | ps   |
| DSI-Dn+/-              | $t_{DRTDATA}$          | Differential rise time for data  | 150           | -   | 0.3UI | ps   |
| DSI-CLK+/-             | $t_{DFTCLK}$           | Differential fall time for clock | 150           | -   | 0.3UI | ps   |
| DSI-Dn+/-              | $t_{DFTDATA}$          | Differential fall time for data  | 150           | -   | 0.3UI | ps   |



The timing definitions are listed in below:

| Parameter                                  | Symbol                         | Parameter   | Specification                      |     |                | Unit |
|--|--------------------------------|---|------------------------------------|-----|----------------|------|
|  |                                |   | MIN                                | TYP | MAX            |      |
| <b>High Speed Data Transmission Bursts</b> |                                |   |                                    |     |                |      |
| DSI-Dn+/-                                  | $T_{LPX}$                      | Length of any low-power state period  | 50                                 | -   | -              | ns   |
| DSI-Dn+/-                                  | $T_{HS-PREPARE}$               | Time to drive LP-00 to prepare for HS transmission  | $40ns + 4UI$                       | -   | $85ns + 6UI$   | ns   |
| DSI-Dn+/-                                  | $T_{HS-PREPARE} + T_{HS-ZERO}$ | $T_{HS-PREPARE}$ + time to drive HS-0 before the sync sequence                                  | $145ns + 10UI$                     | -   | -              | ns   |
| DSI-Dn+/-                                  | $T_{D-TERM-EN}$                | Time to enable Data Lane receiver line termination measured from when Dn crosses $V_{IL(max)}$  | Time for Dn to reach $V_{TERM-EN}$ | -   | $35ns + 4UI$   | ns   |
| DSI-Dn+/-                                  | $T_{HS-SKIP}$                  | Time-out at RX to ignore transition period of EoT   | 40                                 | -   | $55ns + 4UI$   | ns   |
| DSI-Dn+/-                                  | $T_{HS-TRAIL}$                 | Time to drive flipped differential state after last payload data bit of a HS transmission burst | max (8UI, $60ns + 4UI$ )           | -   | -              | ns   |
| DSI-Dn+/-                                  | $T_{HS-EXIT}$                  | Time to drive LP-11 after HS burst  | 100                                | -   | -              | ns   |
| DSI-Dn+/-                                  | $T_{EoT}$                      | Time from start of $T_{HS-TRAIL}$ period to start of LP-11 state                                | -                                  | -   | $105ns + 12UI$ | ns   |

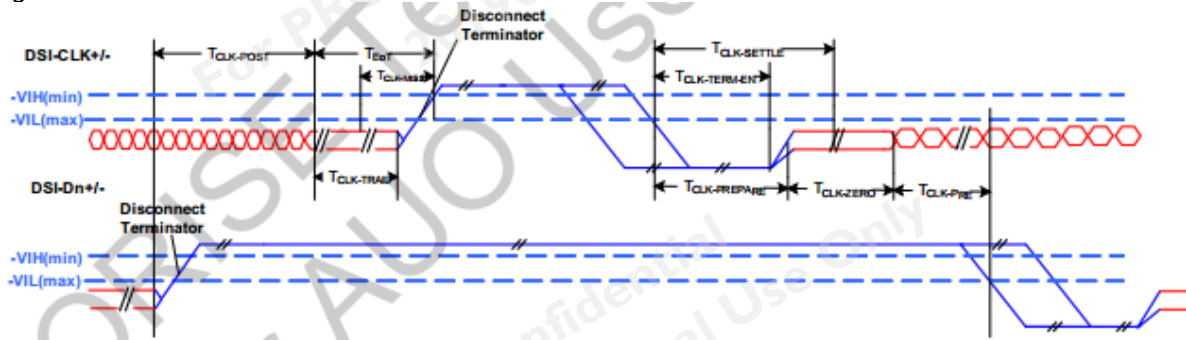
### High-Speed Data Transmission in Bursts





| Parameter  | Symbol                           | Parameter   | Specification                      |     |                | Unit |
|--|----------------------------------|---|------------------------------------|-----|----------------|------|
|  |                                  |   | MIN                                | TYP | MAX            |      |
| Switching the clock Lane between clock Transmission and Low Power Mode |                                  |   |                                    |     |                |      |
| DSI-CLK+/-   | $T_{CLK-POST}$                   | Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode | $60ns + 52UI$                      | -   | -              | ns   |
| DSI-CLK+/-   | $T_{CLK-PRE}$                    | Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode      | 8                                  | -   | -              | UI   |
| DSI-CLK+/-   | $T_{CLK-PREPARE}$                | Time to drive LP-00 to prepare for HS clock transmission  | 38                                 | -   | 95             | ns   |
| DSI-CLK+/-   | $T_{CLK-TERM-EN}$                | Time to enable Clock Lane receiver line termination measured from when Dn crosses $V_{IL(max)}$                           | Time for Dn to reach $V_{TERM-EN}$ | -   | 38             | ns   |
| DSI-CLK+/-   | $T_{CLK-PREPARE} + T_{CLK-ZERO}$ | $T_{CLK-PREPARE}$ + time for lead HS-0 drive period before starting Clock   | 300                                | -   | -              | ns   |
| DSI-CLK+/-   | $T_{CLK-TRAIL}$                  | Time to drive HS differential state after last payload clock bit of a HS transmission burst                               | 60                                 | -   | -              | ns   |
| DSI-CLK+/-   | $T_{EoT}$                        | Time from start of $T_{CLK-TRAIL}$ period to start of LP-11 state   | -                                  | -   | $105ns + 12UI$ | ns   |

Switching the Clock Lane between Clock Transmission and Low-Power Mode





## 5.2 Backlight Unit

### 5.2.1 LED characteristic

Following characteristics are measured under a stable condition using an inverter at 25°C (Room Temperature):

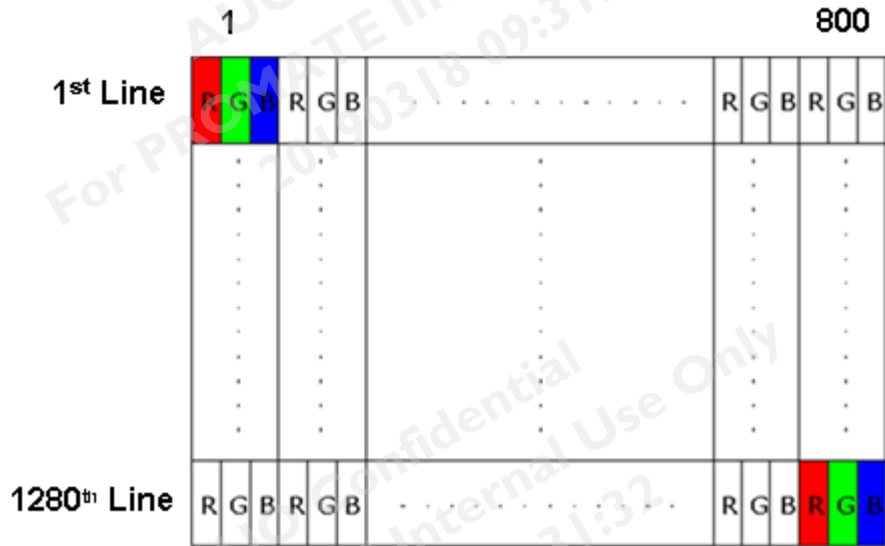
| Parameter                                    | Symbol    | Min     | Typ   | Max  | Units  | Condition            |
|--|-----------|---------|-------|------|--------|----------------------|
| Backlight Power Consumption (W/O Efficiency) | PLED      |         |       | 1.82 | [Watt] | Note 1<br>(Ta= 25°C) |
| LED Forward Voltage                          | VF        | 2.8     | 2.95  | 3.2  | [Volt] | (Ta= 25°C)           |
| LED Forward Voltage of every LED string      | Vf-string | 19.6    | 20.65 | 22.4 | [Volt] |                      |
| LED Forward Current                          | IF        |         | 21    |      | [mA]   | (Ta= 25°C)           |
| LED Life time                                | N/A       | ≥ 15000 |       |      | Hour   | Note 1<br>(Ta=25°C)  |

Note 1: calculator value for reference PLED based on 20 mA

## 6. Signal Characteristic

### 6.1 Pixel Format Image

Following figure shows the relationship between input signal and LCD pixel format.



## 6.2 Integration Interface Requirement

### 6.2.1 MIPI/TP Connector Description

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

| Connector Name / Designation | For Signal Connector |
|------------------------------|----------------------|
| Manufacturer                 | Hirose               |
| Type / Part Number           | FH26W-39S-0.3SHW     |
| Mating Housing/Part Number   | FPC or Compatible    |



## 6.2.2 MIPI Pin Assignment

MIPI is a differential signal technology for LCD interface and high speed data transfer device.

| Pin No. | Symbol     | Description               | I/O |
|---------|------------|---------------------------|-----|
| 1       | NC         | NC                        | -   |
| 2       | NC         | NC                        | -   |
| 3       | NC         | NC                        | -   |
| 4       | FB4        | LED-                      | P   |
| 5       | FB3        | LED-                      | P   |
| 6       | FB2        | LED-                      | P   |
| 7       | FB1        | LED-                      | P   |
| 8       | NC         | NC                        | -   |
| 9       | VLED       | LED+                      | P   |
| 10      | VLED       | LED+                      | P   |
| 11      | VLED       | LED+                      | P   |
| 12      | NC         | 7.5V For VPP              | -   |
| 13      | LED PWMIn  | NC                        | I   |
| 14      | LED PWMOut | LED PWMOut 1.8v           | O   |
| 15      | ID         | ID(GND for AUO)           | I/O |
| 16      | LCD_RST    | Reset                     | I   |
| 17      | NC         | NC                        | -   |
| 18      | NC         | NC                        | -   |
| 19      | VDD        | 3.3V                      | P   |
| 20      | VDD        | 3.3V                      | P   |
| 21      | VDD        | 3.3V                      | P   |
| 22      | IOVCC      | 1.8V                      | P   |
| 23      | IOVCC      | 1.8V                      | P   |
| 24      | GND        | GND                       | P   |
| 25      | D3P        | MIPI Input Data Pair D3P  | I   |
| 26      | D3N        | MIPI Input Data Pair D3N  | I   |
| 27      | GND        | GND                       | P   |
| 28      | D2P        | MIPI Input Data Pair D2P  | I   |
| 29      | D2N        | MIPI Input Data Pair D2N  | I   |
| 30      | GND        | GND                       | P   |
| 31      | CLKP       | MIPI Input Data Pair CLKP | I   |
| 32      | CLKN       | MIPI Input Data Pair CLKN | I   |
| 33      | GND        | GND                       | P   |
| 34      | D1P        | MIPI Input Clock Pair D1P | I   |
| 35      | D1N        | MIPI Input Clock Pair D1N | I   |
| 36      | GND        | GND                       | P   |
| 37      | D0P        | MIPI Input Data Pair D0P  | I   |
| 38      | D0N        | MIPI Input Data Pair D0N  | I   |
| 39      | GND        | GND                       | I   |

## 6.3 MIPI Interface Timing

### 6.3.1 Timing Characteristics

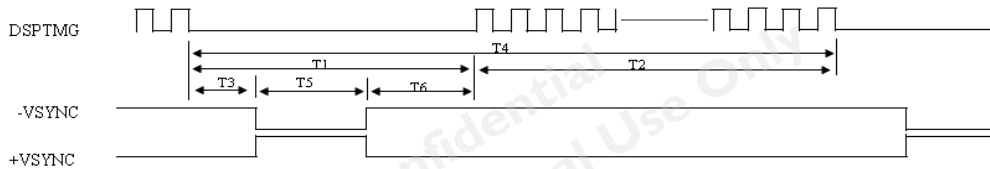
Basically, interface timings should match the 800 x 1280 /60 Hz manufacturing guide line timing.

|                        |            |       |            |
|------------------------|------------|-------|------------|
| Vertical Total         | VT (tv)    | 1300  | line       |
| Vertical Front-Porch   | VFP (tvfp) | 8     | line       |
| Vertical Active        | VA (tvd)   | 1280  | line       |
| Vertical Sync.         | VS (twv)   | 4     | line       |
| Vertical Back-Porch    | VBP (tvbp) | 8     | line       |
| Horizontal Total       | HT (th)    | 960   | clk(pixel) |
| Horizontal Front-Porch | HFP (thfp) | 24    | clk(pixel) |
| Horizontal Active      | HA (thd)   | 800   | clk(pixel) |
| Horizontal Sync.       | HS (thw)   | 4     | clk(pixel) |
| Horizontal Back-Porch  | HBP (thbp) | 132   | clk(pixel) |
| Pixel Frequency        | CLK (fc)   | 75.00 | MHz        |

#### Driving

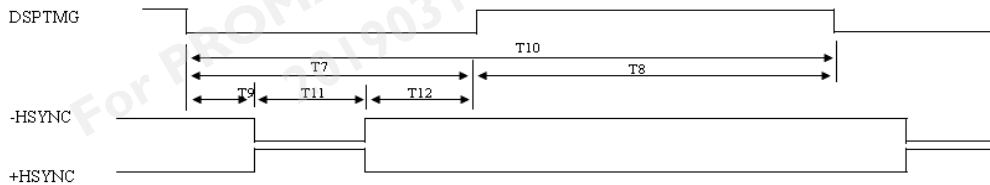
(LVDS Receiver Output)

#### Vertical Timing



| Item  | T1 Vertical Blanking | T2 Active Field | T3 VSYNC Front Porch | T4 Frame Time | T5 VSYNC Width | T6 VSYNC Back Porch |
|-------|----------------------|-----------------|----------------------|---------------|----------------|---------------------|
| Value | 20                   | 1280            | 8                    | 1300          | 4              | 8                   |

#### Horizontal Timing



| Item  | T7 Horizontal Blanking | T8 Active Field | T9 HSYNC Front Porch | T10 H line Time | T11 HSYNC Width | T12 HSYNC Back Porch |
|-------|------------------------|-----------------|----------------------|-----------------|-----------------|----------------------|
| Value | 160                    | 800             | 24                   | 960             | 4               | 132                  |

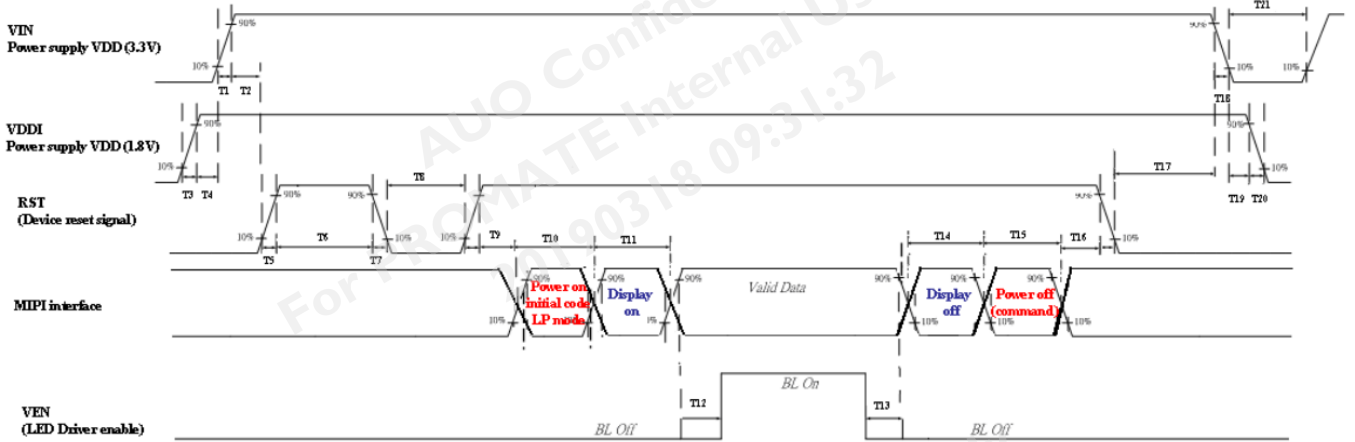
#### Dot Timing

| Item  | Dot Clock Frequency | Data Clock Frequency |
|-------|---------------------|----------------------|
| Value | 75MHz               | Dot Clock Frequency  |

## 6.4 Power ON(Wake Up )/OFF(Stand-by) sequence

### 6.4.1 Power

Power on/off sequence is as follows. Interface signals and LED on/off sequence are also shown in the chart.



Power Sequence Timing

| Parameter | Value |       | Units |
|-----------|-------|-------|-------|
|           | Min.  | Max.  |       |
| T1        | 0.5   | 10    | ms    |
| T2        | 1     | -     |       |
| T3        | 0.5   | 10    |       |
| T4        | 0     | 50    |       |
| T5        | 0     | 0.002 |       |
| T6        | 1     | -     |       |
| T7        | 0     | 0.002 |       |
| T8        | 0.01  | -     |       |
| T9        | 5     | -     |       |
| T10       | 180   | -     |       |
| T11       | 33.4  | -     |       |
| T12       | 200   | -     |       |
| T13       | 200   | -     |       |
| T14       | 33.4  | -     |       |
| T15       | 180   | -     |       |
| T16       | 50    | -     |       |
| T17       | 120   | -     |       |
| T18       | 0     | 10    |       |
| T19       | 0     | 10    |       |
| T20       | 0     | 10    |       |
| T21       | 500   | -     |       |

### 6.4.2 MIPI Command

T10 : power on => initial code + sleep out(0x11) (by panel different)

T11 : display on (0x29)

T14 : display off (0x28)

T15 : power off => sleep in (0x10)

## 7. Panel Reliability Test

### 7.1 Vibration Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 1.5 G
- Frequency: 10 - 500Hz Random
- Sweep: 30 Minutes each Axis (X, Y, Z)

### 7.2 Shock Test

Test Spec:

- Test method: Non-Operation
- Acceleration: 220 G , Half sine wave
- Active time: 2 ms
- Pulse: X,Y,Z .one time for each side

### 7.3 Reliability Test

| Items                      | Required Condition                                | Note   |
|----------------------------|---|--------|
| Temperature Humidity Bias  | Ta= 40°C , 90%RH, 300h                            |        |
| High Temperature Operation | Ta= 50°C , Dry, 300h                              |        |
| Low Temperature Operation  | Ta= 0°C , 300h                                    |        |
| High Temperature Storage   | Ta= 60°C , 300h                                   |        |
| Low Temperature Storage    | Ta= -20°C , 300h                                  |        |
| Thermal Shock Test         | Ta=-20°C to 60°C , Duration at 30 min, 100 cycles |        |
| ESD                        | Contact : ±8 KV<br>Air : ±15 KV                   | Note 1 |

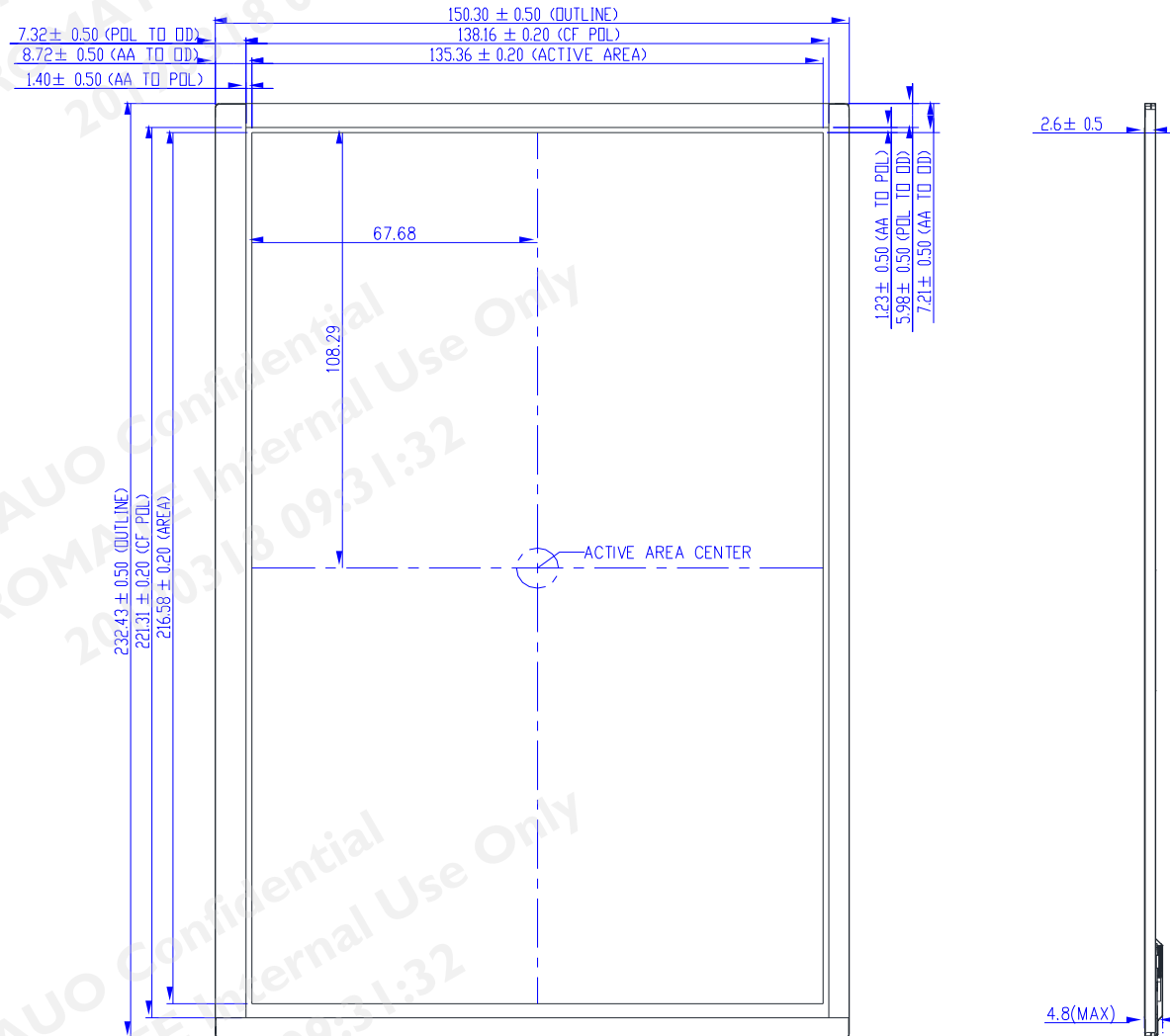
**Note1:** According to EN 61000-4-2 , ESD class B: Some performance degradation allowed. No data lost . Self-recoverable. No hardware failures.

**Remark:** MTBF (Excluding the LED): 30,000 hours with a confidence level 90%



## 8. Mechanical Characteristics

### 8.1 LCM Standard Outline Dimension (Front View)





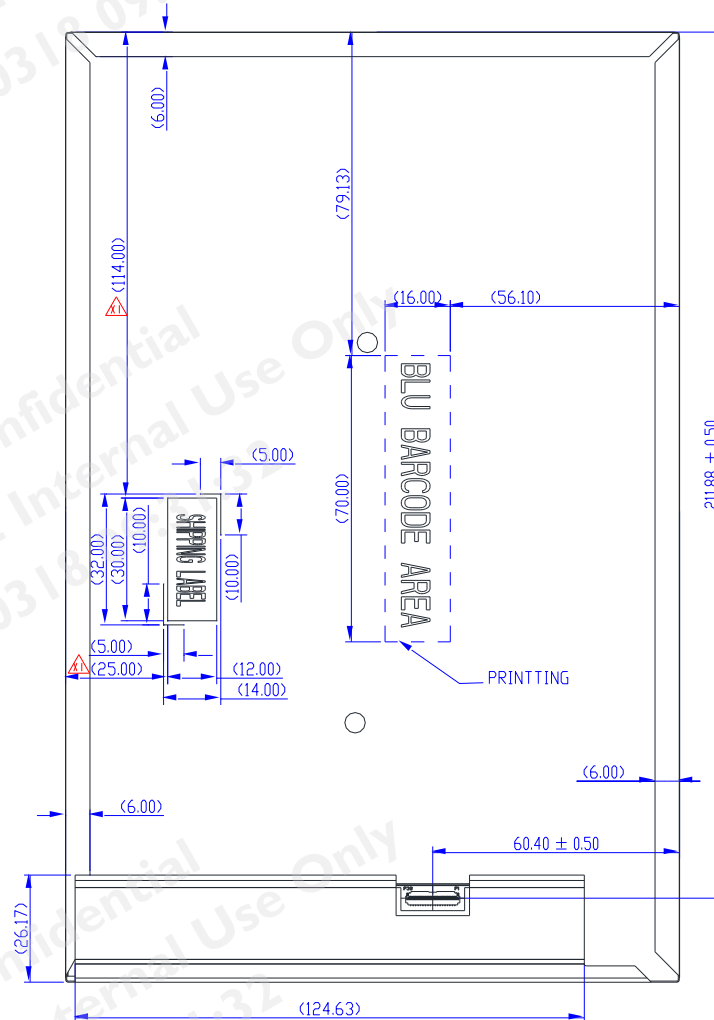


# Product Specification

AU OPTRONICS CORPORATION

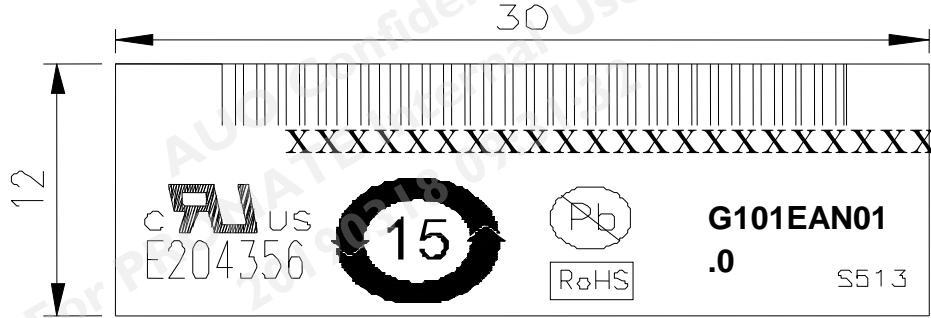
G101EAN01.0

## 8.2 LCM Standard Outline Dimension (Rear View)

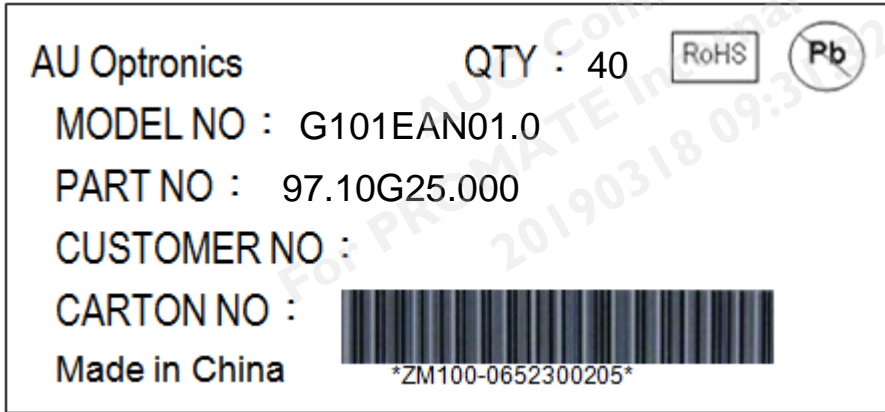


## 9. Label and Packaging

### 9.1 Shipping Label (on the rear side of TFT-LCD display)



### 9.2 Carton Label Format



### 9.3 Shipping Package of Palletizing Sequence

Pallet size : 1150mm x 840mm x 138mm

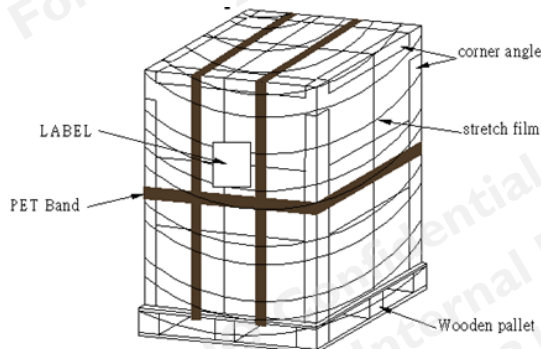
Box stacked\_Max

Module by air : (2x2)x3 layers , one pallet put 12 boxes , total 480 pcs module

Module by sea : (2x2)x3 layers + (2x2)x2 layers , two pallet put 20 boxes , total 800 pcs module

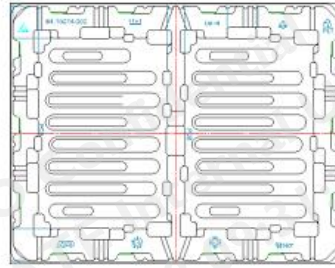
Module by sea\_HQ : (2x2)x3 layers + (2x2)x2 layers , two pallet put 20 boxes , total 800 pcs module

Box stacked on pallet (Picture):

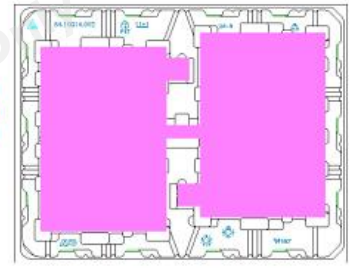




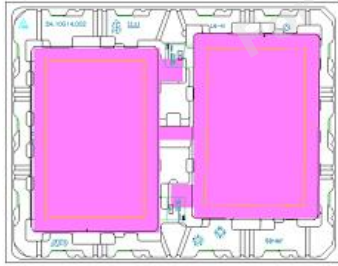
PP Board



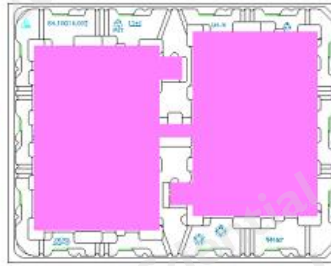
1pcs Flat Tray



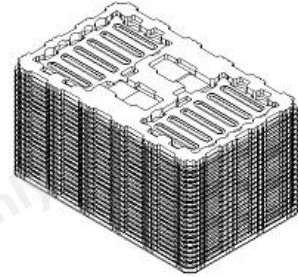
1pcs tray with  
2 pcs EPE Spacer



Put 2 pcs Panel  
(Face down)



1pcs Tray with  
2pcs Panel+2pcs EPE Spacer



Stack flat tray one by one until 21th  
pcs tray, the 21th tray is empty.



Put 40 pcs Panel into  
anti-static bag(use tape to fix)



Put EPE cushion into carton



Then put anti-static bag into carton  
which has EPE cushion in it



Put on top EPE cushion



And use tape to fix carton