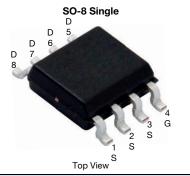
Vishay Siliconix

Si4056DY



N-Channel 100 V (D-S) MOSFET



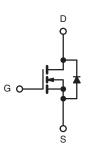
PRODUCT SUMMARY					
V _{DS} (V)	100				
$R_{DS(on)}$ max. (Ω) at V_{GS} = 10 V	0.023				
$R_{DS(on)}$ max. (Ω) at V_{GS} = 7.5 V	0.024				
$R_{DS(on)}$ max. (Ω) at V_{GS} = 4.5 V	0.031				
Q _g typ. (nC)	9.7				
I _D (A) ^a	11.1				
Configuration	Single				

FEATURES

- TrenchFET® power MOSFET
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- DC/DC primary side switch
- Telecom / server
- Industrial
- Synchronous rectification



N-Channel MOSFET

ORDERING INFORMATION				
Package	SO-8			
Lead (Pb)-free and halogen-free	Si4056DY-T1-GE3			

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V _{DS}	100	V
Gate-source voltage		V _{GS}	± 20	
Continuous drain current (T _J = 150 °C)	T _C = 25 °C		11.1	
	T _C = 70 °C		8.8	
	T _A = 25 °C	I _D	7.3 ^{b, c}	
	T _A = 70 °C		5.8 ^{b, c}	
Pulsed drain current (t = 300 µs)		I _{DM}	70	— A
Continuous source-drain diode current	T _C = 25 °C		5.1	
	T _A = 25 °C	I _S	2.2 ^{b, c}	
Single pulse avalanche current		I _{AS}	15	
Avalanche energy	L = 0.1 mH	E _{AS}	11.2	mJ
Maximum power dissipation	T _C = 25 °C		5.7	w
	T _C = 70 °C		3.6	
	T _A = 25 °C	P _D	2.5 ^{b, c}	
	T _A = 70 °C	1	1.6 ^{b, c}	
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +150	°C

THERMAL RESISTANCE RATINGS						
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT	
Maximum junction-to-ambient b, d	$t \le 10 s$	R _{thJA}	35	50	°C/W	
Maximum junction-to-foot (drain)	Steady state	R _{thJF}	18	22		

Notes

a. Based on $T_C = 25 \ ^{\circ}C$

b. Surface mounted on 1" x 1" FR4 board

c. t = 10 s

d. Maximum under steady state conditions is 85 °C/W

S12-1136-Rev. A, 21-May-12

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FREE

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Si4056DY

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static			I	<u>1</u>	I	I	
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	100	-	-	V	
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$		-	67	-		
V _{GS(th)} temperature coefficient	$\Delta V_{GS(th)}/T_J$	l _D = 250 μA	-	-5	-	mV/°C	
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \ \mu A$	1.5	-	2.8	V	
Gate-source leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$	-	-	± 100	nA	
Zere gete veltege drein eurrent		$V_{DS} = 100 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$	-	-	1	μA	
Zero gate voltage drain current	IDSS	$V_{DS} = 100 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ T}_{J} = 55 ^{\circ}\text{C}$	-	-	10		
On-state drain current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	30	-	-	А	
		$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 15 \text{ A}$	-	0.017	0.023	Ω	
Drain-source on-state resistance ^a	R _{DS(on)}	$V_{GS} = 7.5 \text{ V}, \text{ I}_{D} = 12 \text{ A}$	-	0.018	0.024		
		$V_{GS} = 4.5 \text{ V}, \text{ I}_{D} = 10 \text{ A}$	-	0.022	0.031		
Forward transconductance ^a	9 _{fs}	$V_{DS} = 15 \text{ V}, \text{ I}_{D} = 15 \text{ A}$	-	26	-	S	
Dynamic ^b							
Input capacitance	C _{iss}		-	900	-	pF	
Output capacitance	C _{oss}	$V_{DS} = 50 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ f} = 1 \text{ MHz}$	-	340	-		
Reverse transfer capacitance	C _{rss}		-	31	-		
		$V_{DS} = 50 \text{ V}, V_{GS} = 10 \text{ V}, I_{D} = 10 \text{ A}$	-	19.6	29.5		
Total gate charge	gate charge Qg		-	9.7	15		
Gate-source charge	Q _{gs}	$V_{DS} = 50 \text{ V}, \text{ V}_{GS} = 4.5 \text{ V}, \text{ I}_{D} = 10 \text{ A}$	-	2.8	-	nC	
Gate-drain charge	Q _{gd}		-	4.3	-		
Output charge	Q _{oss}	$V_{DS} = 50 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$	-	26.2	40		
Gate resistance	R _g	f = 1 MHz	0.2	0.85	1.7	Ω	
Turn-on delay time	t _{d(on)}		-	13	26		
Rise time	t _r	$V_{DD} = 50 \text{ V}, \text{ R}_{L} = 5 \Omega$	-	14	28		
Turn-off delay time	t _{d(off)}	$I_D \cong 10$ Å, $V_{GEN} = 7.5$ V, $R_g = 1 \Omega$	-	19	38		
Fall time	t _f		-	10	20		
Turn-on delay time	t _{d(on)}		-	11	22	ns	
Rise time	t _r	V_{DD} = 50 V, R_L = 5 Ω	-	10	20	-	
Turn-off delay time	t _{d(off)}	$I_D \cong 10$ Å, $V_{GEN} = 10$ V, $R_g = 1$ Ω	-	20	40		
Fall time	t _f		-	9	18		
Drain-Source Body Diode Characteristi	cs	•	•		•	•	
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	5.1		
Pulse diode forward current ^a	I _{SM}		-	-	70	A	
Body diode voltage	V _{SD}	I _S = 4 A	-	0.77	1.1	V	
Body diode reverse recovery time	t _{rr}	-	-	34	65	ns	
Body diode reverse recovery charge	Q _{rr}	I _F = 5 A, di/dt = 100 A/μs,	-	34	65	nC	
Reverse recovery fall time	t _a	$T_{\rm J} = 25 ^{\circ}{\rm C}$	-	20	-		
Reverse recovery rise time	t _b	1	_	14	_	ns	

Notes

a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %

b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

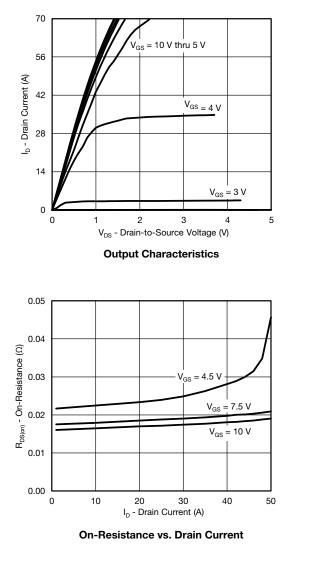
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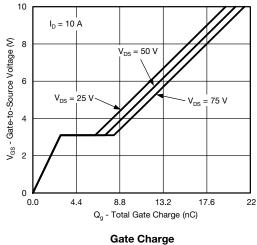


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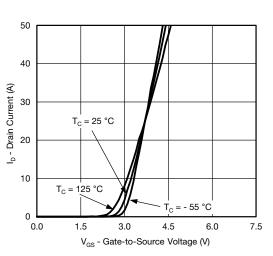
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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

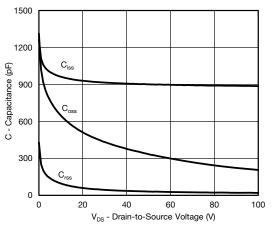




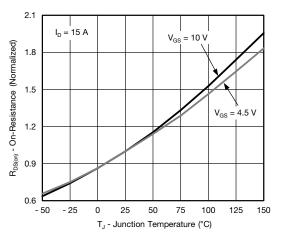




Transfer Characteristics



Capacitance



On-Resistance vs. Junction Temperature

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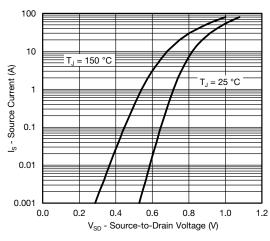
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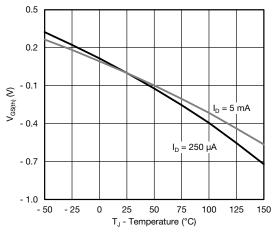
Si4056DY

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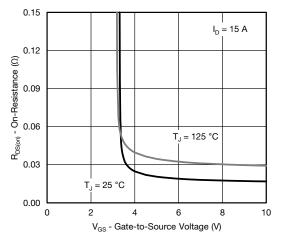
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



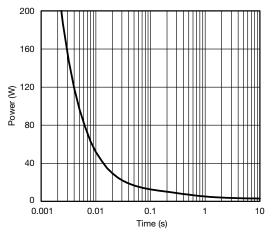
Source-Drain Diode Forward Voltage



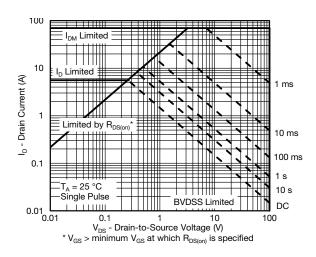




On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Ambient



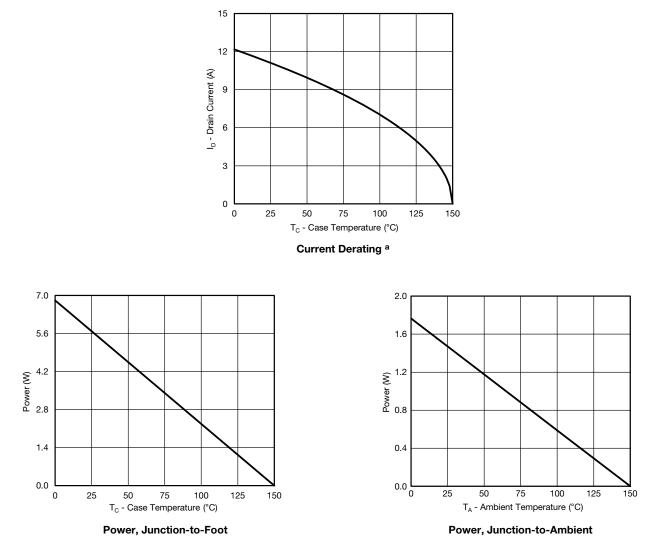
Safe Operating Area, Junction-to-Ambient

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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Note

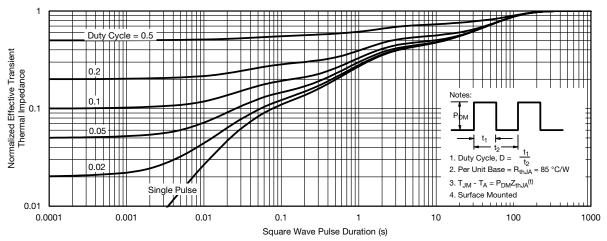
a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



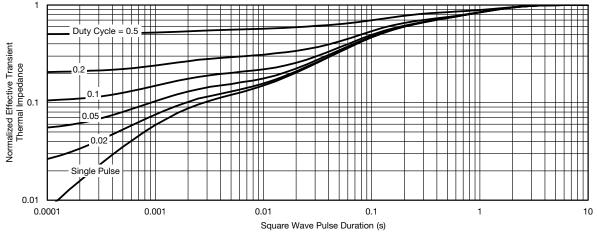
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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62662.

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Package Information

Vishay Siliconix

SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012





	MILLIM	IETERS	INC	HES	
DIM	Min	Мах	Min	Max	
A	1.35	1.75	0.053	0.069	
A ₁	0.10	0.20	0.004	0.008	
В	0.35	0.51	0.014	0.020	
С	0.19	0.25	0.0075	0.010	
D	4.80	5.00	0.189	0.196	
E	3.80	4.00	0.150	0.157	
е	1.27	BSC	0.050 BSC		
н	5.80	6.20	0.228	0.244	
h	0.25	0.50	0.010	0.020	
L	0.50	0.93	0.020	0.037	
q	0°	8°	0°	8°	
S	0.44	0.64	0.018	0.026	
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498					

Application Note 826

Vishay Siliconix



RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads Dimensions in Inches/(mm)

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