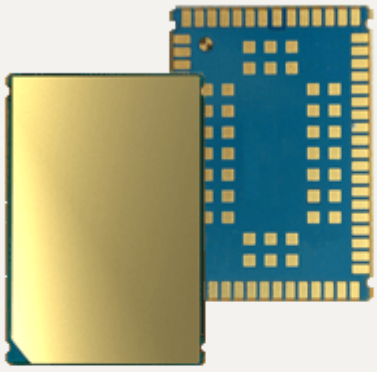
Cinterion® BGS2-E/BGS2-W

Hardware Interface Description

Version: 04.030a
DocId: BGS2_HID_v04.030a



Document Name:	**Cinterion® BGS2-E/BGS2-W Hardware Interface Description**
Version:	**04.030a**
Date:	**2017-03-15**
DocId:	**BGS2_HID_v04.030a**
Status	**Confidential / Released**

Contents

Tables

Figures

0 Document History

Preceding document: "Cinterion® BGS2-E/BGS2-W Hardware Interface Description" v04.030
New document: "Cinterion® BGS2-E/BGS2-W Hardware Interface Description" v**04.030a**

Chapter	What is new
1.3.1, 1.3.2	Updated directives and standards.
6.2.1.1	Added note recommending the 150µm thick stencil.
8.2	Added antenna gain limits and notes for IC.

Preceding document: "Cinterion® BGS2-E/BGS2-W Hardware Interface Description" v03.001a
New document: "Cinterion® BGS2-E/BGS2-W Hardware Interface Description" v04.030

Chapter	What is new
Throughout document	Adapted lowest fixed bit rate for ASC0 and ASC1 (1,200bps --> 300bps)
3.5.6.1	Specified assertion direction for RTS0 and RTS1.
5.5	Revised table layout for power supply ratings.
5.6.1	Added note to Table 29 for <sideTone> parameter.
5.6.3	Added footnote on sidetone gain to Table 30.
6.2.3.1	Revised description for average ramp up and ramp down rates in Table 35.
9.1	Updated ordering information. Added note for module label information.

Preceding document: "Cinterion® BGS2-E/BGS2-W Hardware Interface Description" v03.001
New document: "Cinterion® BGS2-E/BGS2-W Hardware Interface Description" v03.001a

Chapter	What is new
5.4	Revised CLmax value for V180/V285.
6.2.3.1	Added note regarding reflow profile features and ratings listed in Table 35. Revised average ramp-down rate listed in Table 35.

Preceding document: "Cinterion® BGS2-E/BGS2-W Hardware Interface Description" v02.109
New document: "Cinterion® BGS2-E/BGS2-W Hardware Interface Description" v03.001

Chapter	What is new
Throughout document	Replaced RF_OUT with ANT_GSM. Introduced $BATT+_{BB}$ and $BATT+_{RF}$ as distinct names for the BATT+ power supply lines for general power management (BB) and the GSM power amplifier (RF).
3.3.3	Revised startup signal state for GPIO8 (see also Figure 28).
3.4	Revised description to mention class change threshold.
3.9	Revised signal startup state for RING0 shown in Figure 17.
3.16	New section Analog-to-Digital Converter.

Preceding document: "Cinterion® BGS2-E/BGS2-W Hardware Interface Description" v02.000d
New document: "Cinterion® BGS2-E/BGS2-W Hardware Interface Description" v02.109

Chapter	What is new
Throughout document	Added I^2S digital audio interface. GPIO6 configurable as jamming indicator. Introduced BATT+_RF-PA as name for the signal line supplying the GSM power amplifier.
3.3.5.3, 3.3.5.4	Revised description of under- and overvoltage shutdown thresholds.
3.3.3	Revised startup signal states for GPIO5/LED (see also Figure 28).
3.9	Revised signal startup states for DTR0, DCD0 and DSR0 shown in Figure 17.
3.17	New section Jamming Indicator.
5.5	Revised table layout for power supply ratings.
5.6.3	Revised audio mode 6 characteristics listed in Table 30.
9	Removed section on how to get started.
9.1	Updated ordering numbers.

Preceding document: "BGS2-E/BGS2-W Hardware Interface Description" Version 02.000c
New document: "Cinterion® BGS2-E/BGS2-W Hardware Interface Description" v02.000d

Chapter	What is new
6.2	Added note regarding routing of signal tracks.
6.3.2.1	Replaced moisture sensitivity label and humidity indicator card (Figure 58 and Figure 59).

Preceding document: "BGS2-E/BGS2-W Hardware Interface Description" Version 02.000b
New document: "BGS2-E/BGS2-W Hardware Interface Description" Version 02.000c

Chapter	What is new
3.3.5.5	New section Hardware Watchdog.
3.20	Modified values for ASC0 lines at voltage level V285 in Table 18.
5.5	Revised measurement start timing in footnote of Table 28.

Preceding document: "BGS2-E/BGS2-W Hardware Interface Description" Version 01.910
New document: "BGS2-E/BGS2-W Hardware Interface Description" Version 02.000b

Chapter	What is new
3.3.3	Added Digital Audio Interface signals TXDDAI, RXDDAI, TFSDAI, SCLK.
3.3.5.2	New section Deferred Shutdown at Extreme Temperature Conditions.
3.9	Revised section to include V285 voltage level configuration. Applied appropriate modifications to other sections in document.
3.12	Figure 26: Corrected ON signal timing.
5.4	Revised assignment for pads 47 and 48 to GND.
7	Figure 63: Added signals FAST_SHTDWN and TXDDAI, RXDDAI, TFSDAI, SCLK. Removed V285 signal.

8	Figure 65: Changed figure to show reference setup with DSB75, DSB75 module adapter and BGS2-E/BGS2-W evaluation module.
9	New section Getting Started with BGS2-E/BGS2-W.

Preceding document: "BGS2-E/BGS2-W Hardware Interface Description" Version 02.000
New document: "BGS2-E/BGS2-W Hardware Interface Description" Version 01.910

Chapter	What is new
Throughout document	Swapped GPIO9 - now pad 28 - and GPIO10 - now pad 27.
1.3.2	Added note on portable applications.
3.3.4.2	New section Disconnect BGS2-E/BGS2-W BATT+ Lines.
3.14.1	New section I^2C Interface on DSB75.
3.21	New section Fast Shutdown.
7	Revised sample application to include disconnect circuit for BATT+ lines.
8.2	Revised section and specified values for antenna gain.

New document: "BGS2-E/BGS2-W Hardware Interface Description" Version 02.000

Chapter	What is new
--	Initial document setup.

1 Introduction

This document[1] describes the hardware of the Cinterion® BGS2-E/BGS2-W module that connects to the cellular device application and the air interface. It helps you quickly retrieve interface specifications, electrical and mechanical details and information on the requirements to be considered for integrating further components.

1.1 Related Documents

[1] Cinterion® BGS2-E/BGS2-W AT Command Set
[2] Cinterion® BGS2-E/BGS2-W Release Note
[3] DSB75 Development Support Board Hardware Interface Description, v14
[4] Application Note 02: Audio Interface Design for GSM Applications
[5] Application Note 26: Power Supply Design for GSM Applications
[6] Application Note 48: SMT Module Integration for BGS2-E/BGS2-W
[7] BGS2-W MPE calculation - Test report (Maximum Permissible Exposure)

1.2 Terms and Abbreviations

Abbreviation	Description
ADC	Analog-to-digital converter
AGC	Automatic Gain Control
ANSI	American National Standards Institute
ARFCN	Absolute Radio Frequency Channel Number
ARP	Antenna Reference Point
ASC0/ASC1	Asynchronous Controller. Abbreviations used for first and second serial interface of BGS2-E/BGS2-W
BER	Bit Error Rate
BTS	Base Transceiver Station
CB or CBM	Cell Broadcast Message
CE	Conformité Européene (European Conformity)
CHAP	Challenge Handshake Authentication Protocol
CPU	Central Processing Unit
CS	Coding Scheme
CSD	Circuit Switched Data
CTS	Clear to Send
DAC	Digital-to-Analog Converter
DAI	Digital Audio Interface
dBm0	Digital level, 3.14dBm0 corresponds to full scale, see ITU G.711, A-law

1. The document is effective only if listed in the appropriate Release Notes as part of the technical documentation delivered with your Gemalto M2M product.

Abbreviation	Description
DCE	Data Communication Equipment (typically modems, e.g. Gemalto M2M module)
DCS 1800	Digital Cellular System, also referred to as PCN
DRX	Discontinuous Reception
DSB	Development Support Box
DSP	Digital Signal Processor
DSR	Data Set Ready
DTE	Data Terminal Equipment (typically computer, terminal, printer or, for example, GSM application)
DTR	Data Terminal Ready
DTX	Discontinuous Transmission
EFR	Enhanced Full Rate
EGSM	Enhanced GSM
EIRP	Equivalent Isotropic Radiated Power
EMC	Electromagnetic Compatibility
ERP	Effective Radiated Power
ESD	Electrostatic Discharge
ETS	European Telecommunication Standard
EuP	Energy-Using Products
FCC	Federal Communications Commission (U.S.)
FDMA	Frequency Division Multiple Access
FR	Full Rate
GMSK	Gaussian Minimum Shift Keying
GPIO	General Purpose Input/Output
GPRS	General Packet Radio Service
GSM	Global Standard for Mobile Communications
HiZ	High Impedance
HR	Half Rate
I/O	Input/Output
IC	Integrated Circuit
IMEI	International Mobile Equipment Identity
ISO	International Standards Organization
ITU	International Telecommunications Union
kbps	kbits per second
LED	Light Emitting Diode
Li-Ion/Li+	Lithium-Ion
Li battery	Rechargeable Lithium Ion or Lithium Polymer battery
Mbps	Mbits per second
MMI	Man Machine Interface

Abbreviation	Description
MO	Mobile Originated
MS	Mobile Station (GSM module), also referred to as TE
MSISDN	Mobile Station International ISDN number
MT	Mobile Terminated
NTC	Negative Temperature Coefficient
OEM	Original Equipment Manufacturer
PA	Power Amplifier
PAP	Password Authentication Protocol
PBCCH	Packet Switched Broadcast Control Channel
PCB	Printed Circuit Board
PCL	Power Control Level
PCM	Pulse Code Modulation
PCN	Personal Communications Network, also referred to as DCS 1800
PCS	Personal Communication System, also referred to as GSM 1900
PDU	Protocol Data Unit
PLL	Phase Locked Loop
PPP	Point-to-point protocol
PSK	Phase Shift Keying
PSU	Power Supply Unit
PWM	Pulse Width Modulation
R&TTE	Radio and Telecommunication Terminal Equipment
RAM	Random Access Memory
REACH	Registration, Evaluation, Authorisation and Restriction of Chemicals
RF	Radio Frequency
RMS	Root Mean Square (value)
RoHS	Restriction of the use of certain hazardous substances in electrical and electronic equipment.
ROM	Read-only Memory
RTC	Real Time Clock
RTS	Request to Send
Rx	Receive Direction
SAR	Specific Absorption Rate
SAW	Surface Acoustic Wave
SELV	Safety Extra Low Voltage
SIM	Subscriber Identification Module
SMD	Surface Mount Device
SMS	Short Message Service
SMT	Surface Mount Technology

Abbreviation	Description
SRAM	Static Random Access Memory
TA	Terminal adapter (e.g. GSM module)
TDMA	Time Division Multiple Access
TE	Terminal Equipment, also referred to as DTE
Tx	Transmit Direction
UART	Universal asynchronous receiver-transmitter
URC	Unsolicited Result Code
USSD	Unstructured Supplementary Service Data
VSWR	Voltage Standing Wave Ratio

1.3 Regulatory and Type Approval Information

1.3.1 Directives and Standards

BGS2-E/BGS2-W is designed to comply with the directives and standards listed below.

It is the responsibility of the application manufacturer to ensure compliance of the final product with all provisions of the applicable directives and standards as well as with the technical specifications provided in the "BGS2-E/BGS2-W Hardware Interface Description".[1]

Table 1: Directives

2014/53/EU	Directive of the European Parliament and of the council of 16 April 2014 on the harmonization of the laws of the Member States relating to the making available on the market of radio equipment and repealing Directive 1999/05/EC. The product is labeled with the CE conformity mark.
2002/95/EC (RoHS 1) 2011/65/EC (RoHS 2)	Directive of the European Parliament and of the Council of 27 January 2003 (and revised on 8 June 2011) on the restriction of the use of certain hazardous substances in electrical and electronic equipment (RoHS)

Table 2: Standards of North American type approval[1]

CFR Title 47	Code of Federal Regulations, Part 22 and Part 24 (Telecommunications, PCS); US Equipment Authorization FCC
UL 60 950-1	Product Safety Certification (Safety requirements)
OET Bulletin 65 (Edition 97-01)	Evaluating Compliance with FCC Guidelines for Human Exposure to Radiofrequency Electromagnetic Fields
NAPRD.03 V5.30	Overview of PCS Type certification review board Mobile Equipment Type Certification and IMEI control PCS Type Certification Review board (PTCRB)
RSS132 RSS133	Canadian Standard

1. Applies for the quad band module variant BGS2-W only.

Table 3: Standards of European type approval

3GPP TS 51.010-1	Digital cellular telecommunications system (Phase 2); Mobile Station (MS) conformance specification
ETSI EN 301 511 V12.5.1	Global System for Mobile communications (GSM); Mobile Stations (MS) equipment; Harmonized Standard covering the essential requirements of article 3.2 of Directive 2014/53/EU
GCF-CC V3.64	Global Certification Forum - Certification Criteria

1. Manufacturers of applications which can be used in the US shall ensure that their applications have a PTCRB approval. For this purpose they can refer to the PTCRB approval of the respective module.

Table 3: Standards of European type approval

ETSI EN 301 489-1 V2.1.1	ElectroMagnetic Compatibility (EMC) standard for radio equipment and services; Part 1: Common technical requirements; Harmonized Standard covering the essential requirements of article 3.1(b) of Directive 2014/53/EU and the essential requirements of article 6 of Directive 2014/30/EU
Draft ETSI EN 301 489-52 V1.1.0	Electromagnetic Compatibility (EMC) standard for radio equipment and services; Part 52: Specific conditions for Cellular Communication Mobile and portable (UE) radio and ancillary equipment; Harmonized Standard covering the essential requirements of article 3.1(b) of Directive 2014/53/EU
EN 60950-1:2006/ A11:2009+A1:2010+ A12:2011+A2:2013	Safety of information technology equipment

Table 4: Requirements of quality and environment

IEC 60068	Environmental testing
DIN EN 60529	IP codes

Table 5: Standards of the Ministry of Information Industry of the People's Republic of China

SJ/T 11363-2006	"Requirements for Concentration Limits for Certain Hazardous Substances in Electronic Information Products" (2006-06).
SJ/T 11364-2006	"Marking for Control of Pollution Caused by Electronic Information Products" (2006-06).  According to the "Chinese Administration on the Control of Pollution caused by Electronic Information Products" (ACPEIP) the EPUP, i.e., Environmental Protection Use Period, of this product is 20 years as per the symbol shown here, unless otherwise marked. The EPUP is valid only as long as the product is operated within the operating limits described in the Gemalto M2M Hardware Interface Description. Please see Table 6 for an overview of toxic or hazardous substances or elements that might be contained in product parts in concentrations above the limits defined by SJ/T 11363-2006.

Table 6: Toxic or hazardous substances or elements with defined concentration limits

部件名称 Name of the part	有毒有害物质或元素 Hazardous substances					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
金属部件 (Metal Parts)	O	O	O	O	O	O
电路模块 (Circuit Modules)	X	O	O	O	O	O
电缆及电缆组件 (Cables and Cable Assemblies)	O	O	O	O	O	O
塑料和聚合物部件 (Plastic and Polymeric parts)	O	O	O	O	O	O

O:
表示该有毒有害物质在该部件所有均质材料中的含量均在SJ/T11363-2006 标准规定的限量要求以下。
Indicates that this toxic or hazardous substance contained in all of the homogeneous materials for this part is below the limit requirement in SJ/T11363-2006.

X:
表示该有毒有害物质至少在该部件的某一均质材料中的含量超出SJ/T11363-2006标准规定的限量要求。
Indicates that this toxic or hazardous substance contained in at least one of the homogeneous materials used for this part *might exceed* the limit requirement in SJ/T11363-2006.

1.3.2 SAR requirements specific to portable mobiles

Mobile phones, PDAs or other portable transmitters and receivers incorporating a GSM module must be in accordance with the guidelines for human exposure to radio frequency energy. This requires the Specific Absorption Rate (SAR) of portable BGS2-E/BGS2-W based applications to be evaluated and approved for compliance with national and/or international regulations.

Since the SAR value varies significantly with the individual product design manufacturers are advised to submit their product for approval if designed for portable use. For European and US markets the relevant directives are mentioned below. It is the responsibility of the manufacturer of the final product to verify whether or not further standards, recommendations or directives are in force outside these areas.

Products intended for sale on US markets[1]

ES 59005/ANSI C95.1 Considerations for evaluation of human exposure to Electromagnetic Fields (EMFs) from Mobile Telecommunication Equipment (MTE) in the frequency range 30MHz - 6GHz

Products intended for sale on European markets

EN 50360 Product standard to demonstrate the compliance of mobile phones with the basic restrictions related to human exposure to electromagnetic fields (300MHz - 3GHz)

EN 62311:2008 Assessment of electronic and electrical equipment related to human exposure restrictions for electromagnetic fields (0 Hz - 300 Ghz)

IMPORTANT:
Manufacturers of portable applications based on BGS2-E/BGS2-W modules are required to have their final product certified and apply for their own FCC Grant and Industry Canada Certificate related to the specific portable mobile (see also Section 8.2).

1. Applies for the quad band module variant BGS2-W only.

1.3.3 Safety Precautions

The following safety precautions must be observed during all phases of the operation, usage, service or repair of any cellular terminal or mobile incorporating BGS2-E/BGS2-W. Manufacturers of the cellular terminal are advised to convey the following safety information to users and operating personnel and to incorporate these guidelines into all manuals supplied with the product. Failure to comply with these precautions violates safety standards of design, manufacture and intended use of the product. Gemalto M2M assumes no liability for customer's failure to comply with these precautions.

	When in a hospital or other health care facility, observe the restrictions on the use of mobiles. Switch the cellular terminal or mobile off, if instructed to do so by the guidelines posted in sensitive areas. Medical equipment may be sensitive to RF energy. The operation of cardiac pacemakers, other implanted medical equipment and hearing aids can be affected by interference from cellular terminals or mobiles placed close to the device. If in doubt about potential danger, contact the physician or the manufacturer of the device to verify that the equipment is properly shielded. Pacemaker patients are advised to keep their hand-held mobile away from the pacemaker, while it is on.
	Switch off the cellular terminal or mobile before boarding an aircraft. Make sure it cannot be switched on inadvertently. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communications systems. Failure to observe these instructions may lead to the suspension or denial of cellular services to the offender, legal action, or both.
	Do not operate the cellular terminal or mobile in the presence of flammable gases or fumes. Switch off the cellular terminal when you are near petrol stations, fuel depots, chemical plants or where blasting operations are in progress. Operation of any electrical equipment in potentially explosive atmospheres can constitute a safety hazard.
	Your cellular terminal or mobile receives and transmits radio frequency energy while switched on. Remember that interference can occur if it is used close to TV sets, radios, computers or inadequately shielded equipment. Follow any special regulations and always switch off the cellular terminal or mobile wherever forbidden, or when you suspect that it may cause interference or danger.
	Road safety comes first! Do not use a hand-held cellular terminal or mobile when driving a vehicle, unless it is securely mounted in a holder for speakerphone operation. Before making a call with a hand-held terminal or mobile, park the vehicle. Speakerphones must be installed by qualified personnel. Faulty installation or operation can constitute a safety hazard.
	IMPORTANT! Cellular terminals or mobiles operate using radio signals and cellular networks. Because of this, connection cannot be guaranteed at all times under all conditions. Therefore, you should never rely solely upon any wireless device for essential communications, for example emergency calls. Remember, in order to make or receive calls, the cellular terminal or mobile must be switched on and in a service area with adequate cellular signal strength. Some networks do not allow for emergency calls if certain network services or phone features are in use (e.g. lock functions, fixed dialing etc.). You may need to deactivate those features before you can make an emergency call. Some networks require that a valid SIM card be properly inserted in the cellular terminal or mobile.

2 Product Concept

2.1 Key Features at a Glance

Feature	Implementation
General	
Frequency bands	Dual band (BGS2-E): GSM 900/1800MHz Quad band (BGS2-W): GSM 850/900/1800/1900MHz
GSM class	Small MS
Output power (according to Release 99, V5)	Class 4 (+33dBm ±2dB) for EGSM850 (quad band only) Class 4 (+33dBm ±2dB) for EGSM900 Class 1 (+30dBm ±2dB) for GSM1800 Class 1 (+30dBm ±2dB) for GSM1900 (quad band only)
Power supply	3.3V to 4.5V
Operating temperature (board temperature)	Normal operation: -30°C to +85°C Extended operation: -40°C to -30°C, +85°C to +90°C
Physical	Dimensions: 27.6mm x 18.8mm x 2.7mm Weight: approx. 3 g
RoHS	All hardware components fully compliant with EU RoHS Directive
GSM/GPRS features	
Data transfer	GPRS: • Multislot Class 10 • Full PBCCH support • Mobile Station Class B • Coding Scheme 1 – 4 CSD: • V.110, RLP, non-transparent • 2.4, 4.8, 9.6, 14.4kbps • USSD PPP-stack for GPRS data transfer
SMS	Point-to-point MT and MO Cell broadcast Text and PDU mode Storage: SIM card plus 25 SMS locations in mobile equipment Transmission of SMS alternatively over CSD or GPRS. Preferred mode can be user defined.Transmission of SMS over GSM.
Fax	Group 3; Class 1

Feature	Implementation
Audio	Speech codecs: • Half rate HR (ETS 06.20) • Full rate FR (ETS 06.10) • Enhanced full rate EFR (ETS 06.50/06.60/06.80) • Adaptive Multi Rate AMR Handsfree operation, echo cancellation, noise suppression, 7 different ringing tones/melodies Voice prompts
Software	
AT commands	Hayes 3GPP TS 27.007, TS 27.005, Gemalto M2M AT commands for RIL compatibility
Microsoft™ compatibility	RIL for Pocket PC and Smartphone
SIM Application Toolkit	SAT Release 99
TCP/IP stack	Access by AT commands
Firmware update	Generic update from host application over ASC0 or ASC1.
Interfaces	
Module interface	Surface mount device with solderable connection pads (SMT application interface). Land grid array (LGA) technology ensures high solder joint reliability and provides the possibility to use an optional module mounting socket. For more information on how to integrate SMT modules see also [6]. This application note comprises chapters on module mounting and application layout issues as well as on additional SMT application development equipment.
2 serial interfaces	ASC0: • 8-wire modem interface with status and control lines, unbalanced, asynchronous • Adjustable baud rates: 300bps to 230,400bps • Autobauding: 1,200bps to 230,400bps • Supports RTS0/CTS0 hardware handshake and software XON/XOFF flow control. • Multiplex ability according to GSM 07.10 Multiplexer Protocol. ASC1: • 4-wire, unbalanced asynchronous interface • Adjustable baud rates: 300bps to 230,400bps • Supports RTS1/CTS1 hardware handshake and software XON/XOFF flow control
Audio	1 analog interface (with microphone feeding) 1 digital interface (PCM/I^2S)
UICC interface	Supported SIM cards: 3V, 1.8V External SIM card reader has to be connected via interface connector (note that card reader is not part of BGS2-E/BGS2-W)
GPIO interface	GPIO interface with 6 GPIO lines. The GPIO interface is shared with an I2C interface, LED signalling and PWM functionality as well as a jamming indicator.
Antenna	50Ω

Feature	Implementation
Power on/off, Reset	
Power on/off	Switch-on by hardware signal ON Switch-off by AT command (AT^SMSO) Automatic switch-off in case of critical temperature and voltage conditions.
Reset	Orderly shutdown and reset by AT command
Special features	
Real time clock	Timer functions via AT commands
Phonebook	SIM and phone
TTY/CTM support	Integrated CTM modem
TLS security	Transport layer security
RLS monitoring	Jamming detection
Evaluation kit	
Evaluation module	BGS2-W module soldered onto a dedicated PCB that can be connected to an adapter in order to be mounted onto the DSB75.
DSB75	DSB75 Development Support Board designed to test and type approve Gemalto M2M modules and provide a sample configuration for application engineering. A special adapter setup is required to connect the evaluation module to the DSB75. For more information on how to setup such a connection please refer to Chapter 9.

2.2 BGS2-E/BGS2-W System Overview

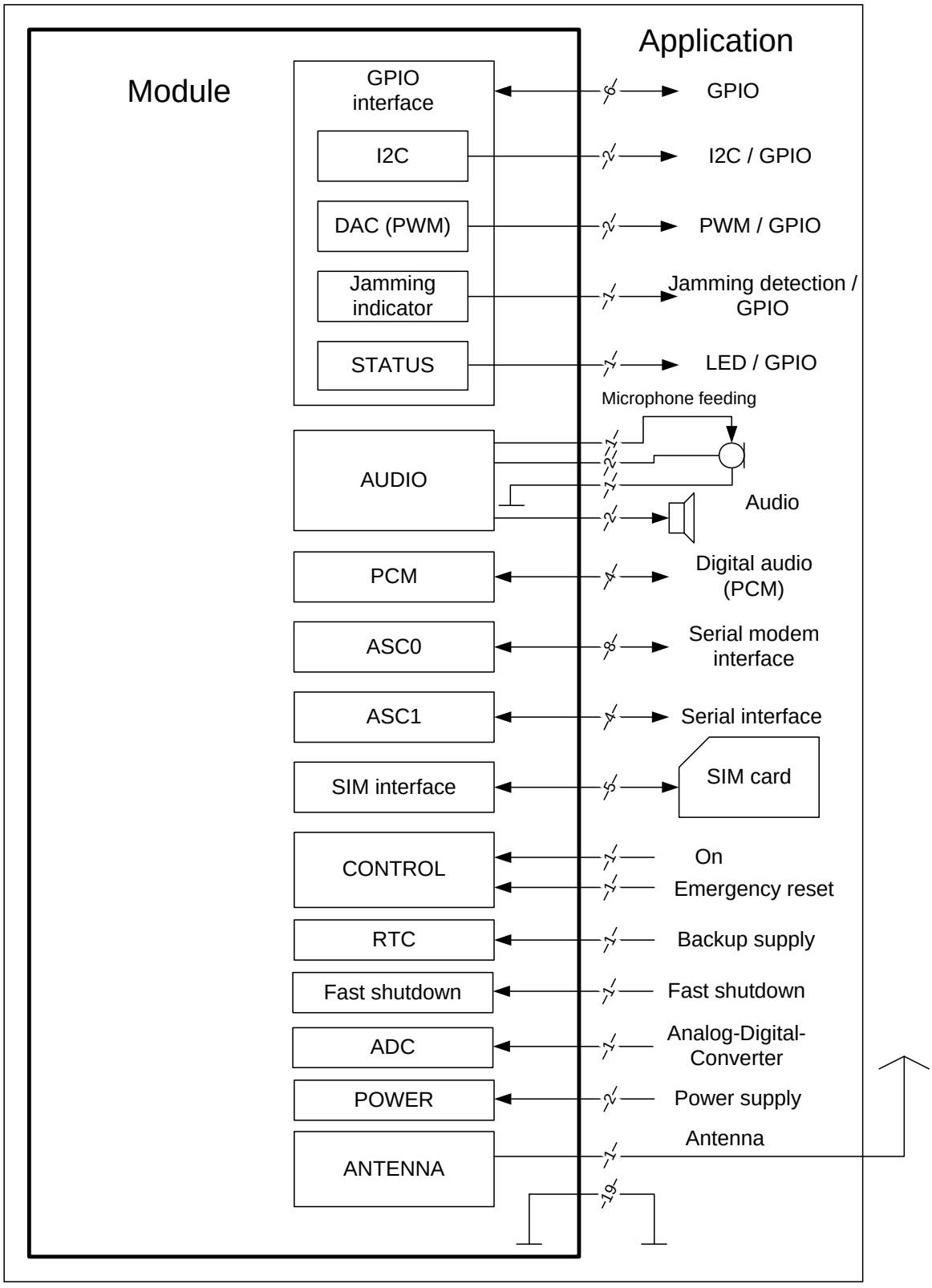


Figure 1: BGS2-E/BGS2-W system overview

2.3 Circuit Concept

Figure 2 shows a block diagram of the BGS2-E/BGS2-W module and illustrates the major functional components:

Baseband block:
- GSM baseband processor and power management
- Stacked flash/PSRAM memory
- Application interface (SMT with connecting pads)

GSM RF section:
- RF transceiver (part of baseband processor IC)
- RF power amplifier/front-end module inc. harmonics filtering
- Receive SAW filters

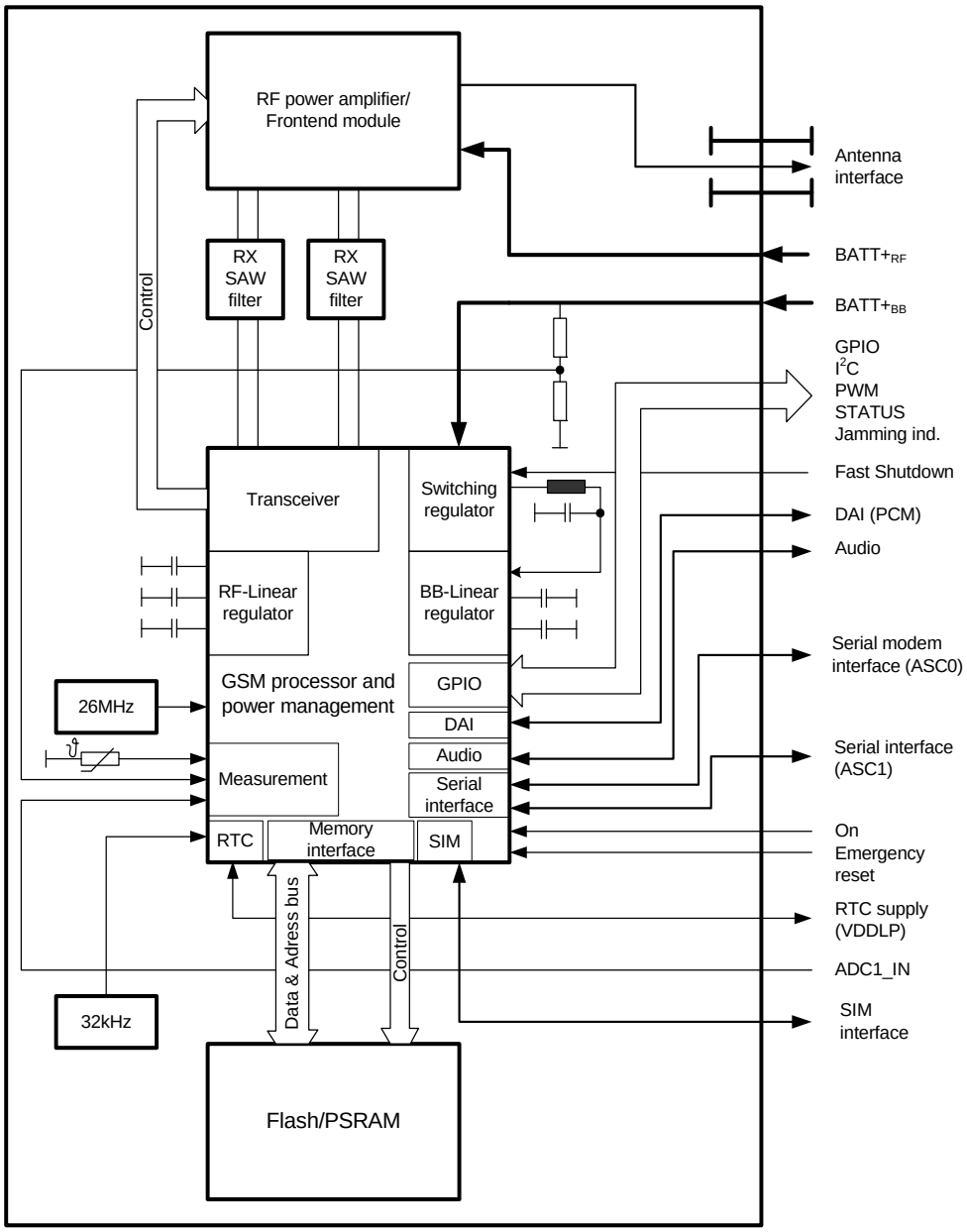


Figure 2: BGS2-E/BGS2-W block diagram

3 Application Interface

BGS2-E/BGS2-W is equipped with an SMT application interface that connects to the external application. The host interface incorporates several sub-interfaces described in the following sections:

- Power supply - see Section 3.2
- RTC backup – see Section 3.7
- SIM interface - see Section 3.8
- Serial interface ASC0 - see Section 3.9
- Serial interface ASC1 - see Section 3.10
- Analog audio interface - see Section 3.11
- Digital audio interface (PCM/I^2S) - see Section 3.12
- GPIO interface - see Section 3.13
- I^2C interface - Section 3.14
- PWM interfaces - Section 3.15
- Analog-to-digital converter - see Section 3.16
- Jamming indicator - Section 3.17
- Status Control - LED: Section 3.18, RING line: Section 3.19, Power indication: Section 3.20
- Fast shutdown - Section 3.21

3.1 Operating Modes

The table below briefly summarizes the various operating modes referred to in the following chapters.

Table 7: Overview of operating modes

Normal operation	GSM/GPRS SLEEP	Various power save modes set with AT+CFUN command. Software is active to minimum extent. If the module was registered to the GSM network in IDLE mode, it is registered and paging with the BTS in SLEEP mode, too. Power saving can be chosen at different levels: The NON-CYCLIC SLEEP mode (AT+CFUN=0) disables the AT interface. The CYCLIC SLEEP modes AT+CFUN=7 and 9 alternatingly activate and deactivate the AT interfaces to allow permanent access to all AT commands.
	GSM IDLE	Software is active. Once registered to the GSM network, paging with BTS is carried out. The module is ready to send and receive.
	GSM TALK	Connection between two subscribers is in progress. Power consumption depends on network coverage individual settings, such as DTX off/on, FR/EFR/HR, hopping sequences, antenna.
	GPRS IDLE	Module is ready for GPRS data transfer, but no data is currently sent or received. Power consumption depends on network settings and GPRS configuration (e.g. multislot settings).
	GPRS DATA	GPRS data transfer in progress. Power consumption depends on network settings (e.g. power control level), uplink/downlink data rates, GPRS configuration (e.g. used multislot settings) and reduction of maximum output power.
Power Down	Normal shutdown after sending the AT^SMSO command. Only a voltage regulator is active for powering the RTC. Software is not active. Interfaces are not accessible. Operating voltage (connected to BATT+) remains applied.	
Alarm mode	Restricted operation launched by RTC alert function while the module is in Power Down mode. Module will not be registered to GSM network. Limited number of AT commands is accessible.	

See the following sections for the various options of waking up BGS2-E/BGS2-W and proceeding from one mode to another.

3.2 Power Supply

BGS2-E/BGS2-W needs to be connected to a power supply at the SMT application interface - 2 lines BATT+, and GND. There are two separate voltage domains for BATT+:

- $BATT+_{BB}$ with a line for the general power management
- $BATT+_{RF}$ with a line for the GSM power amplifier supply

Please note that throughout the document BATT+ refers to both voltage domains and power supply lines - $BATT+_{BB}$ and $BATT+_{RF}$.

The power supply of BGS2-E/BGS2-W has to be a single voltage source at $BATT+_{BB}$ and $BATT+_{RF}$. It must be able to provide the peak current during the uplink transmission.

All the key functions for supplying power to the device are handled by the power management section of the analog controller. This IC provides the following features:

- Stabilizes the supply voltages for the GSM baseband using low drop linear voltage regulators and a DC-DC step down switching regulator.
- Switches the module's power voltages for the power-up and -down procedures.
- SIM switch to provide SIM power supply.

3.2.1 Minimizing Power Losses

When designing the power supply for your application please pay specific attention to power losses. Ensure that the input voltage V_{BATT+} never drops below 3.3V on the BGS2-E/BGS2-W board, not even in a GSM transmit burst where current consumption can rise (for peaks values see the power supply ratings listed in Section 5.5).

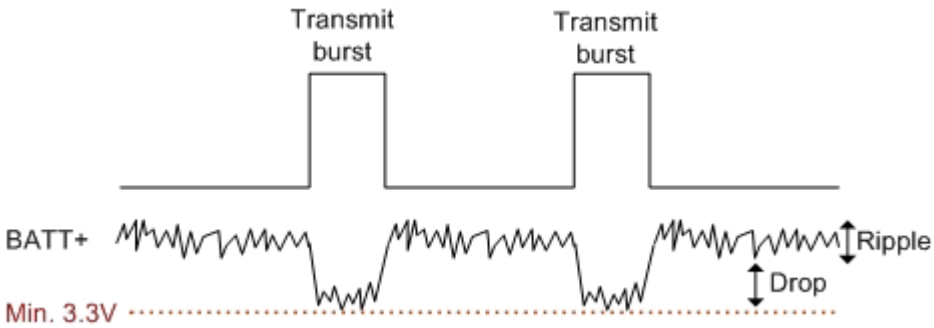


Figure 3: Power supply limits during transmit burst

3.2.2 Measuring the Supply Voltage (V_{BATT+})

To measure the supply voltage V_{BATT+} it is possible to define two reference points GND and BATT+. GND should be the module's shielding, while BATT+ should be a test pad on the external application the module is mounted on. The external BATT+ reference point has to be connected to and positioned close to the SMT application interface's BATT+ pads 5 ($BATT+_{BB}$) or 53 ($BATT+_{RF}$) as shown in Figure 4.

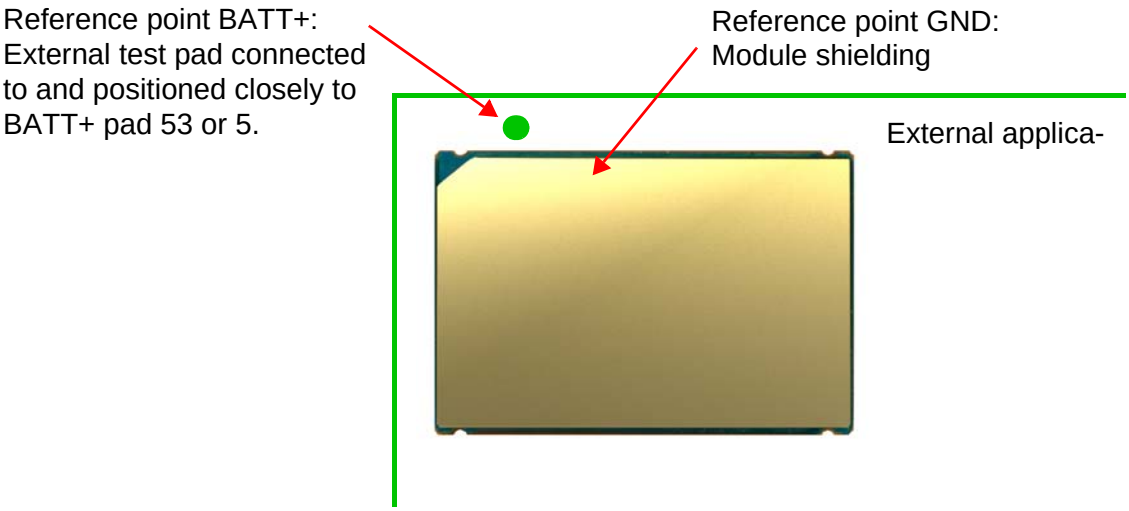


Figure 4: Position of reference points BATT+ and GND

3.2.3 Monitoring Power Supply by AT Command

To monitor the supply voltage you can also use the AT^SBV command which returns the value related to the reference points BATT+ and GND.

The module continuously measures the voltage at intervals depending on the operating mode of the RF interface. The duration of measuring ranges from 0.5 seconds in TALK/DATA mode to 50 seconds when BGS2-E/BGS2-W is in IDLE mode or Limited Service (deregistered). The displayed voltage (in mV) is averaged over the last measuring period before the AT^SBV command was executed.

If the measured average voltage drops below or rises above the specified voltage shutdown thresholds, the module will send an "^SBC" URC and shut down (for details see Section 3.3.5).

3.3 Power Up/Power Down Scenarios

In general, be sure not to turn on BGS2-E/BGS2-W while it is beyond the safety limits of voltage and temperature stated in Chapter 5. BGS2-E/BGS2-W would immediately switch off after having started and detected these inappropriate conditions. In extreme cases this can cause permanent damage to the module.

3.3.1 Turn on BGS2-E/BGS2-W

BGS2-E/BGS2-W can be started as described in the following sections:
- Hardware driven switch on by ON line: Starts Normal mode (see Section 3.3.1.1).
- Wake-up from Power Down mode by using RTC interrupt: Starts Alarm mode (see Section 3.3.1.3).

3.3.1.1 Switch on BGS2-E/BGS2-W Using ON Signal

When the operating voltage BATT+ is applied, BGS2-E/BGS2-W can be switched on by means of the ON signal.

If the operating voltage BATT+ is applied while the ON signal is present, BGS2-E/BGS2-W will be switched on automatically. Please note that if the rise time for the operating voltage BATT+ is longer than 12ms, the module startup will be delayed by about 1 second.

Please also note that if there is no ON signal present right after applying BATT+, BGS2-E/BGS2-W will instead of switching on perform a very short switch on/off sequence (approx. 120 milliseconds) that cannot be avoided.

The ON signal is a high active signal and only allows the input voltage level of the VDDLP signal. The following Figure 5 shows an example for a switch-on circuit (an alternative switch-on possibility is shown in Figure 63).

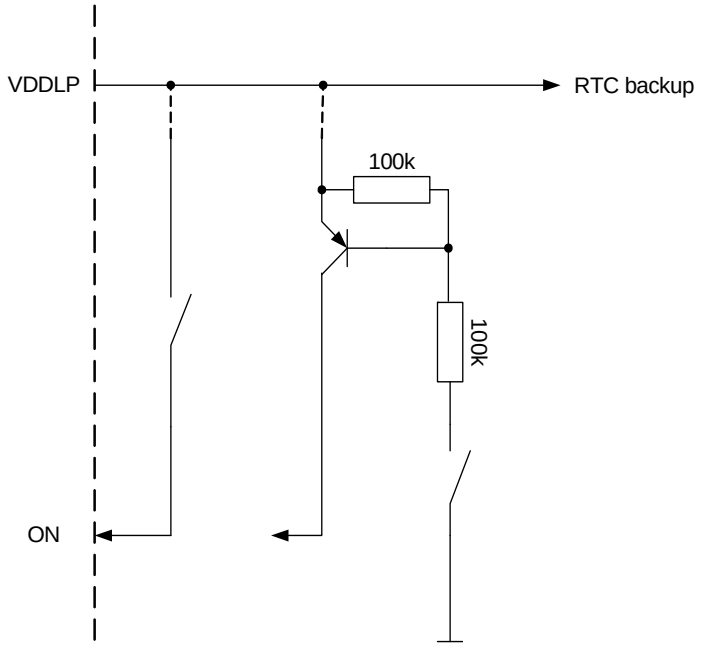


Figure 5: ON circuit sample

It is recommended to set a serial 1kΩ resistor between the ON circuit and the external capacitor or battery at the VDDLP power supply. This serial resistor protection is necessary in case the capacitor or battery has low power (is empty).

Please note that the ON signal is an edge triggered signal. This implies that a micro-second high pulse on the signal line suffices to almost immediately switch on the module, as shown in Figure 6. The following Section 3.3.1.2 describes a sample circuit that may be implemented to prevent possible spikes or glitches on the ON signal line from unintentionally switching on the module.

Please also note that if the state of the ON signal is coupled to the state of the VDDLP line or that if the ON signal otherwise remains active high after switch on, it is no longer possible to switch off BGS2-E/BGS2-W using the AT command AT^SMSO. Using this command will instead automatically restart the module.

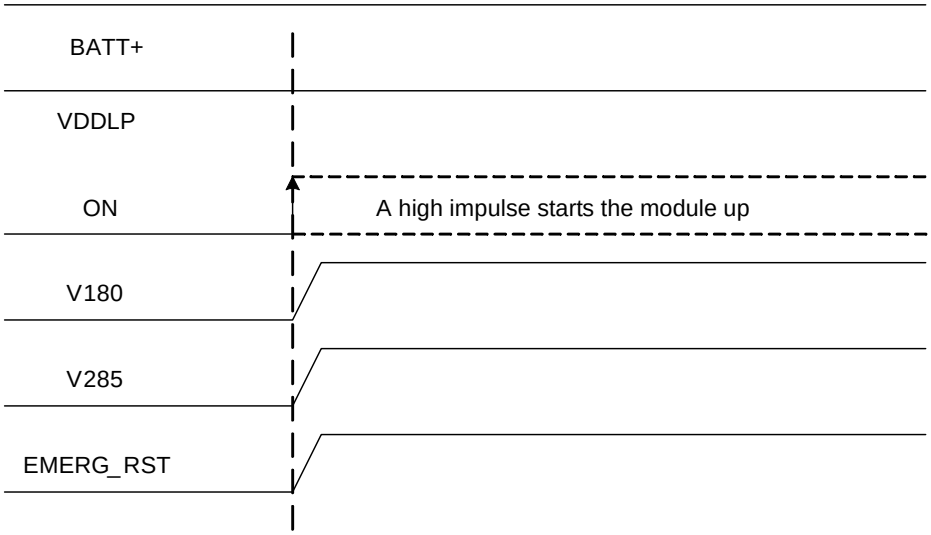


Figure 6: ON timing

If configured to a fixed bit rate (AT+IPR≠0), the module will send the URC "^SYSSTART" which notifies the host application that the first AT command can be sent to the module. The duration until this URC is output varies with the SIM card and may take a couple of seconds, particularly if the request for the SIM PIN is deactivated on the SIM card.

Please note that no "^SYSSTART" URC will be generated if autobauding (AT+IPR=0) is enabled.

To allow the application to detect the ready state of the module we recommend using hardware flow control which can be set with AT\Q (see [1] for details). The default setting is AT\Q0 (no flow control) which shall be altered to AT\Q3 (RTS/CTS handshake). If the application design does not integrate RTS/CTS lines the host application shall wait at least for the "^SYSSTART" URC. However, if the URC is not available (due to autobauding), you will simply have to wait for a period of time (at least 2 seconds) before assuming the module to be in ready state and before entering any data.

Please note that no data must be sent over the ASC0 interface before the interface is active and ready to receive data.

3.3.1.2 Suppressing Unintentional Pulses on ON Signal Line

Since the ON signal is edge triggered and a microsecond high pulse on the signal line suffices to almost immediately switch on the module, it might be necessary to implement a circuit on the external application that prevents possible spikes or glitches on the signal line from unintentionally switching on the module. Figure 7 shows an example for such a circuit.

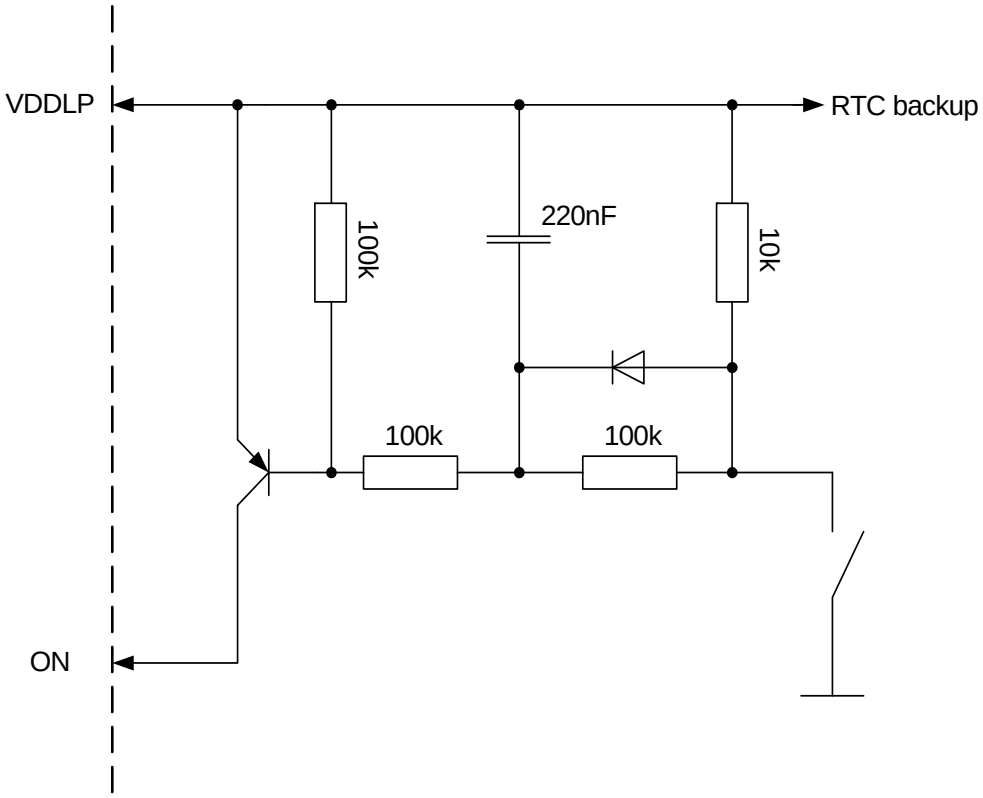


Figure 7: Sample circuit to suppress spikes or glitches on ON signal line

3.3.1.3 Turn on BGS2-E/BGS2-W Using the RTC (Alarm Mode)

Another power-on approach is to use the RTC, which is constantly supplied with power from a separate voltage regulator in the power supply processor. The RTC provides an alert function, which allows the BGS2-E/BGS2-W to wake up whilst the internal voltage regulators are off. This procedure only enables restricted operation, referred to as Alarm mode. It must not be confused with a reminder message that can be activated by using the same AT command, but without switching off power.

Use the AT+CALA command to set the alarm time. The RTC retains the alarm time if BGS2-E/BGS2-W was powered down by AT^SMSO. Once the alarm is timed out and executed, BGS2-E/BGS2-W enters Alarm mode. This is indicated by an Unsolicited Result Code (URC) which reads:

^SYSSTART ALARM MODE

Note that this URC is the only indication of the Alarm mode and will not appear when autobauding AT+IPR=0 was activated (due to the missing synchronization between DTE and DCE upon start-up). Therefore, it is recommended to select a fixed baudrate before using the Alarm mode.

In Alarm mode the module is deregistered from the GSM network and only a limited number of AT commands is available. For a table showing the availability of AT commands depending on the module‘s operating mode please refer to [1].

For the module to change from Alarm mode to full operation (normal operating mode) it is possible to use the AT+CFUN command or to switch on the module using the ON signal. The latter must be implemented in your host application as described in Section 3.3.1.1.

3.3.2 Restart BGS2-E/BGS2-W

After startup BGS2-E/BGS2-W can be re-started as described in the following sections:

- Software controlled reset by AT+CFUN command: Starts Normal mode (see Section 3.3.2.1).
- Hardware controlled reset by EMERG_RST line: Starts Normal mode (see Section 3.3.2.2)

3.3.2.1 Restart BGS2-E/BGS2-W via AT+CFUN Command

To reset and restart the BGS2-E/BGS2-W module use the command AT+CFUN. You can enter the command AT+CFUN=,1 or 1,1 or 7,1 or 9,1. See [1] for details.

If configured to a fix baud rate (AT+IPR≠0), the module will send the URC "^SYSSTART" to notify that it is ready to operate. If autobauding is enabled (AT+IPR=0) there will be no notification. To register to the network SIM PIN authentication is necessary after restart.

3.3.2.2 Restart BGS2-E/BGS2-W Using EMERG_RST

The EMERG_RST signal is internally connected to the central GSM processor. A low level for more than 10 milliseconds sets the processor and with it all the other signal pads to their respective reset state. The reset state is described in Section 3.3.3 as well as in the figures showing the startup behavior of an interface.

After releasing the EMERG-RST line, i.e., with a change of the signal level from low to high, the module restarts. The other signals continue from their reset state as if the module was switched on by the ON signal.

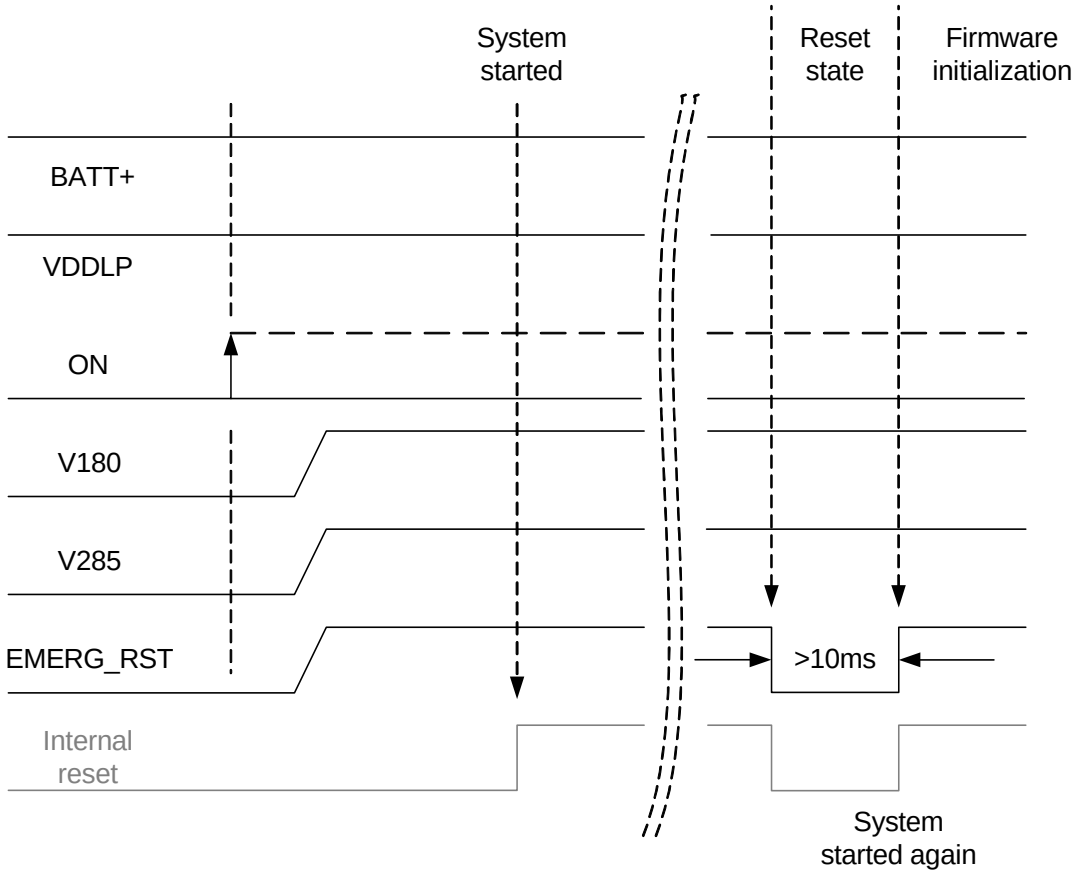


Figure 8: Emergency restart timing

It is recommended to control this EMERG_RST line with an open collector transistor or an open drain field-effect transistor.

Caution: Use the EMERG_RST line only when, due to serious problems, the software is not responding for more than 5 seconds. Pulling the EMERG_RST line causes the loss of all information stored in the volatile memory. Therefore, this procedure is intended only for use in case of emergency, e.g. if BGS2-E/BGS2-W does not respond, if reset or shutdown via AT command fails.

Note: Sometimes even pulling the EMERG_RST line may not suffice in restarting the module. In these cases the module will have to be reset using the power supply BATT+ lines. For more information on how to implement this feature see Section 3.3.4.2.

3.3.3 Signal States after Startup

Table 8 lists the states each interface signal passes through during reset and firmware initialization.

The reset state is reached with the rising edge of the EMERG_RST signal - either after a normal module startup (see Section 3.3.1.1) or after a reset (see Section 3.3.2.2). After the reset state has been reached the firmware initialization state begins. The firmware initialization is completed as soon as the ASC0 interface lines CTS0 and DSR0 as well as the ASC1 interface line CTS1 have turned low (see Section 3.9 and Section 3.10). Now, the module is ready to receive and transmit data.

Table 8: Signal states

Signal name	Reset state	Firmware initialization
CCIN	T / 100k PD	I / 100k PD
CCRST	L	O / L
CCIO	L	O / L
CCCLK	L	O / L
CCVCC	T / PU_B	O / L
RXD0	T / 2 x PU_A	O / H
TXD0	T / 2 x PU_A	I
CTS0	PD_B	O / H
RTS0	T / 10k PU	I / 10k PU
RING0	T / 10k PU	O / H, 10k PU
DTR0	T / PU_A	T / PU_A
DCD0	T / PU_A	T / PU_A
DSR0	T / PD_C	O / H
RXD1	T / PD_B	O / H
TXD1	T / PD_B	I
CTS1	T / PD_B	O / H
RTS1	T / PU_A	I / PU_A
FAST_SHTDWN	T / PU_A	T / PU_A
GPIO5 / LED	T / PU_A	T / PD_A
RXDDAI	T / PD_B	I / PD_B
SCLK	T / PU_B	O / H
TFSDAI	T / PD_B	O / L
TXDDAI	T / PD_B	O / L
GPIO6 / PWM2/Jamming Indicator	T / PU_B	T / PU_B
GPIO7 / PWM1	T / PU_B	T / PU_B
GPIO8	T / PU_B	T / PD_B
GPIO9 / I2CCLK	T / 5k PU / OD	T / 5k PU / OD
GPIO10 / I2CDAT	T / OD	T / OD

Abbreviations used in above Table 8:

L = Low level H = High level L/H = Low or high level T = Tristate I = Input O = Output	OD = Open Drain PD_A = Pull down, 103µA at 1.75V PD_B = Pull down, 51µA at 1.75V PD_C = Pull down, 27µA at 1.75V PU_A = Pull up -102µA at 0.05V PU_B = Pull up -55µA at 0.05V

3.3.4 Turn off BGS2-E/BGS2-W

To switch the module off the following procedures may be used:

- *Software controlled shutdown procedure*: Software controlled by sending the AT^SMSO command over the serial application interface. See Section 3.3.4.1.
- *Hardware controlled shutdown procedure*: Hardware controlled by disconnecting the module's power supply lines BATT+. See Section 3.3.4.2
- *Automatic shutdown (software controlled)*: See Section 3.3.5
  - Takes effect if under- or overvoltage is detected.
  - Takes effect if BGS2-E/BGS2-W board temperature exceeds a critical limit.
  - Takes effect if BGS2-E/BGS2-W's hardware watchdog triggers a shutdown notification
- *Fast shutdown (hardware line)*: See Section 3.21

3.3.4.1 Switch off BGS2-E/BGS2-W Using AT Command

The best and safest approach to powering down BGS2-E/BGS2-W is to issue the *AT^SMSO* command. This procedure lets BGS2-E/BGS2-W log off from the network and allows the software to enter into a secure state and safe data before disconnecting the power supply. The mode is referred to as Power Down mode. In this mode, only the RTC stays active.

Before switching off the device sends the following response:

```
^SMSO: MS OFF

OK
^SHUTDOWN
```

After sending AT^SMSO do not enter any other AT commands. There are two ways to verify when the module turns off:

- Wait for the URC "^SHUTDOWN". It indicates that data have been stored non-volatile and the module turns off in less than 1 second.
- Also, you can monitor the V180/V285 pads. The low state of these pads indicates that the module is switched off.

Be sure not to disconnect the operating voltage V_{BATT+} before the URC "^SHUTDOWN" has been issued and the V180/V285 pads have gone low. Otherwise you run the risk of losing data.

While BGS2-E/BGS2-W is in Power Down mode the application interface is switched off and must not be fed from any other voltage source. Therefore, your application must be designed to avoid any current flow into any digital pads of the application interface.

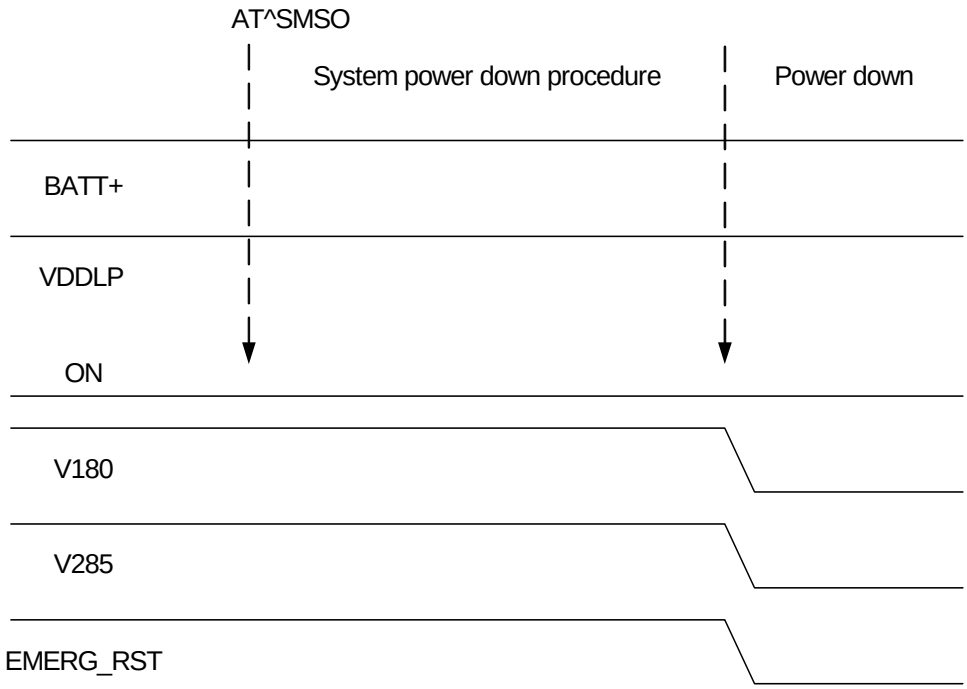


Figure 9: Switch off behavior

3.3.4.2 Disconnect BGS2-E/BGS2-W BATT+ Lines

Figure 10 shows an external application circuit that provides the possibility to temporarily (>100 milliseconds) disconnect the module's BATT+ lines from the external application's power supply. The mentioned MOSFET transistor (T8) should have an R_{DS_ON} value ≤ 50mΩ in order to minimize voltage drops. Such a circuit could be useful to maximize power savings for battery driven applications or to completely switch off and restart the module after a firmware update.

Afterwards the module can be restarted using the ON signal as described in Section 3.3.1.1.

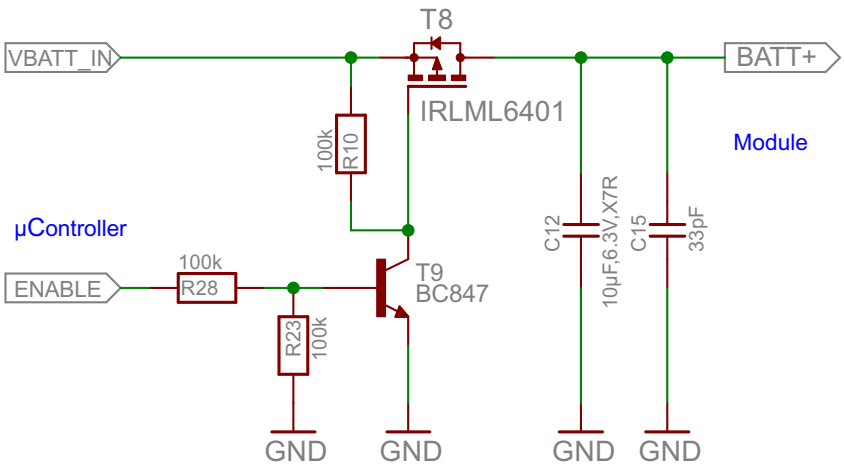


Figure 10: Restart circuit using BATT+ line

3.3.5 Automatic Shutdown

Automatic shutdown takes effect if any of the following events occurs:
- The BGS2-E/BGS2-W board is exceeding the critical limits of overtemperature or undertemperature (see Section 3.3.5.1 and Section 3.3.5.2)
- Undervoltage or overvoltage is detected (see Section 3.3.5.3 and Section 3.3.5.4)
- the internal BGS2-E/BGS2-W hardware watchdog registers a shutdown notification (see Section 3.3.5.5)

The automatic shutdown procedure is equivalent to the power-down initiated with the AT^SMSO command, i.e. BGS2-E/BGS2-W logs off from the network and the software enters a secure state avoiding loss of data.

3.3.5.1 Thermal Shutdown

The board temperature is constantly monitored by an internal NTC resistor located on the PCB. The values detected by the NTC resistor are measured directly on the board and therefore, are not fully identical with the ambient temperature.

Each time the board temperature goes out of range or back to normal, BGS2-E/BGS2-W instantly displays an alert (if enabled).
- URCs indicating the level "1" or "-1" allow the user to take appropriate precautions, such as protecting the module from exposure to extreme conditions. The presentation of the URCs depends on the settings selected with the AT^SCTM write command (for details see [1]):
  AT^SCTM=1: Presentation of URCs is always enabled.
  AT^SCTM=0 (default): Presentation of URCs is enabled during the 2 minute guard period after start-up of BGS2-E/BGS2-W. After expiry of the 2 minute guard period, the presentation will be disabled, i.e. no URCs with alert levels "1" or "-1" will be generated.
- URCs indicating the level "2" or "-2" are instantly followed by an orderly shutdown, except in cases described in Section 3.3.5.2. The presentation of these URCs is always enabled, i.e. they will be output even though the factory setting AT^SCTM=0 was never changed.

The maximum temperature ratings are stated in Section 5.2. Refer to Table 9 for the associated URCs.

Table 9: Temperature dependent behavior

Sending temperature alert (2min after BGS2-E/BGS2-W startup, otherwise only if URC presentation enabled)	
^SCTM_B: 1	Board close to overtemperature limit.
^SCTM_B: -1	Board close to undertemperature limit.
^SCTM_B: 0	Board back to non-critical temperature range.
Automatic shutdown (URC appears no matter whether or not presentation was enabled)	
^SCTM_B: 2	Alert: Board equal or beyond overtemperature limit. BGS2-E/BGS2-W switches off.
^SCTM_B: -2	Alert: Board equal or below undertemperature limit. BGS2-E/BGS2-W switches off.

3.3.5.2 Deferred Shutdown at Extreme Temperature Conditions

In the following cases, automatic shutdown will be deferred if a critical temperature limit is exceeded:

- While an emergency call is in progress.
- During a two minute guard period after power-up. This guard period has been introduced in order to allow for the user to make an emergency call. The start of any one of these calls extends the guard period until the end of the call. Any other network activity may be terminated by shutdown upon expiry of the guard time.

While in a "deferred shutdown" situation, BGS2-E/BGS2-W continues to measure the temperature and
to deliver alert messages, but deactivates the shutdown functionality. Once the 2 minute guard period is expired or the call is terminated, full temperature control will be resumed. If the temperature is still out of range, BGS2-E/BGS2-W switches off immediately (without another alert message).

CAUTION! Automatic shutdown is a safety feature intended to prevent damage to the module. Extended usage of the deferred shutdown facilities provided may result in damage to the module, and possibly other severe consequences.

3.3.5.3 Undervoltage Shutdown

The undervoltage shutdown threshold is 3.25V, i.e., it is 50mV below the specified minimum supply voltage V_{BATT+} given in Table 26.

When the average supply voltage measured by BGS2-E/BGS2-W drops below the undervoltage shutdown threshold the module will send the following URC:

^SBC: Undervoltage

This alert is sent only once before the module shuts down cleanly without sending any further messages.

This type of URC does not need to be activated by the user. It will be output automatically when fault conditions occur.

3.3.5.4 Overvoltage Shutdown

The overvoltage shutdown threshold is 4.6V, i.e., it is 100mV above the specified maximum supply voltage V_{BATT+} given in Table 26.

When the average supply voltage measured by BGS2-E/BGS2-W rises above the overvoltage shutdown threshold the module will send the following URC:

^SBC: Overvoltage

This alert is sent only once before the module shuts down cleanly without sending any further messages.

This type of URC does not need to be activated by the user. It will be output automatically when fault conditions occur.

Keep in mind that several BGS2-E/BGS2-W components are directly linked to BATT+ and, therefore, the supply voltage remains applied at major parts of BGS2-E/BGS2-W. Especially the power amplifier linked to $BATT+_{RF}$ is very sensitive to high voltage and might even be destroyed.

3.3.5.5 Hardware Watchdog

The BGS2-E/BGS2-W chipset features a built-in hardware watchdog. The watchdog is activated automatically after module power up during the firmware initialization phase. In case the watchdog will not be reset within 2.5 seconds, the module will send a shutdown notification on its serial interface and will shut down itself. The module's firmware is designed in such a way that all the main tasks register to the reset procedure of the watchdog. If one of these tasks is not responding, the module will be shutdown.

It is recommended to design an external application in such a way that if the module is powered on, the ignition line is permanently active. If the module then shuts off, it will be restarted automatically because of the active ignition line. On the other hand, the external application will have to take into account that if the module is meant to be powered off, the ignition line must be deactivated.

3.4 Automatic GPRS Multislot Class Change

Please note that automatic GPRS multislot class change applies only for the quad band module variant BGS2-W:

For operation in GPRS Multislot Class 10, temperature control is effective. If the board temperature increases up to 80°C while data is transmitted over GPRS, the module automatically reverts from GPRS Multislot Class 10 (2Tx) to Class 8 (1Tx). This reduces the power consumption and, consequently, causes the board's temperature to decrease. Once the temperature drops to 75°C, BGS2-W returns to the higher Multislot Class. If the temperature stays at the critical level or even continues to rise, BGS2-W will not switch back to the higher class.

After a transition from Multislot Class 10 to Multislot 8 a possible switchback to Multislot Class 10 is blocked for one minute.

Please note that there is not one single cause of switching over to a lower GPRS Multislot Class. Rather it is the result of an interaction of several factors, such as the board temperature that depends largely on the ambient temperature, the operating mode and the transmit power. Furthermore, take into account that there is a delay until the network proceeds to a lower or, accordingly, higher Multislot Class. The delay time is network dependent. In extreme cases, if it takes too much time for the network and the temperature cannot drop due to this delay, the module may even switch off as described in Section 3.3.4.

For BGS2-W general temperature limits please refer Section 5.2.

3.5 Power Saving

SLEEP mode reduces the functionality of the BGS2-E/BGS2-W module to a minimum and, thus, minimizes the current consumption to the lowest level. Settings can be made using the AT+CFUN command. For details see below and [1]. SLEEP mode falls into two categories:

- NON-CYCLIC SLEEP mode AT+CFUN=0
- CYCLIC SLEEP modes, selectable with AT+CFUN=7 or 9.

IMPORTANT: Please keep in mind that power saving works properly only when PIN authentication has been done. If you attempt to activate power saving while the SIM card is not inserted or the PIN not correctly entered (Limited Service), the selected <fun> level will be set, though power saving does not take effect. For the same reason, power saving cannot be used if BGS2-E/BGS2-W operates in Alarm mode.

To check whether power saving is on, you can query the status of AT+CFUN if you have chosen CYCLIC SLEEP mode.

The wake-up procedures are quite different depending on the selected SLEEP mode. Table 10 compares the wake-up events that can occur in NON-CYCLIC and CYCLIC SLEEP modes.

3.5.1 No Power Saving (AT+CFUN=1)

The functionality level <fun>=1 is where power saving is switched off. This is the default after startup.

3.5.2 NON-CYCLIC SLEEP Mode (AT+CFUN=0)

If level 0 has been selected (AT+CFUN=0), the serial interface is blocked. The module shortly deactivates power saving to listen to a paging message sent from the base station and then immediately resumes power saving. Level 0 is called NON-CYCLIC SLEEP mode, since the serial interface is not alternately made accessible as in CYCLIC SLEEP mode.

The first wake-up event fully activates the module, enables the serial interface and terminates the power saving mode. In short, it takes BGS2-E/BGS2-W back to the highest level of functionality <fun>=1.

In NON-CYCLIC mode, the falling edge of the RTS0 or RTS1 lines wakes up the module to <fun>=1. To efficiently use this feature it is recommended to enable hardware flow control (RTS/CTS handshake) as in this case the CTS line notifies the application when the module is ready to send or receive characters. See Section 3.5.6.1 for details.

3.5.3 CYCLIC SLEEP Mode AT+CFUN=7

The functionality level AT+CFUN=7 is referred to as CYCLIC SLEEP modes. The major benefit of all CYCLIC SLEEP modes is that the serial interface remains accessible, and that, in intermittent wake-up periods, characters can be sent or received without terminating the selected mode.

The CYCLIC SLEEP modes give you greater flexibility regarding the wake-up procedures: For example, in all CYCLIC SLEEP modes, you can enter AT+CFUN=1 to permanently wake up the module. In mode CFUN=7, BGS2-E/BGS2-W automatically resumes power saving, after you have sent or received a short message, or made a call or completed a GPRS transfer. Please refer to Table 10 for a summary of all modes.

The CYCLIC SLEEP mode is a dynamic process which alternately enables and disables the serial interface. By setting/resetting the CTS signal, the module indicates to the application whether or not the UART is active. The timing of CTS is described below.

Both the application and the module must be configured to use hardware flow control (RTS/CTS handshake). The default setting of BGS2-E/BGS2-W is AT\Q0 (no flow control) which must be altered to AT\Q3. See [1] for details.

Note: If both serial interfaces ASC0 and ASC1 are connected, both are synchronized. This means that SLEEP mode takes effect on both, no matter on which interface the AT command was issued. Although not explicitly stated, all explanations given in this section refer equally to ASC0 and ASC1, and accordingly to CTS0 and CTS1.

3.5.4 CYCLIC SLEEP Mode AT+CFUN=9

Mode AT+CFUN=9 is similar to AT+CFUN=7, but provides two additional features:

- The time the module stays active after RTS was asserted or after the last character was sent or received, can be configured individually using the command AT^SCFG. Default setting is 2 seconds like in AT+CFUN=7. The entire range is from 0.5 seconds to 1 hour, selectable in tenths of seconds. For details see [1].
- RTS0 and RTS1 are not only used for flow control (as in mode AT+CFUN=7), but also cause the module to wake up temporarily. See Section 3.5.6.1 for details.

3.5.5 Timing of the CTS Signal in CYCLIC SLEEP Modes

The CTS signal is enabled in synchrony with the module's paging cycle. It goes active low each time when the module starts listening to a paging message block from the base station. The timing of the paging cycle varies with the base station. The duration of a paging interval can be calculated from the following formula:
*4.616 ms (TDMA frame duration) * 51 (number of frames) * DRX value*.

DRX (Discontinuous Reception) is a value from 2 to 9, resulting in paging intervals from 0.47 to 2.12 seconds. The DRX value of the base station is assigned by the network operator.

Each listening period causes the CTS signal to go active low: If DRX is 2, the CTS signal is activated every 0.47 seconds, if DRX is 3, the CTS signal is activated every 0.71 seconds and if DRX is 9, the CTS signal is activated every 2.1 seconds.

The CTS signal is active low for 4.6 ms. This is followed by another 4.6 ms UART activity. If the start bit of a received character is detected within these 9.2 ms, CTS will be activated and the proper reception of the character will be guaranteed. CTS will also be activated if any character is to be sent.

After the last character was sent or received the interface will remain active for

- another 2 seconds, if AT+CFUN=7
- or for an individual time defined with AT^SCFG, if AT+CFUN=9. Assertion of RTS has the same effect.

In the pauses between listening to paging messages, while CTS is high, the module resumes power saving and the AT interface is not accessible. See Figure 11 and Figure 12.

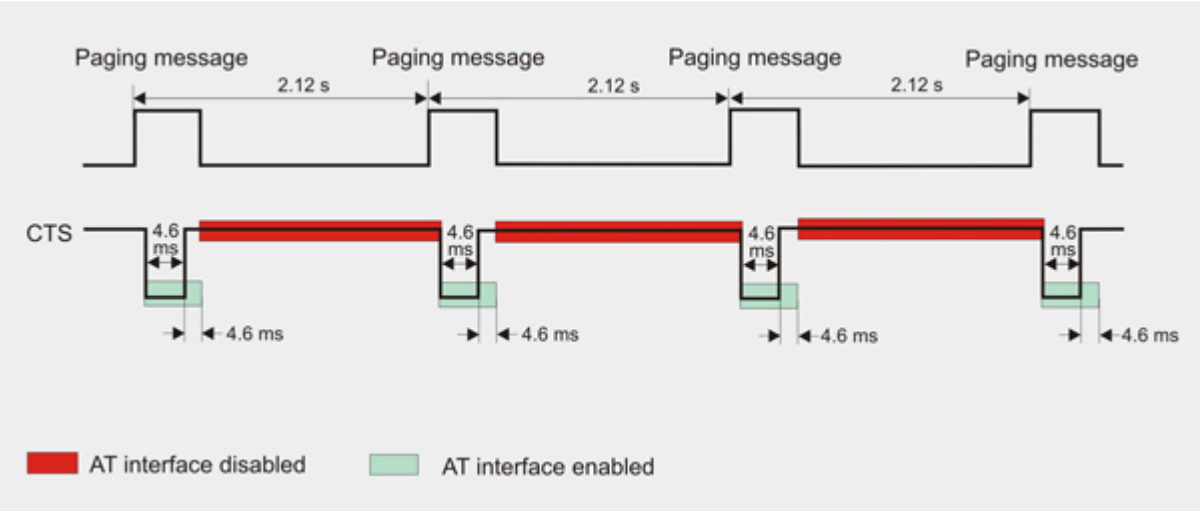


Figure 11: Timing of CTS signal (example for a 2.12 s paging cycle)

Figure 12 illustrates the CFUN=7 modes, which reset the CTS signal 2 seconds after the last character was sent or received.

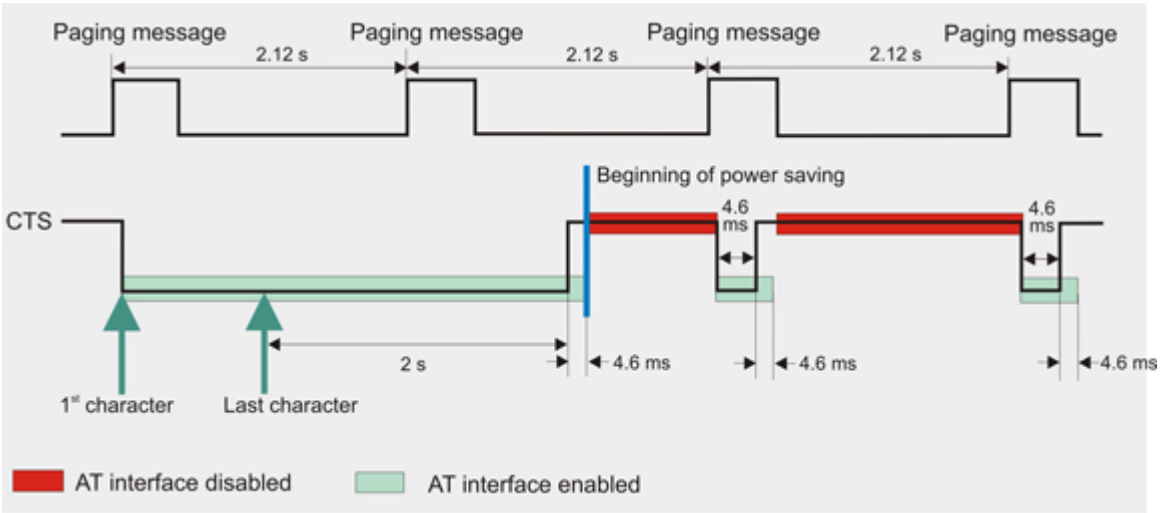


Figure 12: Beginning of power saving if CFUN=7

3.5.6 Wake up BGS2-E/BGS2-W from SLEEP Mode

A wake-up event is any event that causes the module to draw current. Depending on the selected mode the wake-up event either switches SLEEP mode off and takes BGS2-E/BGS2-W back to AT+CFUN=1, or activates BGS2-E/BGS2-W temporarily without leaving the current SLEEP mode.

Definitions of the state transitions described in Table 10:

Quit = BGS2-E/BGS2-W exits SLEEP mode and returns to AT+CFUN=1.

Temporary = BGS2-E/BGS2-W becomes active temporarily for the duration of the event and the mode specific follow-up time after the last character was sent or received on the serial interface.

No effect = Event is not relevant in the selected SLEEP mode. BGS2-E/BGS2-W does not wake up.

Table 10: Wake-up events in NON-CYCLIC and CYCLIC SLEEP modes

Event	Selected mode AT+CFUN=0	Selected mode AT+CFUN=7 or 9
Ignition line	No effect	No effect
RTS0 or RTS1[1)] (falling edge)	Quit + flow control	Mode 7: No effect, RTS is only used for flow control Mode 9: Temporary + flow control
Unsolicited Result Code (URC)	Quit	Temporary
Incoming voice or data call	Quit	Temporary
Any AT command (incl. outgoing voice or data call, outgoing SMS)	Not possible (UART disabled)	Temporary
Incoming SMS depending on mode selected by AT+CNMI: AT+CNMI=0,0 (= default, no indication of received SMS) AT+CNMI=1,1 (= displays URC upon receipt of SMS)	No effect Quit	No effect Temporary
GPRS data transfer	Not possible (UART disabled)	Temporary
RTC alarm[2]	Quit	Temporary
AT+CFUN=1	Not possible (UART disabled)	Quit

1. See Section 3.5.6.1 on wake-up via RTS.
2. Recommendation: In NON-CYCLIC SLEEP mode, you can set an RTC alarm to wake up BGS2-E/BGS2-W and return to full functionality. This is a useful approach because, in this mode, the AT interface is not accessible.

3.5.6.1 Wake-up via RTS0 and RTS1 (if AT+CFUN=0 or AT+CFUN=9)

During the CYCLIC SLEEP mode 7, the RTS0 and RTS1 lines are conventionally used for flow control: The assertion of RTS0 or RTS1 indicates that the application is ready to receive data - without waking up the module.

If the module is in CFUN=0 mode, the assertion of RTS0 and RTS1 (i.e., toggle from inactive high to active low) serves as a wake-up event, giving the application the possibility to intentionally terminate power saving. If the module is in CFUN=9 mode, the assertion of RTS0 or RTS1 can be used to temporarily wake up BGS2-E/BGS2-W for the time specified with the AT^SCFG command (default = 2 seconds). In both cases, if RTS0 or RTS1 is asserted while AT+CFUN=0 or AT+CFUN=9 is set, there may be a short delay until the module is able to receive data again. This delay depends on the current module activities (e.g. paging cycle) and may be up to 60 milliseconds. The ability to receive data is signalized by CTS0 and CTS1. It is therefore recommended to enable RTS/CTS flow control, not only in CYCLIC SLEEP mode, but also in NON-CYCLIC SLEEP mode.

3.6 Summary of State Transitions (except SLEEP Mode)

The table shows how to proceed from one mode to another (grey column = present mode, white columns = intended modes)

Table 11: State transitions of BGS2-E/BGS2-W (except SLEEP mode)

Further mode →→ Present mode	**Power Down**	**Normal mode**	**Alarm mode**
Power Down mode	---	ON >10ms at VDDLP level	Wake-up from Power Down mode (if activated with AT+CALA)
Normal mode	AT^SMSO	EMERG_RST > 10ms	AT+CALA followed by AT^SMSO. BGS2-E/ BGS2-W enters Alarm mode when specified time is reached.
Alarm mode	AT^SMSO	AT+CFUN=x,1 or ON >10ms at VDDLP level	---

3.7 RTC Backup

The internal Real Time Clock of BGS2-E/BGS2-W is supplied from a separate voltage regulator in the power supply component which is also active when BGS2-E/BGS2-W is in Power Down mode and BATT+ is available. An alarm function is provided that allows to wake up BGS2-E/BGS2-W without logging on to the GSM network.

In addition, you can use the VDDLP pad to backup the RTC from an external capacitor. The capacitor is charged from the internal LDO of BGS2-E/BGS2-W. If the voltage supply at BATT+ is disconnected the RTC can be powered by the capacitor. The size of the capacitor determines the duration of buffering when no voltage is applied to BGS2-E/BGS2-W, i.e. the greater the capacitor the longer BGS2-E/BGS2-W will save the date and time. The RTC can also be supplied from an external battery (rechargeable or non-chargeable). In this case the electrical specification of the VDDLP pad (see Section 5.4) has to be taken in to account.

Figure 13 shows an RTC backup configuration.

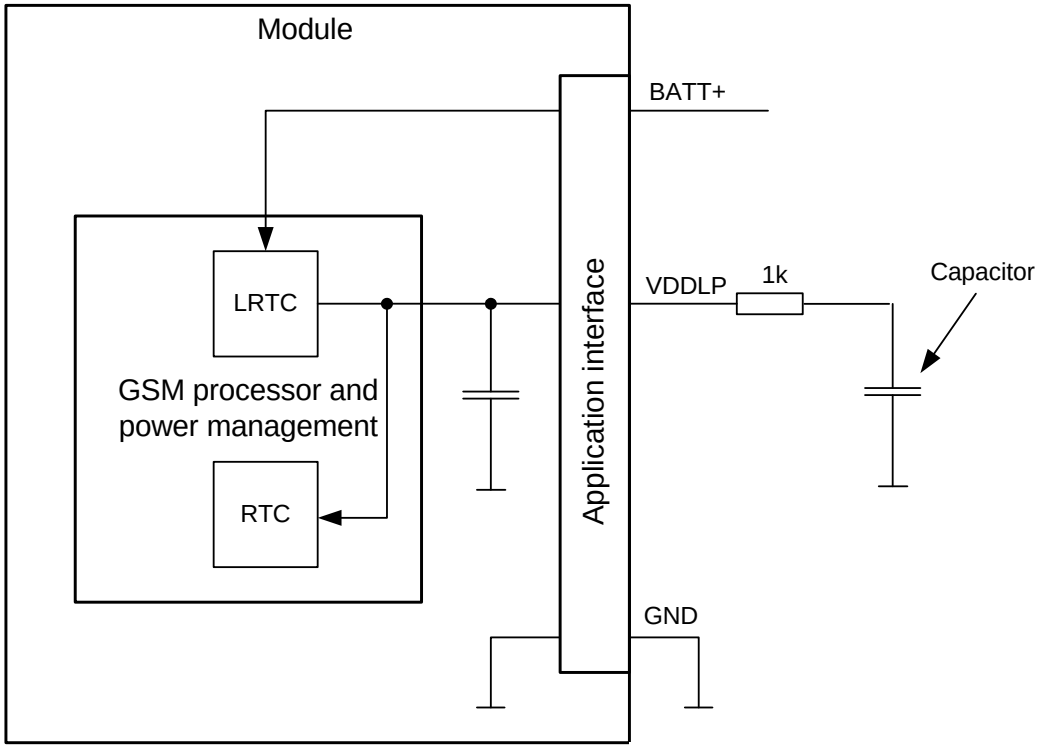


Figure 13: RTC supply variants

3.8 SIM Interface

The baseband processor has an integrated SIM card interface compatible with the ISO/IEC 7816 IC Card standard. This is wired to the host interface in order to be connected to an external SIM card holder. Five pads are reserved for the SIM interface. BGS2-E/BGS2-W supports and automatically detects 3.0V as well as 1.8V SIM cards.

The CCIN pad serves to detect whether a tray is present in the card holder. Using the CCIN pad is mandatory for compliance with the 3GPP TS 11.11 (Rel.99) recommendation if the mechanical design of the host application allows the user to remove the SIM card during operation.

Table 12: Signals of the SIM interface (SMT application interface)

Signal	Description
CCCLK	Chipcard clock, various clock rates can be set in the baseband processor.
CCVCC	SIM supply voltage from PSU-ASIC
CCIO	Serial data line, input and output.
CCRST	Chipcard reset, provided by baseband processor
CCIN	Input on the baseband processor for detecting a SIM card tray in the holder.The default level of CCIN is low (internal pull down resistor, no card inserted). It will change to high level when the card is inserted. To take advantage of this feature, an appropriate contact is required on the cardholder. Ensure that the cardholder on your application platform is wired to output a high signal when the SIM card is present. The CCIN pad is mandatory for applications that allow the user to remove the SIM card during operation. The CCIN pad is solely intended for use with a SIM card. It must not be used for any other purposes. Failure to comply with this requirement may invalidate the type approval of BGS2-E/BGS2-W.

The figure below shows a circuit to connect an external SIM card holder.

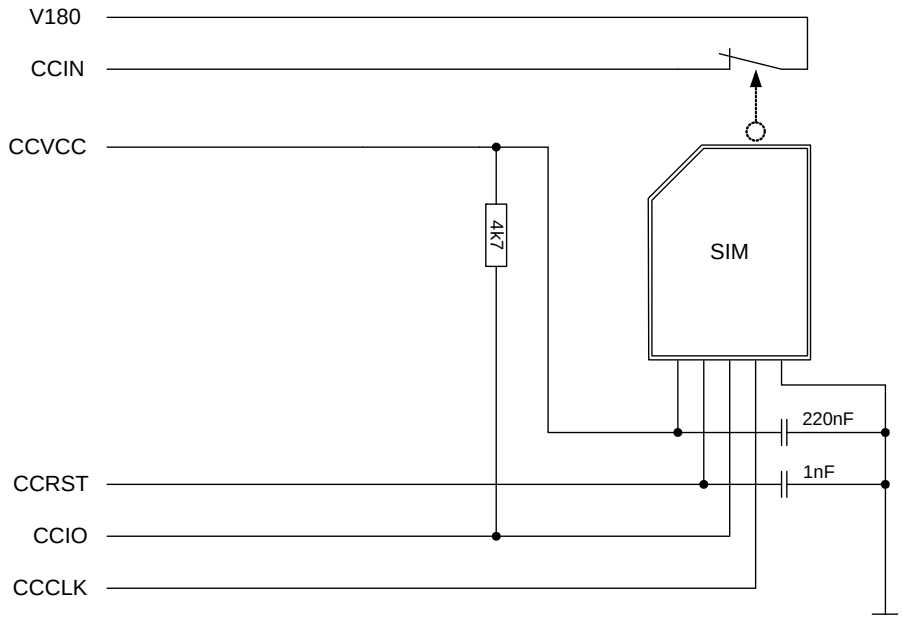


Figure 14: External SIM card holder circuit

It is recommended that the total cable length between SMT application interface pads on BGS2-E/BGS2-W and the connector of the external SIM card holder must not exceed 100mm in order to meet the specifications of 3GPP TS 51.010-1 and to satisfy the requirements of EMC compliance.

To avoid possible cross-talk from the CCCLK signal to the CCIO signal be careful that both lines are not placed closely next to each other. A useful approach would be to use a separate SIM card ground connection to shield the CCIO line from the CCCLK line. A GND line may be employed for such a case.

Notes: No guarantee can be given, nor any liability accepted, if loss of data is encountered after removing the SIM card during operation.
Also, no guarantee can be given for properly initializing any SIM card that the user inserts after having removed a SIM card during operation. In this case, the application must restart BGS2-E/BGS2-W.
If using a SIM card holder without detecting contact please be sure to switch off the module before removing the SIM Card or inserting a new one.

3.9 Serial Interface ASC0

BGS2-E/BGS2-W offers an 8-wire unbalanced, asynchronous modem interface ASC0 conforming to ITU-T V.24 protocol DCE signaling. The electrical characteristics do not comply with ITU-T V.28. The voltage level of the ASC0 interface can be configured to either 1.8V or 2.85/1.8V:

- If the VDIG signal (i.e., application interface pad 10) is connected to the V180 line (i.e., application interface pad 35) the ASC0 interface starts up with a 1.8V signal level. All lines of the ASC0 will be on the 1.8V signal level.
- If the VDIG signal (i.e., application interface pad 10) is connected to the V285 line (i.e., application interface pad 22), the ASC0 interface runs with a 2.85V and a 1.8V signal level. With this configuration the lines TXD0, RXD0, CTS0, RTS0, RING0 will be on the 2.85V, the lines DTR0, DSR0 and DCD0 on the 1.8V signal level.

As the V285 voltage level is not supported by Gemalto M2M 3G modules, it is recommended to use the 1.8V signal level configuration in case a migration to these modules is intended.

The voltage level configuration of the ASC0 interface also has an impact on the PCM and I^2C interfaces as well as on GPIO9/10. PCM, I^2C and GPIO9/10 are also in the power supply domain configured by the VDIG signal (see Section 3.12, Section 3.13, Section 3.14).

For electrical characteristics of the interface signals please refer to Section 5.4.

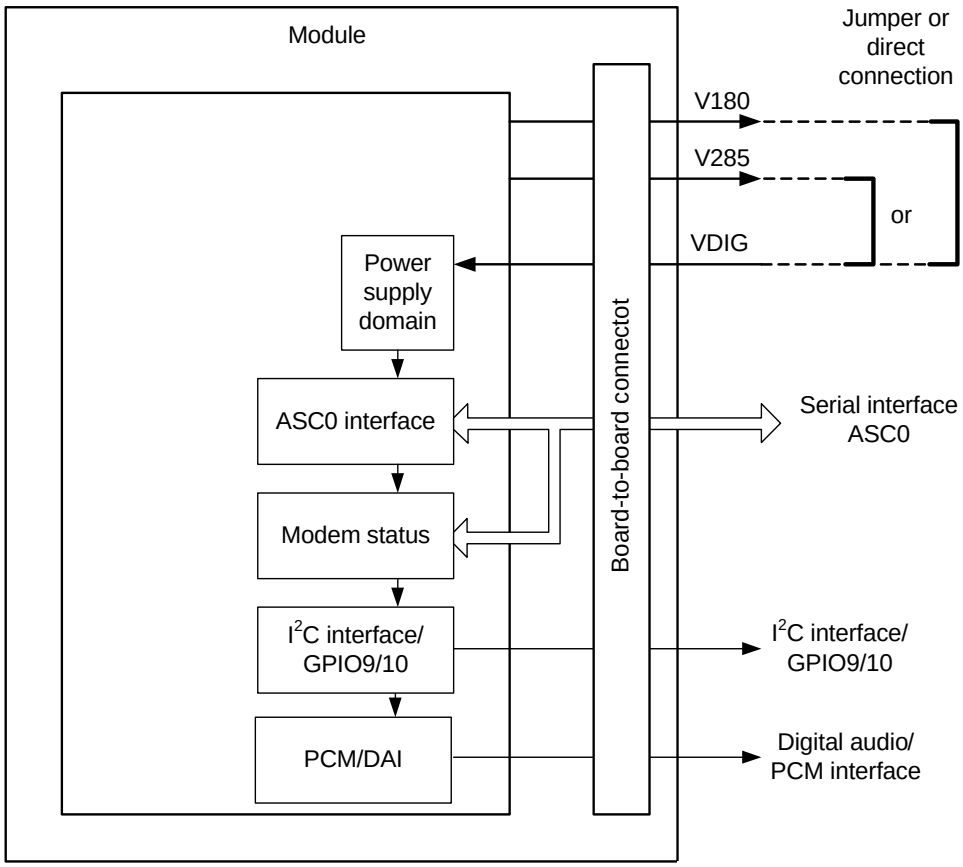


Figure 15: VDIG controlled power supply domain

BGS2-E/BGS2-W is designed for use as a DCE. Based on the conventions for DCE-DTE connections it communicates with the customer application (DTE) using the following signals:

- Port TXD @ application sends data to the module's TXD0 signal line
- Port RXD @ application receives data from the module's RXD0 signal line

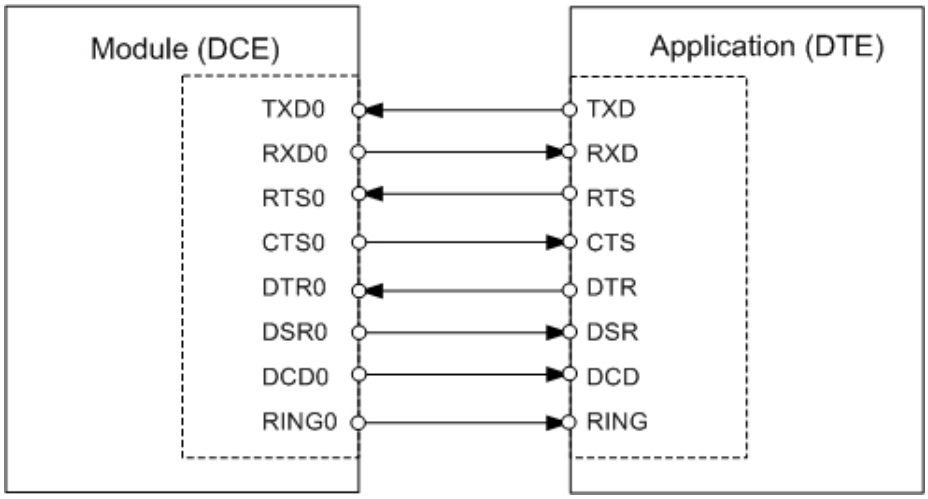


Figure 16: Serial interface ASC0

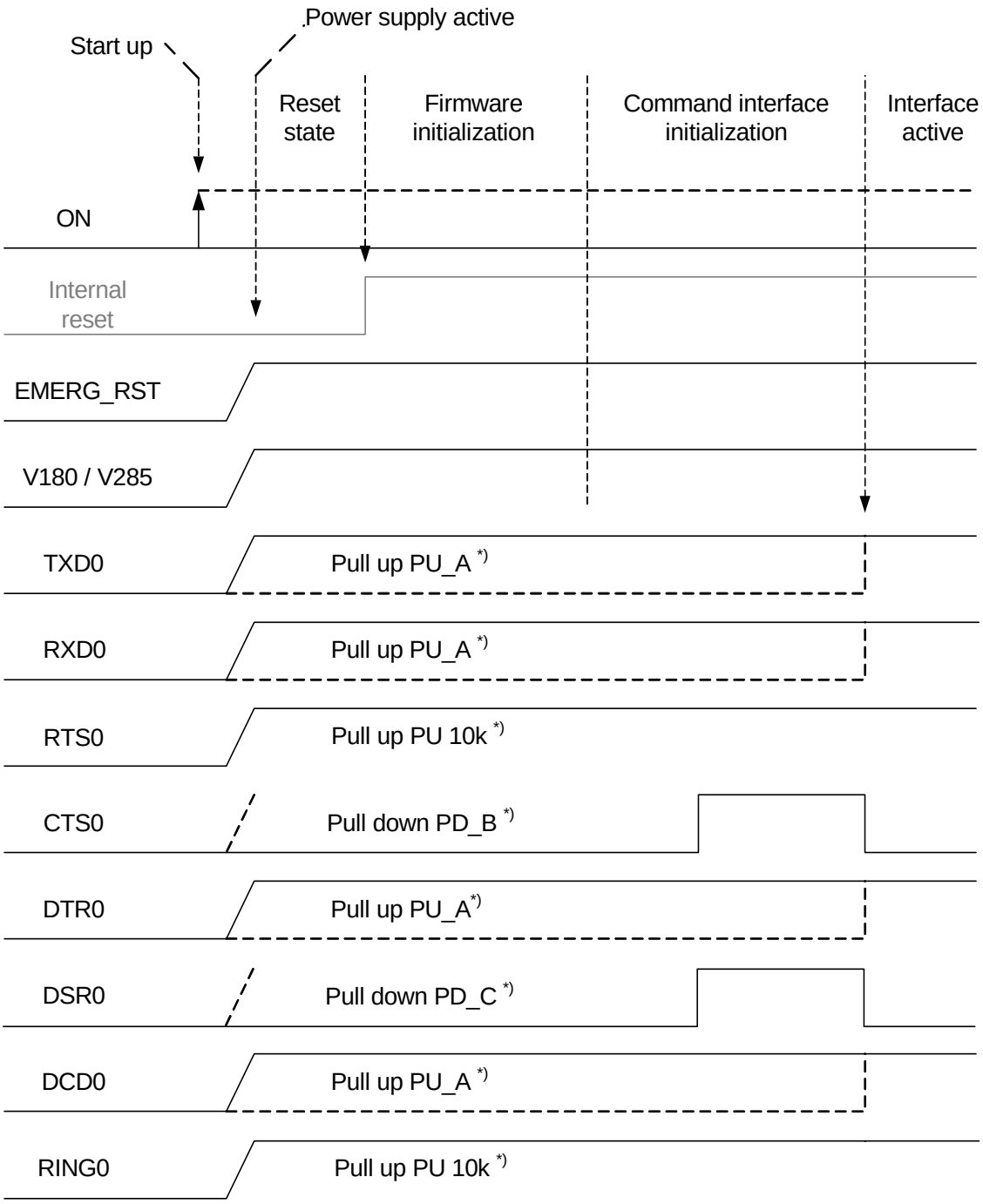
Features:

- Includes the data lines TXD0 and RXD0, the status lines RTS0 and CTS0 and, in addition, the modem control lines DTR0, DSR0, DCD0 and RING0.
- The DTR0 signal will only be polled once per second from the internal firmware of BGS2-E/BGS2-W.
- The RING0 signal serves to indicate incoming calls and other types of URCs (Unsolicited Result Code). It can also be used to send pulses to the host application, for example to wake up the application from power saving state. See [1] for details on how to configure the RING0 line by AT^SCFG.
- By default configured to 8 data bits, no parity and 1 stop bit.
- ASC0 can be operated at fixed bit rates from 300bps to 230,400bps.
- Autobauding supports bit rates from 1,200bps to 230,400bps.
- Supports RTS0/CTS0 hardware flow control and XON/XOFF software flow control.

Table 13: DCE-DTE wiring of ASC0

V.24 circuit	DCE		DTE	
	Pad function	**Signal direction**	**Pad function**	**Signal direction**
103	TXD0	Input	TXD	Output
104	RXD0	Output	RXD	Input
105	RTS0	Input	RTS	Output
106	CTS0	Output	CTS	Input
108/2	DTR0	Input	DTR	Output
107	DSR0	Output	DSR	Input
109	DCD0	Output	DCD	Input
125	RING0	Output	RING	Input

The following figure shows the startup behavior of the asynchronous serial interface ASC0.



*) For pull-up and pull-down values see Table 8.

Figure 17: ASC0 startup behavior

Please note that no data must be sent over the ASC0 interface before the interface is active and ready to receive data (see Section 3.3.1.1).

3.10 Serial Interface ASC1

BGS2-E/BGS2-W offers a 4-wire unbalanced, asynchronous modem interface ASC1 conforming to ITU-T V.24 protocol DCE signaling. The electrical characteristics do not comply with ITU-T V.28. The electrical level of the ASC1 interface is set to 1.8V. For electrical characteristics please refer to Table 25.

BGS2-E/BGS2-W is designed for use as a DCE. Based on the conventions for DCE-DTE connections it communicates with the customer application (DTE) using the following signals:
- Port TXD @ application sends data to module's TXD1 signal line
- Port RXD @ application receives data from the module's RXD1 signal line

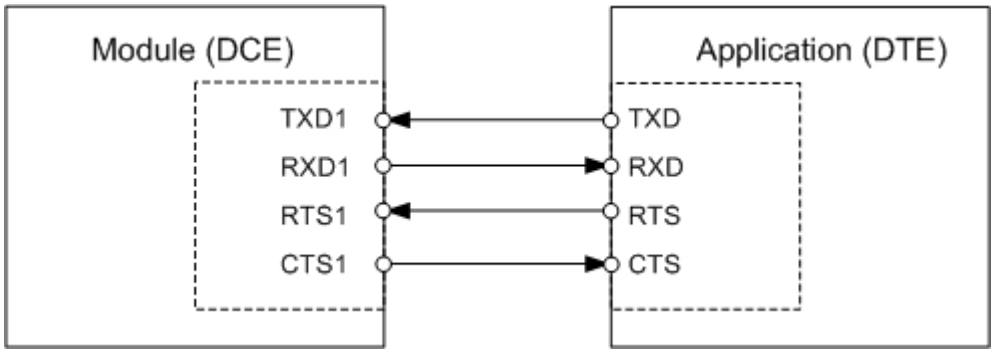


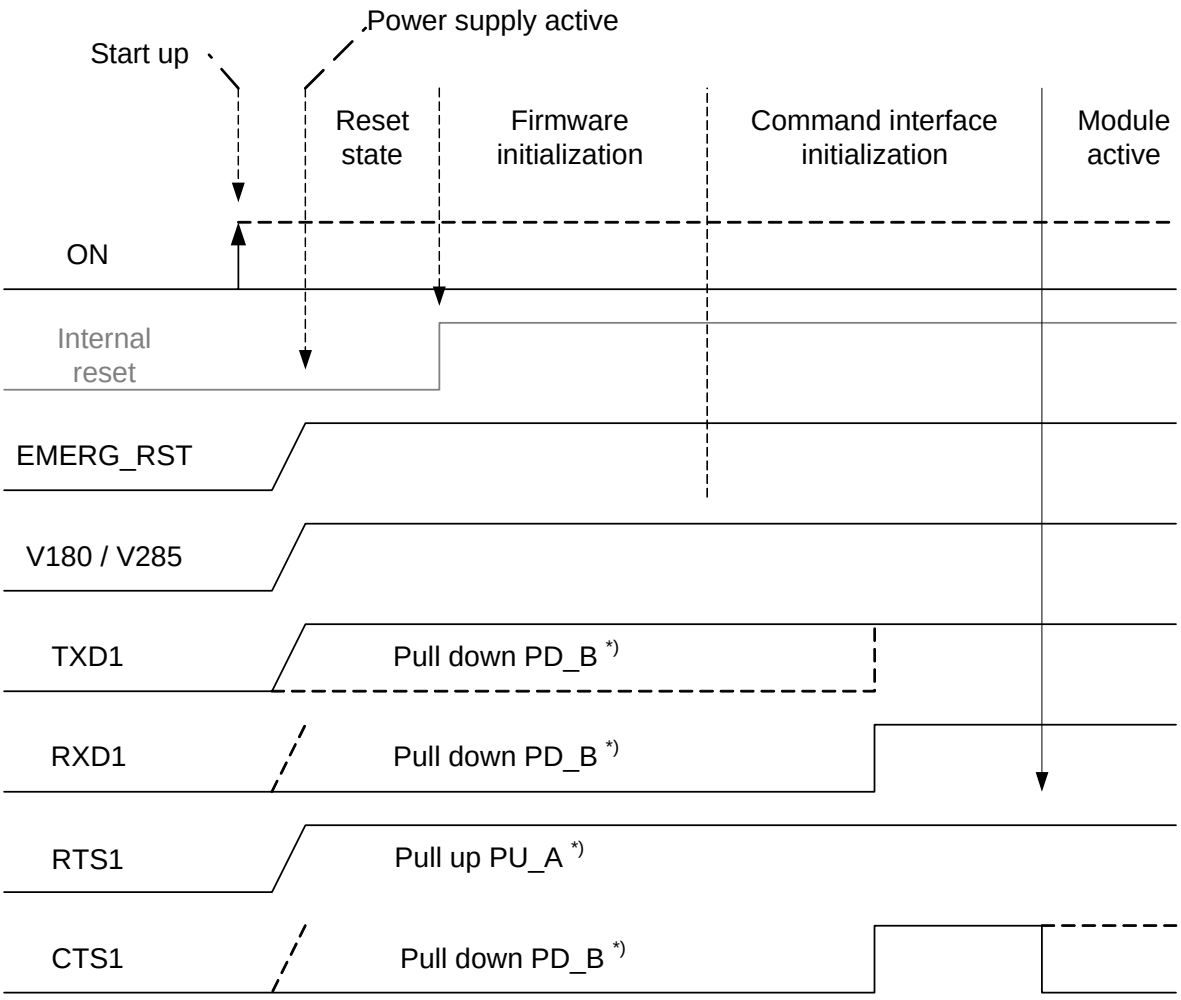
Figure 18: Serial interface ASC1

Features
- Includes only the data lines TXD1 and RXD1 plus RTS1 and CTS1 for hardware handshake.
- On ASC1 no RING line is available. The indication of URCs on the second interface depends on the settings made with the AT^SCFG command. For details refer to [1].
- Configured for 8 data bits, no parity and 1 or 2 stop bits.
- ASC1 can be operated at fixed bit rates from 300bps to 230,400bps. Autobauding is not supported on ASC1.
- Supports RTS1/CTS1 hardware flow control and XON/XOFF software flow control.

Table 14: DCE-DTE wiring of ASC1

V.24 circuit	DCE		DTE	
	Line function	Signal direction	Line function	Signal direction
103	TXD1	Input	TXD	Output
104	RXD1	Output	RXD	Input
105	RTS1	Input	RTS	Output
106	CTS1	Output	CTS	Input

The following figure shows the startup behavior of the asynchronous serial interface ASC1.



*) For pull-up and pull-down values see Table 8.

Figure 19: ASC1 startup behavior

3.11 Analog Audio Interface

BGS2-E/BGS2-W has an analog audio interface with a balanced analog microphone input and a balanced analog earpiece output. A supply voltage and an analog ground connection are provided at dedicated pads.

BGS2-E/BGS2-W offers six audio modes which can be selected with the AT^SNFS command. The electrical characteristics of the voiceband part vary with the audio mode. For example, sending and receiving amplification, sidetone paths, noise suppression etc. depend on the selected mode and can be altered with AT commands (except for mode 1).

Please refer to Section 5.6 for specifications of the audio interface and an overview of the audio parameters. Detailed instructions on using AT commands are presented in [1]. Table 30 summarizes the characteristics of the various audio modes and shows what parameters are supported in each mode.

When shipped from factory, all audio parameters of BGS2-E/BGS2-W are set to audio mode 1. This is the default configuration optimized for the Votronic HH-SI-30.3/V1.1/0 handset and used for type approving the Gemalto M2M reference configuration. Audio mode 1 has fix parameters which cannot be modified. To adjust the settings of the Votronic handset simply change to another audio mode.

In transmit direction, all audio modes contain internal scaling factors (digital amplification) that are not accessible.

3.11.1 Microphone Inputs and Supply

The differential microphone inputs MICP and MICN present an impedance of 50kΩ and must be decoupled by capacitors (typical 100nF). A regulated power supply for electret microphones is available at VMIC. The voltage at VMIC is rated at 2.2V and available while audio is active (e.g., during a call). It can also be controlled by AT^SNFM. It is recommended to use an additional RC-filter if a high microphone gain is necessary. It is also recommended to use the AGND line for grounding the microphone circuit. AGND provides for the same module ground potential the analog circuits of the module refer to.

The following figures show possible microphone and line connections.

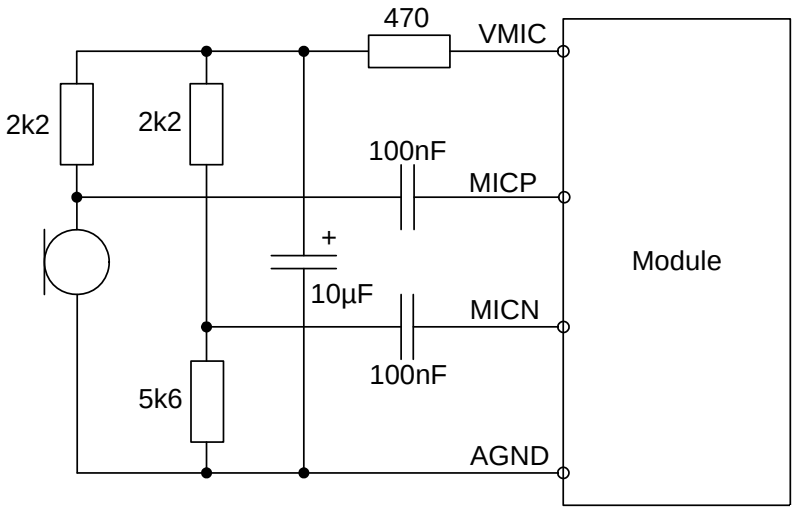


Figure 20: Single ended microphone connection

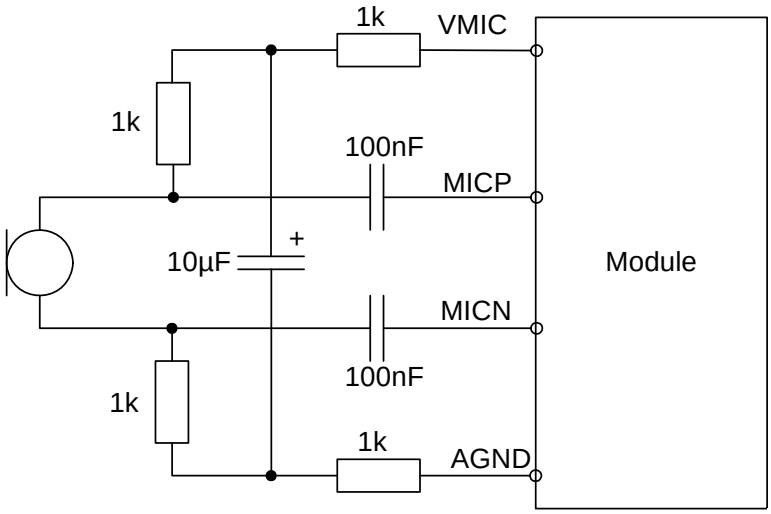


Figure 21: Differential Microphone connection

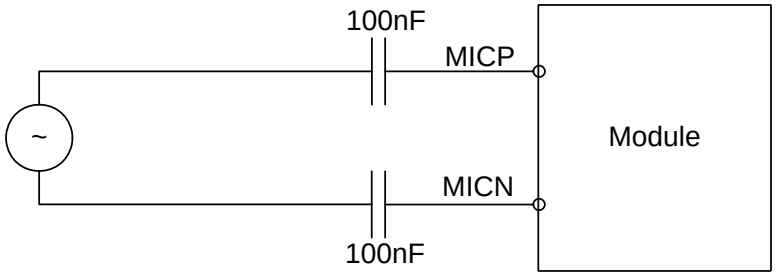


Figure 22: Line Input

3.11.2 Loudspeaker Output

BGS2-E/BGS2-W provides a differential loudspeaker output EPP/EPN. The output is able to deliver a voltage of 3.2Vpp at a load resistance of 16Ω. If it is used as line output (see Figure 24), the application should provide a capacitor decoupled differential input to eliminate GSM humming. A first order low pass filter above 4kHz may be useful to improve the out-of-band signal attenuation. A single ended connection to a speaker or a line input should not be realized.

The following figures show the typical output configurations.

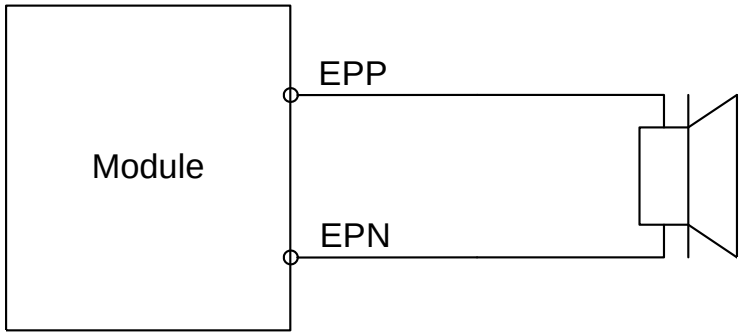


Figure 23: Differential loudspeaker connection

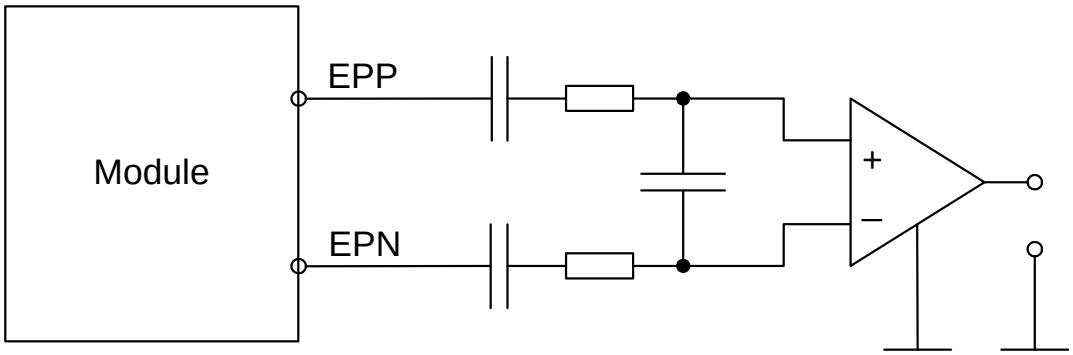


Figure 24: Line output connection

3.12 Digital Audio Interface

BGS2-E/BGS2-W supports a digital audio interface (DAI) that can be employed either as pulse code modulation (see Section 3.12.1) or as inter IC sound interface (see Section 3.12.2). Operation of these interface variants is mutually exclusive.

3.12.1 Pulse Code Modulation Interface

BGS2-E/BGS2-W's DAI interface can be used to connect audio devices capable of pulse code modulation (PCM). The PCM functionality allows for the use of an external codec like the W681360. Using the AT^SAIC command the PCM interface can be activated (see [1]).

The PCM interface supports a 256kHz, long frame synchronization master mode with the following features:

- 16 Bit linear
- 8kHz sample rate
- The most significant bit MSB is transferred first
- 125µs frame duration
- Common frame sync signal for transmit and receive

Table 15 describes the available PCM pins at the digital audio interface. For electrical details see Section 5.4. The details depend on the configured voltage levels for the pins (Section 3.9).

Table 15: Overview of DAI/PCM lines

Signal name on B2B connector	Pin direction	Input/Output
TXDDAI	O	PCM data from module to external codec.
RXDDAI	I	PCM data from external codec to module.
TFSDAI	O	Frame synchronization signal to external codec: Long frame @ 256kHz
SCLK	O	Bit clock to external codec: 256kHz

Figure 25 shows the PCM timing for the master mode available with BGS2-E/BGS2-W.

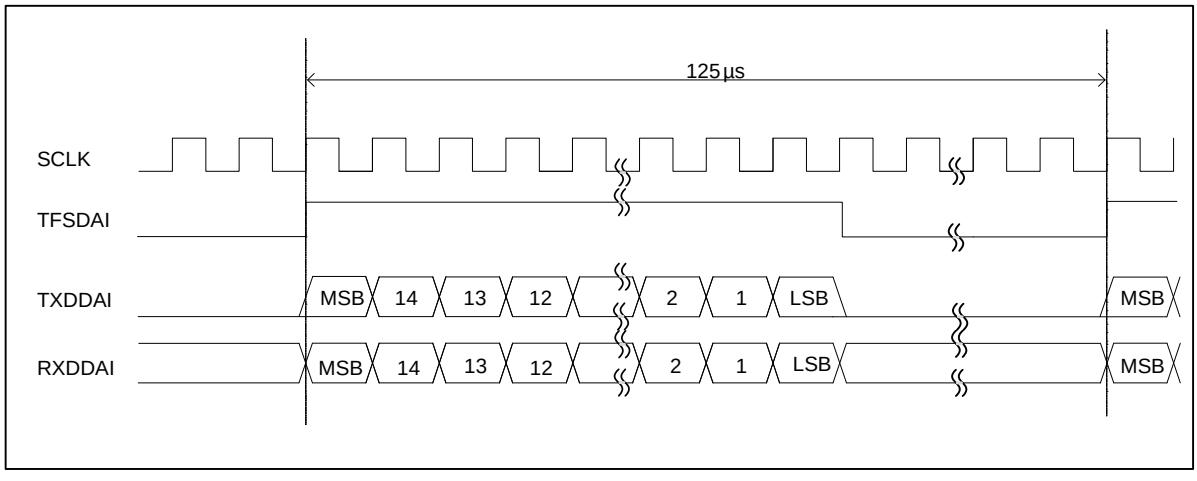


Figure 25: Long frame PCM timing, 256kHz

The following figure shows the start up behavior of the DAI interface. It is possible to set the startup configuration of the DAI interface via AT command (see [1]). The start up configuration of functions will be activated after the software initialization of the command interface. With an active state of RING0, CTS0 or CTS1 (low level) the initialization of the DAI interface is finished.

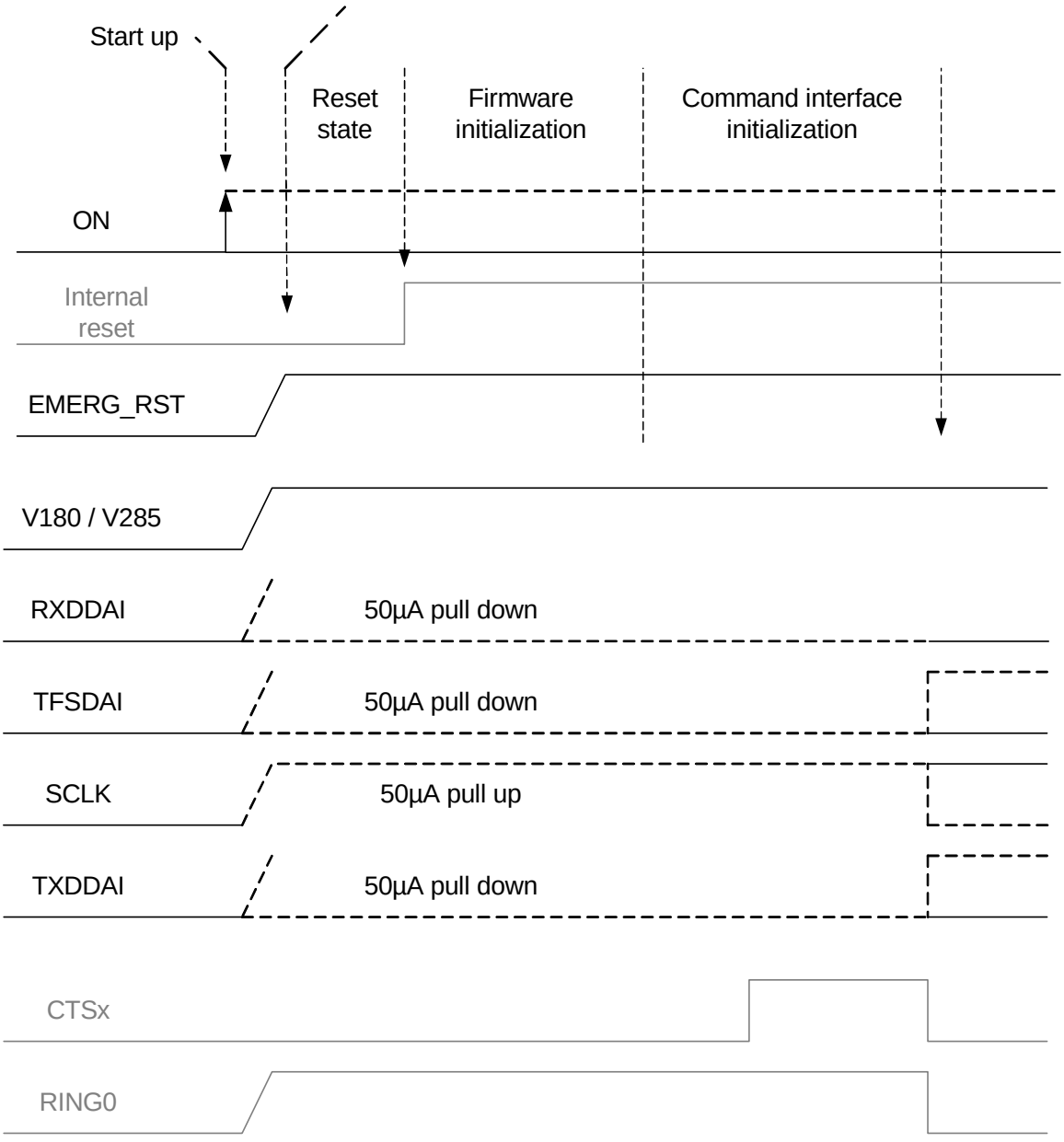


Figure 26: DAI startup timing

3.12.2 Inter IC Sound Interface

The Inter IC Sound interface (I^2S) is enabled using the AT command AT^SAIC (see [1]). An activation is possible only out of call and out of tone presentation. The I^2S properties and capabilities comply with the requirements laid out in the Phillips I^2S Bus Specifications, revised June 5, 1996.

The I^2S interface has the following characteristics:

- Clock Modes: Master with permanent clock option
- Sampling Rate: 8 KHz (narrowband)
- Frame Length: 16 bit mono voice signal. The mono voice signal is transferred in the left channel, the right channel is muted

The digital audio interface pads available for the PCM interface are also available for the I^2S interface. In I^2S mode they have the same electrical characteristics (for more information on the TXDDAI, RXDDAI, TFSDAI and SCLK pads please refer to Section 5.4 and Section 3.12.1).

The table below lists the available pads at the module's digital audio interface.

Table 16: Overview of DAI/I^2S lines

Signal name	Input/Output	Description
TXDDAI	O	I^2S data from module to external codec.
RXDDAI	I	I^2S data from external codec to module.
TFSDAI	O	Frame synchronization signal to external codec: Word alignment (WS)
SCLK	O	Bit clock to external codec: 256kHz

The following figure shows the I^2S timing for the master mode available with the module.

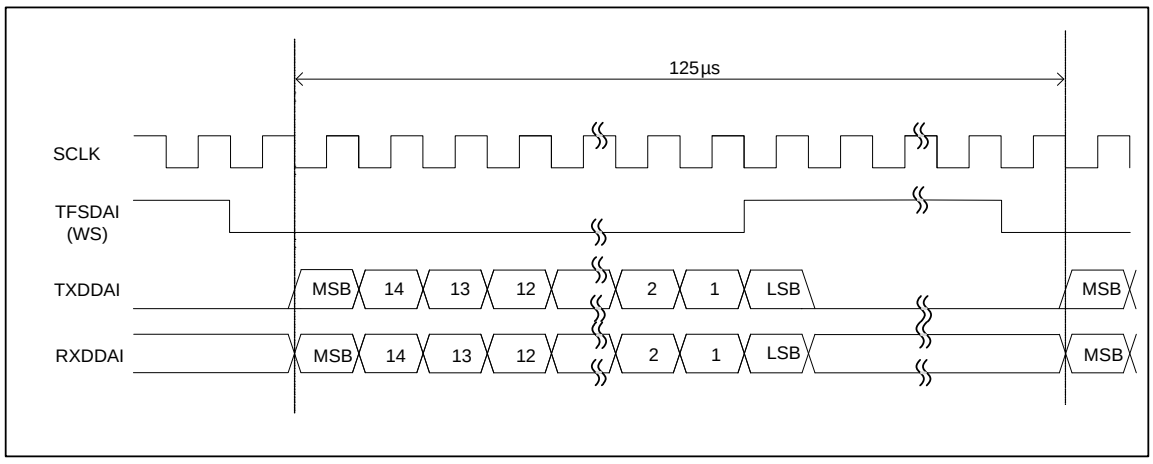


Figure 27: I^2S timing

3.13 GPIO Interface

BGS2-E/BGS2-W offers a GPIO interface with 6 GPIO lines. The GPIO lines are shared with other interfaces, such as I^2C interface (see Section 3.14), Status LED (see Section 3.18), the PWM functionality (see Section 3.15), the jamming indicator (see Section 3.17). All functions are controlled by dedicated AT commands.

The following table shows the configuration variants of the GPIO pads. All variants are mutually exclusive, i.e. a pad configured as GPIO is locked for alternative use.

Table 17: GPIO assignment

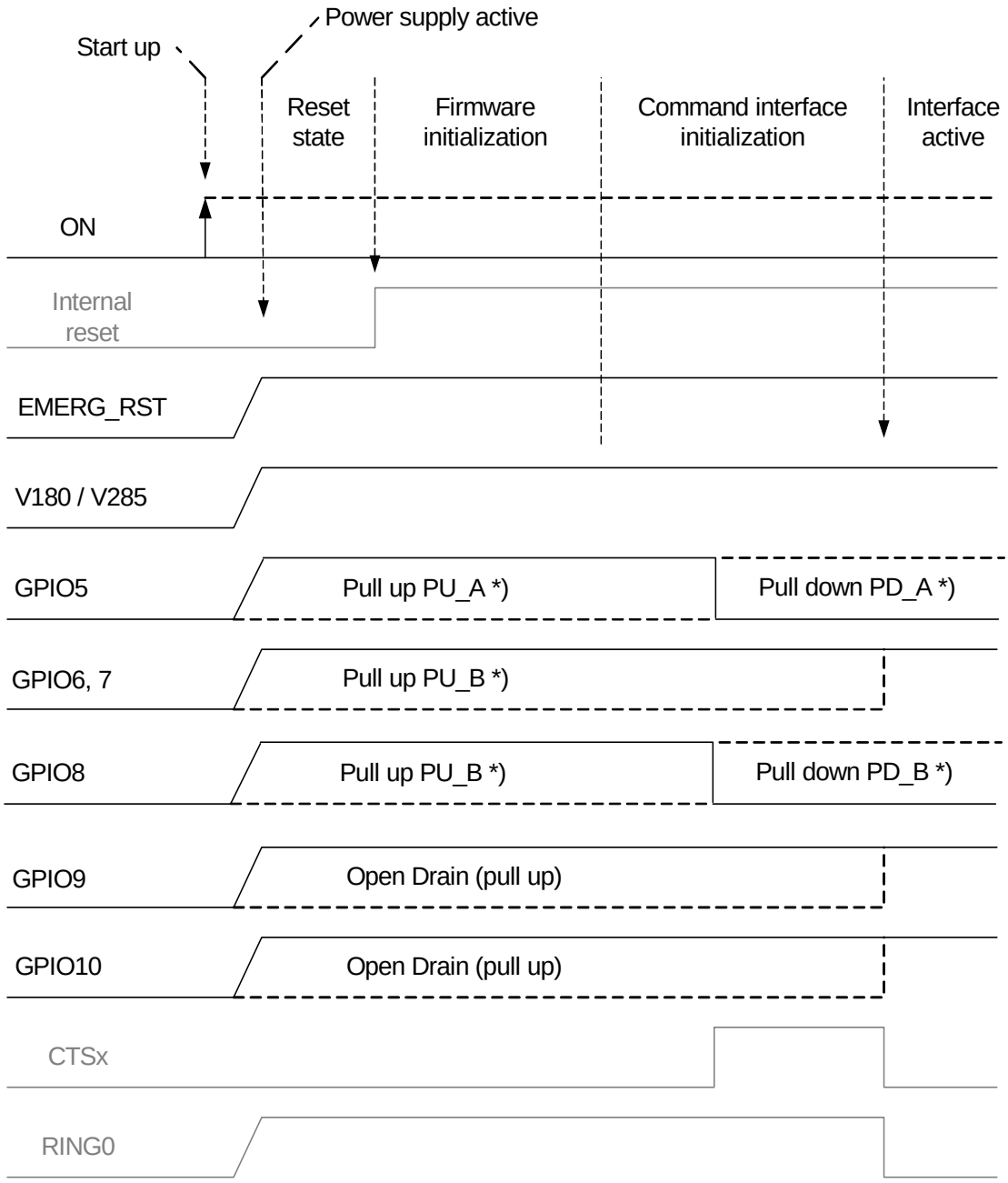
GPIO	I2C	PWM	Status LED	Jamming indicator	Voltage domain
GPIO5			Status LED		V180
GPIO6		PWM2		Jamming indicator	V180
GPIO7		PWM1			V180
GPIO8					V180
GPIO9	I2CCLK				VDIG (=V180)
GPIO10	I2CDAT				VDIG (=V180)

Each GPIO line can be configured for use as input or output. The GPIO related AT commands are the following: AT^SPIO, AT^SCPIN, AT^SGIO, AT^SSIO. A detailed description can be found in [1].

When the BGS2-E/BGS2-W starts up, all GPIO lines are set to high-impedance state after initializing, as described in Section 3.3.3. Therefore, it is recommended to connect external pull-up or pull-down resistors to all GPIO lines you want to use as output. This is necessary to keep these lines from floating or driving any external devices before all settings are done by AT command (at least AT^SPIO, AT^SCPIN), and after closing the GPIOs again.

The power supply domain voltage level for GPIO5 to GPIO8 is 1.8V. GPIO9 and GPIO10 are in the VDIG power supply domain that is recommended to be configured to 1.8V voltage level (see also Section 3.9). I2CCLK (GPIO9) has an internal 5kΩ pull-up resistor, I2CDAT (GPIO10) requires an external pull-up resistor.

The following figure shows the startup behavior of the GPIO interface. With an active state of the ASC0 interface (i.e. RING0, CTS0 or CTS1 are at low level) the initialization of the GPIO interface lines is also finished.



*) For pull-up/-down values see Table 8.

Figure 28: GPIO startup behavior

3.14 I²C Interface

The signal lines of the I²C interface are shared with the GPIO9 and GPIO10 signal pads and are activated by means of AT command. For details see [1]: AT^SSPI.

The voltage level configuration for the ASC0 interface has an impact on the I²C interface since the I²C interface is in the same VDIG controlled power supply domain. If the ASC0 voltage level is set to 1.8V, the I²C interface pads have the same voltage level (see Figure 15).

I²C is a serial, 8-bit oriented data transfer bus for bit rates up to 400kbps in Fast mode. It consists of two lines, the serial data line I2CDAT (GPIO10) and the serial clock line I2CCLK (GPIO9). The module acts as a single master device, e.g. the clock I2CCLK is driven by the module. I2CDAT is a bi-directional line. Each device connected to the bus is software addressable by a unique 7-bit address, and simple master/slave relationships exist at all times. The module operates as master-transmitter or as master-receiver. The customer application transmits or receives data only on request of the module.

The I²C interface can be powered from an external supply or via the V180/V285 line of BGS2-E/BGS2-W. If connected to the V180/V285 line, the I²C interface will be properly shut down when the module enters the Power Down mode. If you prefer to connect the I²C interface to an external power supply, take care that VCC of the application is in the range of V180/V285 and that the interface is shut down when the EMERG_RST signal goes low.

In the application I2CDAT and I2CCLK lines need to be connected to a positive supply voltage via a pull-up resistor. For electrical characteristics please refer to Table 25.

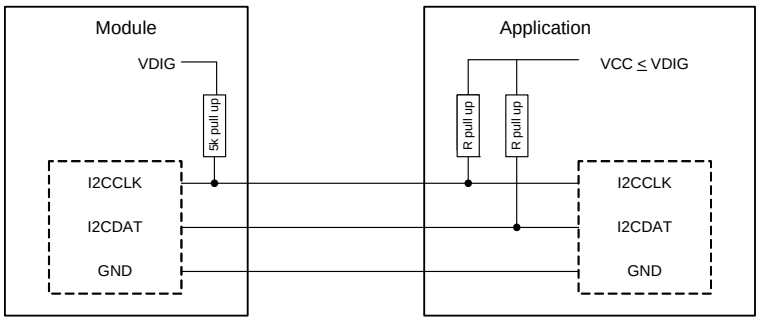


Figure 29: I²C interface connected to VCC of application

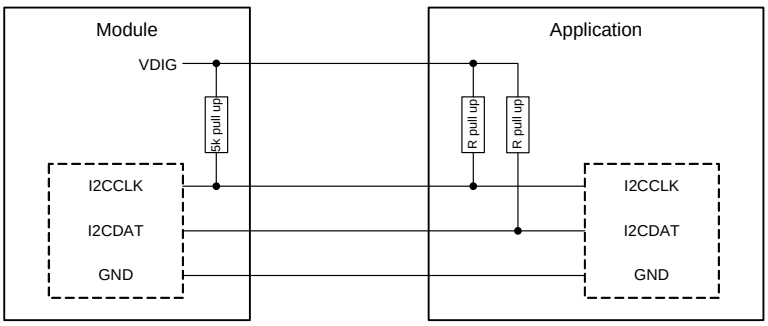


Figure 30: I²C interface connected to VDIG

Note: Good care should be taken when creating the PCB layout of the host application: The traces of I2CCLK and I2CDAT should be equal in length and as short as possible.

The following figure shows the startup behavior of the I²C interface. With an active state of the ASC0 interface (i.e. RING0, CTS0 or CTS1 are at low level) the initialization of the I²C interface is also finished.

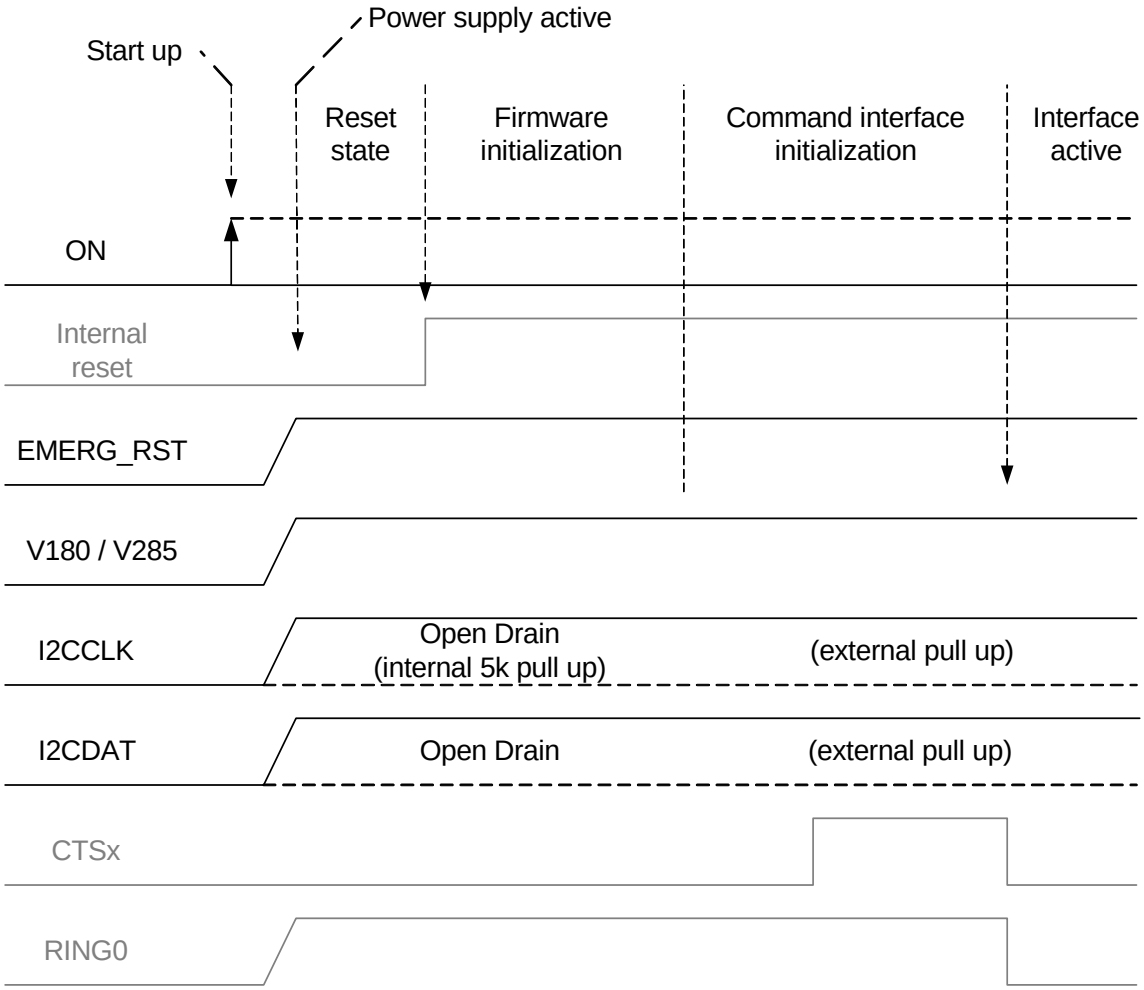


Figure 31: I²C startup behavior

3.14.1 I²C Interface on DSB75

To evaluate the I²C interface employing the DSB75, some modifications are required on the AH6-DSB75 adapter mentioned in Section 9.1. Four components will have to be populated on the adapter: D305 (I²C EEPROM, SOIC-8, 1V8; a suitable EEPROM type would for example be "AT24C1024BN-SH-T" from ATMEL), C300 (decoupling capacitor, 0402 package), R301, R302 (I²C pull-up resistors, 0402 package). For details see Figure 32.

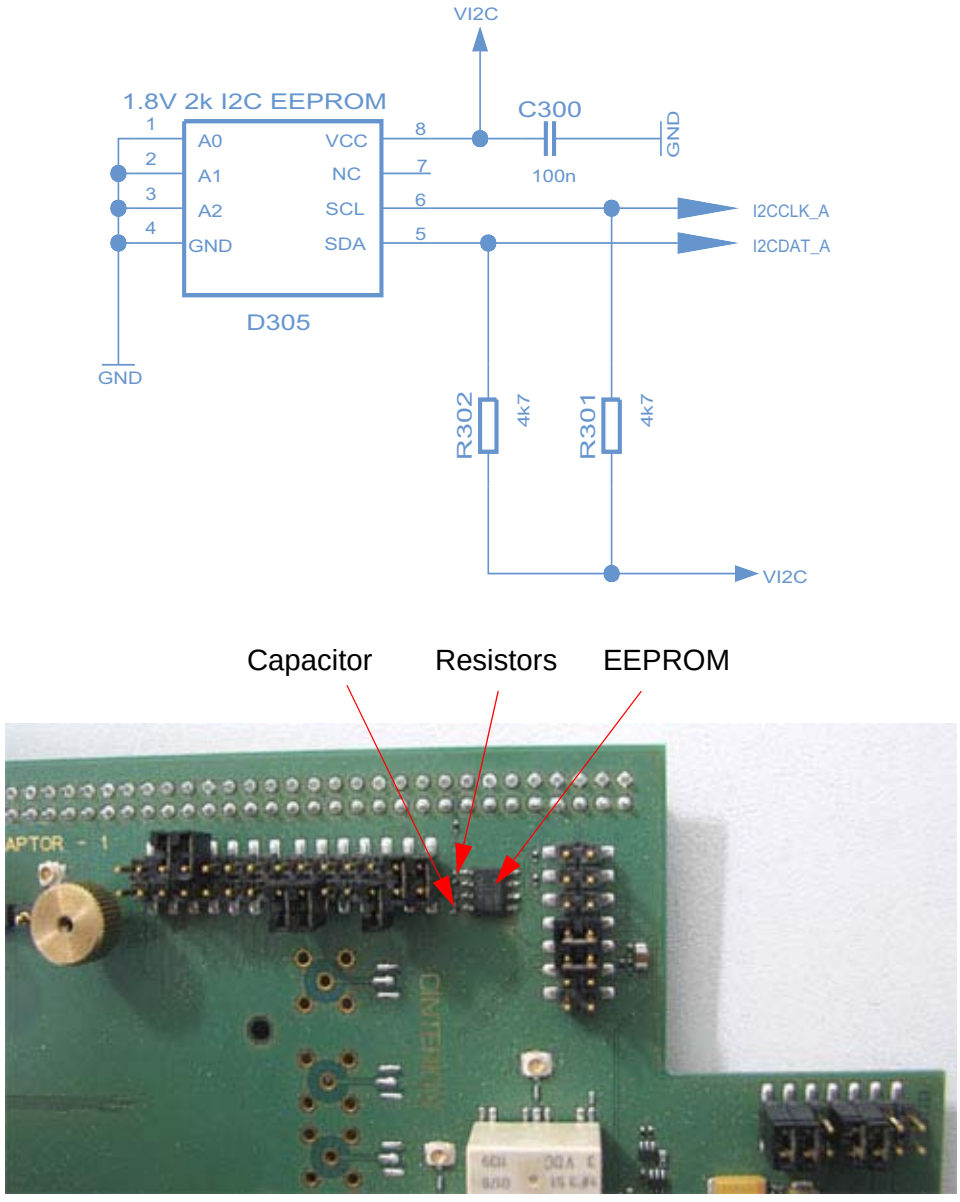


Figure 32: Additional EEPROM to enable usage of I²C interface on DSB75

Furthermore, two jumpers (X171, for pins 7&8, 9&10) must be set in order to connect the module's I²C signals with the memory device's input pins. For details see Figure 33.

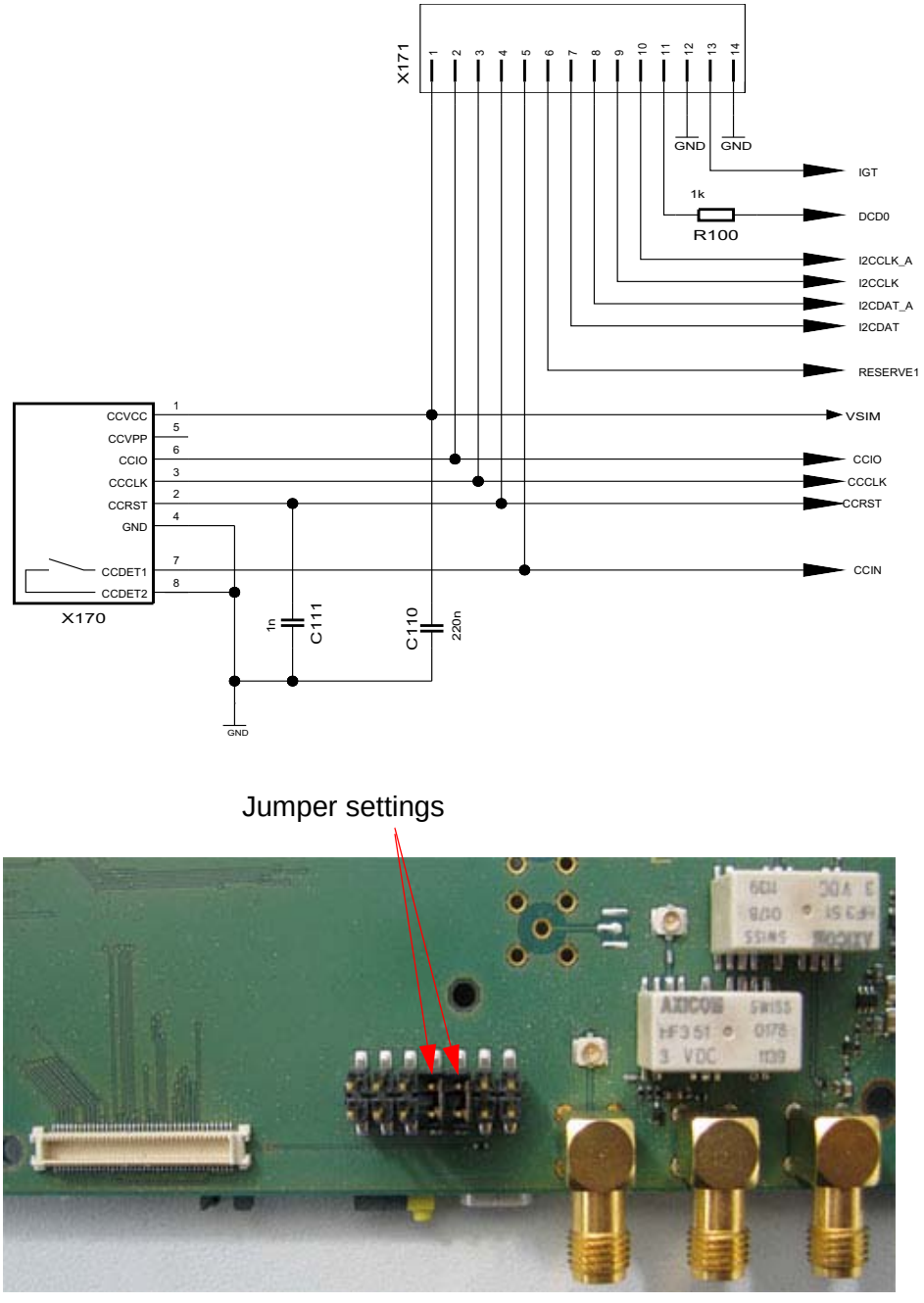


Figure 33: Jumper settings to enable usage of I²C interface on DSB75

3.15 PWM Interfaces

BGS2-E/BGS2-W offers two PWM (Pulse Width Modulation) interfaces, which can be used, for example, to connect buzzers. The PWM1 line is shared with GPIO7 and the PWM2 line is shared with GPIO6 (for GPIOs see Section 3.13). GPIO and PWM functionality are mutually exclusive.

The startup behavior of the lines is shown in Figure 28.

To open and configure a PWM output use the AT^SWDAC command. For details refer to [1].

3.16 Analog-to-Digital Converter

ADC1_IN is used for general purpose voltage measurements. For electrical characteristics see Section 5.4. ADC1_IN can be configured and read by the AT^SRADC command - see [1].

3.17 Jamming Indicator

The GPIO6 interface line can be configured as a jamming indicator by AT command. When possible jamming is detected by the module, GPIO6 is set to high level. This state lasts as long as possible jamming is detected.

By default, the jamming indicator feature is disabled. It has to be enabled using the AT command AT^SCFG "MEopMode/JamDet/If". For details see [1].

3.18 Status LED

The GPIO5 line at the SMT application interface can be configured to drive a status LED which indicates different operating modes of the module (for GPIOs see Section 3.13). GPIO and LED functionality are mutually exclusive.

To take advantage of this function connect an LED to the GPIO5/LED line as shown in Figure 34. The LED can be enabled/disabled by AT command. For details refer to [1]: AT^SSYNC.

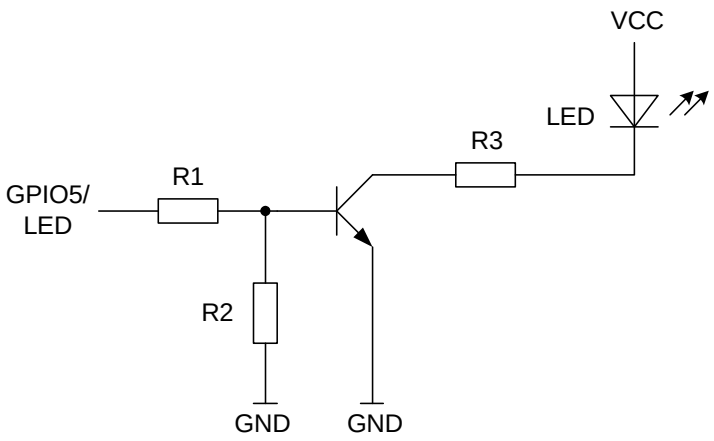


Figure 34: Status signaling with LED driver

3.19 Behavior of the RING0 Line (ASC0 Interface only)

The RING0 line is available on the first serial interface (ASC0). The signal serves to indicate incoming calls and other types of URCs (Unsolicited Result Code).

Although not mandatory for use in a host application, it is strongly suggested that you connect the RING0 line to an interrupt line of your application. In this case, the application can be designed to receive an interrupt when a falling edge on RING0 occurs. This solution is most effective, particularly, for waking up an application from power saving. Note that if the RING0 line is not wired, the application would be required to permanently poll the data and status lines of the serial interface at the expense of a higher current consumption. Therefore, utilizing the RING0 line is an option to significantly reduce your application's overall current consumption.

The behavior of the RING0 line varies with the type of event. Note that the behavior described below is the default behavior, and may be adapted by AT command (for details see [1]):

- When a voice call comes in the RING0 line goes low for 1 second and high for another 4 seconds. Every 5 seconds the ring string is generated and sent over the RXD0 line. If there is a call in progress and call waiting is activated for a connected handset or handsfree device, the RING0 line switches to ground in order to generate acoustic signals that indicate the waiting call.

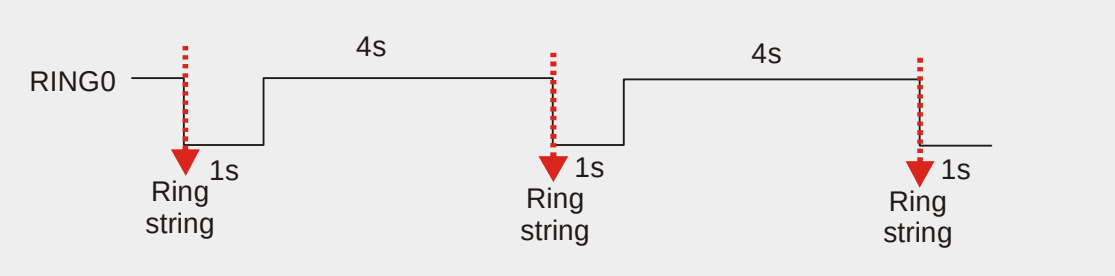


Figure 35: Incoming voice call

- Likewise, when a data or fax call is received, RING0 goes low. However, in contrast to voice calls, the line remains low. Every 5 seconds the ring string is generated and sent over the RXD0 line.

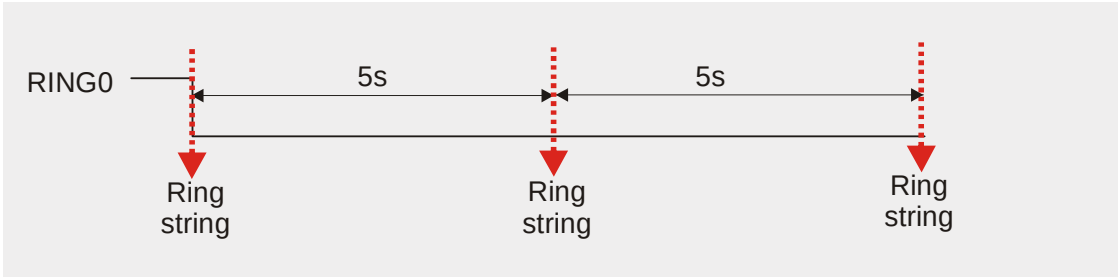


Figure 36: Incoming data or fax call

- All other types of Unsolicited Result Codes (URCs) also cause the RING0 line to go low, however for 1 second only.

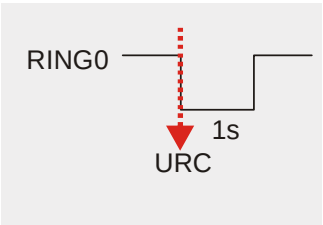


Figure 37: URC transmission

3.20 Power Indication Circuit

In Power Down mode the maximum voltage at any digital or analog interface line must not exceed +0.3V (see also Section 5.1). Exceeding this limit for any length of time might cause permanent damage to the module.

It is therefore recommended to implement a power indication signal that reports the module's power state and shows whether it is active or in Power Down mode. While the module is in Power Down mode all signals with a high level from an external application need to be set to low state or high impedance state. The sample power indication circuit illustrated in Figure 38 denotes the module's active state with a low signal and the module's Power Down mode with a high signal or high impedance state.

The following Table 18 lists two different configurations for the module's interfaces, depending on the power supply domain specified with VDIG. The cases differ in the power supply voltage level configured for the ASC0, ASC1, I^2C and GPIO interface lines and the possibility of back powering through the used interface lines from an external application:

- If all interface lines operate within the V180 power supply domain (i.e., VDIG connected to V180), the V285 power supply voltage line is not prone to back powering. The power indication circuit is therefore controlled by the power supply voltage line V285.
- If the I^2C interface lines operate within the V285 power supply domain (i.e., VDIG connected to V285), the V180 power supply voltage line is not prone to back powering. The power indication circuit is therefore controlled by the power supply voltage line V180.

Table 18: Power indication circuit

Interface	VDIG = V180	VDIG = V285
	Voltage level at interface	Voltage level at interface
ASC0 lines	1.8V	2.85V for TXD0, RXD0, CTS0, RTS0 and RING0 1.8V for DTR0, DSR0 and DCD0
ASC1 lines	1.8V	1.8V
I^2C lines	1.8V	2.85V
GPIO lines	1.8V	1.8V
Voltage control for power indication circuit	V285 controlled	V180 controlled

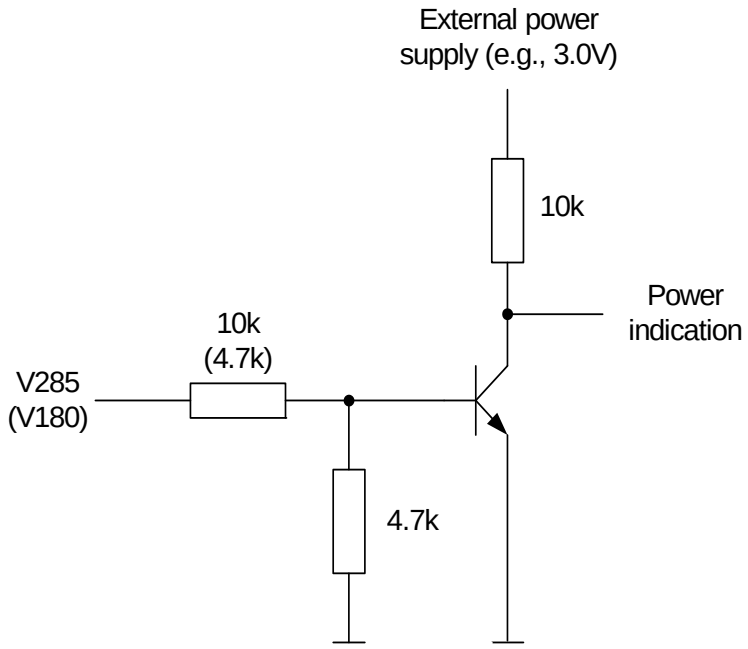


Figure 38: Power indication circuit

3.21 Fast Shutdown

BGS2-E/BGS2-W provides a dedicated fast shutdown signal. The FAST_SHTDWN line is an active low control signal and must be applied for at least 10 milliseconds. If unused this pin can be left open because of a configured internal pull-up resistor.

By default, the fast shutdown feature is disabled. It has to be enabled using the AT command AT^SCFG "MEShutdown/Fso". For details see [1].

If enabled, a low impulse >10 milliseconds on the FAST_SHTDWN line starts the fast shutdown. The fast shutdown procedure still finishes any data activities on the module's flash file system, thus ensuring data integrity, but will no longer deregister gracefully from the network, thus saving the time required for network deregistration.

Please note that if enabled, the normal software controlled shutdown using AT^SMSO will also be a fast shutdown, i.e., without network deregistration. However, in this case no URCs including shutdown URCs will be provided by the AT^SMSO command.

4 Antenna Interface

The RF interface has an impedance of 50Ω. BGS2-E/BGS2-W is capable of sustaining a total mismatch at the antenna lines without any damage, even when transmitting at maximum RF power.

The external antenna must be matched properly to achieve best performance regarding radiated power, modulation accuracy and harmonic suppression. Antenna matching networks are not included on the BGS2-E/BGS2-W module and should be placed in the host application if the antenna does not have an impedance of 50Ω.

Regarding the return loss BGS2-E/BGS2-W provides the following values in the active band:

Table 19: Return loss in the active band

State of module	Return loss of module	Recommended return loss of application
Receive	≥ 8dB	≥ 12dB
Transmit	not applicable	≥ 12dB

4.1 Antenna Installation

The antenna is connected by soldering the antenna pad (ANT_GSM, i.e., pad #59) and its neighboring ground pads (GND, i.e., pads #58 and #60) directly to the application's PCB. The antenna pad is the antenna reference point (ARP) for BGS2-E/BGS2-W. All RF data specified throughout this document is related to the ARP.

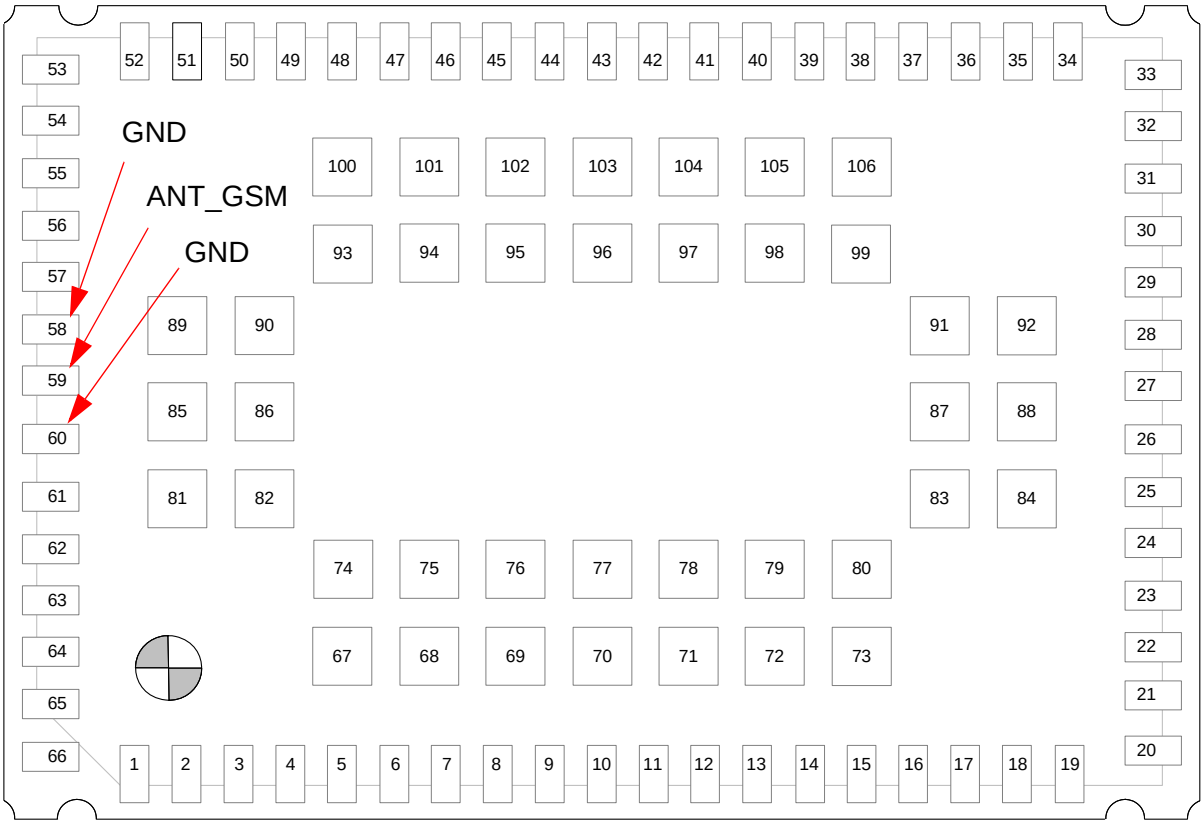


Figure 39: Antenna pads (bottom view)

The distance between the antenna ANT_GSM pad (#59) and its neighboring GND pads (#58, #60) has been optimized for best possible impedance. On the application PCB, special attention should be paid to these 3 pads, in order to prevent mismatch.

The wiring of the antenna connection line, starting from the antenna pad to the application antenna should result in a 50Ω line impedance. Line width and distance to the GND plane needs to be optimized with regard to the PCB's layer stack. Some examples are given in Section 4.2.

To prevent receiver desensitization due to interferences generated by fast transients like high speed clocks on the application PCB, it is recommended to realize the antenna connection line using embedded Stripline rather than Micro-Stripline technology. Please see Section 4.2.1 for an example.

For type approval purposes, the use of a 50Ω coaxial antenna connector (U.FL-R-SMT) might be necessary. In this case the U.FL-R-SMT connector should be placed as close as possible to BGS2-E/BGS2-W's antenna pad.

4.2 RF Line Routing Design

4.2.1 Line Arrangement Examples

Several dedicated tools are available to calculate line arrangements for specific applications and PCB materials - for example from http://www.polarinstruments.com/ (commercial software) or from http://web.awrcorp.com/Usa/Products/Optional-Products/TX-Line/ (free software).

4.2.1.1 Embedded Stripline

This below figure shows a line arrangement example for embedded stripline with 65µm FR4 prepreg (type: 1080) and 710µm FR4 core (4-layer PCB).

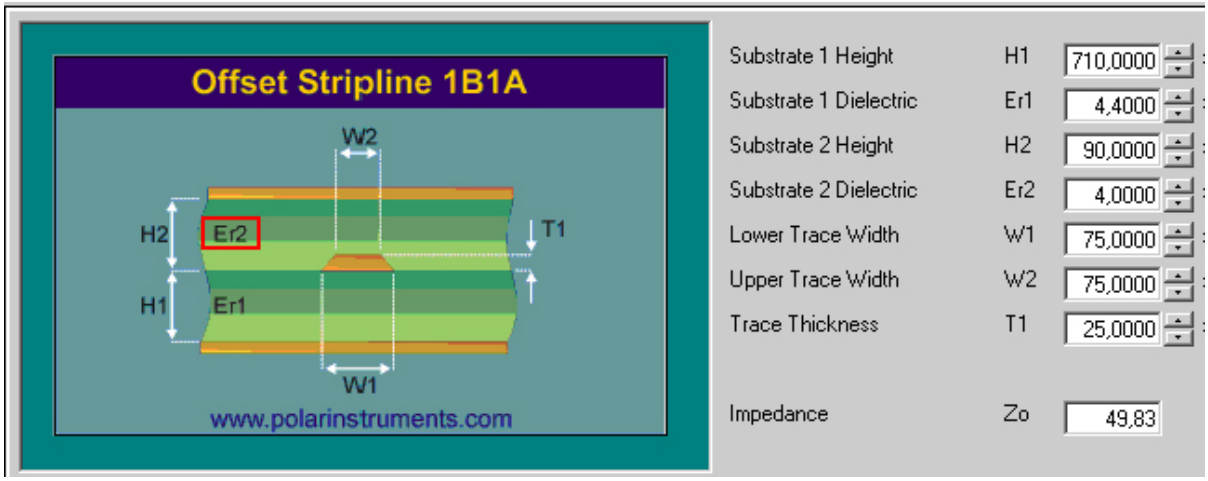


Figure 40: Embedded Stripline with 65µm prepreg (1080) and 710µm core

4.2.1.2 Micro-Stripline

This section gives two line arrangement examples for micro-stripline.

Micro-Stripline on 1.0mm Standard FR4 2-Layer PCB
The following two figures show examples with different values for D1 (ground strip separation).

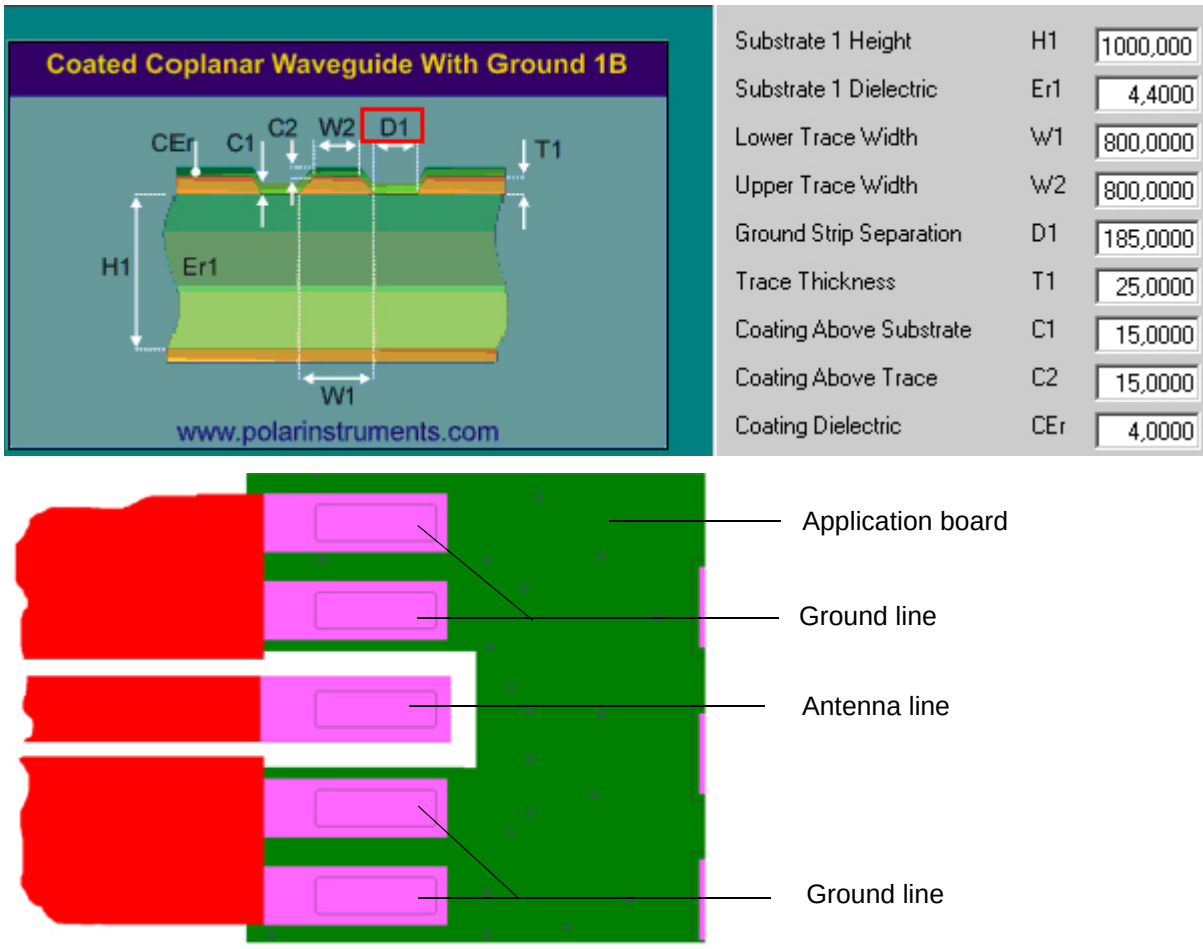


Figure 41: Micro-Stripline on 1.0mm standard FR4 2-layer PCB - example 1

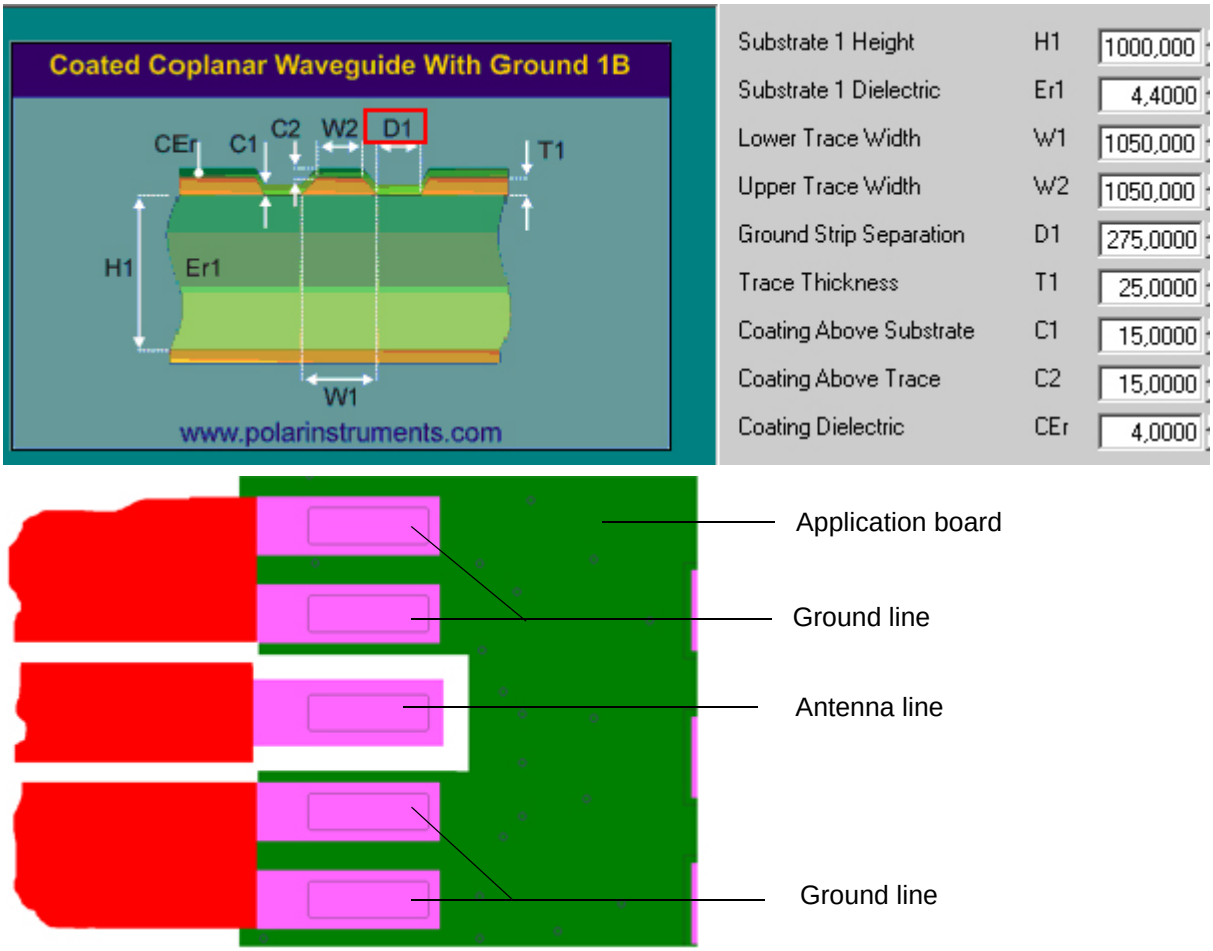


Figure 42: Micro-Stripline on 1.0mm Standard FR4 PCB - example 2

Micro-Stripline on 1.5mm Standard FR4 2-Layer PCB

The following two figures show examples with different values for D1 (ground strip separation).

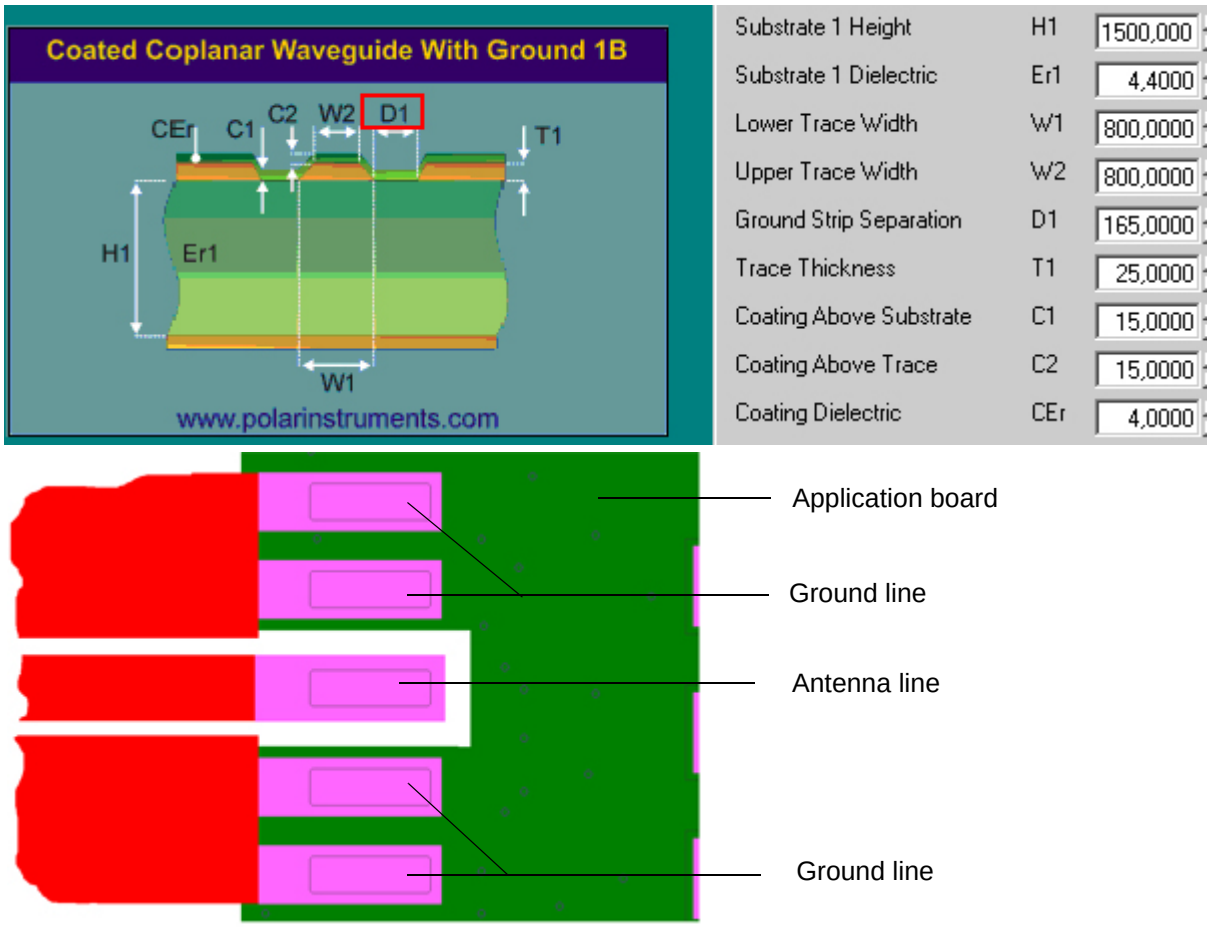


Figure 43: Micro-Stripline on 1.5mm Standard FR4 PCB - example 1

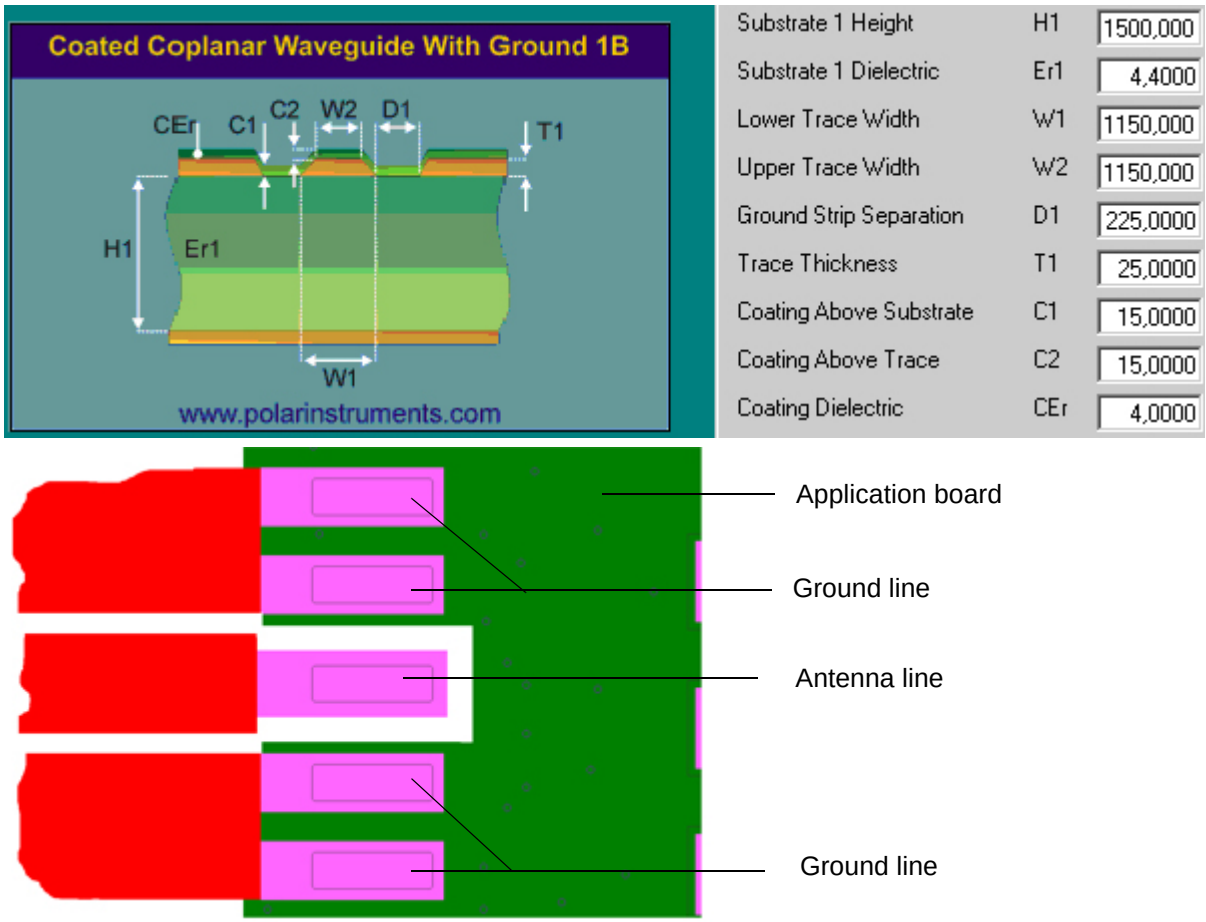


Figure 44: Micro-Stripline on 1.5mm Standard FR4 PCB - example 2

4.2.2 Routing Example

4.2.2.1 Interface to RF Connector

Figure 45 shows the connection of the module‘s antenna pad with an application PCB‘s coaxial antenna connector. Please note that the BGS2-E/BGS2-W bottom plane appears mirrored, since it is viewed from BGS2-E/BGS2-W top side. By definition the top of customer's board shall mate with the bottom of the BGS2-E/BGS2-W module.

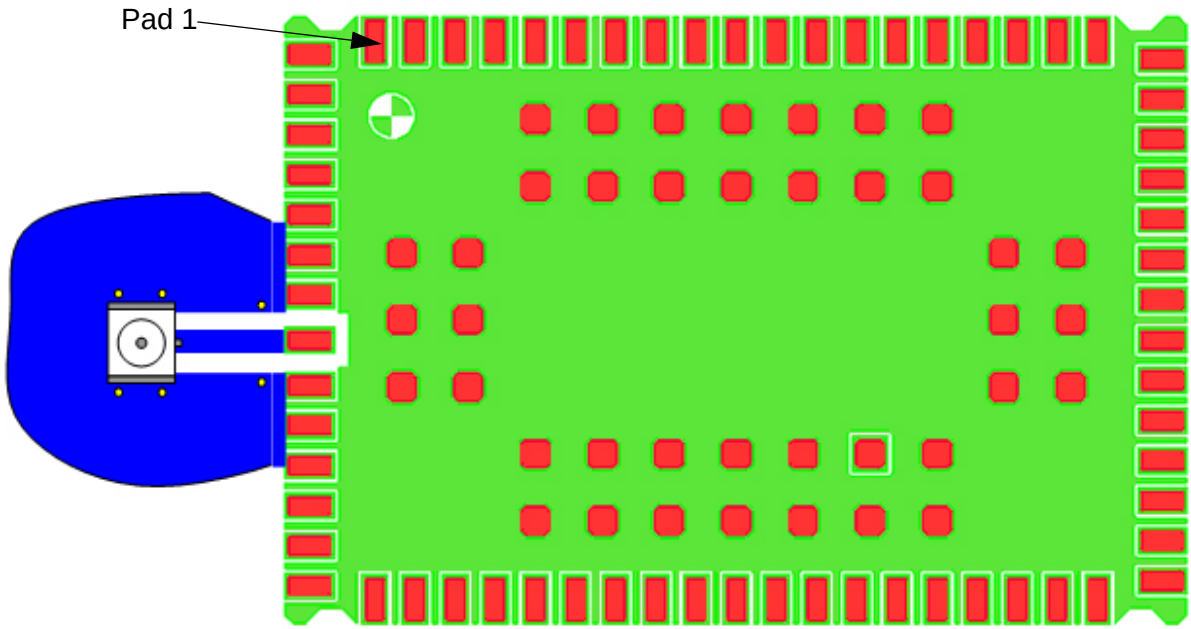


Figure 45: Pouting to application‘s RF connector - top view

5 Electrical, Reliability and Radio Characteristics

5.1 Absolute Maximum Ratings

The absolute maximum ratings stated in Table 20 are stress ratings under any conditions. Stresses beyond any of these limits will cause permanent damage to BGS2-E/BGS2-W.

Table 20: Absolute maximum ratings

Parameter	Min	Max	Unit
Supply voltage $BATT+_{BB}$, $BATT+_{RF}$	-0.3	+6.0	V
Voltage at all digital lines in Power Down mode	-0.3	+0.3	V
Voltage at digital lines 1.8V domain in normal operation	-0.3	+2.2	V
Voltage at digital lines VDIG domain (1.8V) in normal operation	-0.3	+2.2	V
Voltage at digital lines VDIG domain (2.85V) in normal operation	-0.3	+3.3	V
Voltage at SIM interface, CCVCC 1.8V in normal Operation	-0.3	+2.2	V
Voltage at SIM interface, CCVCC 2.85V in normal Operation	-0.3	+3.3	V
Voltage at analog lines in normal operation	-0.3	+3.0	V
Voltage at analog lines in Power Down mode	-0.3	+0.3	V
VDDLP	-0.3	+2.5	V

5.2 Operating Temperatures

Please note that the module's lifetime, i.e., the MTTF (mean time to failure) may be reduced, if operated outside the extended temperature range. A special URC reports whether the module enters or leaves the extended temperature range (see [1]; AT^SCTM).

Table 21: Board temperature

Parameter	Min	Typ	Max	Unit
Normal operation	-30	+25	+85	°C
Extended operation[1]	-40 to -30		+85 to +90	°C
Automatic shutdown[2] Temperature measured on BGS2-E/BGS2-W board	<-40	---	>+90	°C

1. Extended operation allows normal mode speech calls or data transmission for limited time until automatic thermal shutdown takes effect. Within the extended temperature range (outside the normal operating temperature range) the specified electrical characteristics may be in- or decreased.
2. Due to temperature measurement uncertainty, a tolerance of ±3°C on the thresholds may occur.

Table 22: Ambient temperature according to IEC 60068-2 (w/o forced air circulation)

Parameter	Min	Typ	Max	Unit
GSM Call @ max. RF-Power	-40		+75	°C
GPRS Class 8 @ max. RF-Power	-40		+75	°C
GPRS Class 10 @ max. RF-Power	-40		+60	°C
GPRS Class 10 @ max. RF-Power (quad band only)	-40		+60	°C

Table 23: Ambient temperature with forced air circulation (air speed 0.9m/s)

Parameter	Min	Typ	Max	Unit
GSM Call @ max. RF-Power	-40		+80	°C
GPRS Class 8 @ max. RF-Power	-40		+80	°C
GPRS Class 10 @ max. RF-Power	-40		+70	°C
GPRS Class 10 @ max. RF-Power (quad band only)	-40		+70	°C

See also Section 3.3.5.1 for information about the NTC for on-board temperature measurement, automatic thermal shutdown and alert messages.

Note: Within the specified operating temperature ranges the board temperature may vary to a great extent depending on operating mode, used frequency band, radio output power and current supply voltage.

When data are transmitted over GPRS the quad band module variant automatically reverts to a lower Multislot Class if the temperature rises to the limit specified for normal operation and, vice versa, returns to the higher Multislot Class if the temperature is back to normal. For details see Section 3.4.

5.3 Reliability Characteristics

The test conditions stated below are an extract of the complete test specifications.

Table 24: Summary of reliability test conditions

Type of test	Conditions	Standard
Vibration	Frequency range: 10-20Hz; acceleration: 5g Frequency range: 20-500Hz; acceleration: 20g Duration: 20h per axis; 3 axes	DIN IEC 60068-2-6[1]
Shock half-sinus	Acceleration: 500g Shock duration: 1msec 1 shock per axis 6 positions (± x, y and z)	DIN IEC 60068-2-27
Dry heat	Temperature: +70 ±2°C Test duration: 16h Humidity in the test chamber: < 50%	EN 60068-2-2 Bb ETS 300 019-2-7
Temperature change (shock)	Low temperature: -40°C ±2°C High temperature: +85°C ±2°C Changeover time: < 30s (dual chamber system) Test duration: 1h Number of repetitions: 100	DIN IEC 60068-2-14 Na ETS 300 019-2-7
Damp heat cyclic	High temperature: +55°C ±2°C Low temperature: +25°C ±2°C Humidity: 93% ±3% Number of repetitions: 6 Test duration: 12h + 12h	DIN IEC 60068-2-30 Db ETS 300 019-2-5
Cold (constant exposure)	Temperature: -40 ±2°C Test duration: 16h	DIN IEC 60068-2-1

1. For reliability tests in the frequency range 20-500Hz the Standard's acceleration reference value was increased to 20g.

5.4 Pad Assignment and Signal Description

The SMT application interface on the BGS2-E/BGS2-W provides connecting pads to integrate the module into external applications. Figure 46 shows the connecting pads' numbering plan, the following Table 25 lists the pads' assignments.

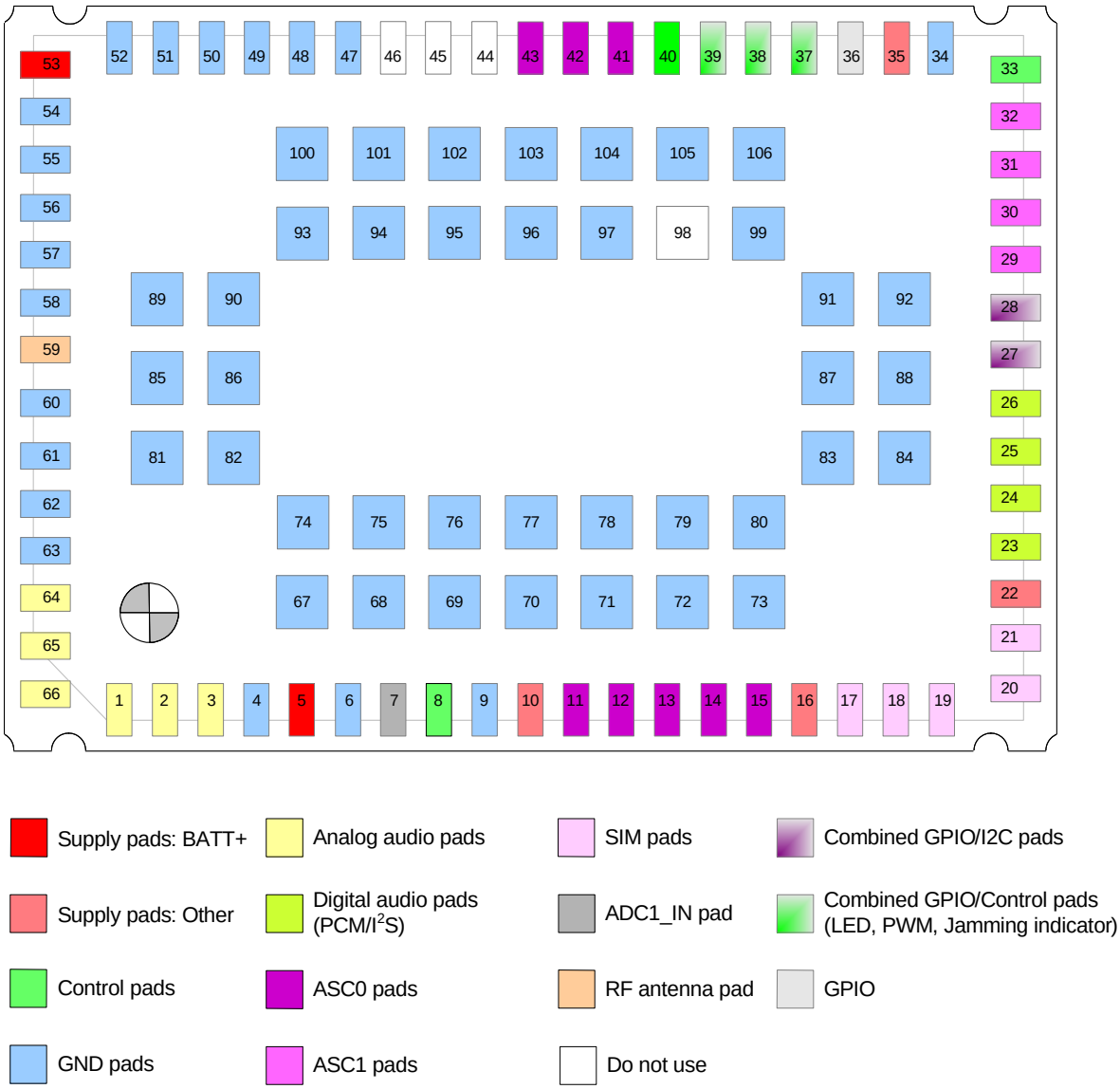


Figure 46: Numbering plan for connecting pads (bottom view)

Table 25: Pad assignments

Pad no.	Signal name	Pad no.	Signal name	Pad no.	Signal name
1	VMIC	23	TXDDAI	45	Do not use
2	EPN	24	TFSDAI	46	Do not use
3	EPP	25	RXDDAI	47	GND
4	GND	26	SCLK	48	GND
5	$BATT+_{BB}$	27	GPIO10/I2CDAT	49	GND
6	GND	28	GPIO9/I2CCLK	50	GND
7	ADC1_IN	29	TXD1	51	GND
8	ON	30	RXD1	52	GND
9	GND	31	RTS1	53	$BATT+_{RF}$
10	VDIG	32	CTS1	54	GND
11	RXD0	33	EMERG_RST	55	GND
12	CTS0	34	GND	56	GND
13	TXD0	35	V180	57	GND
14	RING0	36	GPIO8	58	GND
15	RTS0	37	GPIO7/PWM1	59	ANT_GSM
16	VDDLP	38	GPIO6/PWM2/ Jamming Indicator	60	GND
17	CCRST	39	GPIO5/LED	61	GND
18	CCIN	40	FAST_SHTDWN	62	GND
19	CCIO	41	DSR0	63	GND
20	CCVCC	42	DCD0	64	AGND
21	CCCLK	43	DTR0	65	MICP
22	V285	44	Do not use	66	MICN
				67-106	GND[1]

1. The pads 67-106 are centrally located and should be connected to Ground **except** for pad 98 that is only required for factory tests. Pad 98 must not be connected to the external application, but should be left open.

Signal pads that are not used should not be connected to an external application.

Please note that the reference voltages listed in Table 26 are the values measured directly on the BGS2-E/BGS2-W module. They do not apply to the accessories connected.

Table 26: Electrical description of application interface

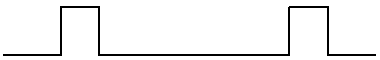
Function	Signal name	IO	Signal form and level	Comment
Power supply	$BATT+_{BB}$ $BATT+_{RF}$	I	$V_I$max = 4.5V $V_I$norm = 4.0V $V_I$min = 3.3V during Tx burst on board I ≈ 1.35A, during Tx burst (GSM)  n Tx = n x 577µs peak current every 4.616ms	Lines of BATT+ and GND must be connected in parallel for supply purposes because higher peak currents may occur. Minimum voltage must not fall below 3.3V including drop, ripple, spikes.
Power supply	GND		Ground	Application Ground
External supply voltage	V180	O	Normal operation: $V_O$norm = 1.80V ±3% $I_O$max = -10mA SLEEP mode Operation: V_OSleep = 1.80V ±5% $I_O$max = -10mA CLmax = 2µF	V180 or V285 may be used for application circuits. If unused keep line open. Not available in Power Down mode. The external digital logic must not cause any spikes or glitches on voltage V180 or V285.
	V285	O	$V_O$norm = 2.85V +1.5%, -2% $I_O$max = -10mA CLmax = 2µF	
Ignition	ON	I	R_I ≈ 32kΩ ±15%, C_I ≈ 1nF V_{IH}max = VDDLP + 0.5V V_{IH}min = 1.2V at ~40µA V_{IL}max = 0.4V ___|¯ _ _ _ _ high impulse	This signal switches the module ON. This line must be driven high by an open drain or open collector driver connected to VDDLP. See Section 3.3.
Emergency restart	EMERG_RST	I	R_I ≈ 1kΩ, C_I ≈ 1nF V_{OH}max = 1.9V V_{IH}min = 1.35V V_{IL}max = 0.3V ~~|___|~~ low impulse width > 10ms	This line must be driven low by an open drain or open collector driver connected to GND. If unused keep line open.
Fast shutdown	FAST_SHTDWN	I	V_{IL}max = 0.34V V_{IH}min = 1.30V V_{IH}max = 1.90V ~~|___|~~ low impulse width > 10ms	This line must be driven low. If unused keep line open.
RTC backup	VDDLP	I/O	$V_O$norm = 2.3V ±5% $I_O$max = 2mA $V_I$max = 2.4V $V_I$min = 1.0V $I_I$typ = 8µA	It is recommended to use a serial resistor between VDDLP and a possible capacitor. See 3.3.1.1. If unused keep line open.

Table 26: Electrical description of application interface

Function	Signal name	IO	Signal form and level	Comment
SIM card detection	CCIN	I	$R_I \approx 110k\Omega$ V_{IH}min = 1.45V at I = 15µA, V_{IH}max= 1.9V V_{IL}max = 0.3V	CCIN = High, SIM card inserted. If unused keep line open.
3V SIM Card Interface	CCRST	O	V_{OL}max = 0.20V at I = 2mA V_{OH}min = 2.40V at I = -2mA V_{OH}max = 2.90V	Maximum cable length or copper track to SIM card holder should not exceed 100mm.
	CCIO	I/O	V_{IL}max = 0.60V V_{IH}min = 1.95V V_{IH}max = 2.90V V_{OL}max = 0.20V at I = 2mA V_{OH}min = 2.40V at I = -2mA V_{OH}max = 2.90V	
	CCCLK	O	V_{OL}max = 0.20V at I = 2mA V_{OH}min = 2.40V at I = -2mA V_{OH}max = 2.90V	
	CCVCC	O	$V_O$min = 2.80V $V_O$typ = 2.85V $V_O$max = 2.90V $I_O$max = -30mA	
1.8V SIM Card Interface	CCRST	O	V_{OL}max = 0.20V at I = 2mA V_{OH}min = 1.50V at I = -2mA V_{OH}max = 1.90V	
	CCIO	I/O	V_{IL}max = 0.37V V_{IH}min = 1.22V V_{IH}max = 1.90V V_{OL}max = 0.20V at I = 2mA V_{OH}min = 1.50V at I = -2mA V_{OH}max = 1.90V	
	CCCLK	O	V_{OL}max = 0.20V at I = 2mA V_{OH}min = 1.50V at I = -2mA V_{OH}max = 1.90V	
	CCVCC	O	$V_O$min = 1.75V $V_O$typ = 1.80V $V_O$max = 1.85V $I_O$max = -30mA	

Table 26: Electrical description of application interface

Function	Signal name	IO	Signal form and level	Comment
Digital Power Supply	VDIG	I	$V_I$min = 1.75V $V_I$max = 2.90V $I_I$max = 50mA	ASC0, I^2C power supply input. Connect this line to the external power supply voltage V180 or V285.
Serial Interface ASC0	*VDIG must be connected to V180, i.e., VDIG = 1.80V*			If unused keep line open. The lines DTR0, DSR0 and DCD0 are always at the 1.8V voltage level, even if VDIG is connected to V285.
	RXD0	O	V_{OL}max = 0.20V at I = 2mA V_{OH}min = 1.50V at I = -2mA V_{OH}max = 1.90V V_{IL}max = 0.34V V_{IH}min = 1.30V V_{IH}max = 1.90V	
	TXD0	I		
	CTS0	O		
	RTS0	I	V_{IL}max = 0.20V at I = -280µA V_{IH}min = 1.20V at I = -160µA V_{IH}max = 1.90V	
	RING0	O	V_{OL}max = 0.30V at I = 2mA V_{OH}min = 1.40V at I = -40µA V_{OH}max = 1.90V	
	DTR0	I	V_{OL}max = 0.20V at I = 2mA V_{OH}min = 1.50V at I = -2mA V_{OH}max = 1.90V V_{IL}max = 0.34V V_{IH}min = 1.30V V_{IH}max = 1.90V	
	DSR0	O		
	DCD0	O		
	VDIG connected to V285, i.e., VDIG = 2.85V			
	RXD0	O	V_{OL}max = 0.20V at I = 2mA V_{OH}min = 2.40V at I = -2mA V_{OH}max = 2.90V V_{IL}max = 0.56V V_{IH}min = 2.05V V_{IH}max = 2.90V	
	TXD0	I		
	CTS0	O		
	RTS0	I	V_{IL}max = 0.30V at I = -380µA V_{IH}min = 1.96V at I = -80µA V_{IH}max = 2.90V	
	RING0	O	V_{OL}max = 0.30V at I = 2mA V_{OH}min = 2.40V at I = -40µA V_{OH}max = 2.90V	
Serial Interface ASC1	RXD1	O	V_{OL}max = 0.20V at I = 2mA V_{OH}min = 1.50V at I = -2mA V_{OH}max = 1.90V V_{IL}max = 0.34V V_{IH}min = 1.30V V_{IH}max = 1.90V	If unused keep line open.
	TXD1	I		
	RTS1	I		
	CTS1	O		

Table 26: Electrical description of application interface

Function	Signal name	IO	Signal form and level	Comment
I^2C	*VDIG connected to V180, i.e., VDIG = 1.80V*			I2CDAT is configured as Open Drain and needs a pull-up resistor in the host application. According to the I^2C Bus Specification Version 2.1 for the fast mode a rise time of max. 300ns is permitted. There is also a maximum V_{OL}=0.4V at 3mA specified. The value of the pull-up depends on the capacitive load of the whole system (I^2C Slave + lines). The maximum sink current of I2CDAT and I2CCLK is 4mA. If lines are unused keep lines open.
	I2CCLK	O	V_{OL}min = 0.4V at I = -3mA	
	I2CDAT	IO	V_{IL}max = 0.5V V_{IH}min = 1.3V V_{IH}max = 2.25V Rpullup >= 470Ω	
	VDIG connected to V285, i.e., VDIG = 2.85V			
	I2CCLK	O	V_{OL}min = 0.4V at I = -3mA	
	I2CDAT	IO	V_{IL}max = 0.8V V_{IH}min = 2.1V V_{IH}max = 3.3V Rpullup >= 820Ω	

Table 26: Electrical description of application interface

Function	Signal name	IO	Signal form and level	Comment
GPIO interface	GPIO5	IO	V_{OL}max = 0.20V at I = 2mA V_{OH}min = 1.50V at I = -2mA V_{OH}max = 1.90V V_{IL}max = 0.34V V_{IH}min = 1.30V V_{IH}max = 1.90V	If unused keep line open. Please note that some GPIO lines can be used for functions other than GPIO - configured by AT command: Status LED line: GPIO5, PWM: GPIO6/GPIO7, Jamming indicator: GPIO6 I^2C: GPIO9/GPIO10. GPIO9 has an open drain output functionality only, but with an internal 5kΩ pull up . With VDIG connected to V180 the minimum value of this external resistor should be 860Ω. With VDIG connected to V285 the minimum value should be 1.5kΩ. GPIO10 also has an open drain output functionality only and will need an external pull-up resistor. With VDIG connected to V180 the minimum value of this external resistor should be 750Ω. With VDIG connected to V285 the minimum value should be 1.1kΩ. For further details see Section 3.13, Section 3.14, Section 3.15, Section 3.18, Section 3.18
	GPIO6	IO		
	GPIO7	IO		
	GPIO8	IO		
	VDIG connected to V180, i.e., VDIG = 1.80V			
	GPIO9, i.e., I2CCLK	IO	Input, Open Drain Output $R_I \approx 5k\Omega$ (internal Pull up) V_{OL}min = 0.4V at I = -3mA V_{OH}max = 1.90V	
	GPIO10, i.e., I2CDAT	IO	Input, Open Drain Output (no Pull up) V_{IL}max = 0.5V V_{IH}min = 1.3V V_{IH}max = 2.20V V_{OL}min = 0.4V at I = -3mA	
	VDIG connected to V285, i.e., VDIG = 2.85V			
	GPIO9, i.e., I2CCLK	IO	Input, Open Drain Output $R_I \approx 5k\Omega$ (internal Pull up) V_{OL}min = 0.4V at I = -3mA V_{OH}max = 2.90V	
	GPIO10, i.e., I2CDAT	IO	Input, Open Drain Output (no Pull up) V_{IL}max = 0.8V V_{IH}min = 2.1V V_{IH}max = 3.3V V_{OL}min = 0.4V at I = -3mA	

Table 26: Electrical description of application interface

Function	Signal name	IO	Signal form and level	Comment
Analog audio interface	VMIC	O	$V_O$typ = 2.2V I_{max} = 4 mA	Microphone supply for customer feeding circuits If unused keep line open.
	EPP	O	Differential, Typ. 3.4Vpp at 16Ω load Typ. 4.5Vpp at no load PCM level = +3dBm0, 1.02 kHz sine wave	Balanced output for ear-phone or balance output for line out If unused keep line open.
	EPN	O		
	MICP	I	$Z_I$typ = 50kΩ || 10nF Vinmax = 0.8Vpp (for 3dBm0 @ 0dB gain)	Balanced differential microphone with external feeding circuit (using VMIC and AGND) or balanced differential line input. Use coupling capacitors. If unused keep lines open.
	MICN	I		
	AGND		Analog Ground	GND level for external audio circuits. If unused keep line open.
Digital audio interface (PCM/I²S)	*VDIG connected to V180, i.e., VDIG = 1.80V*			If unused keep pin open.
	TFSDAI	O	V_{OL}max = 0.20V at I = 2mA V_{OH}min = 1.50V at I = -2mA V_{OH}max = 1.90V	
	SCLK	O		
	TXDDAI	O		
	RXDDAI	I	V_{IL}max = 0.34V V_{IH}min = 1.30V V_{IH}max = 1.90V	
	VDIG connected to V285, i.e., VDIG = 2.85V			
	TFSDAI	O	V_{OL}max = 0.20V at I = 2mA V_{OH}min = 2.40V at I = -2mA V_{OH}max = 2.90V	
	SCLK	O		
	TXDDAI	O		
	RXDDAI	I	V_{IL}max = 0.56V V_{IH}min = 2.05V V_{IH}max = 2.90V	
ADC (Analog-to-Digital Converter)	ADC1_IN	I	R_I = 1MΩ V_I = 0V ... 1.2V, V_{IH} max = 3.3V	If unused keep line open.

5.5 Power Supply Ratings

Table 27 and Table 28 assemble various voltage supply and current consumption ratings of the module.

Table 27: Voltage supply ratings

Parameter	Description	Conditions	Min	Typ	Max	Unit
$BATT+_{BB}$ $BATT+_{RF}$	Supply voltage	Directly measured at module. Voltage must stay within the min/max values, including voltage drop, ripple, spikes.	3.3		4.5	V
	Maximum allowed voltage drop during transmit burst	Normal condition, power control level for $P_{out\ max}$			400	mV
	Voltage ripple	Normal condition, power control level for $P_{out\ max}$ @ f≤250kHz @ f>250kHz			 85 25	mV_{pp}

Table 28: Current consumption ratings[1]

Parameter	Description	Conditions	Typ	Unit
I_{VDDLP}	OFF state supply current	RTC backup @ BATT+ = 0V @ VDDLP = 2.3V	8.0	µA
I_{BATT+} (i.e., sum of $BATT+_{BB}$ and $BATT+_{RF}$)	OFF state supply current	Power Down mode	45	µA
	Average supply current	SLEEP mode, GSM[2] @ DRX = 2 @ DRX = 5 @ DRX = 9	 2.1 1.5 1.1	mA
		SLEEP mode, GPRS[2] @ DRX = 2 @ DRX = 5 @ DRX = 9	 2.2 1.5 1.2	mA
		IDLE mode [2]	8.6	mA
		TALK mode GSM GSM 850/EGSM 900[3] GSM 1800/1900[4]	 200 150	mA
		DATA mode GPRS 1 TX, 4 Rx GSM 850/EGSM 900[3] GSM 1800/1900[4]	 180 145	mA
		DATA mode GPRS 2 Tx, 3 Rx GSM 850/EGSM 900[3] GSM 1800/1900[4]	 330 260	mA

Table 28: Current consumption ratings[1]

Parameter	Description	Conditions		Typ	Unit
I_{BATT+} (i.e., sum of $BATT+_{BB}$ and $BATT+_{RF}$)	Peak current during GSM transmit burst	GSM 850/EGSM 900[3]	@50Ω	1.30	A
			@Total mismatch	1.35	
		GSM 1800/1900[4]	@50Ω	0.95	
			@Total mismatch	0.97	

1. GSM850 and GSM1900 bands are applicable for the quad band module variant BGS2-W only.
2. Measurements start 6 minutes after the module was switched ON,
   Averaging times: SLEEP mode - 3 minutes; IDLE mode - 1.5 minutes,
   Communication tester settings: no neighbour cells, no cell reselection etc.
3. Power control level PCL 5
4. Power control level PCL 0

5.6 Electrical Characteristics of the Voiceband Part

5.6.1 Setting Audio Parameters by AT Commands

The audio modes 2 to 6 can be adjusted according to the parameters listed below. Each audio mode is assigned a separate set of parameters.

Table 29: Audio parameters adjustable by AT command

Parameter	Influence to	Range	Gain range	Calculation
inBbcGain	MICP/MICN analog amplifier gain of baseband controller before ADC	0...7	0...39dB	6dB steps, 3dB between step 6 and 7
inCalibrate	Digital attenuation of input signal after ADC	0...32767	-∞...0dB	20 * log (inCalibrate/ 32768)
outBbcGain	EPP/EPN analog output gain of baseband controller after DAC	0...3	0...-18dB	6dB steps
outCalibrate[n] n = 0...4	Digital attenuation of output signal after speech decoder, before summation of sidetone and DAC present for each volume step[n]	0...32767	-∞...+6dB	20 * log (2 * outCalibrate[n]/ 32768)
sideTone	Digital attenuation of sidetone is corrected internally by outBbcGain to obtain a constant sidetone independent of output volume[1]	0...32767	-∞...0dB	20 * log (sideTone/ 32768)

1. Note: I f queried by AT command, the configured dB value of the <sideTone> parameter is not displayed, but the measurable gain between MICP/MICN and EPP/EPN. The displayed gain is the sum of gains (in dB) between ADC, <inBbcGain>, <inCalibrate>, <sideTone>, <outBbcGain>, DAC and the frequency response correction filters. For more information see also Section 5.6.2 and [1].

Note: The parameters inCalibrate, outCalibrate and sideTone accept also values from 32768 to 65535. These values are internally truncated to 32767.

5.6.2 Audio Programming Model

The audio programming model shows how the signal path can be influenced by varying the AT command parameters.

The parameters <inBbcGain> and <inCalibrate> can be set with AT^SNFI. All the other parameters are adjusted with AT^SNFO and AT^SAIC.

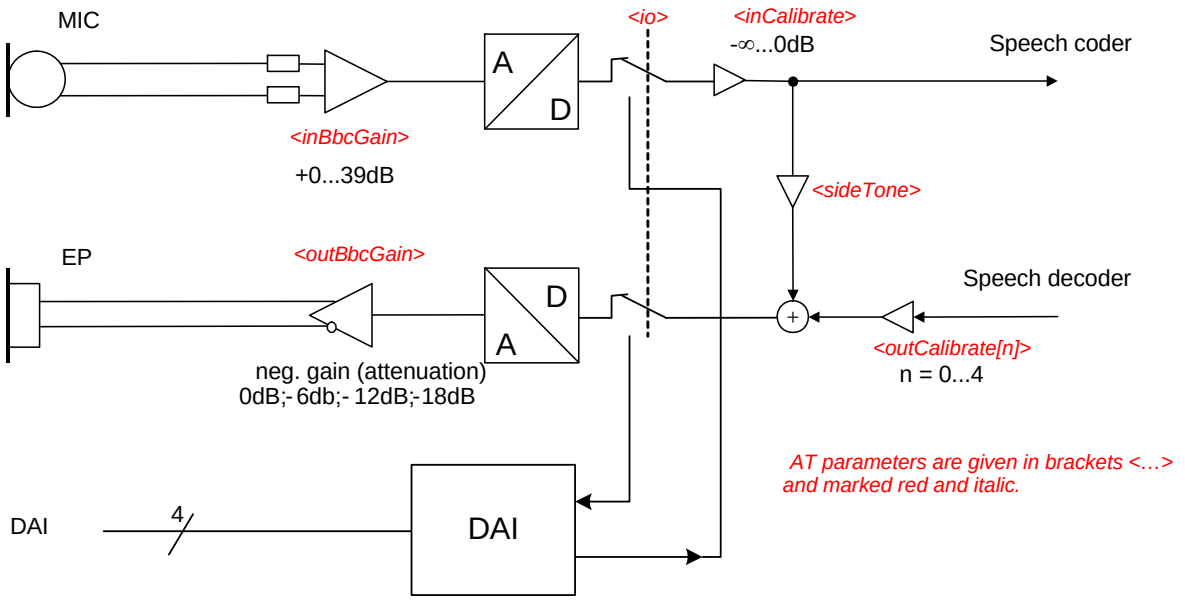


Figure 47: Audio programming model

5.6.3 Characteristics of Audio Modes

The electrical characteristics of the voiceband part depend on the current audio mode set with the AT^SNFS command.

Table 30: Voiceband characteristics (typical)

Audio mode no. AT^SNFS=	**1** (Default settings, not adjustable)	**2**	**3**	**4**	**5**	**6**
Name	Default Handset	Basic Handsfree	Headset	User Handset	Plain Codec	DTMF
Purpose	DSB with Votronic handset	Car Kit	Headset	DSB with individual handset	Direct access to speech coder	Tip and Ring interface for DTMF end-to-end transmission
Gain setting via AT command. Defaults: inBbcGain outBbcGain	Fix 4 (24dB) 0 (0dB)	Adjustable 1 (6dB) 2 (-12dB)	Adjustable 6 (36dB) 2 (-12dB)	Adjustable 4 (24dB) 0 (0dB)	Adjustable 0 (0dB) 0 (0dB)	Adjustable 0 (0dB) 1 (-6dB)
Power supply	ON (2.2V)	ON (2.2V)	ON (2.2V)	ON (2.2V)	ON (2.2V)	ON (2.2V)
Sidetone	ON	--	Adjustable	Adjustable	Adjustable	Adjustable
Volume control	OFF	Adjustable	Adjustable	Adjustable	Adjustable	Adjustable
Echo control (send)	Cancella-tion	Cancella-tion	Cancella-tion	Cancella-tion	--	Line echo cancellation
Noise suppression[1]	12dB	12dB	12dB	12dB	--	--
MIC input signal for 0dBm0 @ 1024 Hz (default gain)	16mV	130mV	7.5mV[2]	16mV	275mV	275mV
EP output signal in mV rms. @ 0dBm0, 1024 Hz, no load (default gain); @ 3.14 dBm0	500mV	160mV	230mV	500mV	1160mV 4.5Vpp	520mV
Sidetone gain at default settings[3]	20dB	-∞	17dB	20dB	-∞	-∞

1. In audio modes with noise reduction, the microphone input signal for 0dBm0 shall be measured with a sine burst signal for a tone duration of 5 seconds and a pause of 2 sec. The sine signal appears as noise and, after approx. 12 sec, is attenuated by the noise reduction by up to 12dB.
2. Signal for -2dBm0 (due to attenuation of uplink filter at 1kHz)
3. The gain in this case specifies the typical, overall sidetone gain measured from MICP/MICN to EPP/EPN in the specific audio mode at 1000Hz (cp. Figure 47).

Note: With regard to acoustic shock, the cellular application must be designed to avoid sending false AT commands that might increase amplification, e.g. for a high sensitive earpiece. A protection circuit should be implemented in the cellular application.

5.6.4 Voiceband Receive Path

Test conditions:

- The values specified below were tested to 1kHz and 0dB gain stage, unless otherwise stated.
- Parameter setup: gs = 0dB means audio mode = 5 for EPP to EPN, inBbcGain= 0, inCalibrate = 32767, outBbcGain = 0, OutCalibrate = 16384, sideTone = 0.

Table 31: Voiceband receive path

Parameter	Min	Typ	Max	Unit	Test condition/remark
Differential output voltage (peak to peak)		3.4 4.5		Vpp	16Ω, no load, from EPPx to EPNx *gs* = 0dB @ 3.14dBm0
Differential output gain settings (*gs*) at 6dB stages (outBbcGain)	-18		0	dB	Set with AT^SNFO
Fine scaling by DSP (outCalibrate)	-∞		+6	dB	Set with AT^SNFO
Output differential DC offset	-50		+50	mV	*gs* = 0dB, outBbcGain = 0 and -6dB
Differential output load resistance	14			Ω	from EPP to EPN
Allowed single ended load capacitance			150	pF	from EPP or EPN to AGND
Absolute gain drift	-5		+5	%	Variation due to change in temperature and life time
Passband ripple			0.5	dB	for f < 3600 Hz
Stopband attenuation	50			dB	for f > 4600 Hz

gs = gain setting

5.6.5 Voiceband Transmit Path

Test conditions:

- The values specified below were tested to 1kHz and 0dB gain stage, unless otherwise stated.
- Parameter setup: Audio mode = 5 for MICP to MICN, inBbcGain= 0, inCalibrate = 32767, outBbcGain = 0, OutCalibrate = 16384, sideTone = 0

Table 32: Voiceband transmit path

Parameter	Min	Typ	Max	Unit	Test condition/Remark
Input voltage (peak to peak) MICP to MICN			0.8	V	
Input amplifier gain in 6dB steps (inBbcGain)[1]	0		39	dB	Set with AT^SNFI
Fine scaling by DSP (inCalibrate)	-∞		0	dB	Set with AT^SNFI
Input impedance MIC		50		kΩ	
Microphone supply voltage		2.2		V	
Microphone supply current			4	mA	

1. 3dB step between inBbcGain 6 and 7.

5.7 Antenna Interface Specification

Measurement conditions: T_{amb}= 25°C, $V_{BATT+\ nom}$ = 4.1V.

Table 33: Antenna interface specifications[1]

Parameter		Min	Typ	Max	Unit
Frequency range Uplink (MS → BTS)	GSM 850	824		849	MHz
	E-GSM 900	880		915	MHz
	GSM 1800	1710		1785	MHz
	GSM 1900	1850		1910	MHz
Frequency range Downlink (BTS → MS)	GSM 850	869		894	MHz
	E-GSM 900	925		960	MHz
	GSM 1800	1805		1880	MHz
	GSM 1900	1930		1990	MHz
Receiver input sensitivity @ ARP Under all propagation conditions according to GSM specification	GSM 850	-102			dBm
	E-GSM 900	-102			dBm
	GSM 1800	-102			dBm
	GSM 1900	-102			dBm
Receiver input sensitivity @ ARP BER Class II <= 2.43% @ static input level (no fading)	GSM 850		-107		dBm
	E-GSM 900		-107		dBm
	GSM 1800		-107		dBm
	GSM 1900		-107		dBm
RF power @ ARP with 50Ω load	GSM 850	31	33	35	dBm
	E-GSM 900	31	33	35	dBm
	GSM 1800	28	30	32	dBm
	GSM 1900	28	30	32	dBm

1. GSM850 and GSM1900 bands are applicable for the quad band module variant BGS2-W only.

5.8 Electrostatic Discharge

The GSM module is not protected against Electrostatic Discharge (ESD) in general. Consequently, it is subject to ESD handling precautions that typically apply to ESD sensitive components. Proper ESD handling and packaging procedures must be applied throughout the processing, handling and operation of any application that incorporates a BGS2-E/BGS2-W module.

Special ESD protection provided on BGS2-E/BGS2-W:
- SIM interface: Serial resistor and ESD protection diode

BGS2-E/BGS2-W has been tested according to group standard ETSI EN 301 489-1 (see Table 3) and test standard EN 61000-4-2. Electrostatic values can be gathered from the following table.

Table 34: Electrostatic values

Specification/Requirements	Contact discharge	Air discharge
EN 61000-4-2		
SIM interface	± 4kV	± 8kV
Antenna interface	± 4kV	± 8kV
JEDEC JESD22-A114D (Human Body Model, Test conditions: 1.5 kΩ, 100 pF)		
ESD at the module	± 1kV	n.a.

Note: The values may vary with the individual application design. For example, it matters whether or not the application platform is grounded over external devices like a computer or other equipment, such as the Gemalto reference application described in Chapter 8.

6 Mechanics, Mounting and Packaging

The following sections describe the mechanical dimensions of BGS2-E/BGS2-W and give recommendations for integrating BGS2-E/BGS2-W into the host application.
Additional information can be found in a number of files containing Gerber data for the external application footprint and product model data in STEP format. These data are zipped in an extra file package supplied along with the BGS2-E/BGS2-W documentation package. To open these files commonly used Gerber and STEP viewers may be employed. The file package is named ags2_bgs2_gerber_stp_v01.7z.

6.1 Mechanical Dimensions of BGS2-E/BGS2-W

Figure 48 shows the top and bottom view of BGS2-E/BGS2-W and provides an overview of the board's mechanical dimensions. For further details see Figure 49.

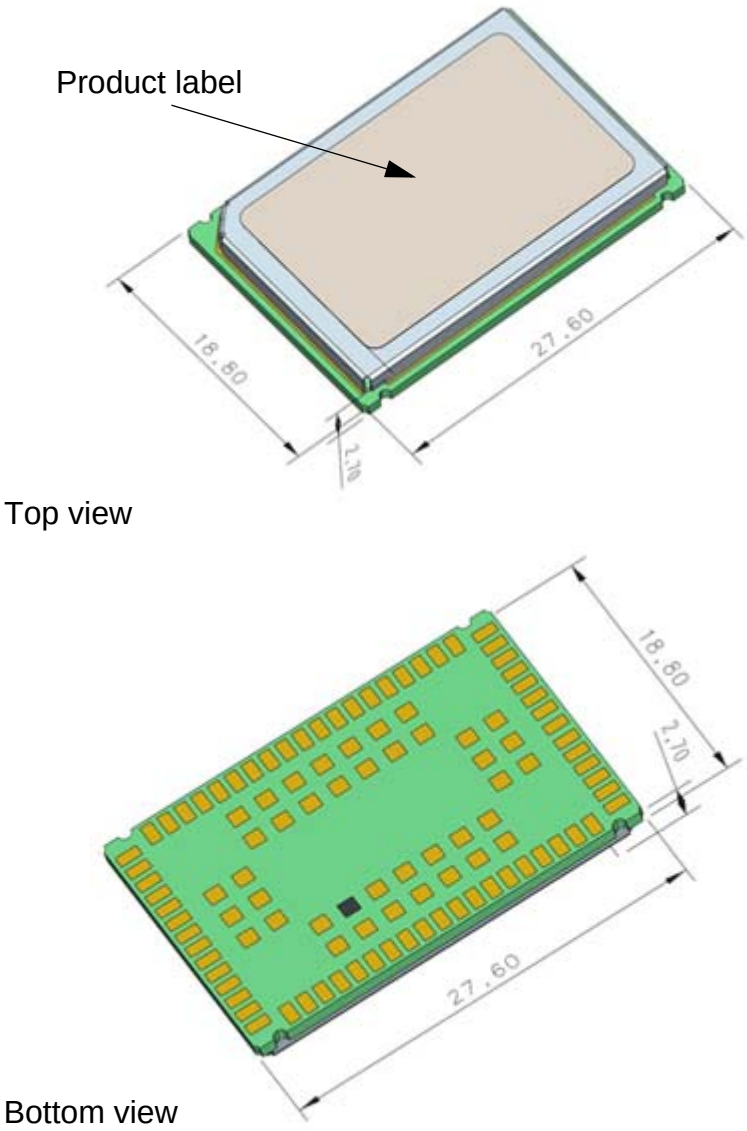


Figure 48: BGS2-E/BGS2-W– top and bottom view

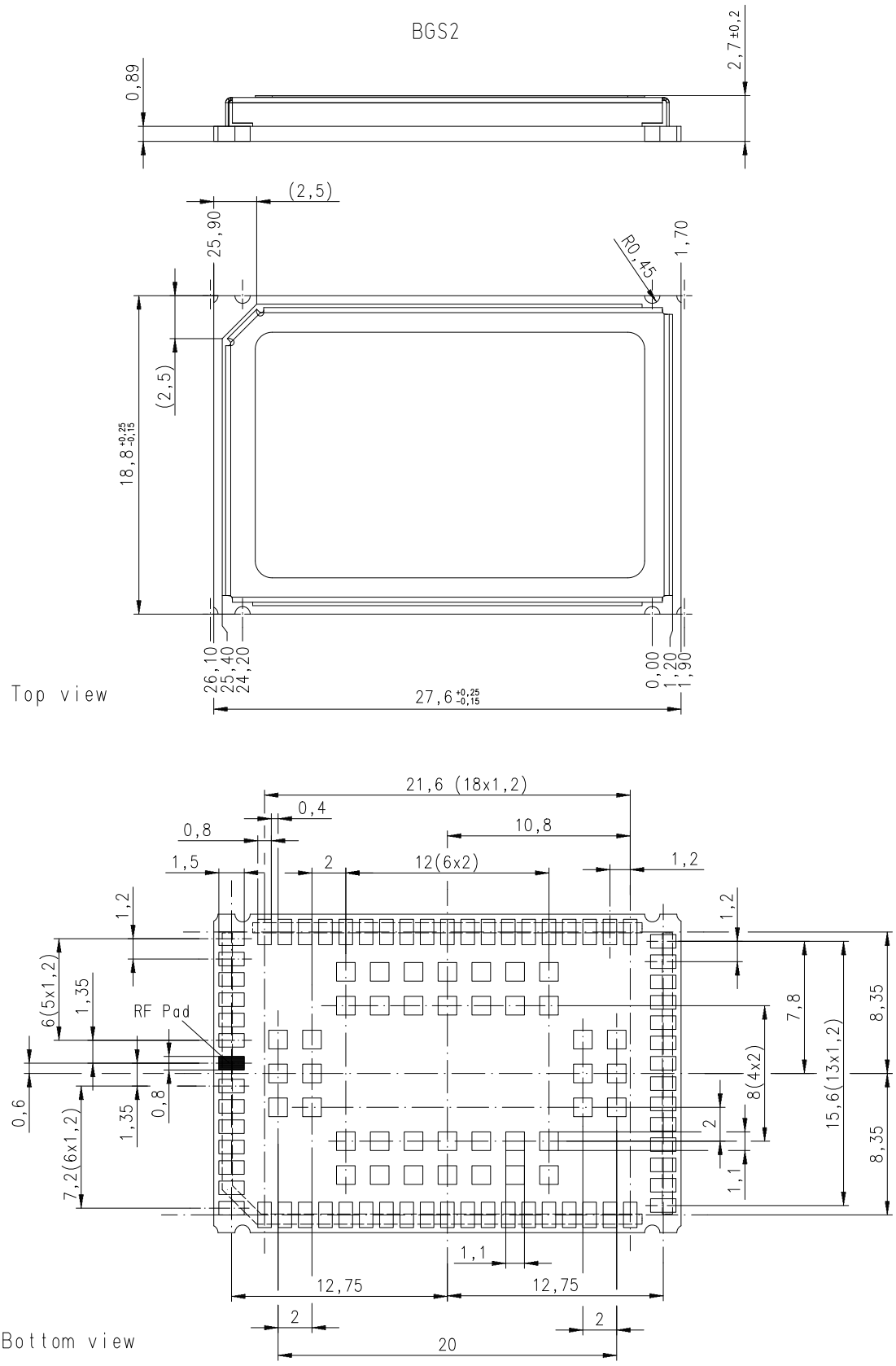


Figure 49: Dimensions of BGS2-E/BGS2-W (all dimensions in mm)

6.2 Mounting BGS2-E/BGS2-W onto the Application Platform

This section describes how to mount BGS2-E/BGS2-W onto the PCBs (=printed circuit boards), including land pattern and stencil design, board-level characterization, soldering conditions, durability and mechanical handling. For more information on issues related to SMT module integration see also [6].

Note: To avoid short circuits between signal tracks on an external application's PCB and various markings at the bottom side of the module, it is recommended not to route the signal tracks on the top layer of an external PCB directly under the module, or at least to ensure that signal track routes are sufficiently covered with solder resist.

6.2.1 SMT PCB Assembly

6.2.1.1 Land Pattern and Stencil

The land pattern and stencil design as shown below is based on Gemalto characterizations for lead-free solder paste on a four-layer test PCB and a 110 respectively 150 micron thick stencil.

The land pattern given in Figure 50 reflects the module‘s pad layout, including signal pads and ground pads (for pad assignment see Section 5.4).

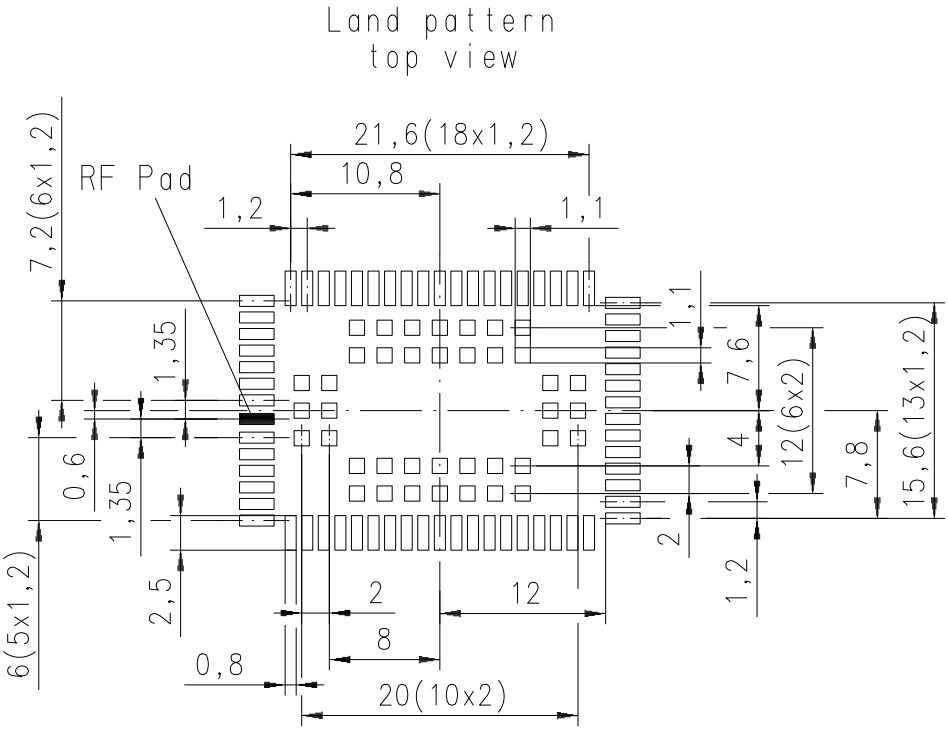


Figure 50: Land pattern (top view)

The stencil designs illustrated in the below figures are the result of extensive tests with Gemalto M2M Daisy Chain modules. Please note however that it is strongly recommended to use the 150µm thick stencil shown in Figure 52 on the customer application PCB. The tests conducted by Gemalto with different stencil thicknesses have shown that the 150µm thick stencil has yielded the most consistent soldering results, and ensures best solder connectivity between the external application's PCB and the module, especially if there is considerable gapping between the application PCB and the module.

The central ground pads are primarily intended for stabilizing purposes, and may show some more voids than the application interface pads at the module's rim. This is acceptable, since they are electrically irrelevant.

Note that depending on coplanarity or other properties of the external PCB, it could be that all of the central ground pads may have to be soldered. For this reason the land pattern design shown in Figure 50 provides for both of these alternatives and only a modification of the stencil may be needed.

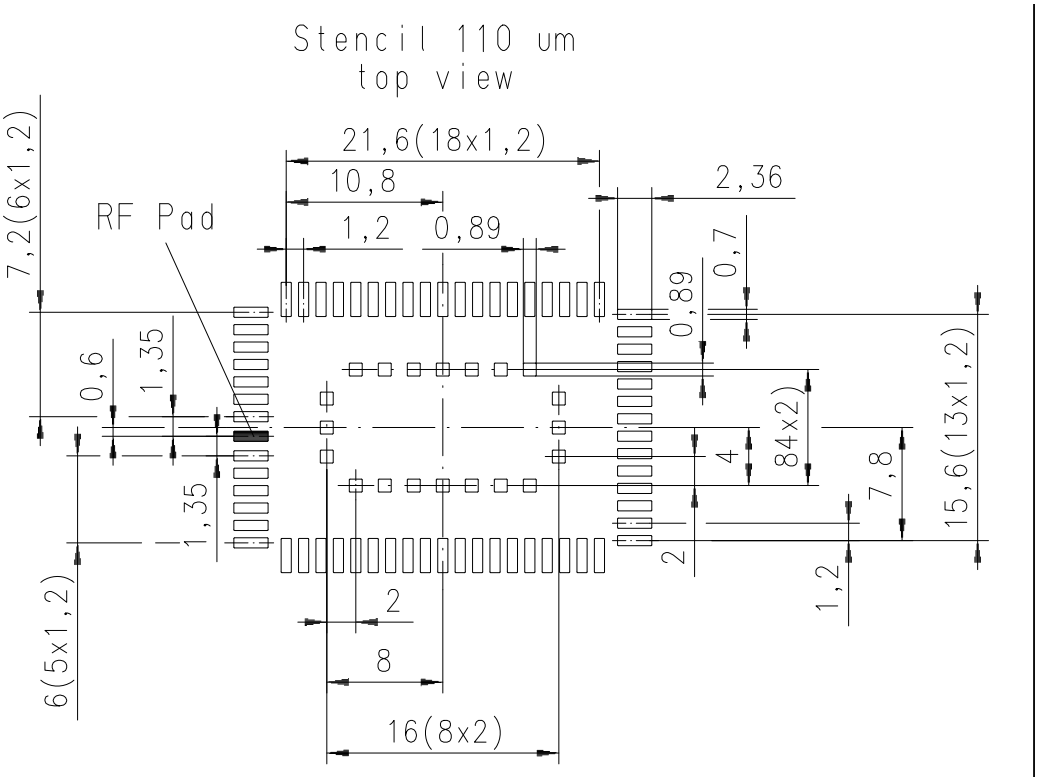


Figure 51: Design for 110 micron thick stencil (top view)

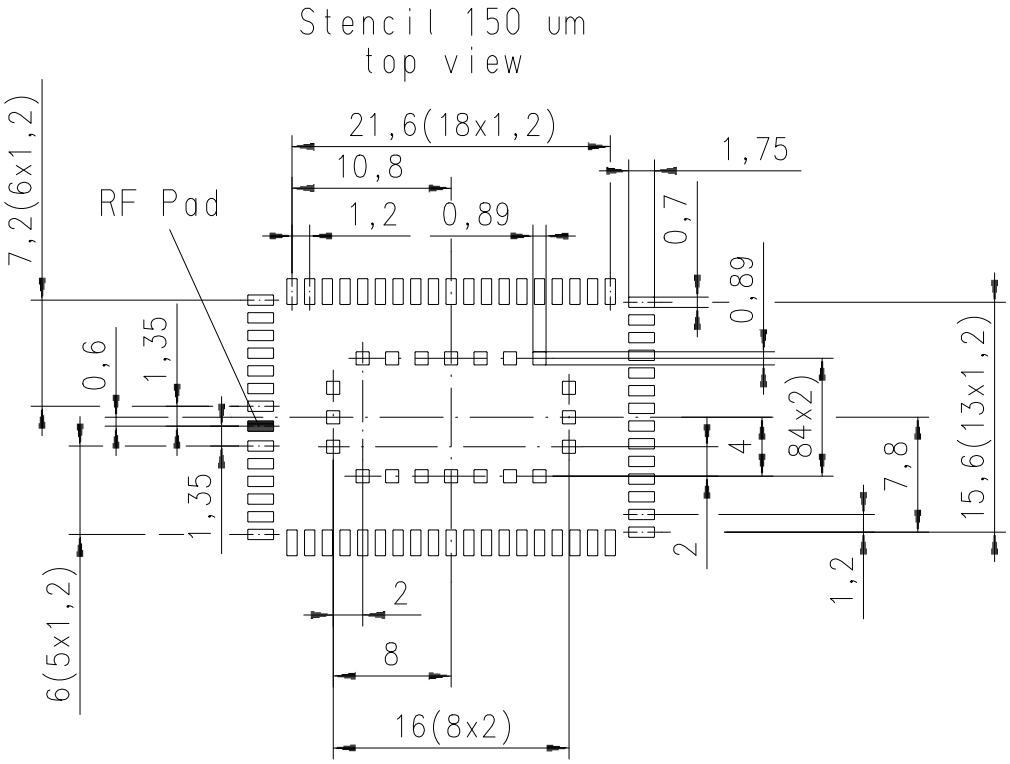


Figure 52: Recommended design for 150 micron thick stencil (top view)

6.2.1.2 Board Level Characterization

Board level characterization issues should also be taken into account if devising an SMT process.

Characterization tests should attempt to optimize the SMT process with regard to board level reliability. This can be done by performing the following physical tests on sample boards: Peel test, bend test, tensile pull test, drop shock test and temperature cycling. Sample surface mount checks are described in [6].

It is recommended to characterize land patterns before an actual PCB production, taking individual processes, materials, equipment, stencil design, and reflow profile into account. For land and stencil pattern design recommendations see also Section 6.2.1.1. Optimizing the solder stencil pattern design and print process is necessary to ensure print uniformity, to decrease solder voids, and to increase board level reliability.

Daisy chain modules for SMT characterization are available on request. For details refer to [6].

Generally, solder paste manufacturer recommendations for screen printing process parameters and reflow profile conditions should be followed. Maximum ratings are described in Section 6.2.3.

6.2.2 Moisture Sensitivity Level

BGS2-E/BGS2-W comprises components that are susceptible to damage induced by absorbed moisture.

Gemalto M2M's BGS2-E/BGS2-W module complies with the latest revision of the IPC/JEDEC J-STD-020 Standard for moisture sensitive surface mount devices and is classified as MSL 4.

For additional MSL (=moisture sensitivity level) related information see Section 6.2.4 and Section 6.3.2.

6.2.3 Soldering Conditions and Temperature

6.2.3.1 Reflow Profile

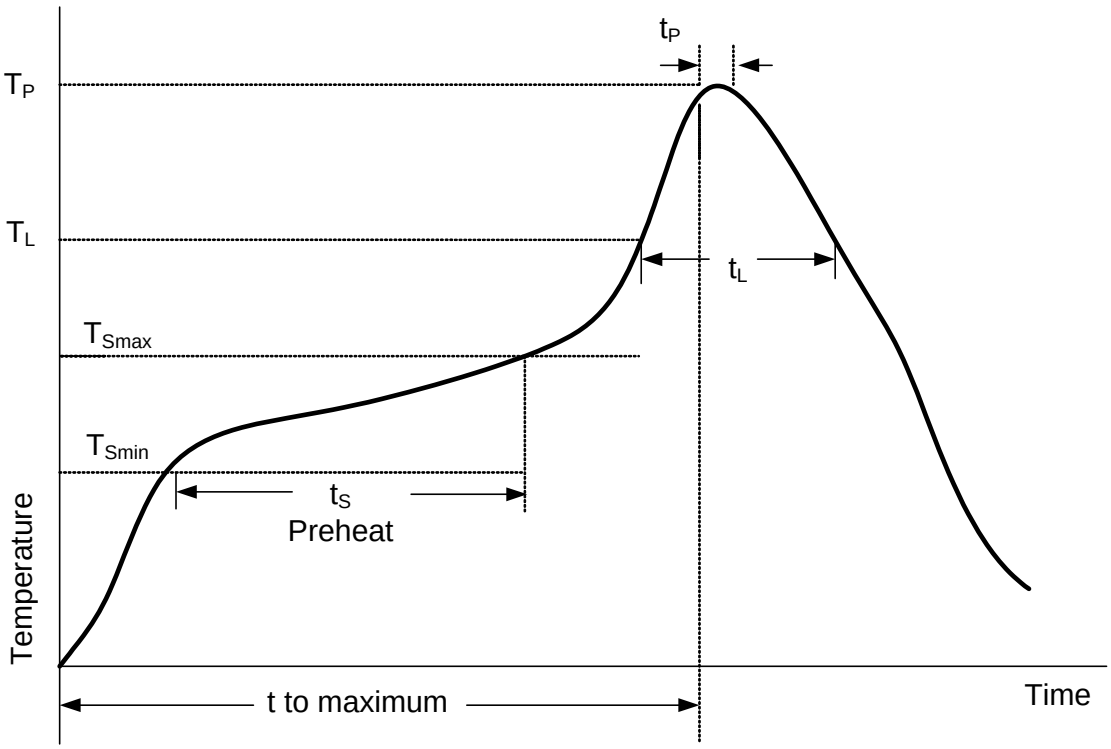


Figure 53: Reflow Profile

Table 35: Reflow temperature ratings[1]

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature Minimum (T_{Smin}) Temperature Maximum (T_{Smax}) Time (t_{Smin} to t_{Smax}) (t_S)	 150°C 200°C 60-120 seconds
Average ramp up rate (T_L to T_P)	3K/second max.

Table 35: Reflow temperature ratings[1]

Profile Feature	Pb-Free Assembly
Liquidous temperature (T_L) Time at liquidous (t_L)	217°C 60-90 seconds
Peak package body temperature (T_P)	245°C +0/-5°C
Time (t_P) within 5 °C of the peak package body temperature (T_P)	30 seconds max.
Average ramp-down rate (T_P to T_L)	1 K/second max.
Time 25°C to maximum temperature	8 minutes max.

1. Please note that the reflow profile features and ratings listed above are based on the joint industry standard IPC/JEDEC J-STD-020D.1, and are as such meant as a general guideline. For more information on reflow profiles and their optimization please refer to [6].

6.2.3.2 Maximum Temperature and Duration

The following limits are recommended for the SMT board-level soldering process to attach the module:

- A maximum module temperature of 245°C. This specifies the temperature as measured at the module's top side.
- A maximum duration of 30 seconds at this temperature.

Please note that while the solder paste manufacturers' recommendations for best temperature and duration for solder reflow should generally be followed, the limits listed above must not be exceeded.

BGS2-E/BGS2-W is specified for one soldering cycle only. Once BGS2-W is removed from the application, the module will very likely be destroyed and cannot be soldered onto another application.

6.2.4 Durability and Mechanical Handling

6.2.4.1 Storage Conditions

BGS2-E/BGS2-W modules, as delivered in tape and reel carriers, must be stored in sealed, moisture barrier anti-static bags. The conditions stated below are only valid for modules in their original packed state in weather protected, non-temperature-controlled storage locations. Normal storage time under these conditions is 12 months maximum.

Table 36: Storage conditions

Type	Condition	Unit	Reference
Air temperature: Low High	-25 +40	°C	IPC/JEDEC J-STD-033A
Humidity relative: Low High	10 90 at 40°C	%	IPC/JEDEC J-STD-033A
Air pressure: Low High	70 106	kPa	IEC TR 60271-3-1: 1K4 IEC TR 60271-3-1: 1K4
Movement of surrounding air	1.0	m/s	IEC TR 60271-3-1: 1K4
Water: rain, dripping, icing and frosting	Not allowed	---	---
Radiation: Solar Heat	1120 600	W/m^2	ETS 300 019-2-1: T1.2, IEC 60068-2-2 Bb ETS 300 019-2-1: T1.2, IEC 60068-2-2 Bb
Chemically active substances	Not recommended		IEC TR 60271-3-1: 1C1L
Mechanically active substances	Not recommended		IEC TR 60271-3-1: 1S1
Vibration sinusoidal: Displacement Acceleration Frequency range	 1.5 5 2-9 9-200	 mm m/s^2 Hz	IEC TR 60271-3-1: 1M2
Shocks: Shock spectrum Duration Acceleration	 semi-sinusoidal 1 50	 ms m/s^2	IEC 60068-2-27 Ea

6.2.4.2 Processing Life

BGS2-E/BGS2-W must be soldered to an application within 72 hours after opening the MBB (=moisture barrier bag) it was stored in.

As specified in the IPC/JEDEC J-STD-033 Standard, the manufacturing site processing the modules should have ambient temperatures below 30°C and a relative humidity below 60%.

6.2.4.3 Baking

Baking conditions are specified on the moisture sensitivity label attached to each MBB (see Figure 58 for details):

- It is *not necessary* to bake BGS2-E/BGS2-W, if the conditions specified in Section 6.2.4.1 and Section 6.2.4.2 were not exceeded.
- It is *necessary* to bake BGS2-E/BGS2-W, if any condition specified in Section 6.2.4.1 and Section 6.2.4.2 was exceeded.

If baking is necessary, the modules must be put into trays that can be baked to at least 125°C. Devices should not be baked in tape and reel carriers at any temperature.

6.2.4.4 Electrostatic Discharge

ESD (=electrostatic discharge) may lead to irreversable damage for the module. It is therefore advisable to develop measures and methods to counter ESD and to use these to control the electrostatic environment at manufacturing sites.

Please refer to Section 5.8 for further information on electrostatic discharge.

6.3 Packaging

6.3.1 Tape and Reel

The single-feed tape carrier for BGS2-E/BGS2-W is illustrated in Figure 54. The figure also shows the proper part orientation. The tape width is 44 mm and the BGS2-W modules are placed on the tape with a 28-mm pitch. The reels are 330 mm in diameter with a core diameter of 100 mm. Each reel contains 500 modules.

6.3.1.1 Orientation

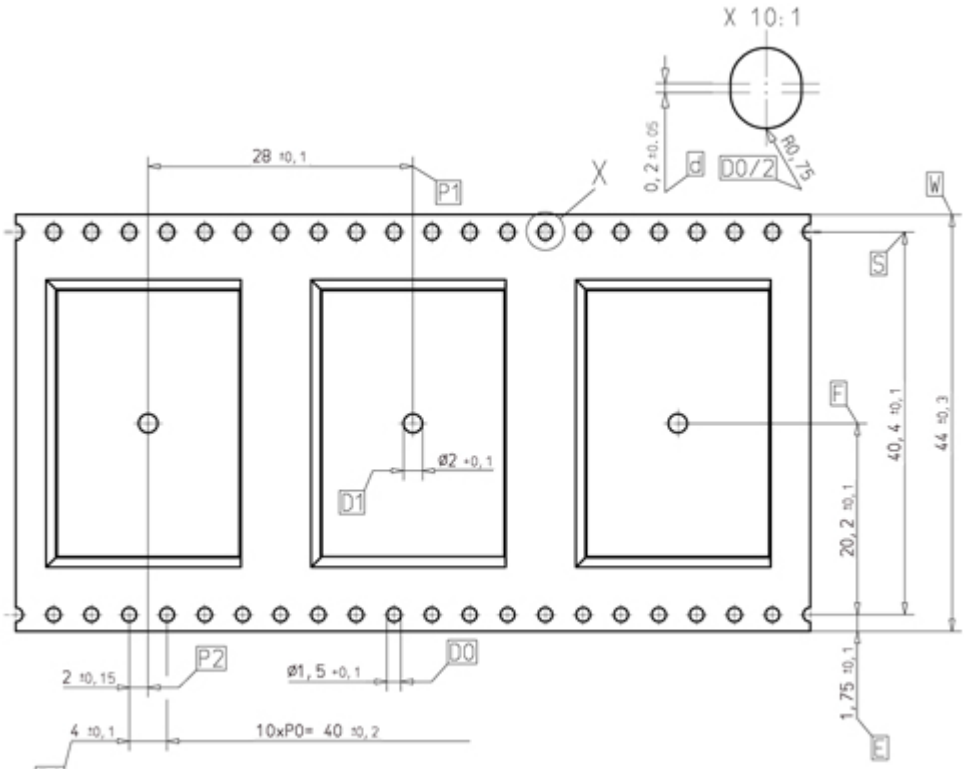


Figure 54: Carrier tape

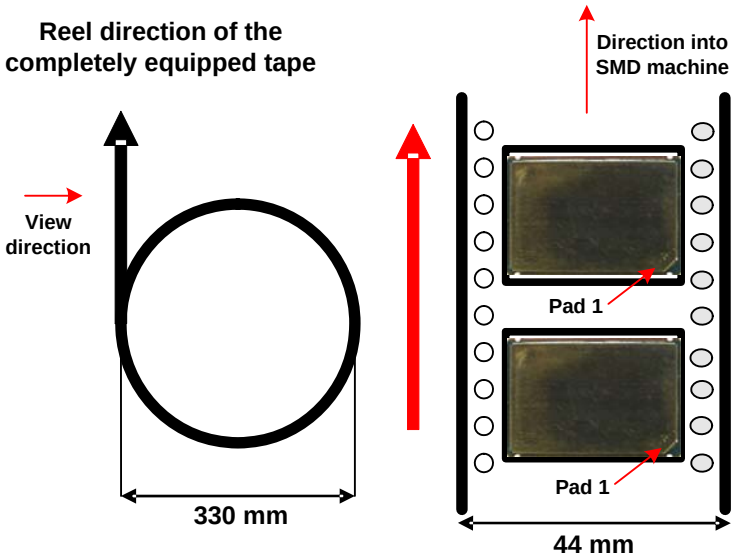


Figure 55: Reel direction

6.3.1.2 Barcode Label

A barcode label provides detailed information on the tape and its contents. It is attached to the reel.

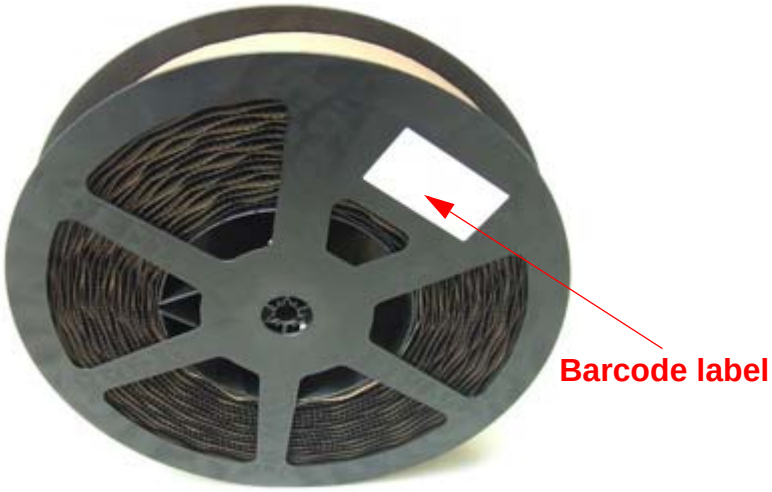


Figure 56: Barcode label on tape reel

6.3.2 Shipping Materials

BGS2-E/BGS2-W is distributed in tape and reel carriers. The tape and reel carriers used to distribute BGS2-E/BGS2-W are packed as described below, including the following required shipping materials:

- Moisture barrier bag, including desiccant and humidity indicator card
- Transportation box

6.3.2.1 Moisture Barrier Bag

The tape reels are stored inside an MBB (=moisture barrier bag), together with a humidity indicator card and desiccant pouches - see Figure 57. The bag is ESD protected and delimits moisture transmission. It is vacuum-sealed and should be handled carefully to avoid puncturing or tearing. The bag protects the BGS2-E/BGS2-W modules from moisture exposure. It should not be opened until the devices are ready to be soldered onto the application.

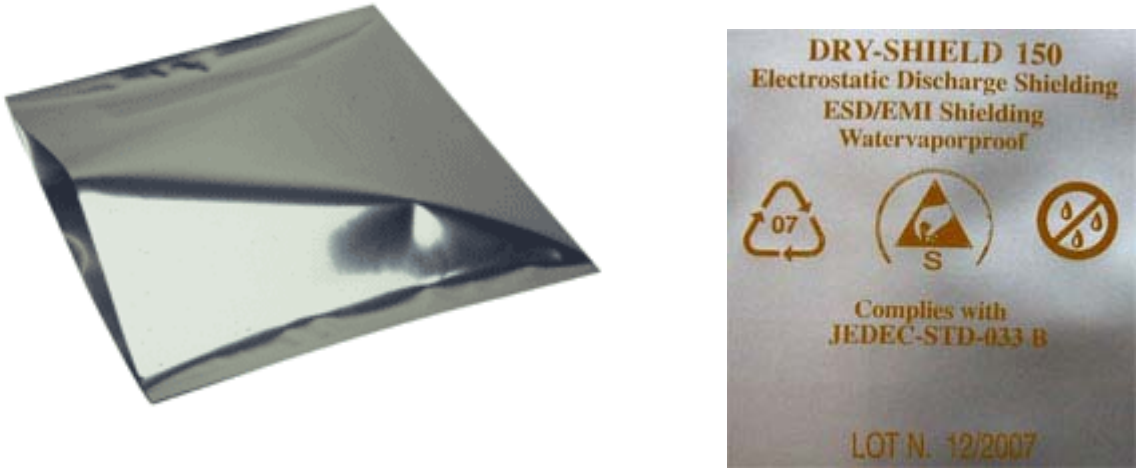


Figure 57: Moisture barrier bag (MBB) with imprint

The label shown in Figure 58 summarizes requirements regarding moisture sensitivity, including shelf life and baking requirements. It is attached to the outside of the moisture barrier bag.

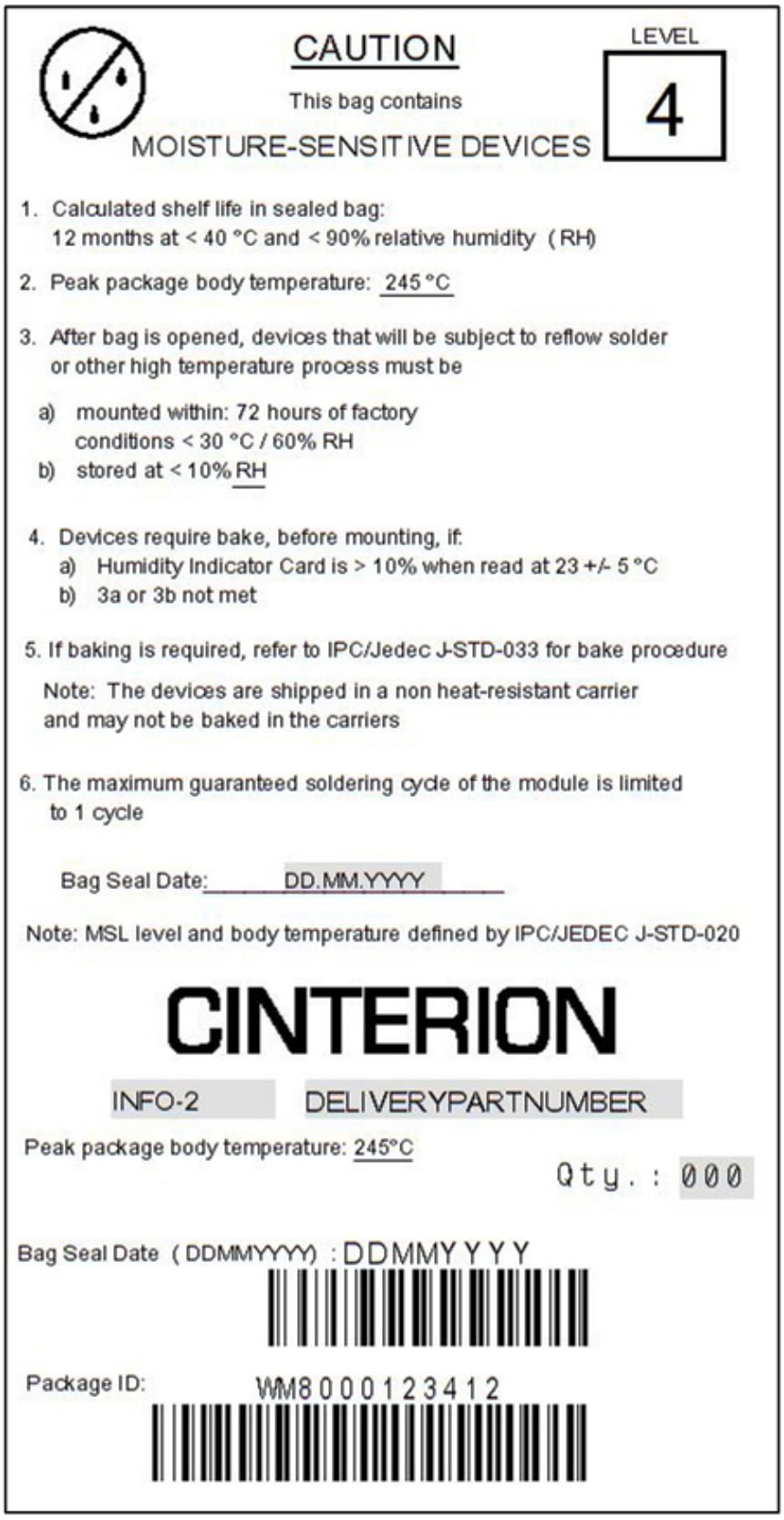


Figure 58: Moisture Sensitivity Label

MBBs contain one or more desiccant pouches to absorb moisture that may be in the bag. The humidity indicator card described below should be used to determine whether the enclosed components have absorbed an excessive amount of moisture.

The desiccant pouches should not be baked or reused once removed from the MBB.

The humidity indicator card is a moisture indicator and is included in the MBB to show the approximate relative humidity level within the bag. Sample humidity cards are shown in Figure 59. If the components have been exposed to moisture above the recommended limits, the units will have to be rebaked.

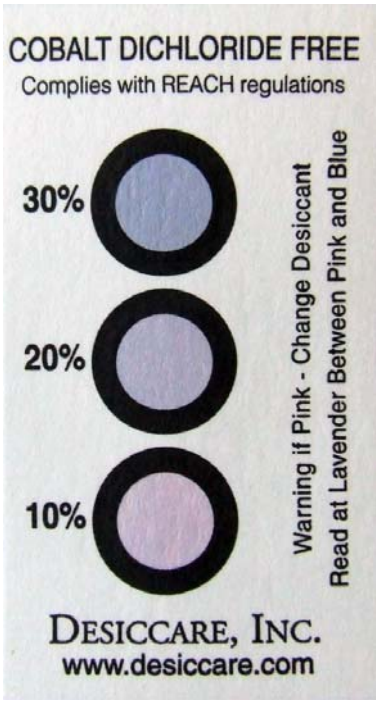


Figure 59: Humidity Indicator Card - HIC

A baking is required if the humidity indicator inside the bag indicates 10% RH or more.

6.3.2.2 Transportation Box

Tape and reel carriers are distributed in a box, marked with a barcode label for identification purposes. A box contains two reels with 500 modules each.

6.3.3 Trays

If small module quantities are required, e.g., for test and evaluation purposes, BGS2-E/BGS2-W may be distributed in trays. The small quantity trays are an alternative to the single-feed tape carriers normally used. However, the trays are not designed for machine processing. They contain modules to be (hand) soldered onto an external application (for information on hand soldering see [6]).

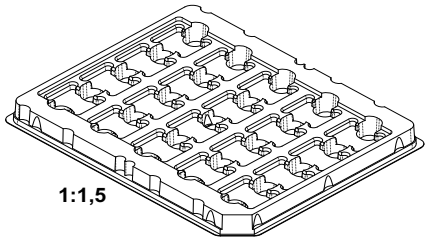


Figure 60: Small quantity tray

Trays are packed and shipped in the same way as tape carriers, including a moisture barrier bag with desiccant and humidity indicator card as well as a transportation box (see also Section 6.3.2).

Figure 61: Tray to ship odd module amounts

Figure 62: Trays with packaging materials

7 Sample Application

Figure 63 shows a typical example of how to integrate a BGS2-E/BGS2-W module with an application. Usage of the various host interfaces depends on the desired features of the application.

The analog audio interface demonstrates the balanced connection of microphone and earpiece. This solution is particularly well suited for internal transducers.

Because of the very low power consumption design, current flowing from any other source into the module circuit must be avoided, for example reverse current from high state external control lines. Therefore, the controlling application must be designed to prevent reverse current flow. Otherwise there is the risk of undefined states of the module during startup and shutdown or even of damaging the module.

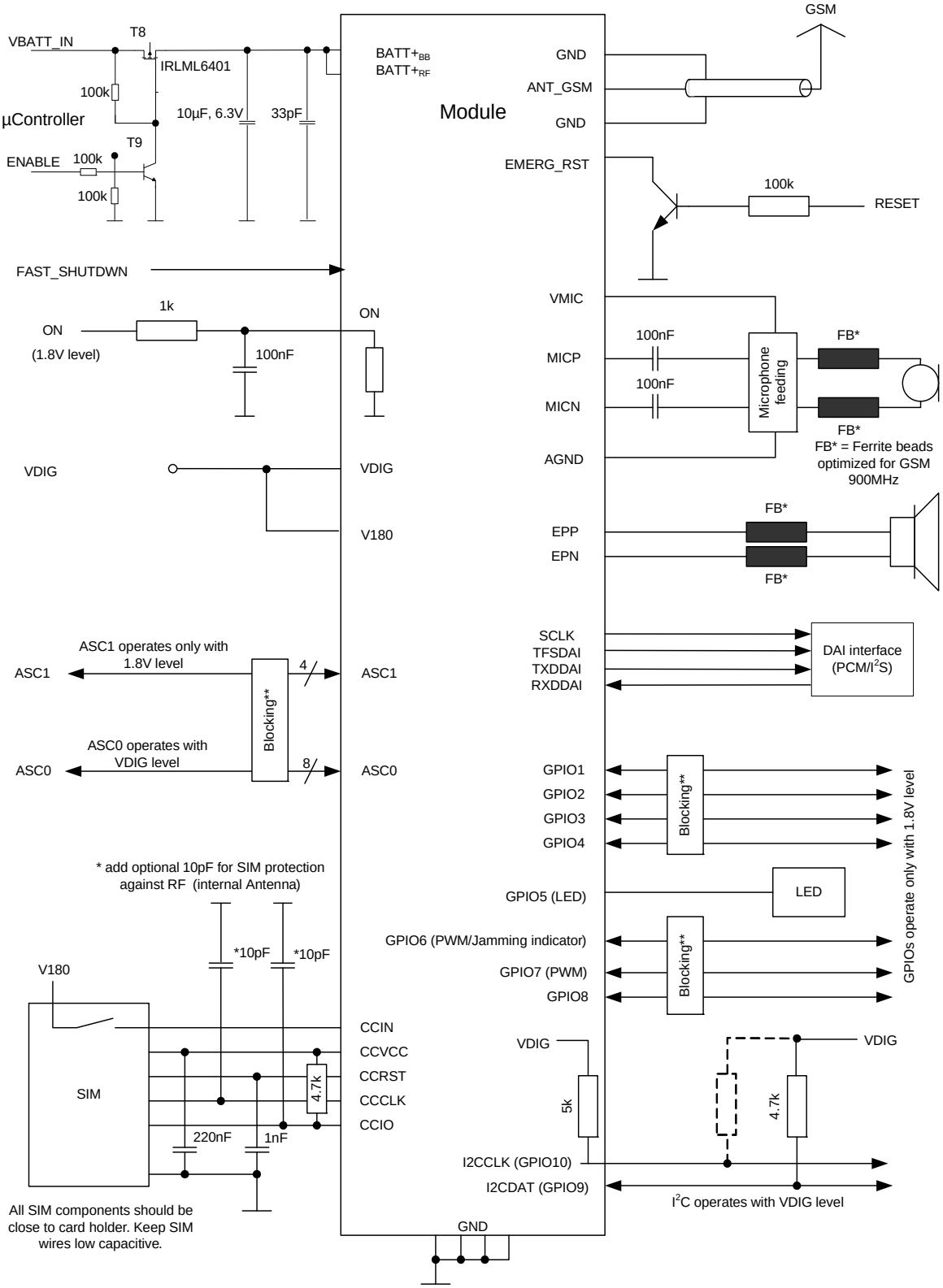
Because of the high RF field density inside the module, it cannot be guaranteed that no self interference might occur, depending on frequency and the applications grounding concept. The potential interferers may be minimized by placing small capacitors (47pF) at suspected lines (e.g. RXD0, RXT0, VDDLP, and ON).

While developing SMT applications it is strongly recommended to provide test points for certain signals, i.e., lines to and from the module - for debug and/or test purposes. The SMT application should allow for an easy access to these signals. For details on how to implement test points see [6].

The EMC measures are best practice recommendations. In fact, an adequate EMC strategy for an individual application is very much determined by the overall layout and, especially, the position of components. For example, mounting the internal acoustic transducers directly on the PCB eliminates the need to use the ferrite beads shown in the sample schematic.

Note: BGS2-E/BGS2-W is not intended for use with cables longer than 3m.

Disclaimer
No warranty, either stated or implied, is provided on the sample schematic diagram shown in Figure 63 and the information detailed in this section. As functionality and compliance with national regulations depend to a great amount on the used electronic components and the individual application layout manufacturers are required to ensure adequate design and operating safeguards for their products using BGS2-E/BGS2-W modules.



Blocking** = For more details see Section 7.1

Figure 63: Schematic diagram of BGS2-E/BGS2-W sample application

7.1 Blocking against RF on Interface Lines

To reduce EMI issues there are serial resistors, or capacitors to GND, implemented on the module for the ignition, emergency restart, and SIM interface lines (cp. Section 5.8). However, all other signal lines have no EMI measures on the module and there are no blocking measures at the module's interface to an external application.

Dependent on the specific application design, it might be useful to implement further EMI measures on some signal lines at the interface between module and application. These measures are described below.

There are five possible variants of EMI measures (A-E) that may be implemented between module and external application depending on the signal line (see Figure 64 and Table 37). Pay attention not to exceed the maximum input voltages and prevent voltage overshots if using inductive EMC measures.

The maximum value of the serial resistor should be lower than 1kΩ on the signal line. The maximum value of the capacitor should be lower than 50pF on the signal line. Please observe the electrical specification of the module interface and the application interface.

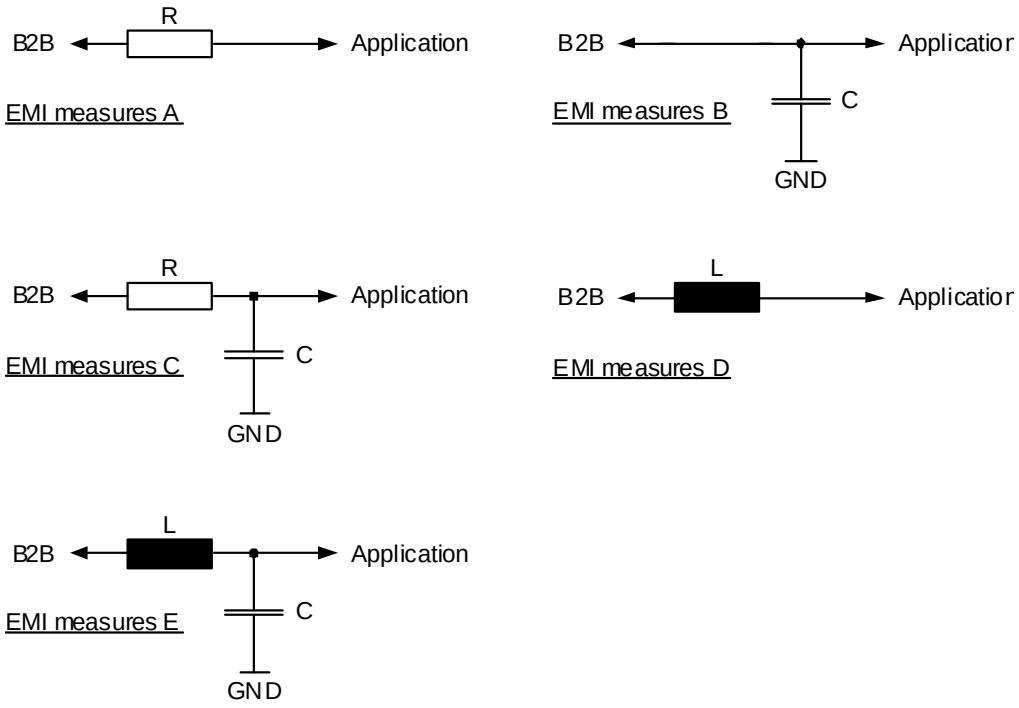


Figure 64: EMI circuits

The following table lists for each signal line at the SMT application interface the EMI measures that may be implemented.

Table 37: EMI measures on the application interface

Signal name	EMI measures					Remark
	A	B	C	D	E	
CCIN	x			x		
CCRST		x				The external capacitor should be not higher than 30pF. The value of the capacitor depends on the external application.
CCIO		x				
CCCLK		x				
RXD0	x	x	x	x	x	
TXD0	x	x	x	x	x	
CTS0	x	x	x	x	x	
RTS0				x		
RING0				x		
DTR0	x	x	x	x	x	
DCD0	x	x	x	x	x	
DSR0	x	x	x	x	x	
RXD1	x	x	x	x	x	
TXD1	x	x	x	x	x	
CTS1	x	x	x	x	x	
RTS1	x	x	x	x	x	
GPIO5/LED	x	x	x	x	x	
GPIO6/PWM2/ Jamming indicator	x	x	x	x	x	
GPIO7/PWM1	x	x	x	x	x	
GPIO8	x	x	x	x	x	
GPIO9/I2CCLK		x		x		The rising signal edge is reduced with an additional capacitor.
GPIO10/I2CDAT		x		x		
V180		x		x	x	
V285		x		x	x	
VDIG		x		x	x	

8 Reference Approval

8.1 Reference Equipment for Type Approval

The Gemalto M2M reference setup submitted to type approve BGS2-E/BGS2-W is shown in the following figure:

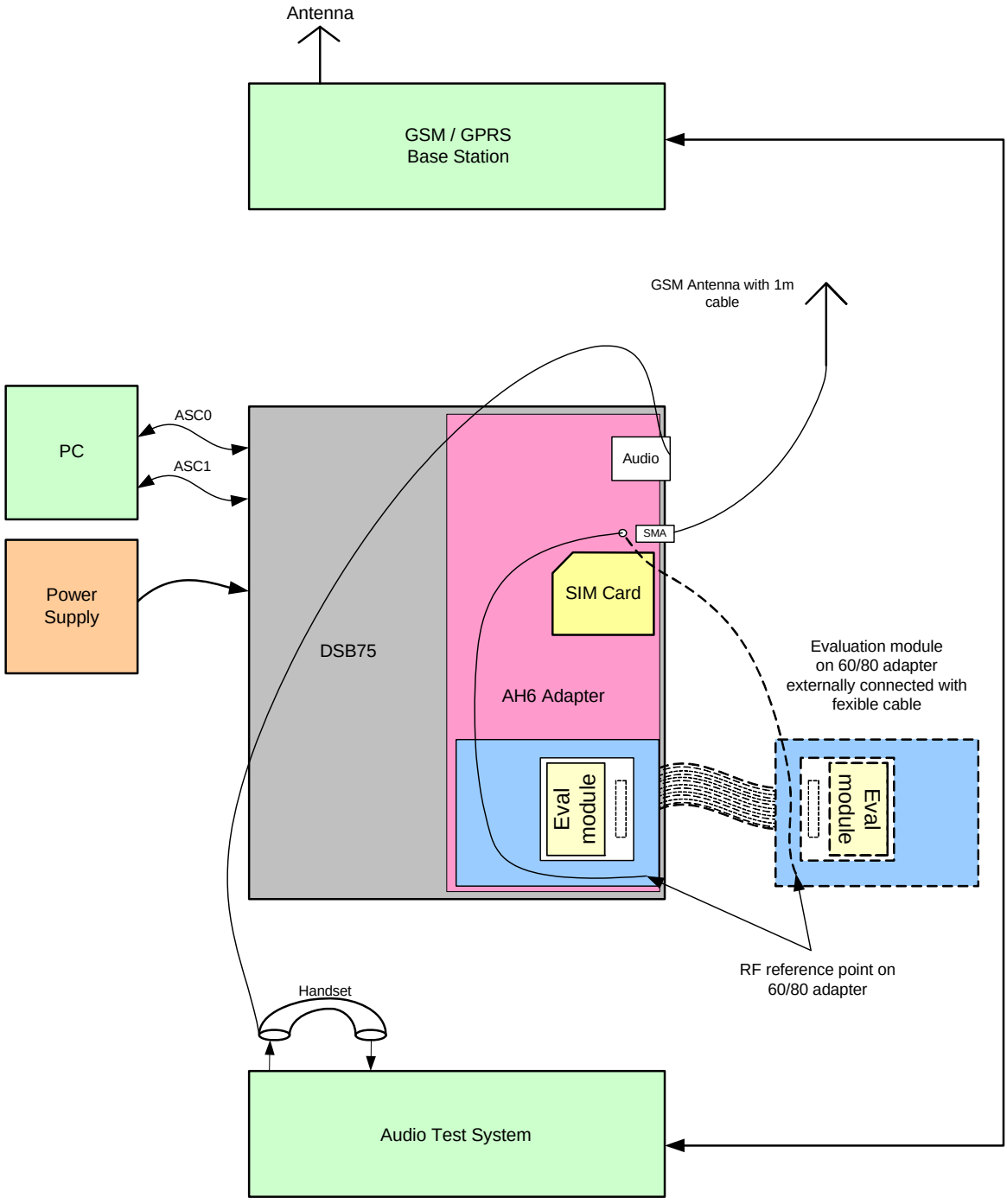


Figure 65: Reference equipment for Type Approval

8.2 Compliance with FCC and IC Rules and Regulations

The Equipment Authorization Certification for the Gemalto M2M reference application described in Section 8.1 will be registered under the following identifiers:

FCC Identifier: QIPBGS2
Industry Canada Certification Number: 7830A-BGS2
Granted to Gemalto M2M GmbH

Manufacturers of mobile or fixed devices incorporating BGS2-W modules are authorized to use the FCC Grants and Industry Canada Certificates of the BGS2-W modules for their own final products according to the conditions referenced in these documents. In this case, an FCC/ IC label of the module shall be visible from the outside, or the host device shall bear a second label stating "Contains FCC ID: QIPBGS2", and accordingly “Contains IC: 7830A-BGS2“. The integration is limited to fixed or mobile categorized host devices, where a separation distance between the antenna and any person of min. 20cm can be assured during normal operating conditions.

For mobile and fixed operation configurations the antenna gain, including cable loss, must not exceed the limits in following Table 38 for FCC and IC.

Table 38: Antenna gain limits for FCC and IC

Operating band	FCC limit	IC limit	Unit
Maximum gain in lower operating bands with f=850MHz (GSM)	7.24	6.4	dBi
Maximum gain in higher operating bands with f=1900MHz (GSM)	3.30	11.8	dBi

IMPORTANT:
Manufacturers of portable applications incorporating BGS2-W modules are required to have their final product certified and apply for their own FCC Grant and Industry Canada Certificate related to the specific portable mobile. This is mandatory to meet the SAR requirements for portable mobiles (see Section 1.3.2 for detail).

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Note:
This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

This Class B digital apparatus complies with Canadian ICES-003.

If Canadian approval is requested for devices incorporating BGS2 / BGS2-E modules the above note will have to be provided in the English and French language in the final user documentation. Manufacturers/OEM Integrators must ensure that the final user documentation does not contain any information on how to install or remove the module from the final product.

Notes (IC):
(EN) This Class B digital apparatus complies with Canadian ICES-003 and RSS-210. Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

(FR) Cet appareil numérique de classe B est conforme aux normes canadiennes ICES-003 et RSS-210. Son fonctionnement est soumis aux deux conditions suivantes: (1) cet appareil ne doit pas causer d'interférence et (2) cet appareil doit accepter toute interférence, notamment les interférences qui peuvent affecter son fonctionnement.

(EN) Radio frequency (RF) Exposure Information
The radiated output power of the Wireless Device is below the Industry Canada (IC) radio frequency exposure limits. The Wireless Device should be used in such a manner such that the potential for human contact during normal operation is minimized.
This device has also been evaluated and shown compliant with the IC RF Exposure limits under mobile exposure conditions (antennas at least 20cm from a person‘s body).

(FR) Informations concernant l'exposltion aux fréquences radio (RF)
La puissance de sortie émise par l'appareil de sans fiI est inférieure à la limite d'exposition aux fréquences radio d‘Industry Canada (IC). Utilisez l'appareil de sans fil de façon à minimiser les contacts humains lors du fonctionnement normal.

Ce périphérique a également été évalué et démontré conforme aux limites d'exposition aux RF d'IC dans des conditions d'exposition à des appareils mobiles (les antennes se situent à moins de 20cm du corps d'une personne).

9 Appendix

9.1 List of Parts and Accessories

Table 39: List of parts and accessories

Description	Supplier	Ordering information
BGS2-E/BGS2-W	Gemalto M2M	Standard module Gemalto M2M IMEI: Packaging unit (ordering) number: Module label number[1]: L30960-N2200-A400 (BGS2-E) L30960-N2210-A400 (BGS2-W)
DSB75 Evaluation Board	Gemalto M2M	Ordering number: L36880-N8811-A100
Mounting adapters: 1) AH6-DSB75 Adapter 2) 60/80 Adapter	Gemalto M2M	 Ordering number: L30960-N2301-A100 Ordering number: L30960-N2502-A100
Votronic Handset	Gemalto M2M, Votronic	Gemalto ordering number: L36880-N8301-A107 Votronic ordering number: HH-SI-30.3/V1.1/0 Votronic Entwicklungs- und Produktionsgesellschaft für elektronische Geräte mbH Saarbrücker Str. 8 66386 St. Ingbert Germany Phone: +49-(0)6 89 4 / 92 55-0 Fax: +49-(0)6 89 4 / 92 55-88 Email: contact@votronic.com
SIM card holder incl. push button ejector and slide-in tray	Molex	Ordering numbers: 91228 91236 Sales contacts are listed in Table 40.

1. Note: At the discretion of Gemalto M2M, module label information can either be laser engraved on the module's shielding or be printed on a label adhered to the module's shielding.

Table 40: Molex sales contacts (subject to change)

Molex For further information please click: http://www.molex.com	Molex Deutschland GmbH Otto-Hahn-Str. 1b 69190 Walldorf Germany Phone: +49-6227-3091-0 Fax: +49-6227-3091-8100 Email: mxgermany@molex.com	American Headquarters Lisle, Illinois 60532 U.S.A. Phone: +1-800-78MOLEX Fax: +1-630-969-1352
Molex China Distributors Beijing, Room 1311, Tower B, COFCO Plaza No. 8, Jian Guo Men Nei Street, 100005 Beijing P.R. China Phone: +86-10-6526-9628 Fax: +86-10-6526-9730	Molex Singapore Pte. Ltd. 110, International Road Jurong Town, Singapore 629174 Phone: +65-6-268-6868 Fax: +65-6-265-6044	Molex Japan Co. Ltd. 1-5-4 Fukami-Higashi, Yamato-City, Kanagawa, 242-8585 Japan Phone: +81-46-265-2325 Fax: +81-46-265-2365

About Gemalto

Gemalto (Euronext NL0000400653 GTO) is the world leader in digital security with 2015 annual revenues of €3.1 billion and blue-chip customers in over 180 countries. Our 14,000+ employees operate out of 118 offices, 45 personalization and data centers, and 27 research and software development centers located in 49 countries.

We are at the heart of the rapidly evolving digital society. Billions of people worldwide increasingly want the freedom to communicate, travel, shop, bank, entertain and work - anytime, everywhere - in ways that are enjoyable and safe. Gemalto delivers on their expanding needs for personal mobile services, payment security, authenticated cloud access, identity and privacy protection, eHealthcare and eGovernment efficiency, convenient ticketing and dependable machine-to-machine (M2M) applications.

Gemalto develops secure embedded software and secure products which we design and personalize. Our platforms and services manage these secure products, the confidential data they contain and the trusted end-user services they enable. Our innovations enable our clients to offer trusted and convenient digital services to billions of individuals.

Gemalto thrives with the growing number of people using its solutions to interact with the digital and wireless world.

For more information please visit
m2m.gemalto.com, www.facebook.com/gemalto, or Follow@gemaltom2m on twitter.

Gemalto M2M GmbH
Werinherstrasse 81
81541 Munich
Germany

➲ M2M.GEMALTO.COM

gemalto
security to be free