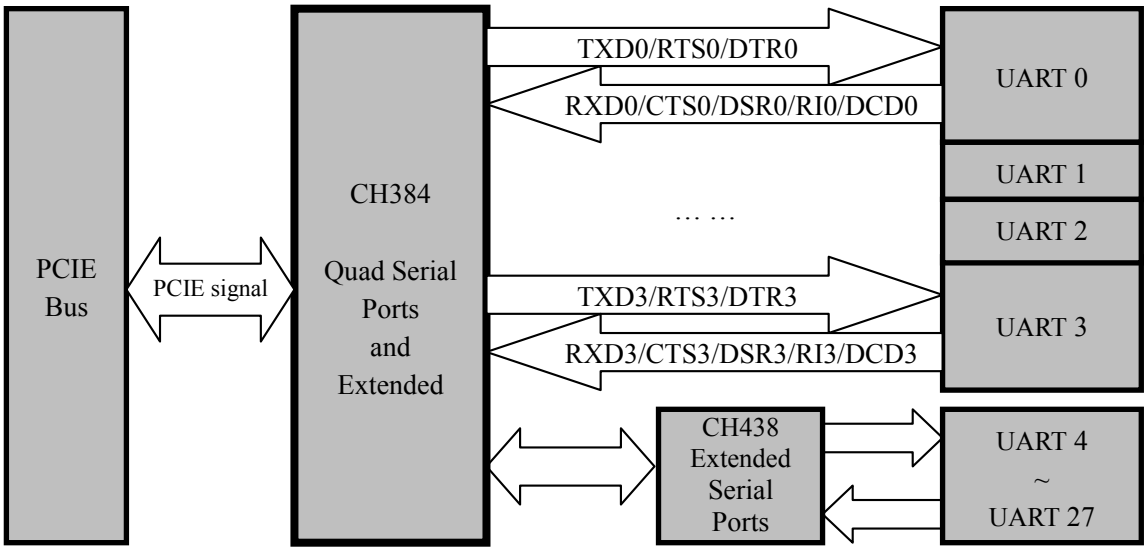
PCIE to Quad Serial Ports and Printer Port Chip CH384

Datasheet (II): Quad UARTs + Extended Multiple UARTs

Version: 1

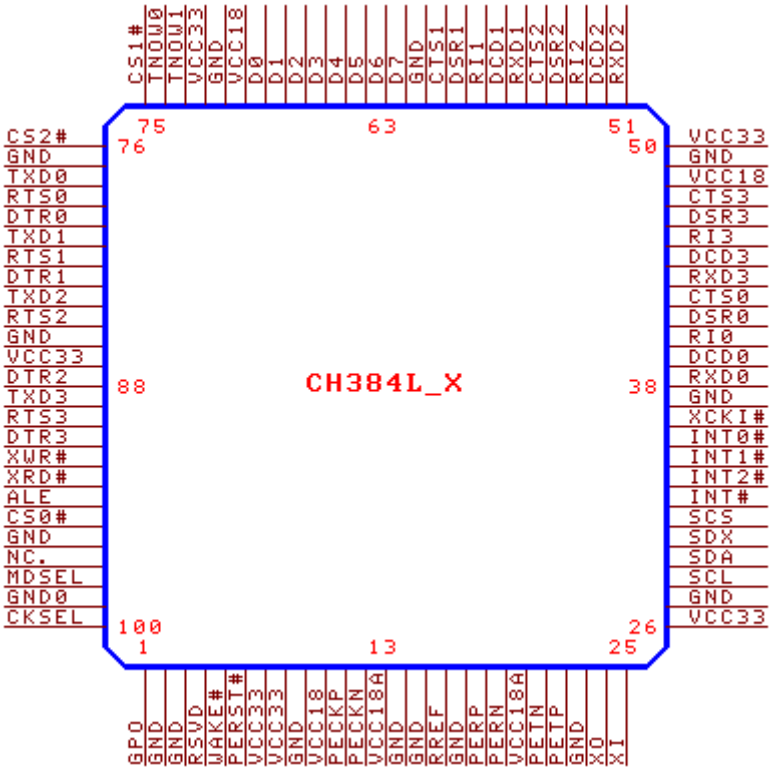
http://wch.cn

1. Application Block Diagram



2. Package

Quad Serial Ports + Extended



Refer to the Datasheet (I) CH384DS1.PDF for the application instructions and pin diagrams of quad serial ports + parallel port.

3. Pins

3.1. Power Line

Pin No.	Pin Name	Type	Pin Description
7,8,26,50,72,87	VCC33	Power	3.3V I/O power
10,48,70	VCC18	Power	1.8V core power
13,20	VCC18A	Power	1.8V transmission power
2,3,9,14,15,17,23,27, 37,49,61,71,77,86,96,99	GND	Power	Ground
97	NC.	None	No connection

3.2. PCIE Bus Signal Line

Pin No.	Pin Name	Type	Pin Description
6	PERST#	Input	System reset signal lines, active low
11,12	PECKP/PECKN	Input	Differentia input of system reference clock
18,19	PERP/PERN	PCIE input	Differential signal input of PCIE receiver
22,21	PETP/PETN	PCIE output	Differential signal output of PCIE transmitter
5	WAKE#	Open-drain output	Bus wake-up output, active low, not connected if not used

3.3. UART 0~3 Signal Lines

Pin No.	Pin Name	Type	Pin Description
42/60 55/47	CTS0/CTS1 CTS2/CTS3	Input	MODEM signal, clear to send, active low, built-in pull-up resistor
41/59 54/46	DSR0/DSR1 DSR2/DSR3	Input	MODEM signal, data send ready, active low, built-in pull-up resistor
40/58 53/45	RI0/RI1 RI2/RI3	Input	MODEM signal, ring indicator, active low, built-in pull-up resistor
39/57 52/44	DCD0/DCD1 DCD2/DCD3	Input	MODEM signal, data carrier detect, active low, built-in pull-up resistor
38/56 51/43	RXD0/RXD1 RXD2/RXD3	Input	Received data, built-in pull-up resistor
80/83 88/91	DTR0/DTR1 DTR2/DTR3	Output	MODEM signal, data terminal ready, active low
79/82 85/90	RTS0/RTS1 RTS2/RTS3	Output	MODEM signal, request to send, active low
78/81 84/89	TXD0/TXD1 TXD2/TXD3	Output	Transmitted data
74/73	TNOW0/TNOW1	Output	Serial port sending status output (half duplex receive-transmit switching), active high

3.4. Extended CH438 Signal Line

Pin No.	Pin Name	Type	Pin Description
62-69	D7～D0	Tri-status and bi-direction	8-digit parallel data output and input, built-in pull-up resistor, connect to D7-D0

92	XWR#	Output	Write strobe output, active low, connect to WR#
93	XRD#	Output	Read strobe output, active low, connect to RD#
94	ALE	Output	Address latch enables output of multiplexed address; active high, connect to ALE
95	CS0#	Output	Chip selection 0 output of extended serial port, connected to CS# of 0# CH438, active low
75	CS1#	Output	Chip selection 1 output of extended serial port, connected to CS# of 1# CH438, active low
76	CS2#	Output	Chip selection 2 output of extended serial port, connected to CS# of 2# CH438, active low
35	INT0#	Input	Interrupt status output of 0# CH438, active low, built-in pull-up resistor
34	INT1#	Input	Interrupt status output of 1# CH438, active low, built-in pull-up resistor
33	INT2#	Input	Interrupt status output of 2# CH438, active low, built-in pull-up resistor
32	INT#	Input	Interrupt status output of backup, active low, built-in pull-up resistor

3.5. Auxiliary Signal Line

Pin No.	Pin Name	Type	Pin Description
16	RREF	Input	System reference current input; connect a external 12KΩ resistor to GND
25	XI	Input	Optional, input of crystal oscillator, connect to crystal and oscillation capacitor externally
24	XO	Input / Output	Optional, inverted output of crystal oscillator, connect to crystal and oscillation capacitor externally
28	SCL	Output	General output, clock output of external configuration chip, connect to the SCL pin of the serial EEPROM configuration chip 24CXX externally
29	SDA	Open-drain output and input	General output and input, built-in pull-up resistor, connect to the SDA pin of the serial EEPROM configuration chip 24CXX externally
30	SDX	Tri-status and bi-direction	General output and input, built-in pull-up resistor
31	SCS	Output	General output
100	CKSEL	Input	Serial port clock frequency selection input, built-in pull-up resistor
98	MDSEL	Input	Software recognition mode selection input, built-in pull-up resistor
36	XCKI#	Input	Serial Clock source selection input of external input serial port, built-in pull-up resistor
1	GPO	Output	General output
4	RSVD	Reserved	Reserved, not connection

4. Configuration

CH384 has two main hardware function modes: quad UARTs + parallel port, quad UARTs + extended multiple serial ports. The pin definitions are different in two function modes, and this datasheet only involves the latter. Please refer to Datasheet (I) CH384DS1.PDF for the former.

MDSEL pin of CH384 is used to select the software identification mode:

MDSEL connects to VCC33 or suspend, namely, MDSEL=1, which is an 8 serial ports mode (extended 8 serial ports, and internal 4 serial ports are disabled);

MDSEL connects to GND, namely, MDSEL=0, it is a 28 serial ports (internal 4 serial ports + extended 3*8 serial ports).

XCKI# pin of CH384 is used to select the clock source of internal 4 serial ports and disable the internal crystal oscillator in 28 serial ports mode:

XCKI# connects to VCC33 or suspend, namely, XCKI#=1, the clock is generated by the internal crystal oscillator plus the external crystal or PLL;

XCKI# connects to GND, namely, XCKI#=0, the internal crystal oscillator is disabled, and the external clock is input from XO pin.

CKSEL pin of CH384 is used to select the clock frequency of the internal 4 serial ports:

CKSEL connects to VCC33 or suspend, namely, CKSEL=1, the clock is inputted from XO pin, frequency depends on external crystal or clock source, and the internal frequency coefficient is 1/12 frequency division by default, and 2 frequency doubling is selected through CK2X or CKnS;

CKSEL connects to GND, namely, CKSEL=0, the clock is inputted from XO pin, frequency depends on external crystal or clock source, and the internal frequency coefficient is always forced to be 2 frequency doubling;

CKSEL connects to PERST# pin, namely, CKSEL=R, the internal crystal oscillator is disabled, the internal PLL provides the clock with a frequency of 125MHz, and the internal frequency coefficient is 1/12 frequency division by default, and no frequency division is selected through CK2X or CKnS.

In 8 serial ports mode, CKSEL shall be connected to PERST# pin to disable the internal crystal oscillator, and XCKI# shall be suspended.

Please refer to Datasheet (I) for instructions on external configuration chip, serial port internal clock, PCIE configuration space, register of I/O base address 0, bit of register and serial port register.

5. Function Descriptions

5.1. Query and Interrupt

The multiple serial ports of CH384 share a PCIE interrupt request pin, so after entering the PCIE interrupt service, firstly analyzing whether it is ch384 request interrupt and it is which UART. After entering the interrupt service, there are two methods: specialized status analysis and sequential query.

Specialized status analysis means that reading the internal interrupt status register IINT and external interrupt status register XINT firstly. The IINT bit 0 flag is valid indicates the UART 0 interrupted, the IINT bit 1 flag is valid indicates the UART 1 interrupted, the IINT bit 2 flag is valid indicates the UART 2 interrupted, the IINT bit 3 flag is valid indicates the UART 3 interrupted, the XINT bit 5 flag is valid indicates the extended 0# CH438 interrupted, the XINT bit 6 flag is valid indicates the extended 1# CH438 interrupted, the XINT bit 7 flag is valid indicates the extended 0# CH438 interrupted. Directly process and exit it based on the analysis result, directly exit it without interrupt.

Sequential query means reading the IIR register of the UART 0 firstly, there is an interrupt, then process and

exit, read the IIR register of UART 1 without interrupt, process and exit with an interrupt, read the IIR register of UART 2 without interrupt, process and exit with an interrupt, read the IIR register of UART 3 without interrupt, process and exit with an interrupt; read the IIR register of the first extended serial port without interrupt, process and exit with an interrupt, read the IIR register of the second extended serial port without interrupt , until all extended serial ports are queried.

After ensuring that it is an interrupt of a certain UART, if it is necessary can further analyze the LSR register, analyze the reason of the interrupt and process it.

If the serial port works in the interrupt mode, then setting the IER register to allow the corresponding interrupt request, and set OUT2 of the MCR register to allow interrupt output.

If the serial port works in the query mode, then do not to set OUT2 of IER and MCR, and only need to query the LSR register, and analyze and process it.

5.2. Serial Port Operation

For specific operations, please refer to the specifications for single serial port 16C550 or dual UARTs CH432 or octal UARTs CH438.

5.3. Application Specification

Please refer to Datasheet (I) for the application specification of related serial ports

Note that the output pins of the extended serial ports for CH438 are at 3.3V LVCMOS level and compatible with 5V TTL level. The input pins are compatible with 3.3V LVCMOS and LVTTL levels, but cannot support 5V withstand voltage.

CH384 can be used to expand additional high-speed RS232 serial port for computer through PCIE bus, and support high baud rate serial port with automatic hardware speed control, RS422 or RS485 communication interfaces, SIR infrared communication interfaces, etc.

6. Parameter

Refer to Datasheet (I) CH384DS1.PDF.

7. Application

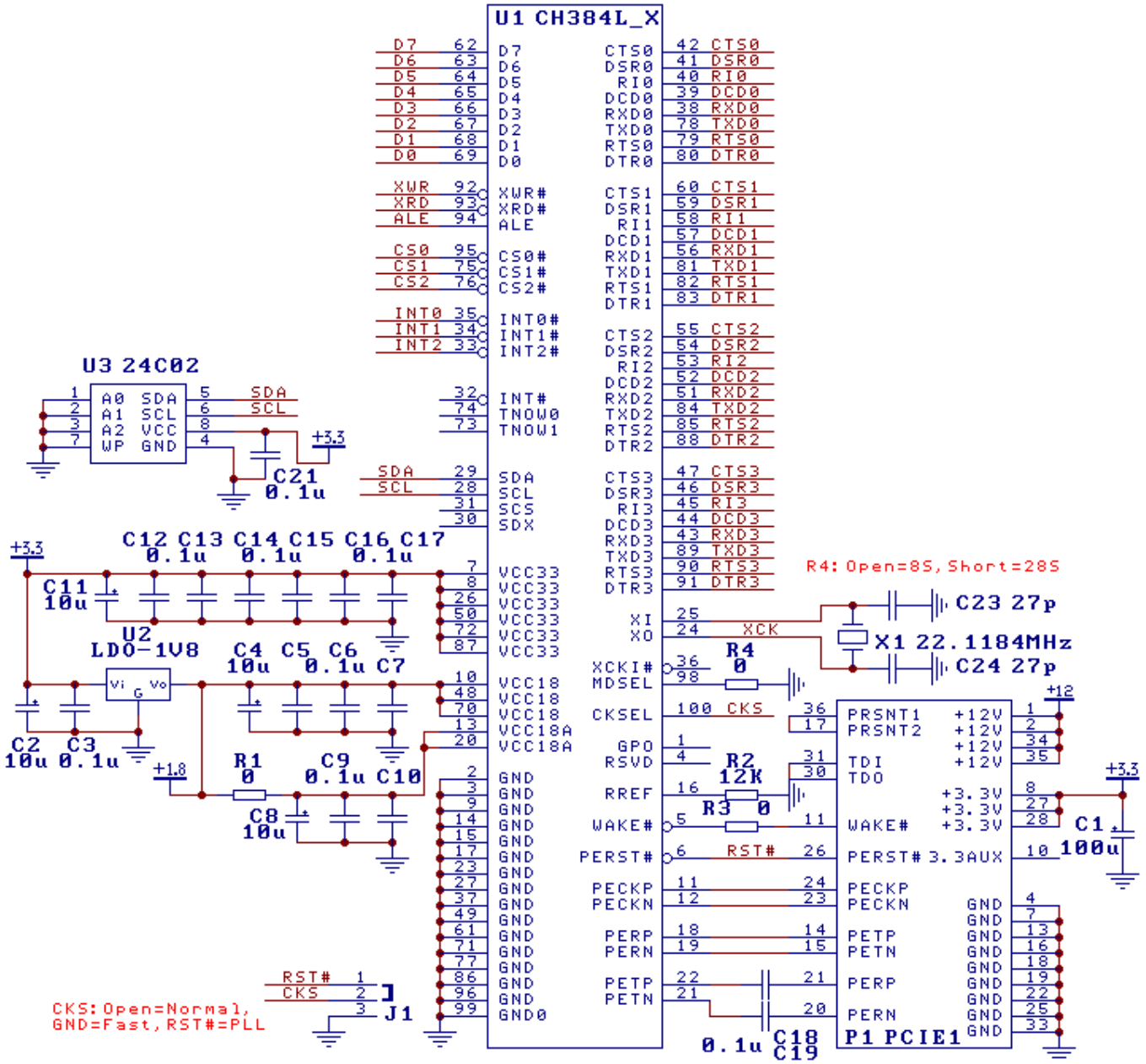
7.1. Quad UARTs + Extended Multiple UARTs

This is the basic circuit of CH384 for PCIE quad UARTs + extended multiple serial ports. The figure does not include externally extended CH438 and RS232 level conversion chip.

U3 is an optional external configuration chip, providing the online configuration tool software for Windows system on the website.

The crystal X1 and the capacitors C23 and C24 are used for the clock oscillation circuits, and the XO pin of CH384 can provide a clock to the extended XI pin of CH438. Other capacitors are used for power decoupling. The capacitor with a capacity of 10uF is a tantalum capacitor, and the capacitor with a capacity of 0.1uF is a monolithic or high-frequency ceramic capacitor, which are connected in parallel nearby to the power pins of CH384 respectively.

CH384 is a high frequency circuit. Please refer to PCIE bus specification or PCIE_PCB.PDF document when designing the PCB board.


U1 CH384L_X
U3 24C02
A0 SDA
A1 SCL
A2 VCC
WP GND
SDA
SCL
+3.3
C21
0.1u
C12 C13 C14 C15 C16 C17
0.1u 0.1u 0.1u
C11
10u
U2
LDO-1V8
C4 C5 C6
10u 0.1u C7
C2 C3
10u 0.1u
+1.8
R1
0
C9
0.1u C10
C8
10u
R4: Open=8S, Short=28S
C23 27p
X1 22.1184MHz
C24 27p
R4
0
R2
12K
R3 0
C18
0.1u C19
+12
C1
100u
P1 PCIE1
PRSNT1
PRSNT2
TDI
TDO
WAKE#
PERST#
PECKP
PECKN
PETP
PETN
PERP
PERN
+12V
+3.3V
3.3AUX
GND
RST#
CKS
J1
CKS: Open=Normal,
GND=Fast, RST#=PLL