



Product Specification

M320QAN02.0

AU OPTRONICS CORPORATION

AUO-General

() Preliminary Specification

(V) Final Specification

Module	32.0" Color TFT-LCD
Model Name	M320QAN02.0

Customer	Date
_____	_____
Approved by	
_____	_____
<p>Note: This Specification is subject to change without notice.</p>	

Approved by	Date
<i><u>PY Cheng</u></i>	<u>Sep. 25, 2020</u>
Prepared by	Date
<i><u>CJ Huang</u></i>	<u>Sep. 25, 2020</u>
<p>AU Optronics corporation</p>	

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Record of Revision

Version	Date	Page	Old description	New Description	Remark																																																																																				
0.1	2020/6/23	All	First version release	-																																																																																					
0.2	2020/7/1	8	2.3 <table border="1"> <thead> <tr> <th>Symbol</th> <th>Description</th> <th>Min.</th> <th>Typ.</th> </tr> </thead> <tbody> <tr> <td>Lw</td> <td>White Luminance (Center of screen)</td> <td>290</td> <td>350</td> </tr> </tbody> </table>	Symbol	Description	Min.	Typ.	Lw	White Luminance (Center of screen)	290	350	2.3 <table border="1"> <thead> <tr> <th>Symbol</th> <th>Description</th> <th>Min.</th> <th>Typ.</th> </tr> </thead> <tbody> <tr> <td>Lw</td> <td>White Luminance (Center of screen)</td> <td>280</td> <td>350</td> </tr> </tbody> </table>	Symbol	Description	Min.	Typ.	Lw	White Luminance (Center of screen)	280	350																																																																					
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I Handling Precautions

- 1) Since polarizer is easily damaged, do not touch or press the surface of polarizer with hand.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open or modify the Module Assembly.
- 8) Do not press the reflector sheet at the back of the module to any directions.
- 9) In case a TFT-LCD Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the LED lightbar edge. Otherwise the TFT-LCD Module may be damaged.
- 10) Insert or pull out the interface connector, be sure not to rotate nor tilt it of the TFT-LCD Module.
- 11) Do not twist nor bend the TFT -LCD Module even momentary. It should be taken into consideration that no bending/twisting forces are applied to the TFT-LCD Module from outside. Otherwise the TFT-LCD Module may be damaged.
- 12) Please avoid touching COF position while you are doing mechanical design.
- 13) When storing modules as spares for a long time, the following precaution is necessary: Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5°C and 35°C at normal humidity.
- 14) Do not apply the same pattern for a long time, it will enhance relevant defect.
- 15) When this reverse-type model(PCBA on bottom side) is used as forward-type model(PCBA on top side) , AUO can not guarantee any defects of LCM .

2 General Description

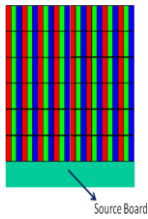
This specification applies to the 32.0 inch wide Color a-Si TFT-LCD Module M320QAN02.0. The display supports the UHD - 3840(H) x 2160(V) screen format and 1.07B colors (RGB 8bits + Hi-FRC). The input interface is 8-lanes eDP and this module doesn't contain an driver board for backlight.

2.1 Display Characteristics

The following items are characteristics summary on the table under 25°C condition:

ITEMS	Unit	SPECIFICATIONS
Screen Diagonal	[mm]	812.8 (32.0")
Active Area	[mm]	708.48 (H) x 398.52 (V)
Pixels H x V	-	3840(x3) x 2160
Pixel Pitch	[um]	184.5 (per one triad) x 184.5
Pixel Arrangement	-	R.G.B. Vertical Stripe Note 2-1
Display Mode	-	AHVA Mode (Advances Hyper-Viewing Angle), Normally Black
White Luminance (Center)	[cd/m ²]	350 (typ.)
Contrast Ratio	-	1000 (Typ.)
Response Time	[msec]	12 (Typ., Gray to Gray)
Power Consumption (LCD Module + Backligh unit)	[Watt]	35.77 W (Typ.) LCD module : PDD(Typ.)=12.72W@white pattern,60Hz,12V Backlight unit : PBLU (Typ.) =23.05 W @Is=90mA
Weight	[Grams]	4800 +/- 240
Outline Dimension	[mm]	721.68 (H) x 417.93 (V) x 15.47 (D) Typ.
Electrical Interface	-	8-lanes eDP , 10bits RGB data input
Support Color	-	1.07B colors (RGB 8bits + Hi-FRC)
Surface Treatment	-	SAG25%, 3H
Temperature Range Operating Storage (Shipping)	[°C] [°C]	0 to +50 -20 to +60
RoHS Compliance	-	RoHS Compliance
TCO Compliance	-	TCO 8.0 Compliance

Note 2-1: The following shows the figure of pixel arrangement



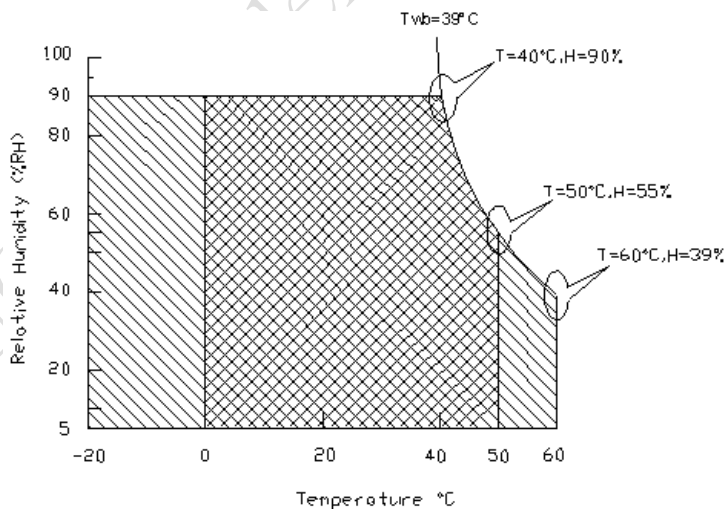
2.2 Absolute Maximum Rating of Environment

Permanent damage may occur if exceeding the following maximum rating.

Symbol	Description	Min.	Max.	Unit	Remark
TOP	Operating Temperature	0	+50	[°C]	Note 2-2
TGS	Glass surface temperature (operation)	0	+68	[°C]	Note 2-2 Function judged only
HOP	Operation Humidity	5	90	[%RH]	Note 2-2
TST	Storage Temperature	-20	+60	[°C]	
HST	Storage Humidity	5	90	[%RH]	

Note 2-2: Temperature and relative humidity range are shown as the below figure.

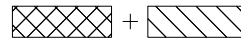
- 90% RH Max ($T_a \leq 39^\circ\text{C}$)
- Max wet-bulb temperature at 39°C or less. ($T_a \leq 39^\circ\text{C}$)
- No condensation



Operating Range



Storage Range



2.3 Optical Characteristics

The optical characteristics are measured on the following test condition.

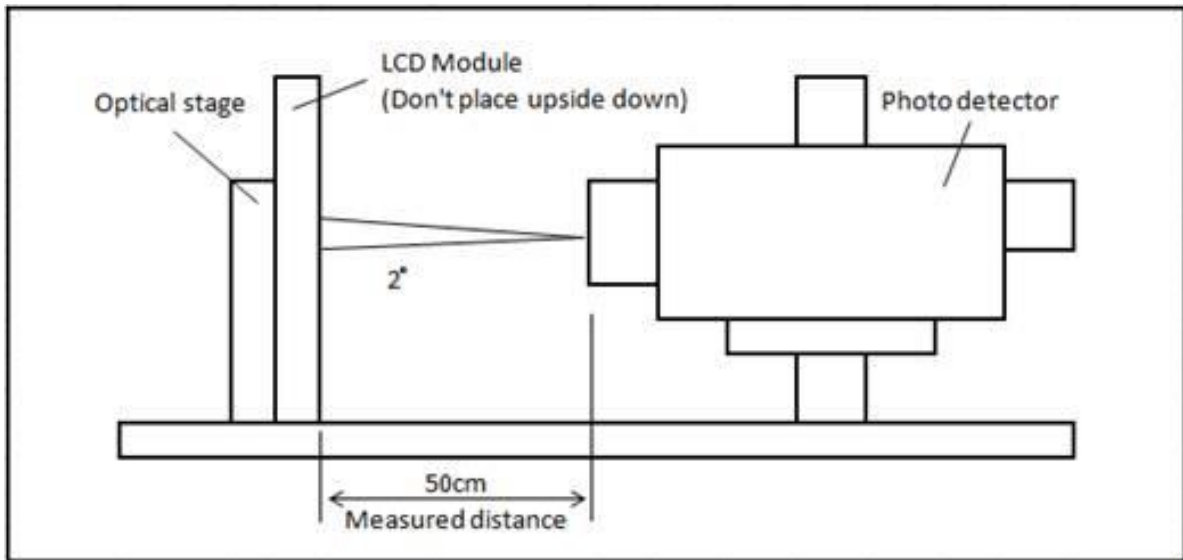
Test Condition:

1. Equipment setup: Please refer to *Note 2-3*.
2. Panel Lighting time: 30 minutes
3. VDD=12.0V, Fv=60Hz, Ta=25°C

Symbol	Description		Min.	Typ.	Max.	Unit	Remark		
L _w	White Luminance (Center of screen)		280	350	-	[cd/m ²]	Note 2-3 By SR-3		
L _{uni}	Luminance Uniformity (9 points)		75	80	-	[%]	<i>Note 2-4</i> By SR-3		
CR	Contrast Ratio (Center of screen)		600	1000	-	-	<i>Note 2-5</i> By SR-3		
θ _R	Horizontal Viewing Angle (CR=5)	Right	75	89	-	[degree]	<i>Note 2-6</i> By SR-3		
θ _L		Left	75	89	-				
Φ _H	Vertical Viewing Angle (CR=5)	Up	75	89	-				
Φ _L		Down	75	89	-				
T _{GTG}	Response Time		Gray to Gray		-	12	-	[msec]	<i>Note 2-7</i> By TRD-100
R _x	Color Coordinates (CIE 1931)		Red x		0.631	0.661	0.691	-	By SR-3
R _y			Red y		0.302	0.332	0.362		
G _x			Green x		0.269	0.299	0.329		
G _y			Green y		0.603	0.633	0.663		
B _x			Blue x		0.118	0.148	0.178		
B _y			Blue y		0.022	0.052	0.082		
W _x			White x		0.283	0.313	0.343		
W _y			White y		0.299	0.329	0.359		
Ru'	Color Coordinates (CIE 1976)		Red u'		-	0.467	-	-	By SR-3
Rv'			Red v'		-	0.528	-		
Gu'			Green u'		-	0.120	-		
Gv'			Green v'		-	0.570	-		
Bu'			Blue u'		-	0.178	-		
Bv'			Blue v'		-	0.141	-		
Wu'			White u'		-	0.198	-		

Wv'		White v'	-	0.468	-		
sRGB coverage ratio				99		[%]	By SR-3

Note 2-3: Equipment setup:

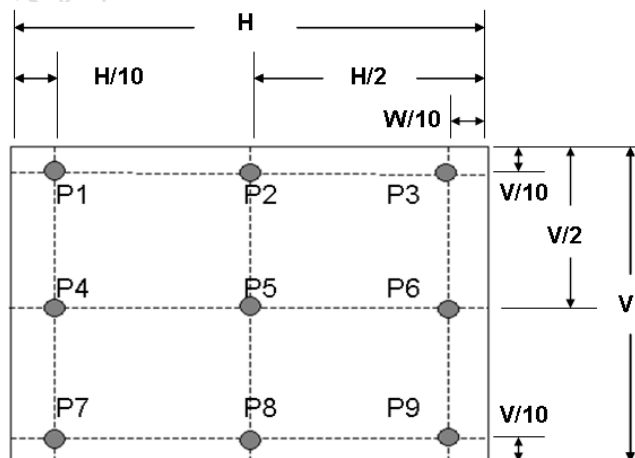


Note 2-4: Luminance Uniformity Measurement

Definition:

$$\text{Luminance Uniformity} = \frac{\text{Minimum Luminance of 9 Points (P1 ~ P9)}}{\text{Maximum Luminance of 9 Points (P1 ~ P9)}}$$

a. Test pattern: White Pattern



Note 2-5: Contrast Ratio Measurement

Definition:

$$\text{Contrast Ratio} = \frac{\text{Luminance of White pattern}}{\text{Luminance of Black pattern}}$$

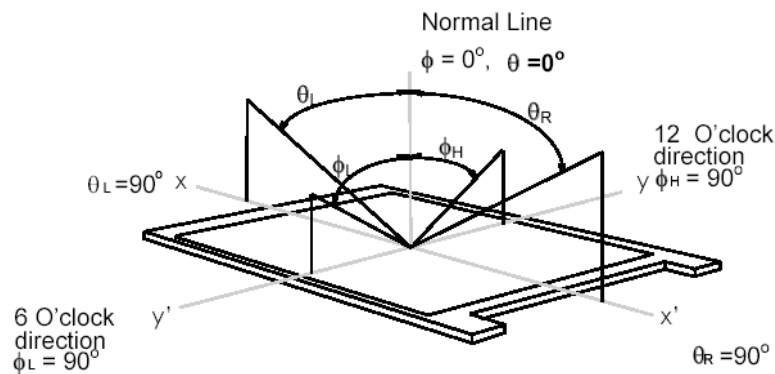
- a. Measured position: Center of screen (P5) & perpendicular to the screen ($\theta = \Phi = 0^\circ$)

Note 2-6: Viewing angle measurement

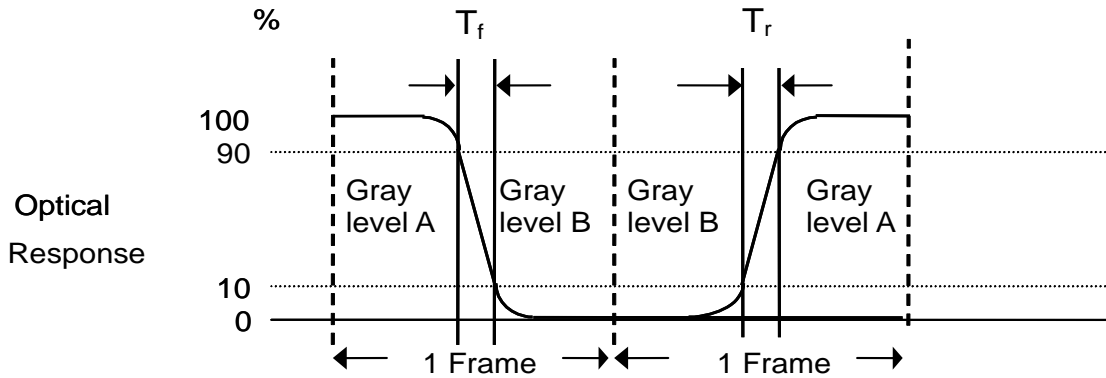
Definition: The angle at which the contrast ratio is greater than 10 & 5 .

- a. Horizontal view angle: Divide to left & right (θ_L & θ_R)

Vertical view angle: Divide to up & down (Φ_H & Φ_L)



Note 2-7: Response time measurement



The output signals of photo detector are measured when the input signals are changed from “Gray level A” to “Gray level B” (falling time, T_f), and from “Gray level B” to “Gray level A” (rising time, T_r), respectively. The response time is interval between the 10% and 90% of optical response.

The gray to gray response time is defined as the following table.

The gray to gray response time is defined as the following table.

Gray Level to Gray Level		Target gray level				
		L0	L255	L511	L767	L1023
Start gray level	L0					
	L255					
	L511					
	L767					
	L1023					

■ T_{GTG_typ} is the total average time at rising time and falling time of gray to gray.

2.8 Mechanical Characteristics

Symbol	Description	Min.	Max.	Unit	Remark
P _{bc}	Backside Compression	2.5	-	[Kgf]	Note 2-8

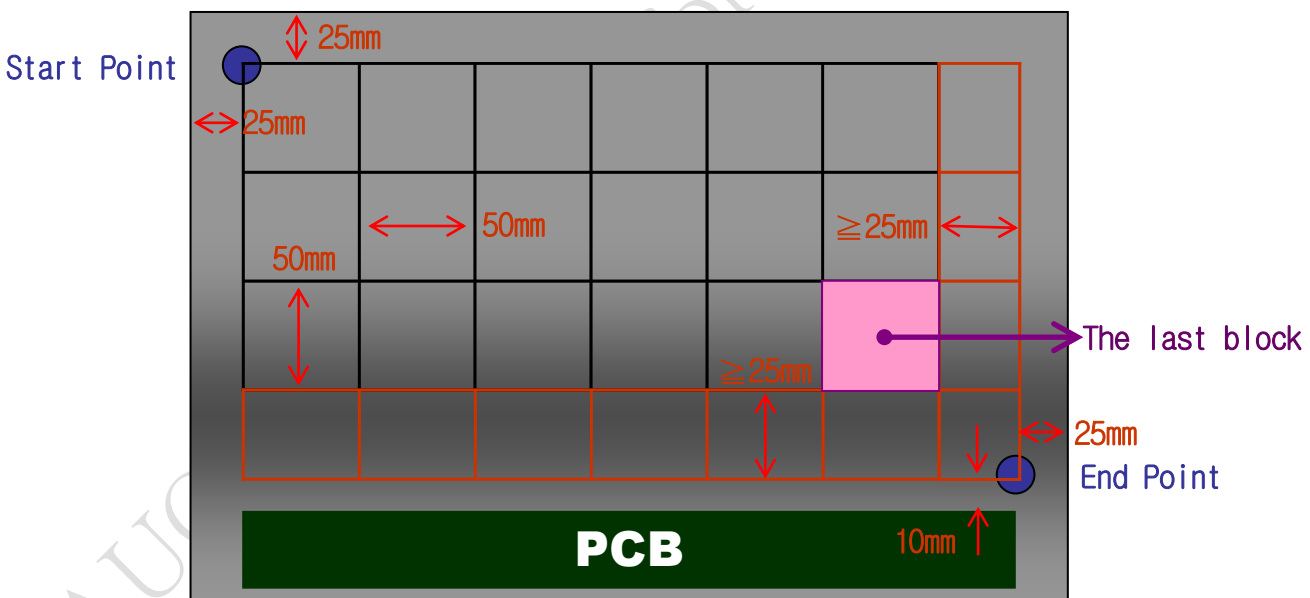
Note 2-8: a. Test Method:

The point is at a distance from right-downside 25mm x 25mm defined as the Start Point of Measure Points, and the point is at a distance 25mm from left-side & around 10mm from PCB defined as the End Point.

Align 50mm x 50mm block from Start Point on the Bezel Back, and the corners of each block are Measure Points.

If the distance from the last block to each side of the End Point \geq 25mm, add other blocks to make sure that most area of Bezel Back can be measured.

a. Test pattern: It is listed as following.

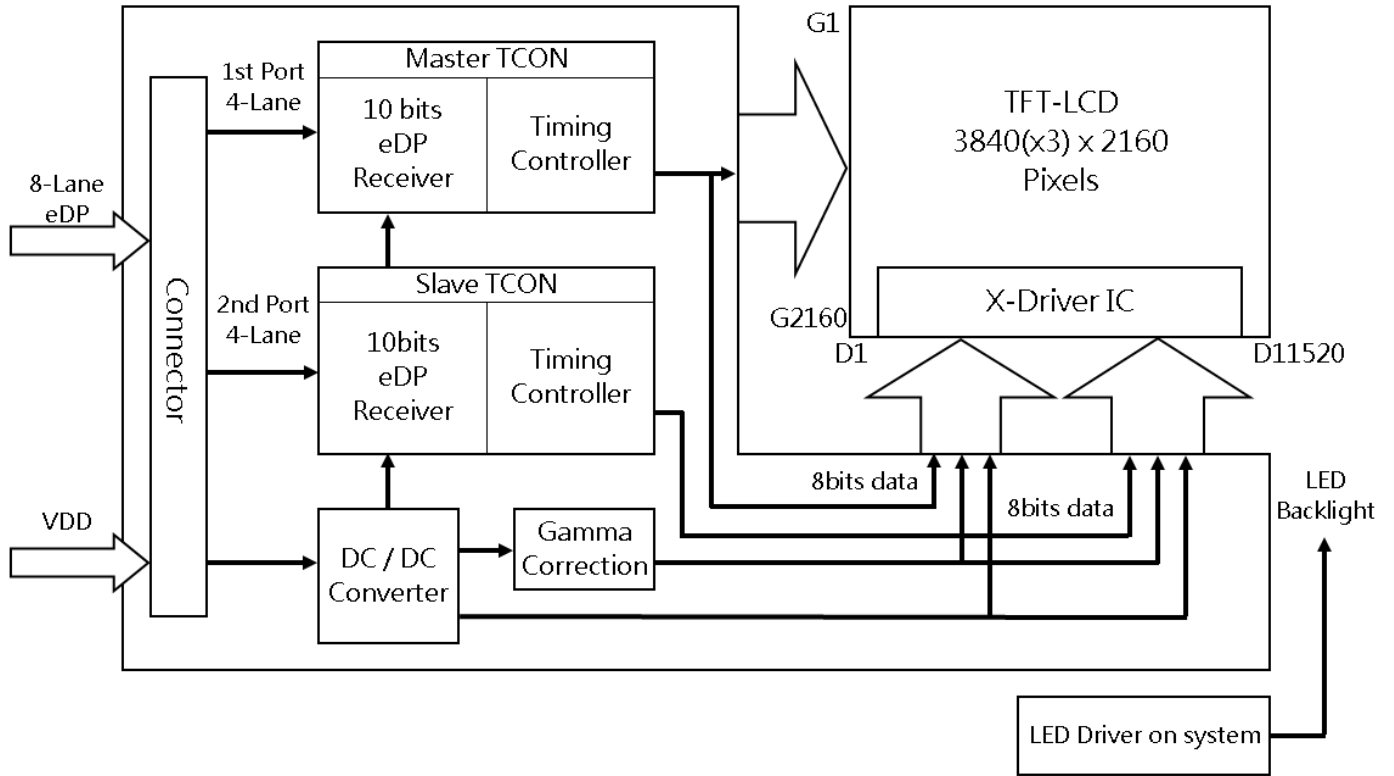


Note 2-9: Evaluation test and mass production inspection shall be applied with LED current I_s @ HDR off condition if there is not specified condition.

3 TFT-LCD Module

3.1 Block Diagram

The following shows the block diagram of the 32.0 inch Color TFT-LCD Module.



3.2 Interface Connection

3.2.1 Connector Type

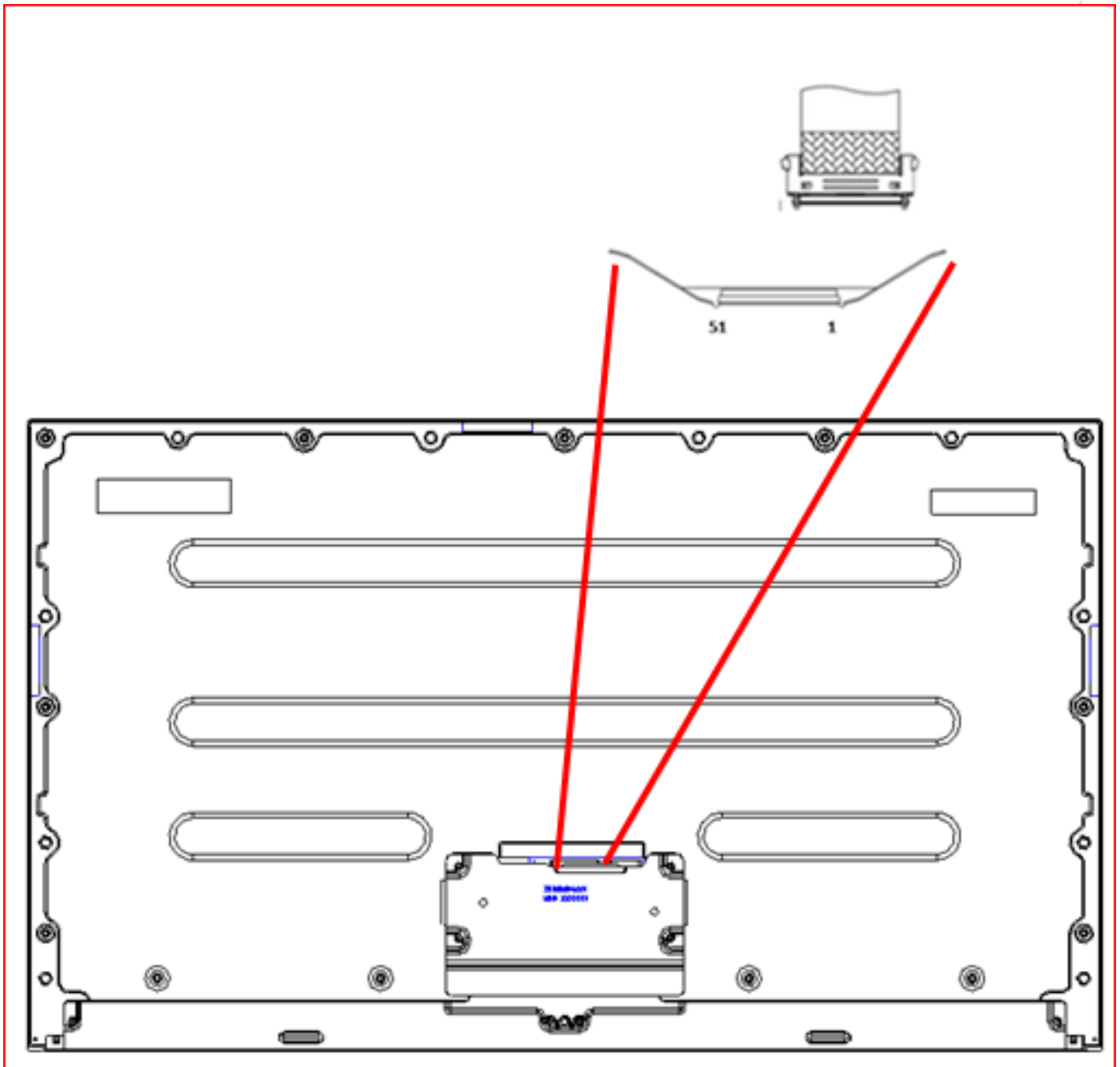
TFT-LCD Connector	Manufacturer	JAE	P-TWO	STARCONN (CHIEF LAND)
	Part Number	FI-RTE5ISZ-HF	I87059-5122	115E51-0000RA-M3-R
Mating Connector	Manufacturer	JAE or Compatible		
	Part Number	FI-RE51CL (Locked Type)		

3.2.2 Connector Pin Assignment

PIN #	Symbol	Description	Remark
1	VDD	Power +12V	
2	VDD	Power +12V	
3	VDD	Power +12V	
4	VDD	Power +12V	
5	VDD	Power +12V	
6	GND	Ground	
7	GND	Ground	
8	GND	Ground	
9	NC	No connection (for AUO test only. Do not connect)	
10	NC	No connection (for AUO test only. Do not connect)	
11	NC	No connection (for AUO test only. Do not connect)	
12	NC	No connection (for AUO test only. Do not connect)	
13	NC	No connection (for AUO test only. Do not connect)	
14	NC	No connection (for AUO test only. Do not connect)	
15	NC	No connection (for AUO test only. Do not connect)	
16	NC	No connection (for AUO test only. Do not connect)	
17	GND	Ground	
18	1st Lane3_N	Negative eDP differential data input	
19	1st Lane3_P	Positive eDP differential data input	
20	GND	Ground	

21	Ist Lane2_N	Negative eDP differential data input	
22	Ist Lane2_P	Positive eDP differential data input	
23	GND	Ground	
24	Ist Lane1_N	Negative eDP differential data input	
25	Ist Lane1_P	Positive eDP differential data input	
26	GND	Ground	
27	Ist Lane0_N	Negative eDP differential data input	
28	Ist Lane0_P	Positive eDP differential data input	
29	GND	Ground	
30	Ist AUX_CH_P	Positive AUX Channel differential data input	
31	Ist AUX_CH_N	Negative AUX Channel differential data input	
32	GND	Ground	
33	NC	No connection (for AUO test only. Do not connect)	
34	GND	Ground	
35	2nd Lane3_N	Negative eDP differential data input	
36	2nd Lane3_P	Positive eDP differential data input	
37	GND	Ground	
38	2nd Lane2_N	Negative eDP differential data input	
39	2nd Lane2_P	Positive eDP differential data input	
40	GND	Ground	
41	2nd Lane1_N	Negative eDP differential data input	
42	2nd Lane1_P	Positive eDP differential data input	
43	GND	Ground	
44	2nd Lane0_N	Negative eDP differential data input	
45	2nd Lane0_P	Positive eDP differential data input	
46	GND	Ground	
47	2nd AUX_CH_P	Positive AUX Channel differential data input	
48	2nd AUX_CH_N	Negative AUX Channel differential data input	
49	GND	Ground	

50	HPD	Hot plug detection	
51	GND	Ground	



3.3 Electrical Characteristics

3.3.1 Absolute Maximum Rating

Permanent damage may occur if exceeding the following maximum rating.

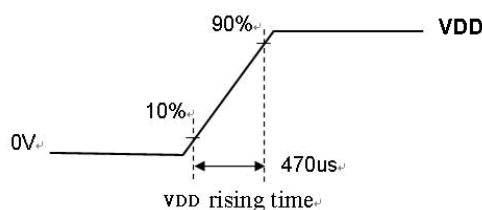
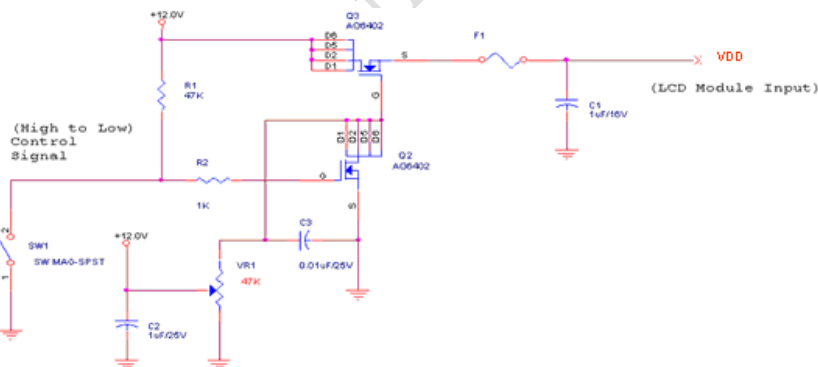
Symbol	Description	Min	Max	Unit	Remark
VDD	Power Supply Input Voltage	GND-0.3	14	[Volt]	Ta=25°C

3.3.2 Recommended Operating Condition

Symbol	Description	Min	Typ	Max	Unit	Remark
VDD	Power supply Input voltage	10.8	12.0	13.2	[Volt]	
IDD	Power supply Input Current (RMS)	-	1.06	1.28	[A]	VDD= 12V, Whie Pattern, Fv=60Hz
		-	1.11	1.34		VDD= 12V, Whie Pattern, Fv=65Hz
PDD	VDD Power Consumption	-	12.72	15.36	[Watt]	VDD= 12V, Whie Pattern, Fv=60Hz
		-	13.32	16.08		VDD= 12V, Whie Pattern, Fv=65Hz
IRush	Inrush Current	-	-	3.0	[A]	Note 3-2
VDDrp	Allowable VDD Ripple Voltage	-	-	500	[mVolt]	VDD= 12V, Whie Pattern, Fv=60Hz

Note 3-1: Inrush Current measurement:

Test circuit:



The duration of VDD rising time: 470us.



3.4.2 eDP Data Format

1st Lane0	1st Lane1	1st Lane2	1st Lane3
R1-9:2	R2-9:2	R3-9:2	R4-9:2
R1-1:0IG1-9:4	R2-1:0IG2-9:4	R3-1:0IG3-9:4	R4-1:0IG4-9:4
G1-3:0IB1-9:6	G2-3:0IB2-9:6	G3-3:0IB3-9:6	G4-3:0IB4-9:6
B1-5:0IR5-9:8	B2-5:0IR6-9:8	B3-5:0IR7-9:8	B4-5:0IR8-9:8
R5-7:0	R6-7:0	R7-7:0	R8-7:0
G5-9:2	G6-9:2	G7-9:2	G8-9:2
G5-1:0IB5-9:4	G6-1:0IB6-9:4	G7-1:0IB7-9:4	G8-1:0IB8-9:4
B5-3:0IR9-9:6	B6-3:0IR10-9:6	B7-3:0IR11-9:6	B8-3:0IR12-9:6
R9-5:0IG9-9:8	R10-5:0IG10-9:8	R11-5:0IG11-9:8	R12-5:0IG12-9:8
G9-7:0	G10-7:0	G11-7:0	G12-7:0
B9-9:2	B10-9:2	B11-9:2	B12-9:2
B9-1:0IR13-9:4	B10-1:0IR14-9:4	B11-1:0IR15-9:4	B12-1:0IR16-9:4
R13-3:0IG13-9:6	R14-3:0IG14-9:6	R15-3:0IG15-9:6	R16-3:0IG16-9:6
G13-5:0IB13-9:8	G14-5:0IB14-9:8	G15-5:0IB15-9:8	G16-5:0IB16-9:8
B13-7:0	B14-7:0	B15-7:0	B16-7:0
.	.	.	.
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2nd Lane0	2nd Lane1	2nd Lane2	2nd Lane3
R1921-9:2	R1922-9:2	R1923-9:2	R1924-9:2
R1921-1:0IG1921-9:4	R1922-1:0IG1922-9:4	R1923-1:0IG1923-9:4	R1924-1:0IG1924-9:4
G1921-3:0IB1921-9:6	G1922-3:0IB1922-9:6	G1923-3:0IB1923-9:6	G1924-3:0IB1924-9:6
B1921-5:0IR1925-9:8	B1922-5:0IR1926-9:8	B1923-5:0IR1927-9:8	B1924-5:0IR1928-9:8
R1925-7:0	R1926-7:0	R1927-7:0	R1928-7:0
G1925-9:2	G1926-9:2	G1927-9:2	G1928-9:2
G1925-1:0IB1925-9:4	G1926-1:0IB1926-9:4	G1927-1:0IB1927-9:4	G1928-1:0IB1928-9:4
B1925-3:0IR1929-9:6	B1926-3:0IR1930-9:6	B1927-3:0IR1931-9:6	B1928-3:0IR1932-9:6
R1929-5:0IG1929-9:8	R1930-5:0IG1930-9:8	R1931-5:0IG1931-9:8	R1932-5:0IG1932-9:8
G1929-7:0	G1930-7:0	G1931-7:0	G1932-7:0
B1929-9:2	B1930-9:2	B1931-9:2	B1932-9:2
B1929-1:0IR1933-9:4	B1930-1:0IR1934-9:4	B1931-1:0IR1935-9:4	B1932-1:0IR1936-9:4
R1933-3:0IG1933-9:6	R1934-3:0IG1934-9:6	R1935-3:0IG1935-9:6	R1936-3:0IG1936-9:6
G1933-5:0IB1933-9:8	G1934-5:0IB1934-9:8	G1935-5:0IB1935-9:8	G1936-5:0IB1936-9:8
B1933-7:0	B1934-7:0	B1935-7:0	B1936-7:0
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3.4.4 eDP Specification (Follow as VESA DisplayPort Standard Version 1.2)

a. DisplayPort main link signal:

DisplayPort main link					
		Min	Typ	Max	unit
Frequency	Main link Frequency	-	2.7	-	Gbps
UI	Unit Interval	-	370	-	ps
VCM	RX input DC Common Mode Voltage	-	0	-	[Volt]
VDiff _{P-P}	Peak-to-peak Voltage at a receiving Device	150	-	-	[mVolt]
Down_Spread_Freq	Link clock down spread frequency	30	-	33	KHz
Down_Spread_Amplitude	Link clock down spread amplitude	-	-	0.5	%

Point	Time (UI)	Voltage (V)
1	0.245	0
2	0.5	75mV
3	0.755	0
4	0.5	-75mV

Figure 5.55.3 Downstream Device EYE Mask at Receiver Connector for HBR

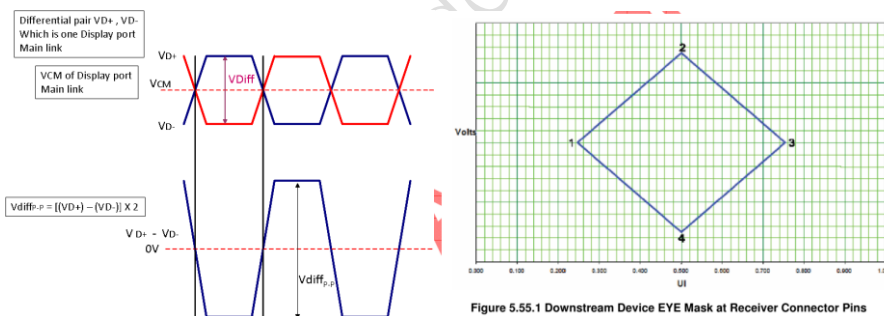
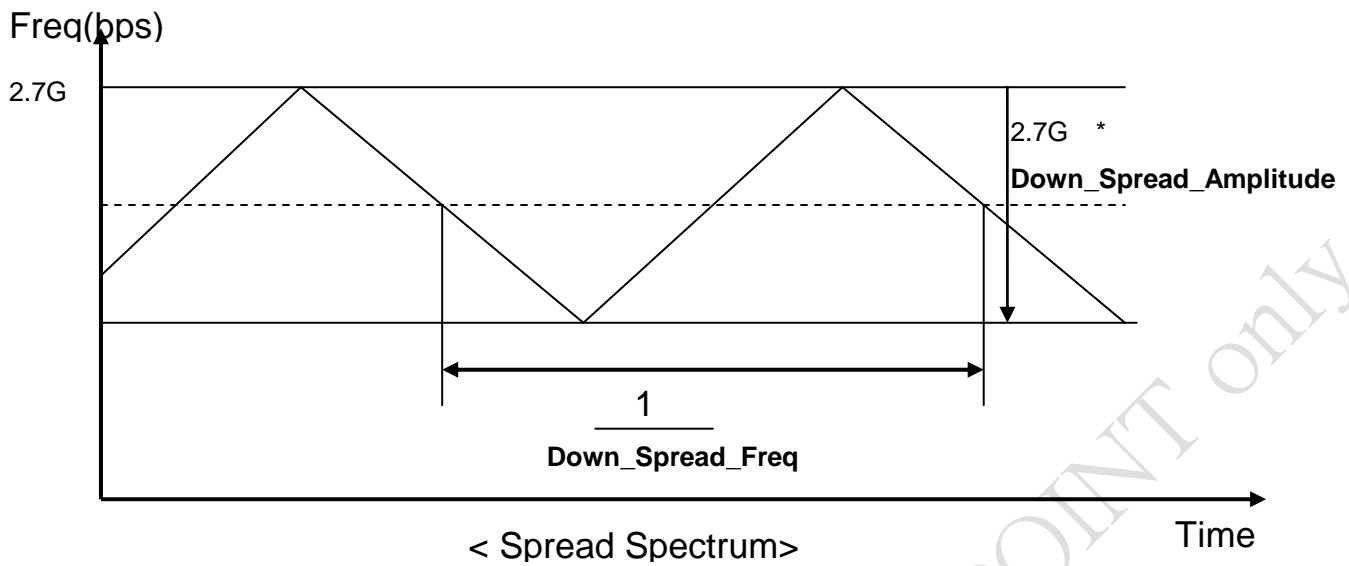
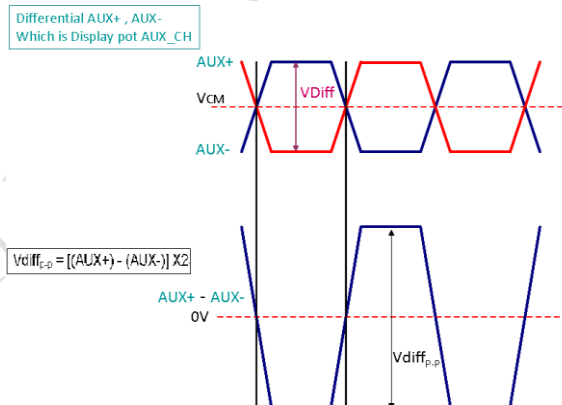


Figure 5.55.1 Downstream Device EYE Mask at Receiver Connector Pins



b. DisplayPort AUX_CH signal:

DisplayPort AUX_CH					
		Min	Typ	Max	unit
VCM	AUX DC Common Mode Voltage	0	-	2.0	[Volt]
VDiff _{p,p}	AUX Peak-to-peak voltage at a receiving device	0.27	-	1.36	[Volt]



c. DisplayPort VHPD signal:

Display Port VHPD					
		Min	Typ	Max	unit
VHPD	HPD Voltage	2.25	-	3.6	[Volt]



d. Intra-Pair skew

LRX-SKEW-INTRA_PAIR					
		Min	Typ	Max	unit
LRX-SKEW-INTRA_PAIR	Lane Intra-pair Skew Tolerance	-	-	60	[ps]

e. Inter-Pair Skew

LRX-SKEW-INTER_PAIR					
		Min	Typ	Max	unit
LRX-SKEW-INTER_PAIR	Lane-to-Lane Skew at RX package pins	-	-	5200	[ps]

3.4.5 Input Timing Specification

The input timing is shown as the following table.

Symbol	Description		Min.	Typ.	Max.	Unit	Remark
Tv	Vertical Section	Period	2180	2200	4500	Th	
Tdisp (v)		Active	2160	2160	2160	Th	
Tblk (v)		Blanking	20	40	2340	Th	
Fv		Frequency	29	60	65	Hz	<i>Note 3-5</i> <i>Note 3-6</i>
Th	Horizontal Section	Period	2000	2100	3520	Tclk	
Tdisp (h)		Active	1920	1920	1920	Tclk	
Tblk (h)		Blanking	80	180	1600	Tclk	
Fh		Frequency	40.0	131.9	144.0	kHz	<i>Note 3-3</i>
Tclk	Pixel Clock	Period	3.5	3.6	12.5	ns	1/Fclk
Fclk		Frequency	80.0	277.0	288.0	MHz	<i>Note 3-4</i>
Link Rate per Lane			2.7			Gbps	

Note 3-3: The equation is listed as following. Please don't exceed the above recommended value.

$$Fh (\text{Min.}) = Fclk (\text{Min.}) / Th (\text{Min.})$$

$$Fh (\text{Typ.}) = Fclk (\text{Typ.}) / Th (\text{Typ.})$$

$$Fh (\text{Max.}) = Fclk (\text{Max.}) / Th (\text{Min.})$$

Note 3-4: The equation is listed as following. Please don't exceed the above recommended value.

$$\text{1st Lane N \& 2nd Lane N skew} < 200\text{ns}$$

$$Fclk (\text{Typ.}) = Fv (\text{Typ.}) \times Th (\text{Typ.}) \times Tv (\text{Typ.})$$

$$Fclk (\text{Min.}) \leq Fv \times Th \times Tv \leq Fclk (\text{Max.})$$

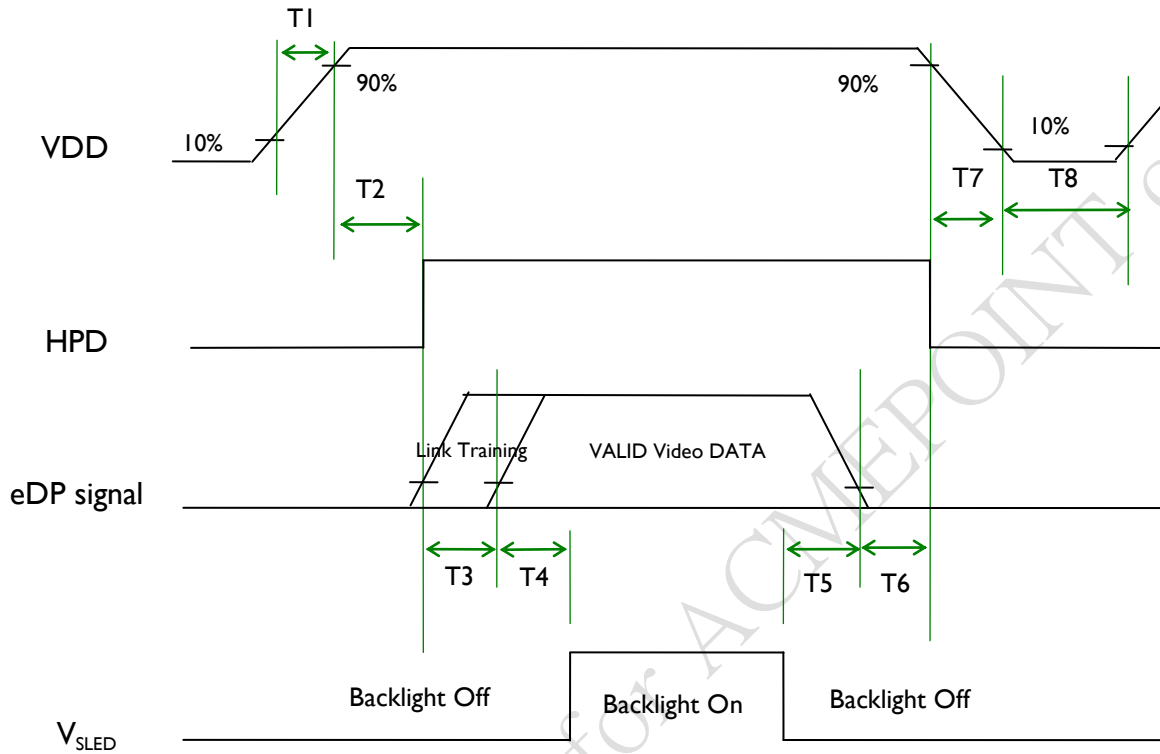
Note 3-5: The equation is listed as following. Please don't exceed the above recommended value.

$$Fv = Fclk(\text{Typ.}) / (Tv \times Th)$$

Note 3-6: The optimal Vertical Frequency is 50~65 Hz for best picture quality.

3.5 Power ON/OFF Sequence

VDD power, eDP signal and backlight on/off sequence are as following. eDP signals from any system shall be Hi-Z state when VDD is off.



Power Sequence Timing

Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
T1	0.5	-	10	[ms]	
T2	0	-	200	[ms]	
T3	0	-	-	[ms]	<i>Note 3-7</i>
T4	500	-	-	[ms]	
T5	100	-	-	[ms]	
T6	0	-	50	[ms]	<i>Note 3-8</i> <i>Note 3-9</i>
T7	0	-	200	[ms]	<i>Note 3-9</i> <i>Note 3-10</i>
T8	1000	-	-	[ms]	

Note 3-7: During T3 period, eDP link training time by customer's system.

Note 3-8: Recommend setting T6 = 0ms to avoid electronic noise when VDD is off.

Note 3-9: During T6 & T7 period, please keep the level of input eDP signals with Hi-Z state.



Product Specification

M320QAN02.0

AU OPTRONICS CORPORATION

AUO-General

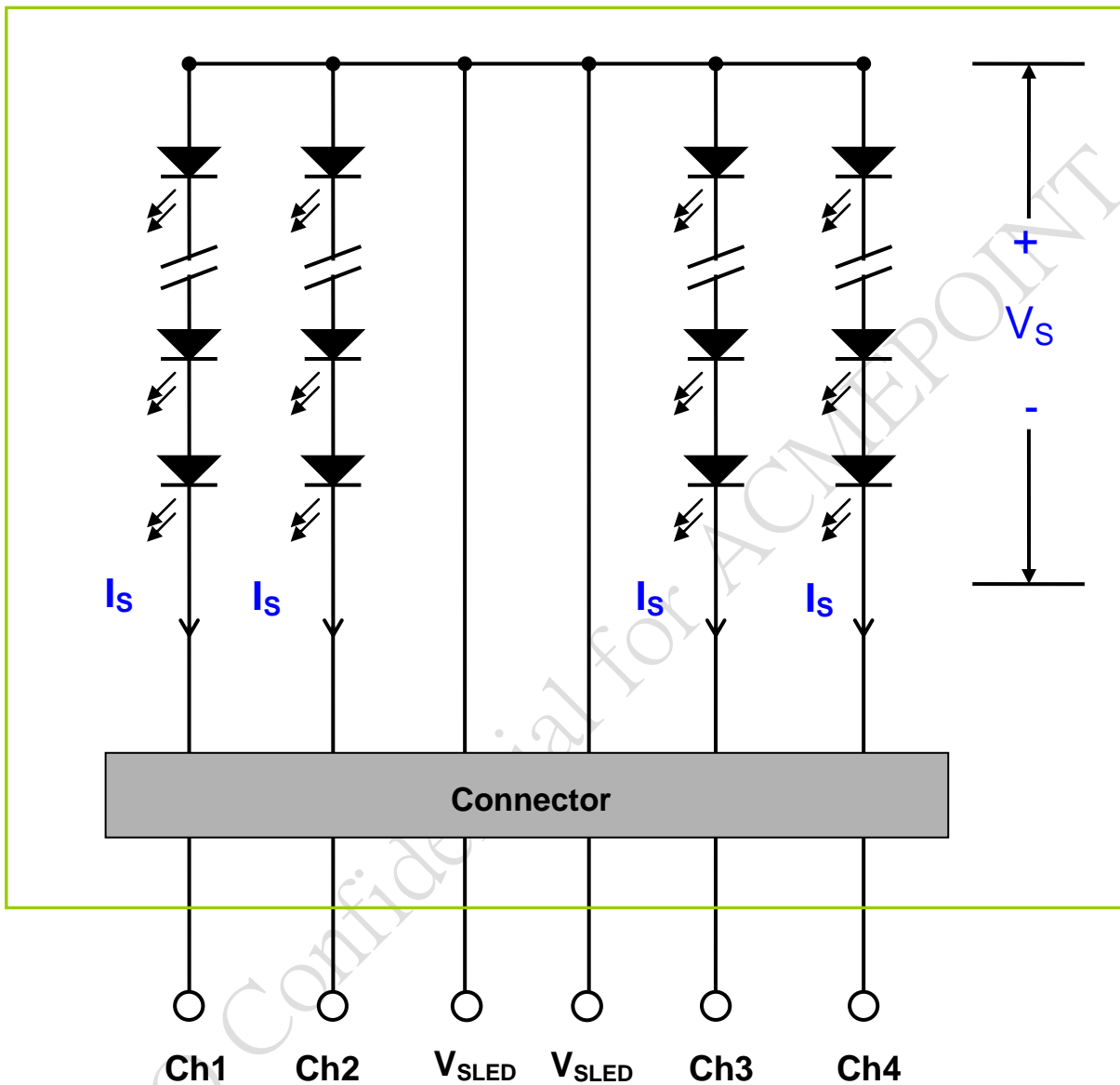
Note 3-10: Voltage of VDD must decay smoothly after power-off.(customer system decide this value)

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4 Backlight Unit

4.1 Block Diagram

The following shows the block diagram of the 32.0 inch Backlight Unit. And it includes 2 pcs LED light bar in Backlight Unit. Each LED light bar includes 44 pcs LED package. (4 strings and 11 pcs LED of one string).



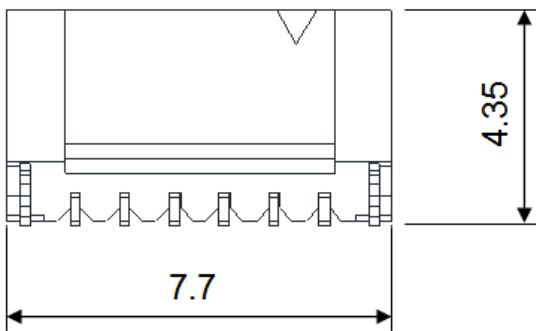
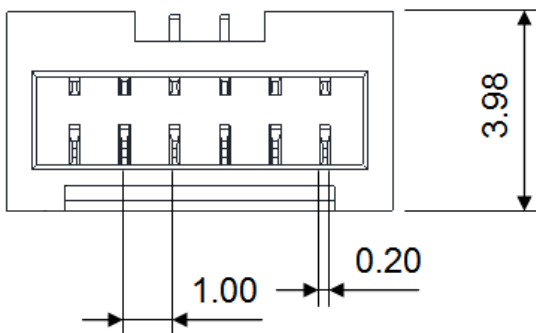
4.2 Interface Connection

4.2.1 Connector Type

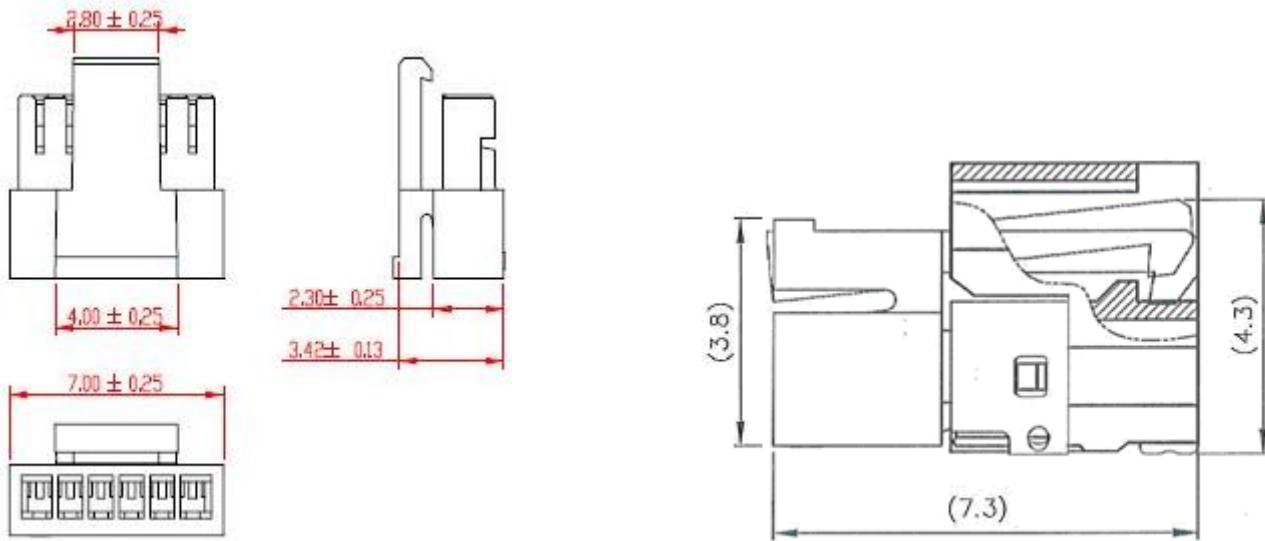
Backlight Connector	Manufacturer	Cvilux
	Part Number	CII406MIVLD-NH
Mating Connector	Manufacturer	ENTERY
	Part Number	HI12K-P06N-00B (Non-Locking type) HI12K-P06N-11B(White) (Locking type) HI12K-P06N-13B(Black) (Locking type)

Backlight Connector dimension:

$$H \times V \times D = 13.9 \times 3.00 \times 4.25, \text{Pitch} = 1.0(\text{unit} = \text{mm})$$

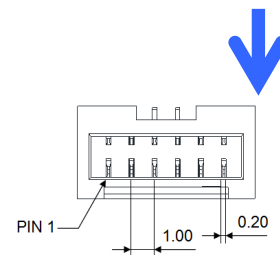
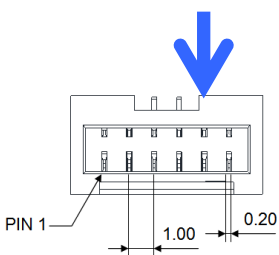
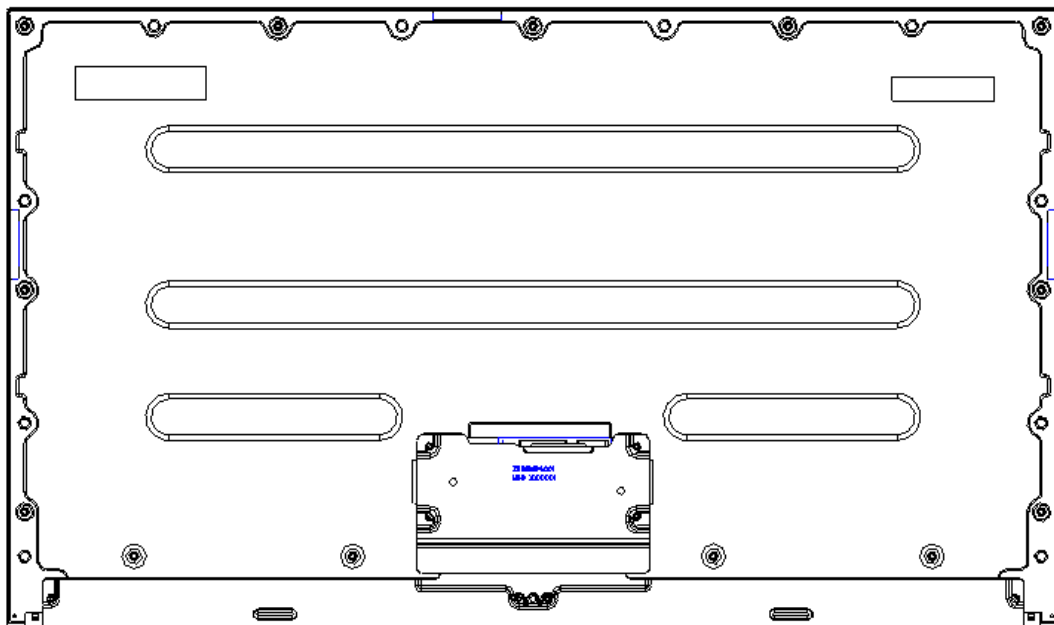


Mating Connector dimension:



4.2.2 Connector Pin Assignment

Pin#	Symbol	Description	Remark
1	Ch1	LED Current Feedback Terminal (Channel 1)	
2	Ch2	LED Current Feedback Terminal (Channel 2)	
3	V _{SLED}	LED Power Supply Voltage Input Terminal	
4	V _{SLED}	LED Power Supply Voltage Input Terminal	
5	Ch3	LED Current Feedback Terminal (Channel 3)	
6	Ch4	LED Current Feedback Terminal (Channel 4)	



4.3 Electrical Characteristics

4.3.1 Absolute Maximum Rating

Permanent damage may occur if exceeding the following maximum rating.

(Ta=25°C)

Symbol	Description	Min	Max	Unit	Remark
Is	LED String Current	0	120	[mA]	100% duty ratio

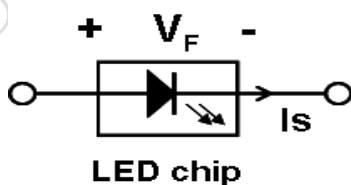
4.3.2 Recommended Operating Condition

Symbol	Description	Min.	Typ.	Max.	Unit	Remark
Is	LED String Current		90	99	[mA]	100% duty ratio of LED chip;
Vs	LED String Voltage	29.92	32.01	36.3	[Volt]	Is=90mA @100% duty ratio; Note 4-1&Note 4-5
ΔVs	Maximum Vs Voltage Deviation of light bar			2.2	[Volt]	Is=90mA @ 100% duty ratio; Note 4-2
P _{BLU}	LED Light Bar Power Consumption	21.54	23.05	26.14	[Watt]	Note 4-3
LT _{LED}	LED Life Time	30000			[Hour]	Note 4-4
OVP	Over Voltage Protection in system board	110% Vs(Max.)			[Volt]	Note 4-5

Note 4-1: $V_s (Typ.) = V_F (Typ.) \times \text{LED No. (one string)}$;

a. V_F : LED chip forward voltage , $V_F (Min.) = 2.72 \text{ V}$, $V_F (Typ.) = 2.91 \text{ V}$, $V_F (Max.) = 3.3 \text{ V}$

b. The same equation to calculate $V_s (Min.)$ & $V_s (Max.)$ for respective $V_F (Min.)$ & $V_F (Max.)$;



Note 4-2: $\Delta V_s (Max.) = \Delta V_F \times \text{LED No. (one string)}$;

a. ΔV_F : LED chip forward voltage deviation (0.2 V , each Bin of LED V_F)

Note 4-3: $P_{BLU} (Typ.) = V_s (Typ.) \times I_s (Typ.) \times 8$ (8 is total String No. of BLU)

$$P_{BLU} (Max.) = V_s (Max.) \times I_s (Typ.) \times 8$$

Note 4-4: Definition of life time:

- a. Brightness of LED becomes to 50% of its original value
- b. Test condition: $I_s = 90mA$ and $25^{\circ}C$ (Room Temperature)

Note 4-5: Recommendation for LED driver power design:

Due to there are electrical property deviation in LED & monitor set system component after long time operation. AUO strongly recommend the design value of LED driver board OVP (over voltage protection) should be 10% higher than max. value of LED string voltage (V_s) at least.

Note 4-6: AUO strongly recommend “Analog Dimming” method for backlight brightness control for Way Noise Free. Otherwise, recommend that Dimming Control Signal (PWM Signal) should be synchronized with Frame Frequency

Note 4-7 Ensure that the LED light bar is not subjected either forward or reverse voltage while monitor set is on standby mode or not in use.

5 Reliability Test

AUO reliability test items are listed as following table. (*Bare Panel only*)

Items	Condition	Remark
Temperature Humidity Bias (THB)	Ta= 50°C, 80%RH, 300hours	
High Temperature Operation (HTO)	Ta= 50°C, 50%RH, 300hours	
Low Temperature Operation (LTO)	Ta= 0°C, 300hours	
High Temperature Storage (HTS)	Ta= 60°C, 300hours	
Low Temperature Storage (LTS)	Ta= -20°C, 300hours	
Vibration Test (Non-operation)	Frequency:10~57Hz/Vibration width(one side):0.075mm : 58~500Hz/Acceleration:9.8 m/s ² Sweep time: 11 minutes Test period: 3 hours(1h for each direction of X,Y,Z)	
Shock Test (Non-operation)	Acceleration: 50 G Wave: Half-sine Active Time: 20 ms Direction: ±X, ±Y, ±Z (one time for each Axis)	
Thermal Shock Test (TST)	-20°C/30min, 60°C/30min, 100 cycles	Note 5-1
On/Off Test	On/10sec, Off/10sec, 30,000 cycles	
ESD (Electro Static Discharge)	Contact Discharge: ± 15KV, 150pF(330Ω) 1sec, 8 points, 25 times/ point.	Note 5-2
	Air Discharge: ± 15KV, 150pF(330Ω) 1sec 8 points, 25 times/ point.	
Altitude Test	Operation:18,000 ft Non-Operation:40,000 ft	

- Note 5-1:** a. A cycle of rapid temperature change consists of varying the temperature from -20°C to 60°C, and back again. Power is not applied during the test.
b. After finish temperature cycling, the unit is placed in normal room ambient for at least 4 hours before power on.

- Note 5-2:** EN61000-4-2, ESD class B: Certain performance degradation allowed
No data lost
Self-recoverable
No hardware failures.

ESD discharged points should avoid display area and periphery front bezel of display area. Suggest points were 4 side parallel edge of display area surface.

Metal front bezel must cover half area of BM (black matrix), and metal front

bezel must connect with metal back bezel to protect source IC of panel by ESD damaged.



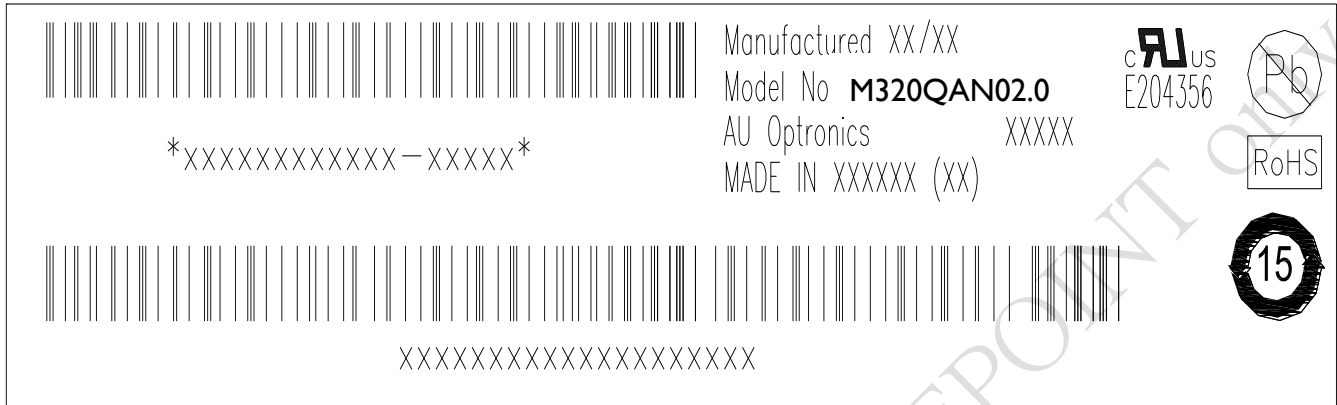
Note 5-3: Result Evaluation Criteria:

TFT-LCD panels test should take place after gradually cooling enough at room temperature. In the normal application, there should be no particular problems that may affect the display function.

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6 Shipping Label

The label is on the panel as shown below:



Note 6-1: For Pb Free products, AUO will add  for identification.

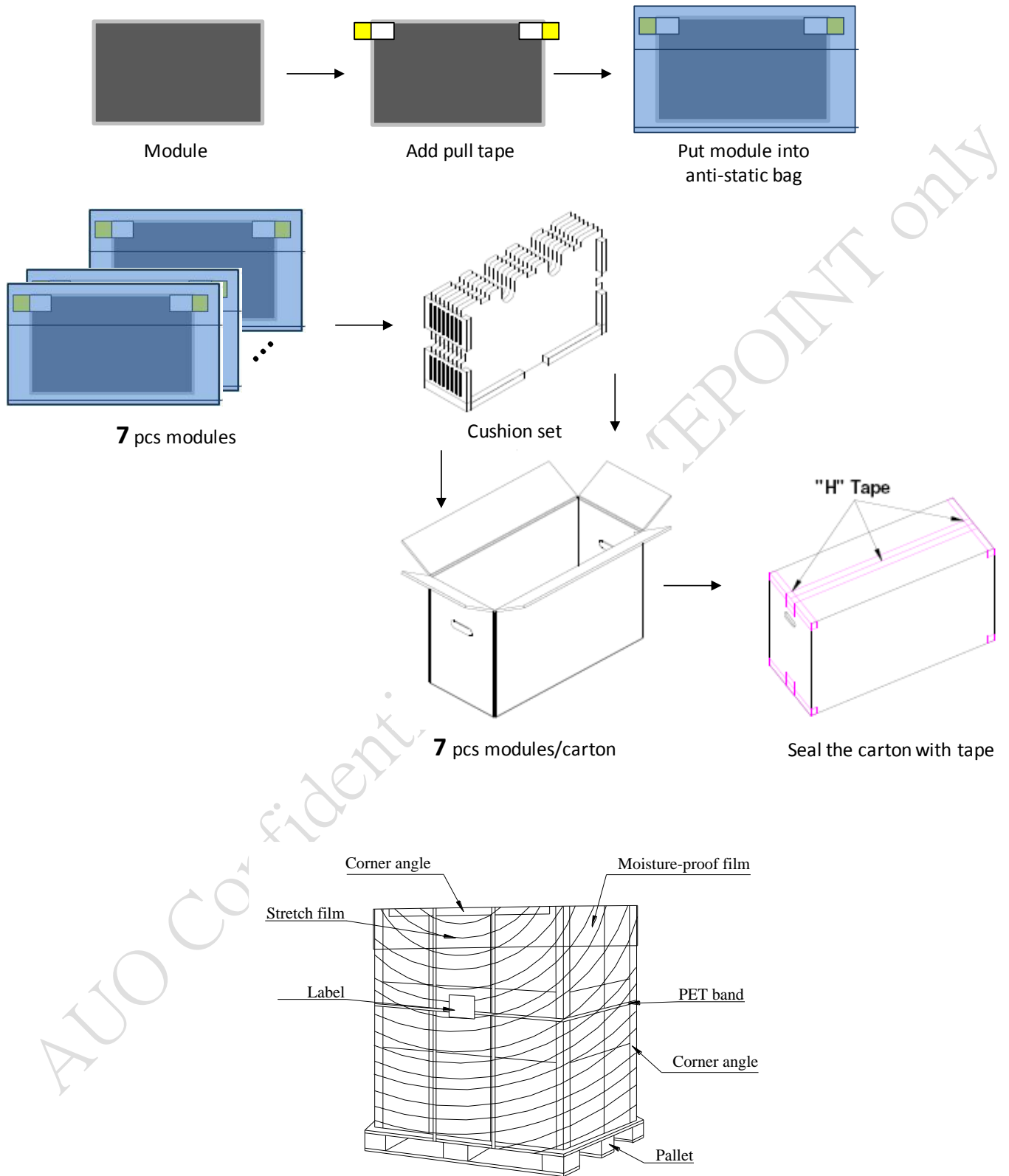
Note 6-2: For RoHS compatible products, AUO will add  for identification.

Note 6-3: For China RoHS compatible products, AUO will add  for identification.

Note 6-4: The Green Mark will be presented only when the green documents have been ready by AUO Internal Green Team.

8 Packing Specification

8.1 Packing Flow



8.2 Pallet and shipment information

Item	Specification			Remark
	Q'ty	Dimension	Weight(kg)	
Panel	1	721.68 (H)mm x 417.93 (V)mm x 15.57 (D)mm	4.90	
Cushion	1	-	4.54	
Box	1	805(L)mm x 280(W)mm x 514(H)mm		without Panel
Packing Box	7 pcs/Box	805(L)mm x 280(W)mm x 514(H)mm	38.84	with panel & cushion & Box
Pallet	1	1150(L)mm x 840(W)mm x 132(H)mm	13.6	
Pallet after Packing	8 boxes/pallet	1150(L)mm x 840(W)mm x 1160(H)mm	324.32	

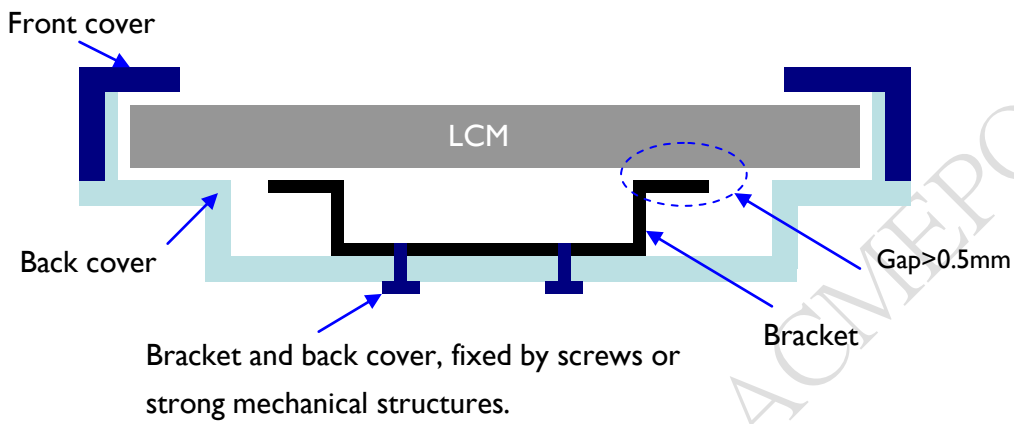
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9 Design Guide for System

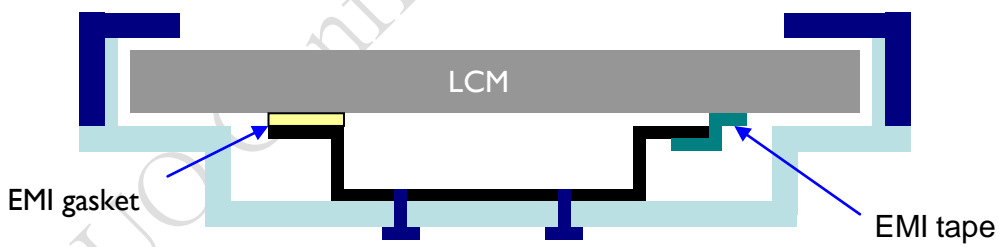
9.1 AHVA design guide

9.1.1 The gap between LCM and system rear bracket should be bigger than 0.5mm.

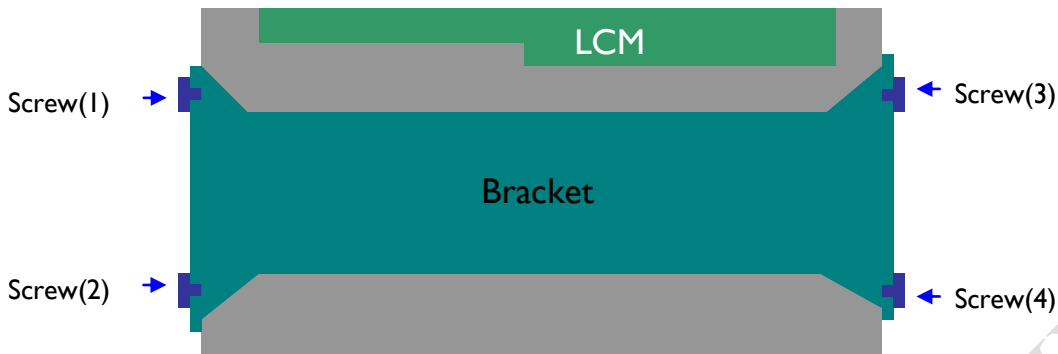
9.1.2 The system bracket should be fixed on back cover firmly.



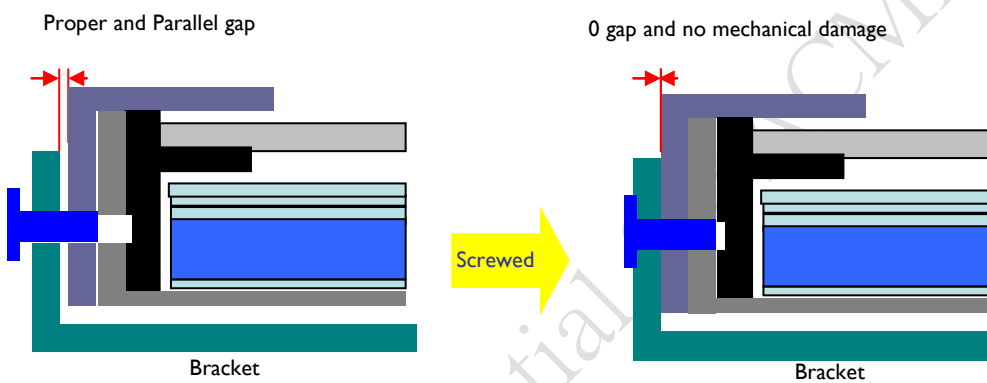
9.1.3 The EMI gasket should be uniform and not push panel strongly.



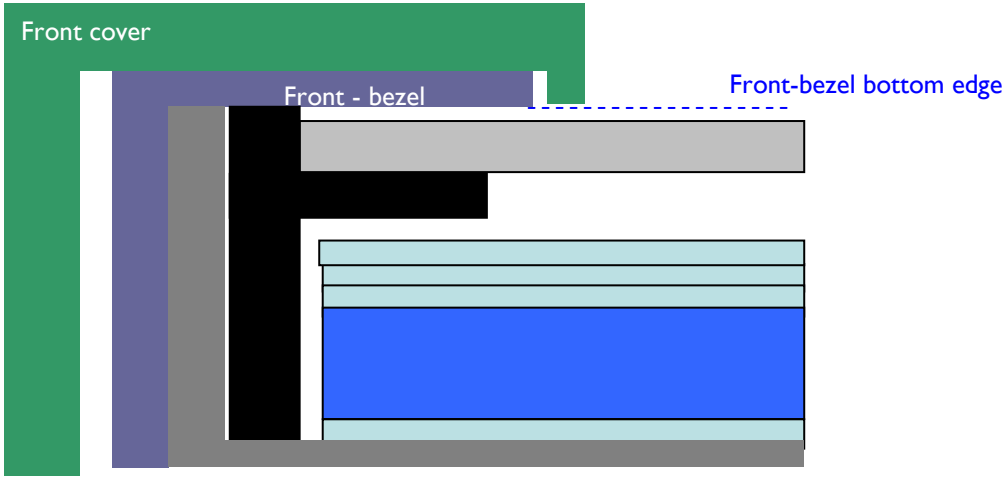
9.1.4 For stable assembly, the system bracket should use 4 screws to fix system and panel by dual sides.



9.1.5 The system bracket and panel should be in parallel with having no gap after inserting screws.



9.1.6 Avoid scratching LCM, the rib on system front-cover should not exceed the bottom edge of LCM's front-bezel.



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