2.13 inch EPD (104*212) Module

Product Specification P0

(preliminary)

IC Type：SSD1675

Buyer	
Supplier	**BEIJING BOE Optoelectronics Technology CO. LTD**

ITEM	SIGNATURE	DATE
Approved		
Reviewed		
Prepared		

BEIJING BOE OPTOELECTRONICS TECHNOLOGY

REVISION HISTORY

REV.	ECN No.	DESCRIPTION OF CHANGES	DATE	PREPARED
P0		Initial Release	2019.05.13	Gao Yinan

Contents

1. Over View

The display is an Active Matrix Electrophoretic Display (AM EPD), with interface and a reference system design. The display is capable to display images at 1-bit white, black and red full display capabilities. The 2.13 inch active area contains 104*212 pixels. The module is a TFT-array driving electrophoresis display, with integrated circuits including gate driver, source driver, MCU interface, timing controller, oscillator, DC-DC, SRAM, LUT, VCOM. Module can be used in portable electronic devices, such as Electronic Shelf Label (ESL) System.

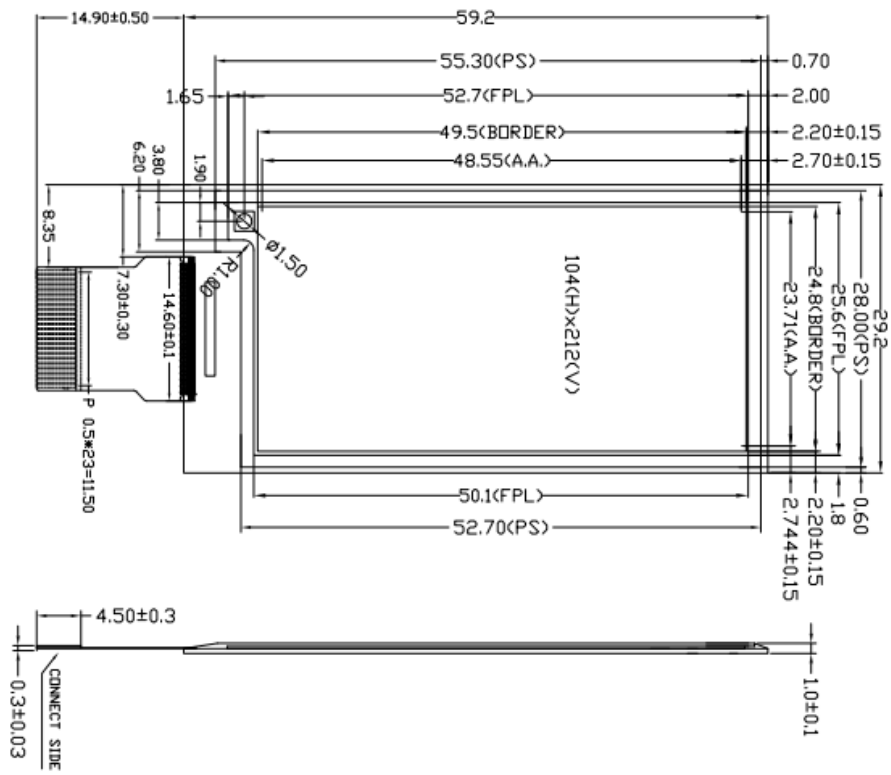
2. Features

- 104(S)*212(G) pixels display
- High contrast High reflectance
- Ultra wide viewing angle Ultra low power consumption
- Pure reflective mode
- Bi-stable display
- Commercial temperature range
- Landscape portrait modes
- Hard-coat antiglare display surface
- Ultra Low current deep sleep mode
- On chip display RAM
- Waveform can stored in On-chip OTP or written by MCU
- Serial peripheral interface available
- On-chip oscillator, On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- I2C signal master interface to read external temperature sensor
- Built-in temperature sensor

3. Mechanical Specification

Parameter	Specifications	Unit	Remark
Screen Size	2.13	Inch	
Display Resolution	104(H)×212(V)	Pixel	DPI：110
Active Area	23.71(H)×48.55(V)	mm	
Pixel Size	0.228×0.229	mm	
Outline Dimension	29.2(H)×59.2(V)×1.0(T)	mm	
Weight	3.2±0.5	g	

4. Mechanical Drawing of EPD Module



5. Input/output Pin Assignment （Connector:FH34SRJ-24S-0.5SH）

NO.	Name	I/O	Description	Remark
1	NC	NC	Do not connect with other NC pins	Keep Open
2	GDR	O	N-Channel MOSFET Gate Drive Control	
3	RESE	I	Current Sense Input for the Control Loop	
4	NC	NC	Do not connect with other NC pins	Keep Open
5	VDHR	C	Positive Source driving voltage(Red)	
6	TSCL	O	I2C Interface to digital temperature sensor Clock pin	
7	TSDA	I/O	I2C Interface to digital temperature sensor Data pin	
8	BS	I	Bus Interface selection pin	Note 5-1
9	BUSY_N	O	Busy state output pin	Note 5-2
10	RST_N	I	Reset signal input	Note 5-3
11	DC	I	Data /Command control pin	Note 5-4
12	CSB	I	Chip select input pin	Note 5-5
13	SCL	I	Serial Clock pin (SPI)	
14	SDA	I	Serial Data pin (SPI)	
15	VDDIO	P	Power Supply for interface logic pins. It should be connected with VDD	
16	VDD	P	Power Supply for the chip	
17	GND	P	Ground	

5. Input/output Pin Assignment

NO.	Name	I/O	Description	Remark
18	VDDD	C	Core logic power pin VDDD can be regulated internally from VDD. A capacitor should be connected between VDDD and GND	
19	VPP	P	Power Supply for OTP Programming.	
20	VSH	C	Positive Source driving voltage	
21	VGH	C	Power Supply pin for Positive Gate driving voltage and VSH	
22	VSL	C	Negative Source driving voltage	
23	VGL	C	Power Supply pin for Negative Gate driving voltage VCOM and VSL	
24	VCOM	C	VCOM driving voltage	

Note:

1. I = Input Pin, O =Output Pin, I/O = Bi-directional Pin (Input/output), P = Power Pin, C = Capacitor Pin
2. Note 5-1: Bus interface selection pin

BS State	MUC Interface
L	4-lines serial peripheral interface(SPI) - 8 bits SPI
H	3-lines serial peripheral interface(SPI) - 9 bits SPI

3. Note 5-2: This pin (BUSY_N) is Busy state output pin. When BUSY_N is HIGH: Driver is busy, data/VCOM is transforming. BUSY_N is LOW : non-busy. Host side can send command/data to driver.
4. Note 5-3: This pin (RST_N) is reset signal input. When RST_N become low, driver will reset.
5. Note 5-4: This pin is (DC) Data/Command control pin connecting to the MCU in 4-wire SPI mode. When the pin is pulled HIGH, the data at SDA will be interpreted as data. When the pin is pulled LOW, the data at SDA will be interpreted as command.
6. Note 5-5: This pin (CSB) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CSB is pulled LOW.

6. Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Logic supply voltage	VDD	-0.5 to +4.0	V
Logic Input voltage	VIN	-0.5 to VDD +0.5	V
Logic Output voltage	VOUT	-0.5 to VDD +0.5	V
Operating Temp range Max	TOPRm	0 to +40	ºC.
Storage Temp range	TSTG	-25 to +60	ºC.

Note: Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Panel DC Characteristics tables.

7. Electrical Characteristics

7.1 Panel DC Characteristics

The following specifications apply for: GND=0V, VDD=3.0V, TOPR =25ºC.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
Single ground	GND	-		-	0	-	V
Logic supply voltage	VDD	-	VDD	2.3	3.0	3.6	V
Core logic voltage	VDDD		VDDD	1.7	1.8	1.9	V
High level input voltage	V_{IH}	-	-	0.8 VDD	-	-	V
Low level input voltage	V_{IL}	-	-	-	-	0.2 VDD	V
High level output voltage	V_{OH}	I_{OH} = -100uA	-	0.9 VDD	-	-	V

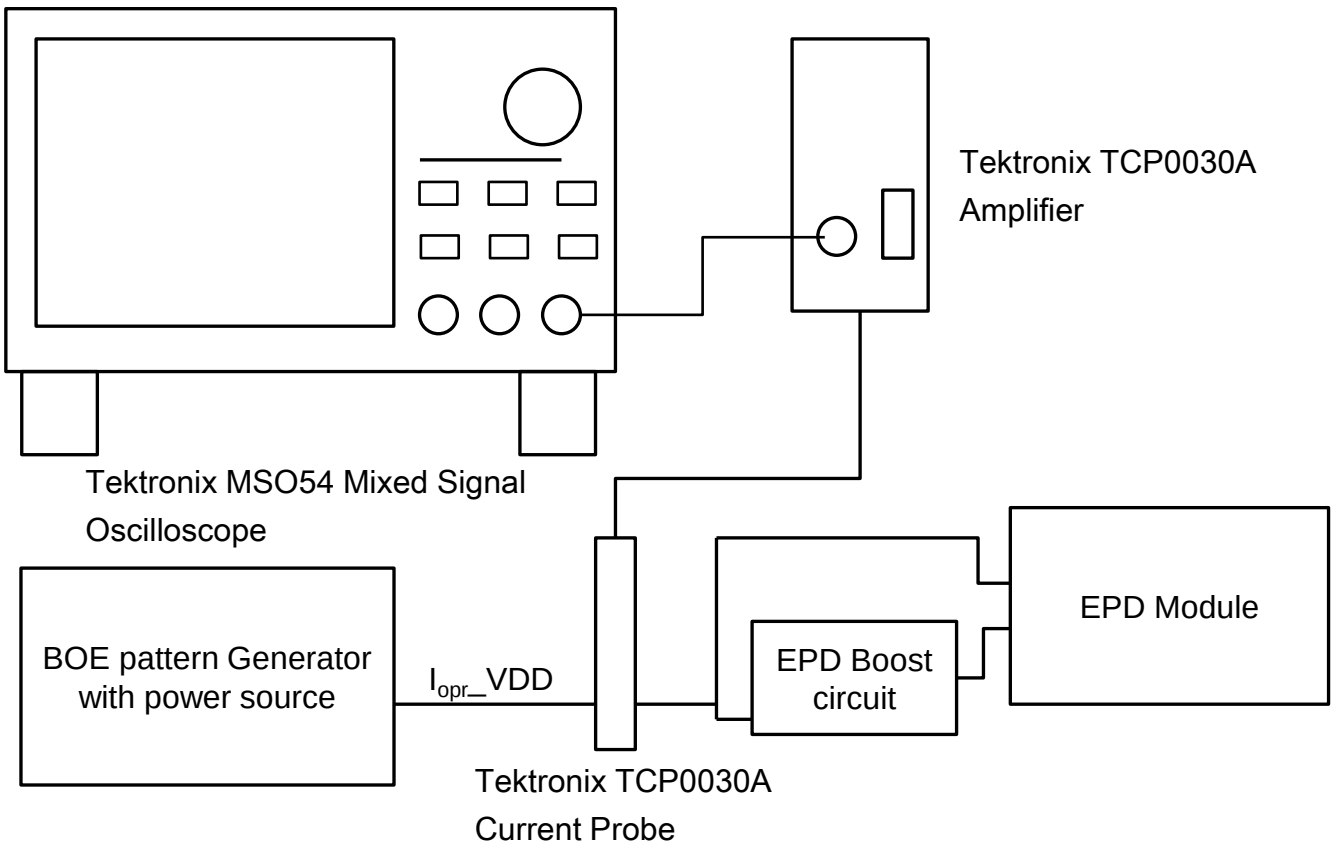
Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
Low level output voltage	V_{OL}	I_{OL} = 100uA	-	-	-	0.1 VDD	V
Typical power	P_{TYP}	VDD=3.0V	-	-	15	-	mW
Deep sleep mode	P_{STPY}	VDD=3.0V	-	-	0.003	-	mW
Typical operating current	I_{opr}_VDD	VDD=3.0V	-	-	5	-	mA
Image update time	-	25 ºC	-	-	14	-	sec
Sleep mode current	I_{slp}_VDD	DC/DC off No clock No input load Ram data retain	-	-	20	-	uA
Deep sleep mode current	I_{dslp}_VDD	DC/DC off No clock No input load Ram data not retain	-	-	1	-	uA

Note：

1. The typical power is measured with following pattern.

2. The deep sleep power is the consumed power when the panel controller is in deep sleep mode.
3. I_{opr}_VDD: The mean current of VDD(EPD Boost circuit)

Current Measurement



7.2 Panel DC Characteristics(Driver IC Internal Regulators)

The following specifications apply for: GND=0V, VDD=3.0V, TOPR =25ºC.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
VCOM output voltage	VCOM	-	VCOM	-3.0	-	-0.1	V
Positive Source output voltage	VSH	-	S0~S103	+14.5	+15	+15.5	V
Negative Source output voltage	VSL	-	S0~S103	-15.5	-15	-14.5	V
Positive gate output voltage	VGH	-	G0~G211	+19	+20	+21	V
Negative gate output voltage	VGL	-	G0~G211	-21	-20	-19	V

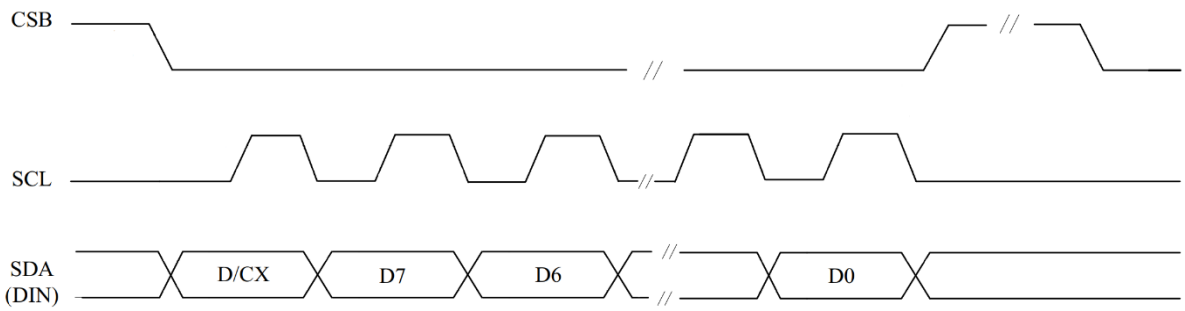
7.3 MCU Interface Selection

The pin assignment at different interface mode is summarized in Table 6-4-1. Different MCU mode can be set by hardware selection on BS1 pins. The display panel only supports 4-wire SPI or 3-wire SPI interface mode.

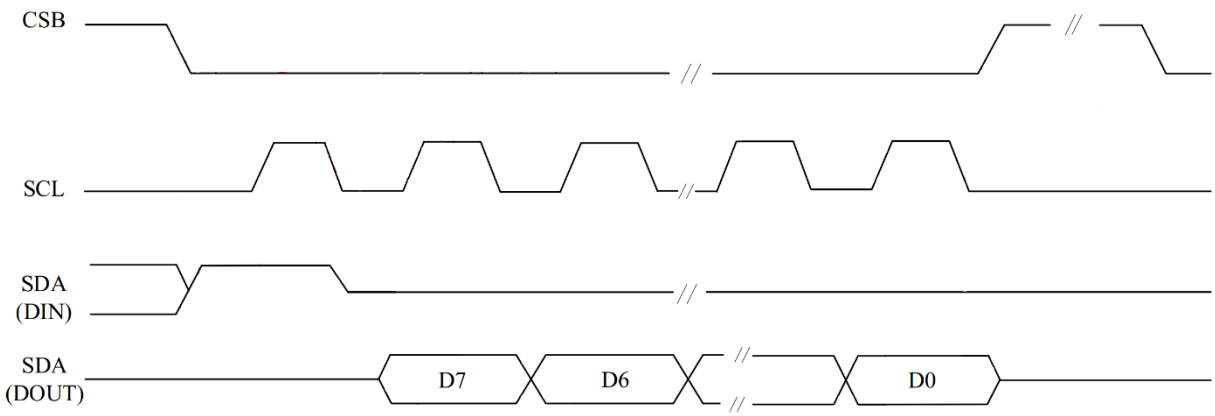
Pin Name	Data/Command Interface		Control Signal		
Bus interface	SDA	SCL	CSB	DC	RST_N
BS1=L 4-wire SPI	SDA	SCL	CSB	DC	RST_N
BS1=H 3-wire SPI	SDA	SCL	CSB	L	RST_N

7.3.1 3-wire Serial Port Interface

3-Wire communication can be bi-directional controlled by the “R/W” bit in address field. 3-Wire engine act as a “slave mode” for all the time, and will not issue any command to the 3-Wire bus itself. Under read mode, 3-Wire engine will return the data during “Data phase”. The returned data should be latched at the rising edge of SCL by external controller. Data in the “Hi-Z phase” will be ignored by 3-Wire engine during write operation, and should be ignored during read operation also. During read operation, external controller should float SDA pin under “Hi-Z phase” and “Data phase”



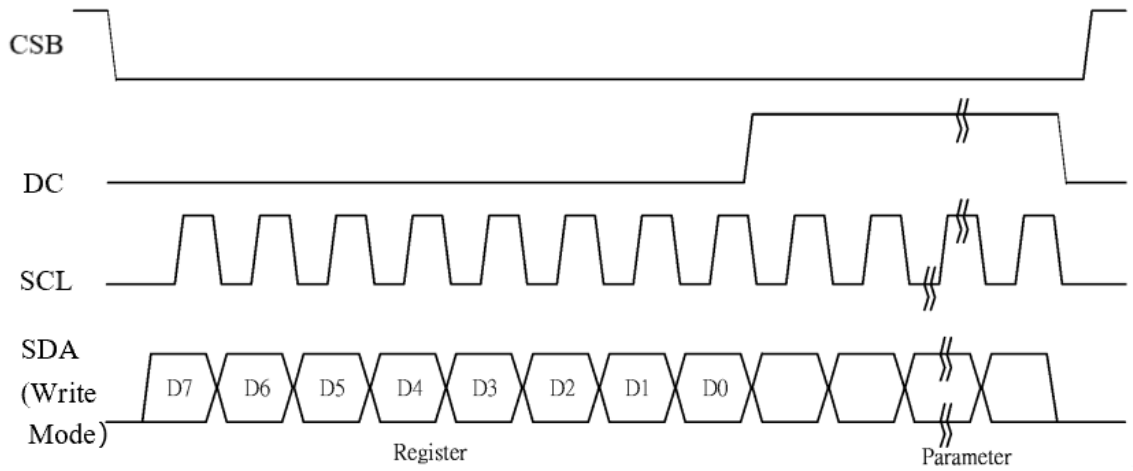
3 pin serial interface characteristics (write mode)



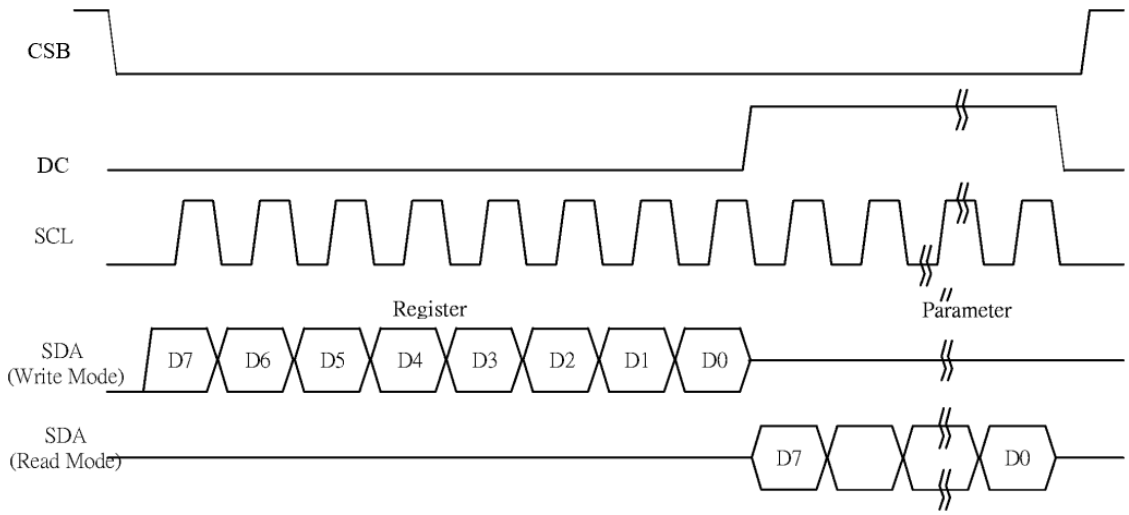
3 pin serial interface characteristics (read mode)

7.3.2 4-wire Serial Port Interface

The serial interface consists of serial clock SCL, serial data SDA, DC, CSB. This interface supports Write mode and Read mode.



4 pin serial interface characteristics (write mode)



4 pin serial interface characteristics (read mode)

8. Optical Characteristics

8.1 Test Conditions

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	ºC
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{DD}	3.0	V

Note: Image is updated with above condition.

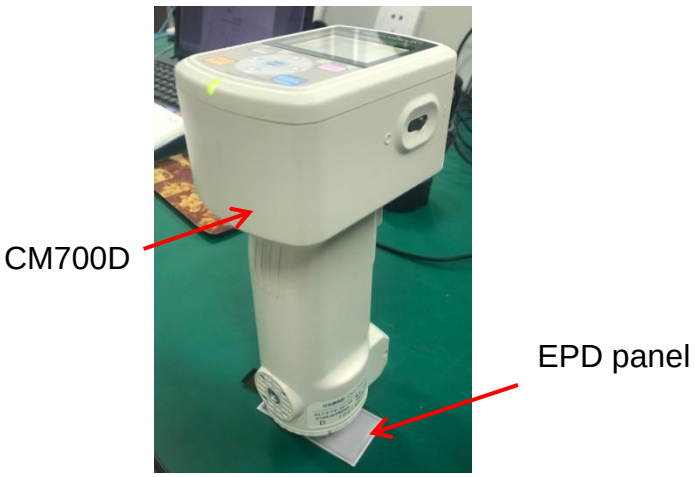
8.2 Optical Specifications

8.2.1 Optical Measurement

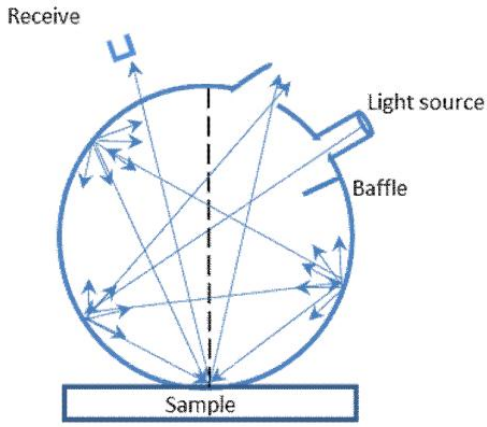
Item	Color	Symbol	Rating			Unit	Note
			Min.	Typ.	Max.		
Contrast ratio	Black/ White	CR	10	-	-	-	$\theta_x=\theta_y=0$ (1),(2),(5),(6)
Refresh Time	Black/ White/ Red	T_r	-	14	-	Sec	(1),(3),(4),(6)
Black state	Black	L*	-	-	16	-	$\theta_x=\theta_y=0$ (1),(2),(6)
	Black	a*	-	-	4		
White state	White	L*	68	-	-	-	$\theta_x=\theta_y=0$ (1),(2),(6)
	White	a*	-	-	0.5		

Item	Color	Symbol	Rating			Unit	Note
			Min.	Typ.	Max.		
Red state	Red	L*	27	-	-	-	$\theta_x=\theta_y=0$ (1),(2),(6)
	Red	a*	37	-	-		
Reflectance	White	R%	30	35	-	%	(1),(2),(6)

Note（1）: Panel is driven by BOE waveform without masking film and optical measurement by ” CM700D” with D65 light source and SCE mode.

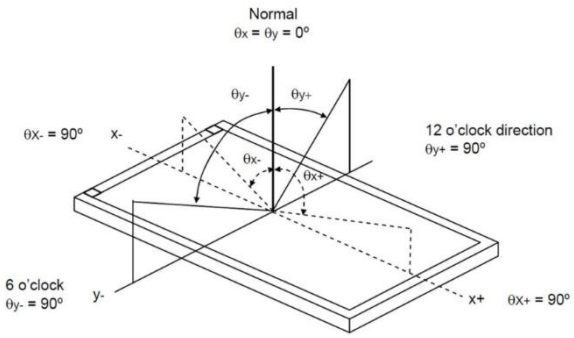


EPD panel face up and remove protection film



SCE Mode

Note（2）：Definition of Viewing Angle(θ_x，θ_y)



Definition of Viewing Angle to Measure Contrast Ratio

Note (3): Refresh time is the time that e-paper particles move not including the power on and off time. The refresh time is measured at 25 ºC. The refresh time and contrast ratio varies due to different films, display performance requirements, and ambient temperatures.

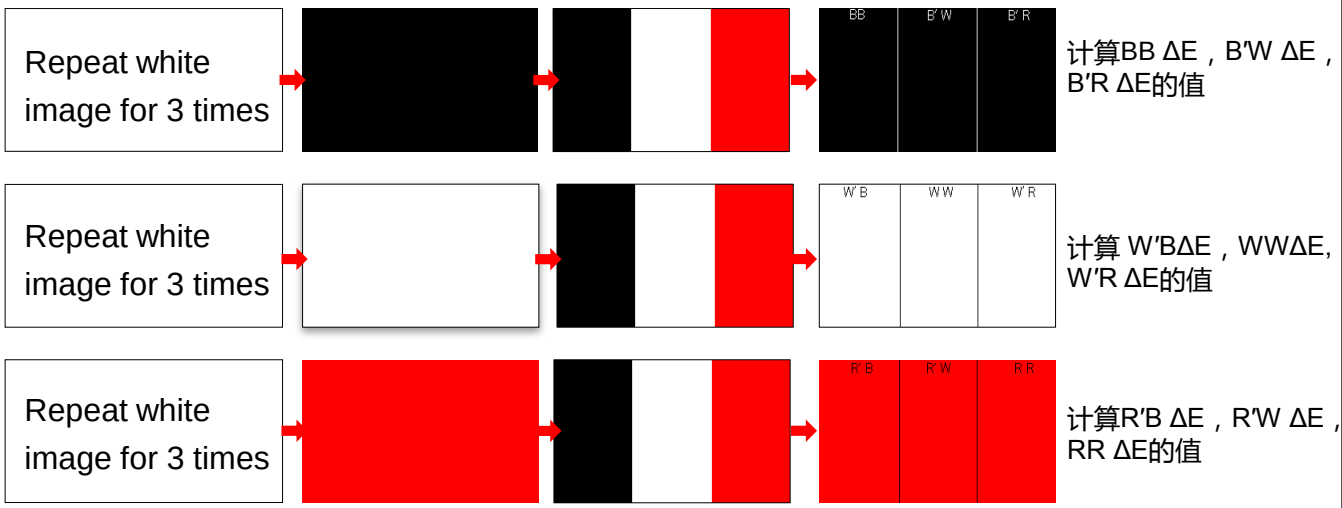
Note (4): Tr is the refresh time for an image which has no Red. For an image with Red, Red/White, Red/Black, or Red/Black/White, the total update time is (Tr).

Note (5): Contrast ratio (CR): The Contrast ratio is calculated by the following expression. CR =(R% White)/(R% Black).

Note (6): Optical data is measured at 60 seconds after refresh with BOE's global update procedure.

8.2.2 Ghosting Measurement

Below are test method to verify if ghosting is within an acceptable range. The measured data (L*, a*, b*) to calculate color different, $\triangle E_{00}$ (CIEDE 2000).The condition of measurement is to follow " Table 7-1 Optical Measurement Conditions".



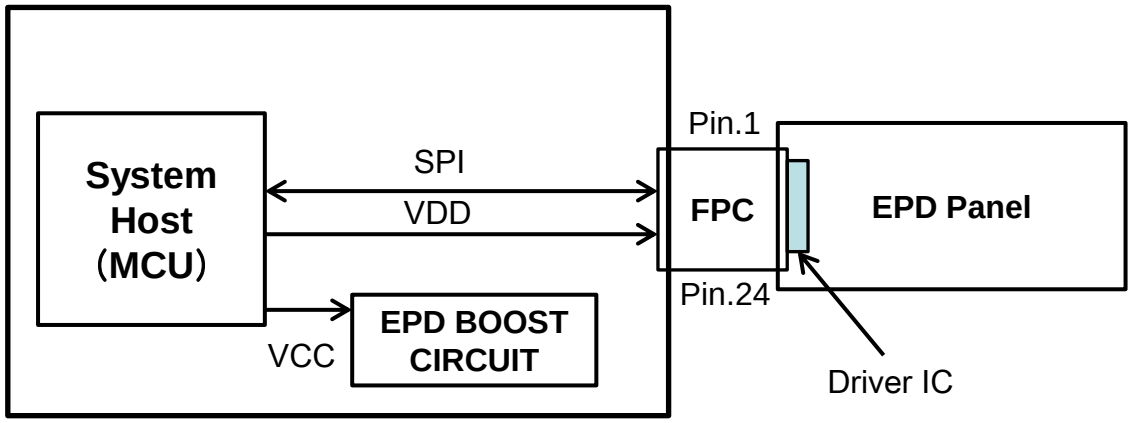
Note: Measurement of ghosting at all image , the SPEC is ΔE<2.

9. Reliability Test Conditions

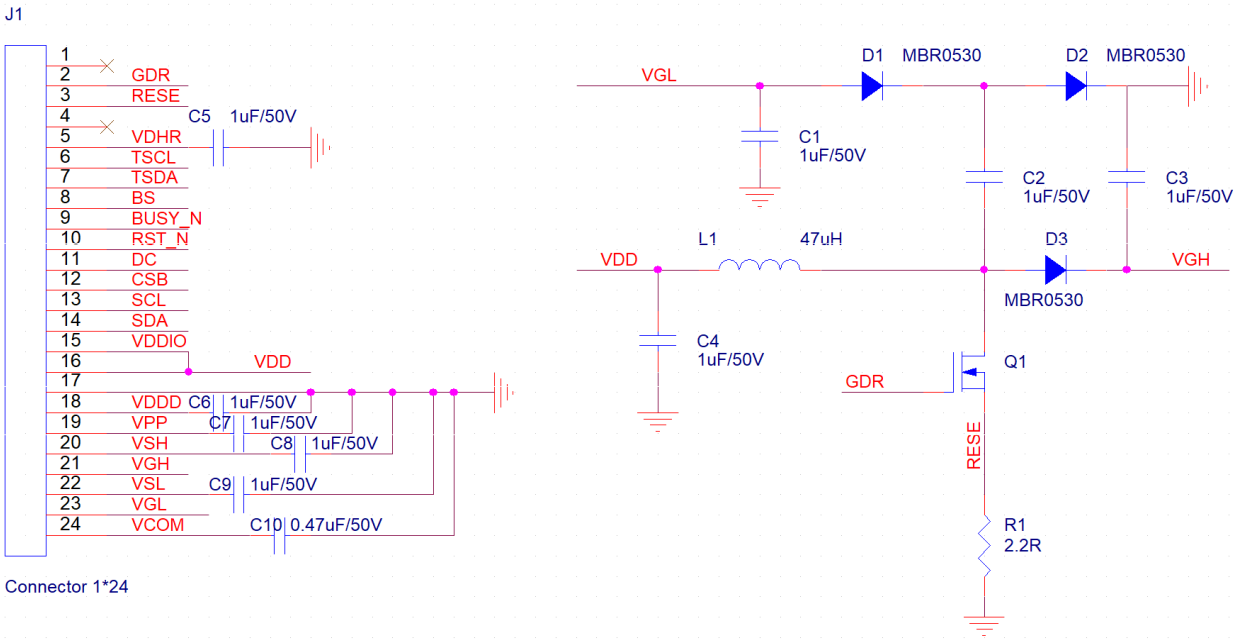
NO	Test items	Test condition
1	High-Temperature Operation	T=40ºC, RH=35%, 240h
2	High-Temperature, High-Humidity Operation	T=40ºC, RH=80%, 240h
3	Low-Temperature Operation	0ºC, 240h
4	Low-Temperature Storage	T = -25˚C, 240h Test in white pattern
5	High-Temperature Storage	T=60ºC, RH=35%, 240h Test in white pattern
6	High Temperature, High-Humidity Storage	T=50ºC, RH=80%, 240h Test in white pattern
7	Temperature Shock (Storage)	1 cycle:[-25˚C 30min]→[+60 ˚C 30 min] , 100 cycles Test in white pattern
8	ESD Gun	Air+/-8KV;Contact+/-2KV (Including IC and FPC area)

Note: Put in normal temperature for 2 hour after test finished, display performance is ok .

10. Application Circuit Block Diagram

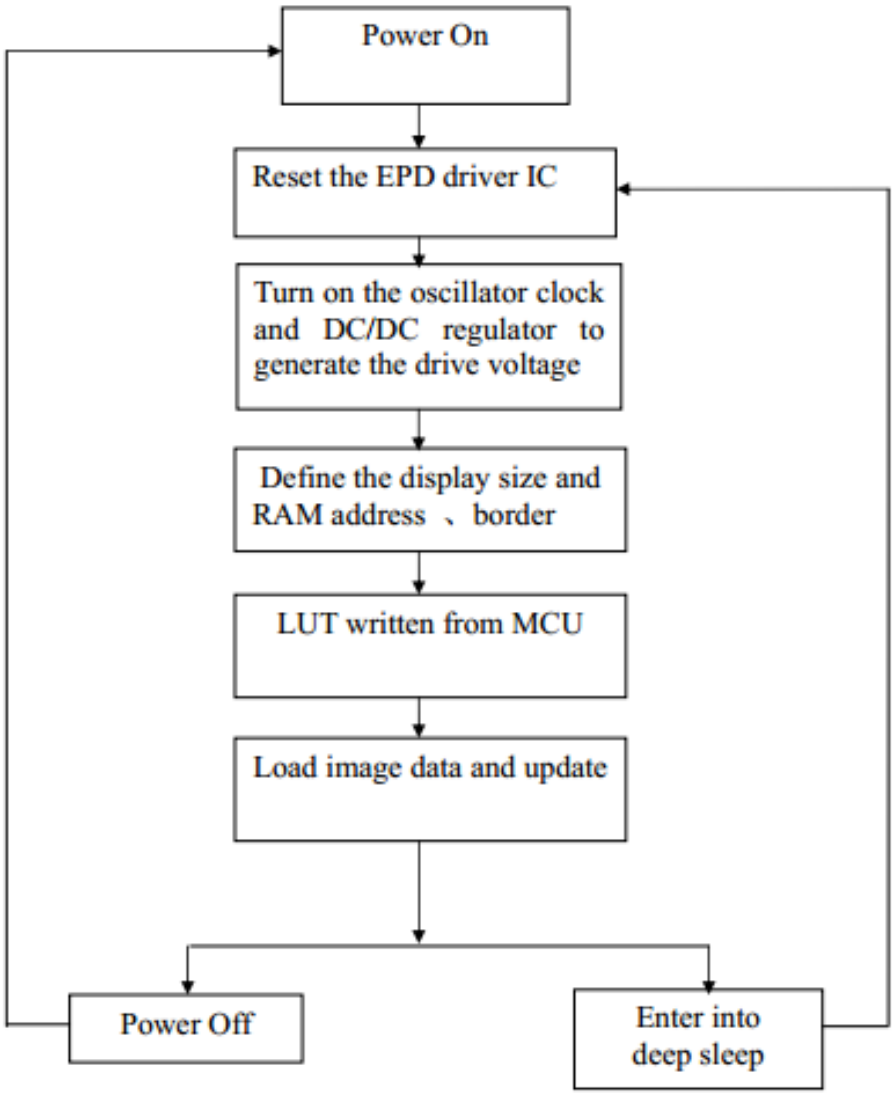


11. Typical Application Circuit with SPI Interface



12. Typical Operating Sequence

12.1 Normal Operation Flow



12.2 Normal Operation Reference Program Code

Command	Data	Comment
VDD on		
Hardware Reset		
Read BUSY_N Pin		Wait for BUSY_N High
R74h	0x54	Set Analog Block Control
R7Eh	0x3B	Set Digital Block Control
R01h	0x27,0x01,0x01	Driver output control
R11h	0x01	Data entry mode setting
R44h	0x00,0x0C	Set RAM X address start/end position
R45h	0xD3,0x00, 0x00,0x00	Set RAM Y address start/end position
R3Ch	0x01	Set border
R18h	0x80	use the internal temperature sensor
R22h	0xB1	
R20h	0x00	
Read BUSY_N Pin		Wait for BUSY_N Low
R4Eh	0x00	
R4Fh	0x27,0x01	
R24h	2756 Bytes	Write RAM(BW) (104/8*212)
R4Eh	0x00	
R4Fh	0x27,0x01	
R26h	2756 Bytes	Write RAM(Red) (104/8*212)
R22h	0xC7	Image update
R20h	0x00	
Read BUSY_N Pin		Wait for BUSY_N Low
R10h	0x01	Enter deep sleep mode
Power off		

13. Handling & Cautions

1. The EPD Panel / Module is manufactured from fragile materials such as glass and plastic, and may be broken or cracked if dropped. Please handle with care. Do not apply force such as bending or twisting to the EPD panel. Please put on gloves to handle EPD to avoid slash.
2. It is recommended to assemble or install EPD panels in a clean working area. Dust and oil may cause electrical shorts or degrade / scratch / dent the protection sheet film.
3. Do not apply pressure to the EPD panel in order to prevent damaging it.
4. Do not connect or disconnect the interface connector while the EPD panel is in operation.
5. Please support as the bezel with your finger while connecting the interface cable such as the FPC.
6. Do not stack the EPD panels / Modules.
7. Do not press the FPC on the glass edge or Pull FPC up / down to 90°.
8. Do not touch the FPC lead connector.
9. Do not touch IC bonding area. It may scratch TFT lead or damage IC function.
10. Wear a Wrist Strap (Grounding connect) when handling and during assembly. Semiconductor devices are included in the EPD Panel / Module and they should be handled with care to prevent any electrostatic discharge (ESD).
11. Keep the EPD Panel / Module in the specified environment and original packing boxes when storage in order to avoid scratching and keep original performance.
12. Do not disassemble or reassemble the EPD panel.
13. Use a soft dry cloth without chemicals for cleaning. Please don't press hard for cleaning because the surface of the protection sheet film is very soft and without hard coating. This behavior would make dent or scratch on protection sheet.
14. Please be mindful of moisture to avoid its penetration into the EPD panel, which may cause damage during operation.
15. It's low temperature operation product. Please be mindful the temperature different to make frost or dew on the surface of EPD panel. Moisture may penetrate into the EPD panel because of frost or dew on surface of EPD panel, and makes EPD panel damage.
16. If the EPD Panel / Module is not refreshed every 24 hours, a phenomena known as “Ghosting” or “Image Sticking” may occur. It is recommended that customer refreshed the ESL / EPD Tag every 24 hours in use case. It is recommended that customer ships or stores the ESL / EPD Tag with a completely white image to avoid this issue.

17. High temperature, high humidity, sunlight or fluorescent light may degrade the EPD panel's performance. Please do not expose the unprotected EPD panel to high temperature, high humidity, sunlight, or fluorescent for long periods of time.
18. The label ink used for marking the Panel ID number is erased easily by solvent. Please avoid using solvent to clean the EPD panel.
19. The EPD is vacuum packed.
20. Before approved by BOE and customer, products and product specifications may be subject to change without notice. Confirm that you have received the latest product standards or specifications before final design, purchase or use.
21. BOE makes every attempt to ensure that its products are of high quality and reliability. However, contact BOE sales office before using the product in an application that demands especially high quality and reliability or where its failure or malfunction may directly threaten human life or cause risk of bodily injury, such as aerospace, aeronautics, nuclear power, combustion control, transportation, traffic, safety equipment or medical equipment for life support.
22. Design your application so that the product is used within the ranges guaranteed by BOE particularly for maximum rating, operating supply voltage range, heat radiation characteristics, installation conditions and other characteristics. BOE bears no responsibility for failure or damage when used beyond the guaranteed ranges. Even within the guaranteed ranges, consider normally foreseeable failure rates or failure modes in semiconductor devices and employ systemic measures such as fail safes, so that the equipment incorporating BOE product does not cause bodily injury, fire or other consequential damage due to operation of the BOE product.
23. This product is not designed to be radiation resistant.